

ROCKWELL 1984 DATA BOOK

SECOND EDITION

SEMICONDUCTOR PRODUCTS DIVISION

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Rockwell International

1984 DATA BOOK

Second Edition

Rockwell International



Semiconductor Products Division

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SY6502	R6502
SY6503	R6503
SY6504	R6504
SY6505	R6505
SY6506	R6506
SY6507	R6507
SY6512	R6512
SY6513	R6513
SY6514	R6514
SY6515	R6515
SY6520	R6520
SY6522	R6522
SY6530	R6530
SY6532	R6532
SY6545-1	R6545-1
SY6551	R6551

INTEL ROCKWELL

2816	R5213
8272	R6765
2816A	R5516A
P2764	R2764P
P2732A	R27C32P

MOTOROLA ROCKWELL

MC6820	R6520
(1)MC6821	R6520
(2)MC6845	R6545-1
(2)MC6845M	R6545-1
MC68000	R68000

(1) except application of (2) TTL loads
(2) ask customer for evaluation

MOS TECHNOLOGY ROCKWELL

MPS6502	R6502
MPS6503	R6503
MPS6504	R6504
MPS6505	R6505
MPS6506	R6506
MPS6507	R6507
MPS6512	R6512
MPS6513	R6513
MPS6514	R6514
MPS6515	R6515
MPS6520	R6520
MPS6522	R6522
MPS6530	R6530
MPS6532	R6532

NCR ROCKWELL

NCR6500/1E	R6500/1EC
NCR6500/1	R6500/1
NCR6500/11	R6500/11
NCR6500/12	R6500/12
NCR6500/13	R6500/13
NCR6500/11E	R6511Q
NCR6500/41	R6500/41
NCR6500/42	R6500/42
NCR6500/43	R6500/43
NCR6500/41E	R6541Q
NCR65C02	R65C02

SEEQ ROCKWELL

5213/2816	R5213/2816
5516A	R5516A/2816A
5133A	R2764P
52B33	R52B33

GTE ROCKWELL

G65SC02	R65C02
G65SC21	R65C21
G65SC51	R65C51
	R23C64

RICOH ROCKWELL

RD5H32	R87C32
RD5H64	R87C64

NATIONAL ROCKWELL

NMC27C32	R87C32
NMC9716E	R5213

AMI ROCKWELL

S2333	R2332
S2364	R2364
S23128	R23128
S6551	R6551

FUJITSU ROCKWELL

MBM27C64	R87C64
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AMD ROCKWELL

AM2764	R87C64
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RCA ROCKWELL

CDP65564	R23C64
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NEC ROCKWELL

785	R6765
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SECTION 1

R68000 MICROPROCESSOR AND PERIPHERALS

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R68000 MICROPROCESSOR AND PERIPHERAL FAMILY

16-bit Speed and Data Capacity, Peripherals to Build Efficient Systems

Rockwell peripherals give a designer everything the 68000 family promises. They allow you to design functional systems utilizing all the speed and data handling potential of the 16-bit 68000 family.

First of these are the Rockwell designed 16-bit peripherals—multi-protocol communications controller, double density floppy disk controller, local area network controller—each a significant “first” that eliminates the “glue parts” between a CPU and peripherals.

Not to be ignored, however, is the very wide and complete family of 8-bit devices—processors, peripherals, memory, single-chip microcomputers—compatible with the R68000 family. All of the R6500 family of devices described in this Data Book are directly compatible with the R68000 bus. They often provide efficient, economical and very flexible ways of implementing system designs.

The Rockwell R68000 16-bit microprocessor (MPU) operates at clock speeds of 4, 6, 8, 10 or 12.5 MHz to match essentially any application.

The R68561 multi-protocol communications controller (MPCC) is the highest throughput communications device

ever made commercially available. It operates up to 4 Mbits/sec and supports all major communication protocols. It's available to work with either 16-bit or 8-bit busses and can be adapted to function with essentially any of today's more common busses.

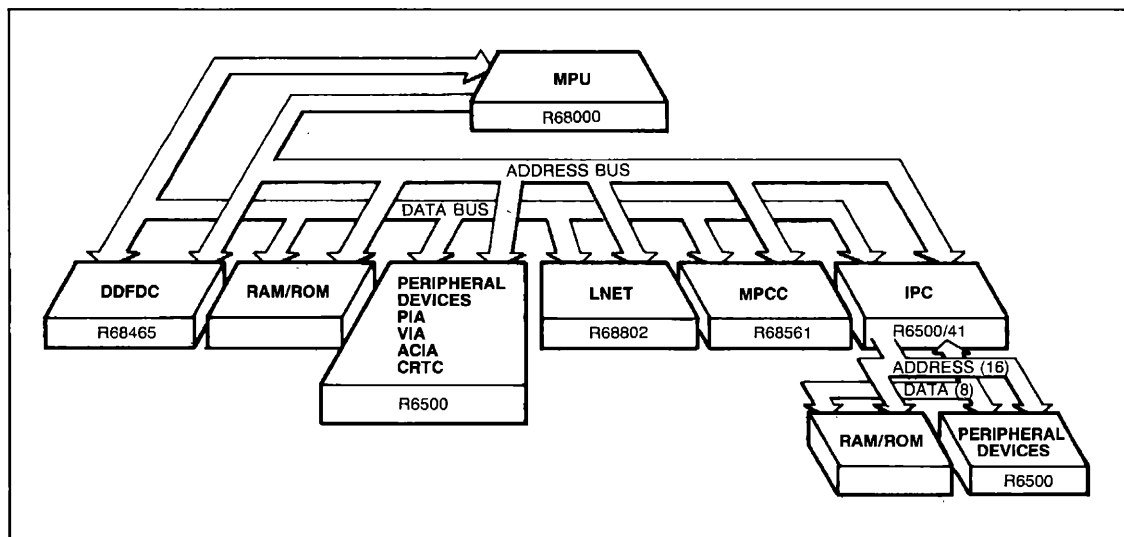
The R68465 double density floppy disk controller (DDFDC) is an intelligent device that can run up to four disk drives without the many support devices previously required.

The R68802* provides a flexible local area network (LNET) controller for the R68000. It supports both the IEEE 802.3 and Ethernet* standards based on the proven CSMA/CD technique together with network statistics.

Rockwell lets you build efficient and economical 16-bit systems through families of 16-bit and 8-bit peripherals, all compatible. No other supplier offers you more.

**R68802 is a trademark of the Rockwell International Corp.*

**Ethernet is a trademark of the Xerox Corp.*



R68000/R6500 Peripheral Migration



R68000 16-BIT MICROPROCESSING UNIT (MPU)

1

PRELIMINARY

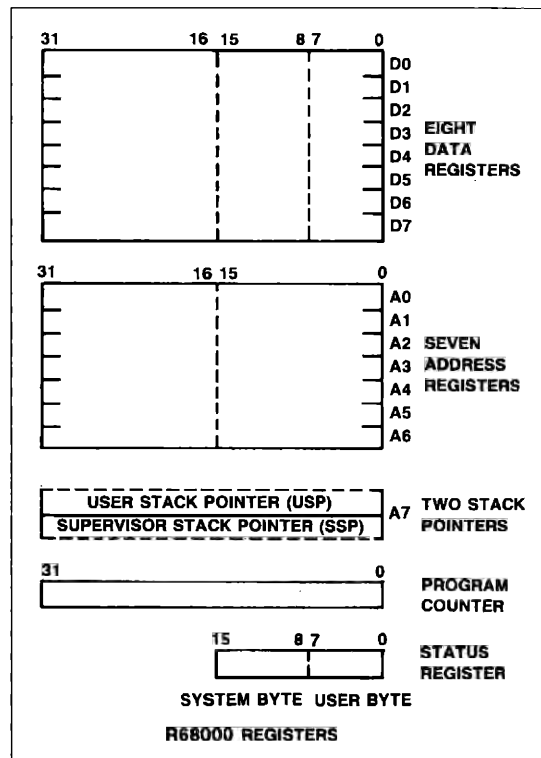
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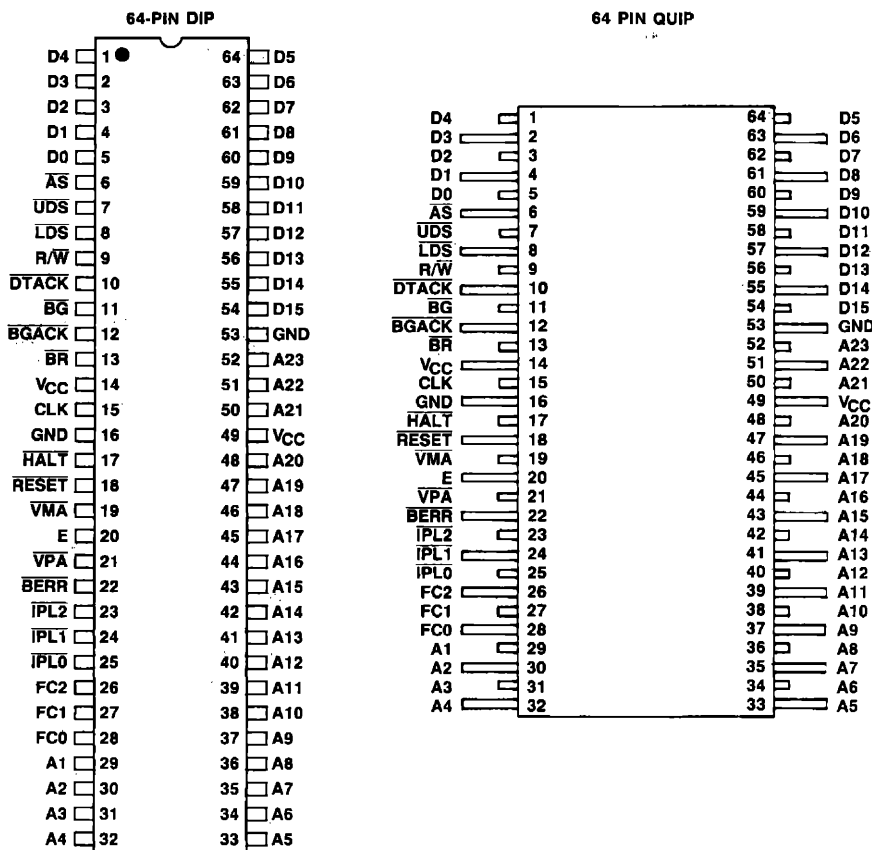
The R68000 microprocessor is designed for high performance where operational computation and versatility is required. The R68000 provides powerful mass-memory handling capability and architectural features designed to fit the broad range of 16-bit needs. The Rockwell family of 16-bit products also includes a wide range of peripherals that will allow complete system design and manufacture.

The R68000 offers seventeen 32-bit registers in addition to the 32-bit program counter and a 16-bit status register. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) data operations. The second set of seven registers (A0-A6) and the system stack pointer may be used as software stack pointers and base address registers. In addition, these registers may be used for word and long word address operations. All 17 registers may be used as index registers.

FEATURES

- 16M byte (8M word) Linear Addressing Range
- 14 Operand Addressing Modes
- 56 Powerful Instruction Types
- Instruction Set Supports Structured High-Level Languages
- Pipelining Instruction Execution
- 32-Bit Program Counter
- 16-Bit Data Bus
- 23-Line Address Bus
- 32-Bit Data and Address Registers Including:
 - Eight General Purpose Data Registers
 - Seven Address Registers
 - Two Stack Pointers (User, Supervisory)
- All 17 Registers Can Be Index Registers
- Memory Mapped Peripheral Devices
- Vector Generated Exception Processing
- Seven Unique Autovectors for Interrupt Service Routines
- Trace Mode for Software Debugging
- Operations Occur on Five Main Data Types
 - Bit
 - BCD
 - Byte
 - Word
 - Long Word
- Asynchronous and Synchronous Peripheral Interface Capability
- Many Peripheral Chips Available
 - R68560 Multi-Protocol Communications Controller
 - R68465 Double Density Floppy Disk Controller
 - R68802 Local Network Controller
- Up to 12.5 MHz Input Clock
- +5 VDC Power Supply





R68000 PIN CONFIGURATION

ORDERING INFORMATION

Order Number	Package Type	Frequency	Temperature Range
R68000C4	Ceramic DIP	4 MHz	0°C to +70°C
R68000C6	Ceramic DIP	6 MHz	0°C to +70°C
R68000C8	Ceramic DIP	8 MHz	0°C to +70°C
R68000C10	Ceramic DIP	10 MHz	0°C to +70°C
R68000C12	Ceramic DIP	12.5 MHz	0°C to +70°C
R68000Q8	Plastic QUIP	8 MHz	0°C to +55°C
R68000Q10	Plastic QUIP	10 MHz	0°C to +55°C

SIGNAL DESCRIPTION

The following paragraphs briefly describe the input and output signals and also reference (if applicable) other paragraphs that contain more detail about the function being performed. Bus operation during the various machine cycles and operations is also discussed. The input and output signals can be functionally organized into the groups shown in Figure 1.

Note

The terms assertion and negation are used to avoid confusion when dealing with a mixture of "active-low" and "active-high" signals. The terms assert, or assertion, indicates that a signal is active, or true, independent of whether that voltage is low or high. The term negate, or negation, indicates that a signal is inactive or false.

ADDRESS BUS (A1 THROUGH A23). This 23-bit, unidirectional, three-state bus can address eight megawords of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 encode the interrupt level to be serviced while address lines A4 through A23 are all set high.

DATA BUS (D0 THROUGH D15). This 16-bit, bidirectional, three-state bus is the general purpose data path. It transfers and accepts data in either word or byte length. During an interrupt acknowledge cycle, an external device supplies the vector number on data lines D0-D7.

ASYNCHRONOUS BUS CONTROL. Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

Address Strobe (\overline{AS}). The \overline{AS} output indicates that there is a valid address on the address bus.

Read/Write (R/\overline{W}). The R/\overline{W} output defines the data bus transfer as a read or write cycle. The R/\overline{W} signal also works in conjunction with the upper and lower data strobes as explained in the following paragraph.

Upper and Lower Data Strobes (\overline{UDS} , \overline{LDS}). The \overline{UDS} and \overline{LDS} outputs control the data on the data bus, as shown in Table 1. When the R/\overline{W} line is high, the processor reads from the data bus as indicated. When the R/\overline{W} line is low, the processor writes to the data bus as shown.

Data Transfer Acknowledge (\overline{DTACK}). The \overline{DTACK} input indicates that the data transfer is completed. When the processor recognizes \overline{DTACK} during a read cycle, data is latched and the bus cycle terminated. When \overline{DTACK} is recognized during a write cycle, the bus cycle terminates. Refer to **ASYNCHRONOUS VERSUS SYNCHRONOUS OPERATION**.

BUS ARBITRATION CONTROL. These three signals form a bus arbitration circuit to determine which device will be the bus master device.

Bus Request (\overline{BR}). The \overline{BR} input indicates to the processor that some other device desires to become the bus master. This input can be externally ORed with all other devices that could be bus masters.

Bus Grant (\overline{BG}). The \overline{BG} output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

Bus Grant Acknowledge (\overline{BGACK}). The \overline{BGACK} input indicates that some other device has become the bus master. This signal cannot be asserted until the following four conditions are met:

- a bus grant (\overline{BG}) has been received,
- address strobe (\overline{AS}) is inactive which indicates that the processor is not using the bus

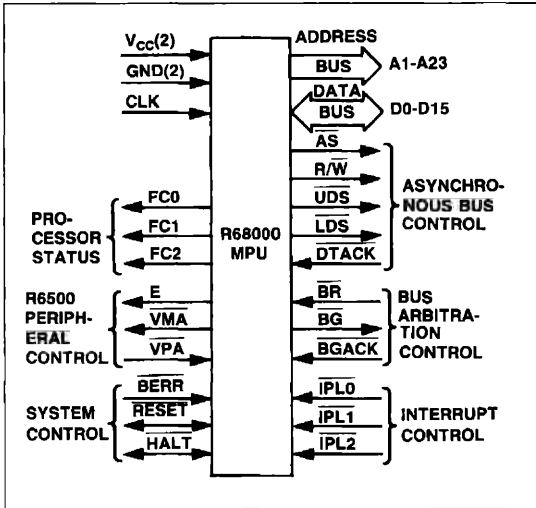


Figure 1. Input and Output Signals

Table 1. Data Strobe Control of Data Bus

\overline{UDS}	\overline{LDS}	R/\overline{W}	D8-D15	D0-D7
High	High	—	No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7*	Valid data bits 0-7
Low	High	Low	Valid data bits 8-15	Valid data bits 8-15*

* These conditions are a result of current implementation and may not appear on future devices.

3. data transfer acknowledge (\overline{DTACK}) is inactive which indicates that neither memory nor peripherals are using the bus, and
4. bus grant acknowledge (\overline{BGACK}) is inactive which indicates that no other device is still claiming bus mastership.

INTERRUPT CONTROL ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$). These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. Level seven cannot be masked. $\overline{IPL0}$ is the least significant bit while $\overline{IPL2}$ is the most significant bit. To insure an interrupt is recognized, the interrupt control lines (\overline{IPLX}) must remain stable until the processor signals interrupt acknowledge (FC0, FC1, and FC2 all high).

SYSTEM CONTROL. The system control inputs either reset or halt the processor or indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

Bus Error (\overline{BERR}). The \overline{BERR} input informs the processor that a problem exists with the cycle currently being executed. Problems may be a result of:

1. nonresponding devices,
2. interrupt vector number acquisition failure,
3. illegal access request as determined by a memory management unit, or
4. other application dependent errors.

The Bus Error (\overline{BERR}) signal interacts with the \overline{HALT} signal to determine if exception processing should be performed or the current bus cycle should be retried.

Refer to BUS ERROR AND HALT OPERATION paragraph for additional information about the interaction of the bus error and halt signals.

Reset (\overline{RESET}). This bidirectional signal line acts to reset (initiate a system initialization sequence) the processor and system in response to an external reset signal. An internally generated reset (result of a RESET instruction) resets all external devices while not affecting the internal state of the processor. A total system reset (processor and external devices) is the result of external \overline{HALT} and \overline{RESET} signals applied simultaneously. Refer to RESET OPERATION paragraph for additional information.

Halt (\overline{HALT}). The bidirectional \overline{HALT} line, when driven by an external device, will cause the processor to stop at the completion of the current bus cycle. Halting the processor using \overline{HALT} causes all control signals to go inactive and all three-state lines to go to their high-impedance state. Refer to BUS ERROR AND HALT OPERATION paragraph for additional information about the interaction between the \overline{HALT} and \overline{BERR} signals.

When the processor has stopped executing instructions, such as in a double bus fault condition, the \overline{HALT} line is driven by the processor to indicate to external devices that the processor has stopped. Refer to paragraph on Double Bus Faults.

R6500 PERIPHERAL CONTROL. These control signals are used to allow the interfacing of synchronous R6500 peripheral devices with the asynchronous R68000. These signals are explained in the following paragraphs.

Enable (E). The E output signal is the standard enable signal ($\emptyset 2$ clock) common to all R6500 type peripheral devices. The period for this output is ten R68000 clock periods (six clocks low; four clocks high). Enable is generated by an internal ring counter which may come up in any state (i.e., at power on, it is impossible to guarantee phase relationship of E to CLK). E is a free-running clock and runs regardless of the state of the bus on the MPU.

Valid Peripheral Address (\overline{VPA}). The \overline{VPA} input indicates that the device or region addressed is a R6500 family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt. Refer to INTERFACE WITH R6500 PERIPHERALS.

Valid Memory Address (\overline{VMA}). The \overline{VMA} output indicates to R6500 peripheral devices that there is a valid address on the address bus and that the processor is synchronized to enable. This signal only responds to a valid peripheral address (\overline{VPA}) input which indicates that the peripheral is a R6500 family device.

PROCESSOR STATUS (FC0, FC1, FC2). These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown in Table 2. The information indicated by the function code outputs is valid whenever address strobe (\overline{AS}) is active.

CLOCK (CLK). The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input should not be gated off at any time and the clock signal must conform to minimum and maximum pulse width times.

SIGNAL SUMMARY. Table 3 summarizes all the signals discussed in the previous paragraphs.

Table 2. Function Code Outputs

FC2	FC1	FC0	Cycle Type
Low	Low	Low	(Undefined, Reserved)
Low	Low	High	User Data
Low	High	Low	User Program
Low	High	High	(Undefined, Reserved)
High	Low	Low	(Undefined, Reserved)
High	Low	High	Supervisor Data
High	High	Low	Supervisor Program
High	High	High	Interrupt Acknowledge

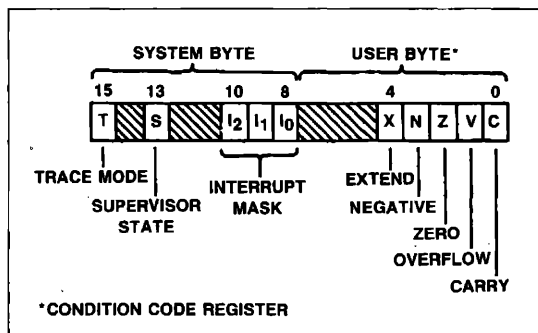
Table 3. Signal Summary

Signal Name	Mnemonic	Input/Output	Active State	HI-Z	
				On $\overline{\text{HALT}}$	On $\overline{\text{BGACK}}$
Address Bus	A1-A23	Output	High	Yes	Yes
Data Bus	D0-D15	Input/Output	High	Yes	Yes
Address Strobe	$\overline{\text{AS}}$	Output	Low	No	Yes
Read/Write	$\overline{\text{R/W}}$	Output	Read-High Write-Low	No	Yes
Upper and Lower Data Strobes	$\overline{\text{UDS}}, \overline{\text{LDS}}$	Output	Low	No	Yes
Data Transfer Acknowledge	$\overline{\text{DTACK}}$	Input	Low	No	No
Bus Request	$\overline{\text{BR}}$	Input	Low	No	No
Bus Grant	$\overline{\text{BG}}$	Output	Low	No	No
Bus Grant Acknowledge	$\overline{\text{BGACK}}$	Input	Low	No	No
Interrupt Priority Level	$\overline{\text{IPL0}}, \overline{\text{IPL1}}, \overline{\text{IPL2}}$	Input	Low	No	No
Bus Error	$\overline{\text{BERR}}$	Input	Low	No	No
Reset	$\overline{\text{RESET}}$	Input/Output	Low	No*	No*
Halt	$\overline{\text{HALT}}$	Input/Output	Low	No*	No*
Enable	$\overline{\text{E}}$	Output	High	No	No
Valid Memory Address	$\overline{\text{VMA}}$	Output	Low	No	Yes
Valid Peripheral Address	$\overline{\text{VPA}}$	Input	Low	No	No
Function Code Output	FC0, FC1, FC2	Output	High	No	Yes
Clock	CLK	Input	High	No	No
Power Input	VCC	Input	—	—	—
Ground	GND	Input	—	—	—

*Open drain.

REGISTER DESCRIPTION AND DATA ORGANIZATION

STATUS REGISTER. The status register contains the eight level interrupt mask as well as the condition codes; extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and/or in a supervisor (S) state.



Status Register

OPERAND SIZE

Operand sizes are defined as follows: a byte equals 8 bits, a word equals 16 bits, and a long word equals 32 bits. The operand size for each instruction is either explicitly encoded in the instruction or implicitly defined by the instruction operation. Implicit instructions support some subset of all three sizes.

DATA ORGANIZATION IN REGISTERS

The eight data registers support data operands of 1, 8, 16, or 32 bits. The seven address registers together with the active stack pointer support address operands of 32 bits.

DATA REGISTERS. Each data register is 32 bits wide. Byte operands occupy the low order 8 bits, word operands the low order 16 bits, and long word operands the entire 32 bits. The least significant bit is addressed as bit zero; the most significant bit is addressed as bit 31. When a data register is used as either a source or destination operand, only the appropriate low-order portion is changed; the remaining high order portion is neither used nor changed.

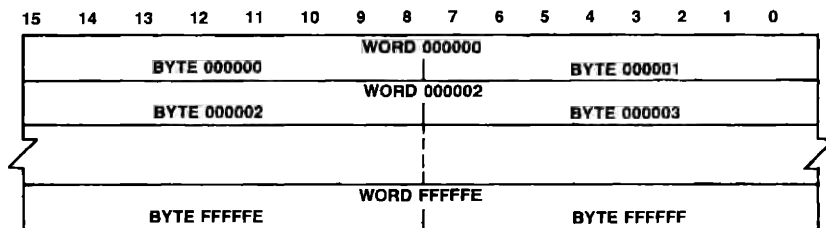


Figure 2. Word Organization In Memory

ADDRESS REGISTERS. Each address register and the stack pointer is 32 bits wide and holds a full 32-bit address. Address registers do not support byte sized operands. Therefore, when an address register is used as a source operand, either the low order word or the entire long word operand is used depending upon the operation size. When an address register is used as the destination operand, the entire register is affected regardless of the operation size. If the operation size is word, any other operands are sign extended to 32 bits before the operation is performed.

DATA ORGANIZATION IN MEMORY

Bytes are individually addressable with the high order byte having an even address the same as the word, as shown in Figure 2. The low order byte has an odd address that is one higher than the word address. Instructions and multi-byte data are accessed only on word (even byte) boundaries. If a long word datum is located at address n (n even), then the second word of that datum is located at address $n + 2$.

The data types supported by the R68000 are: bit data, integer data of 8, 16, or 32 bits, 32-bit addresses and binary coded decimal data. Each of these data types is put in memory, as shown in Figure 3. The numbers indicate the order in which data is accessed from the processor.

BUS OPERATION

The following paragraphs explain control signal and bus operation during data transfer operations, bus arbitration, bus error and halt conditions, and reset operation.

DATA TRANSFER OPERATIONS. Transfer of data between devices involves the following signals:

- Address Bus A1 through A23
- Data Bus D0 through D15
- Control Signals

The address and data buses are separate parallel buses which transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the R68000 for interlocked multiprocessor communications.

Read Cycle. During a read cycle, the processor receives data from memory or a peripheral device. The processor reads bytes of data in all cases, and for a word (or double word) operation, the processor reads both upper and lower bytes simultaneously by asserting both upper and lower data strobes. When the instruction specifies byte operation, the processor uses an internal AO bit to determine which byte to read and then issues the data strobe required for that byte. When the AO bit equals zero, the upper data strobe is issued, and when the AO bit equals one, the lower data strobe is issued. The processor correctly positions the received data internally.

A word read cycle flow chart is given in Figure 4. A byte read cycle flow chart is given in Figure 5. Read cycle timing is given in Figure 6. Figure 7 details word and byte read cycle operations.

Write Cycle. During a write cycle, the processor sends bytes of data to memory or a peripheral device. If the instruction specifies a word operation, the processor writes both bytes. When the instruction specifies a byte operation, the processor uses an internal AO bit to determine which byte to write and then issues the data strobe required for that byte. When the AO bit equals zero, the upper data strobe is issued and when the AO bit equals one, the lower data strobe is issued. A word write cycle flow chart is given in Figure 8. A byte write cycle flow chart is given in Figure 9. Write cycle timing is given in Figure 6. Figure 10 details word and byte write cycle operation.

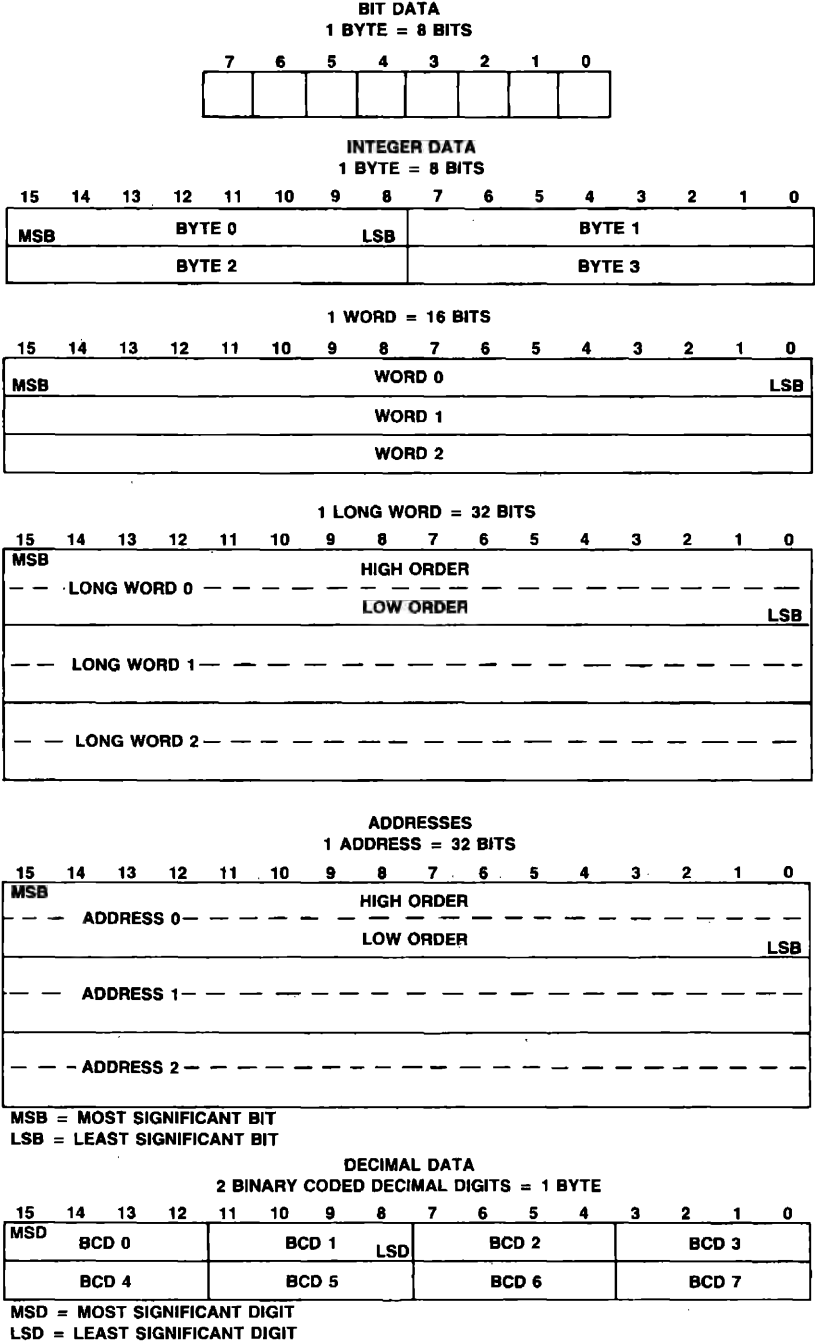


Figure 3. Data Organization In Memory

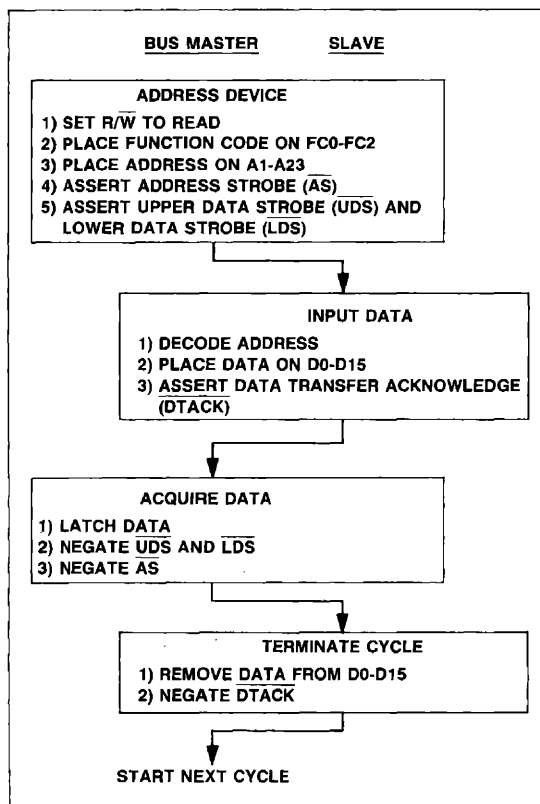


Figure 4. Word Read Cycle Flow Chart

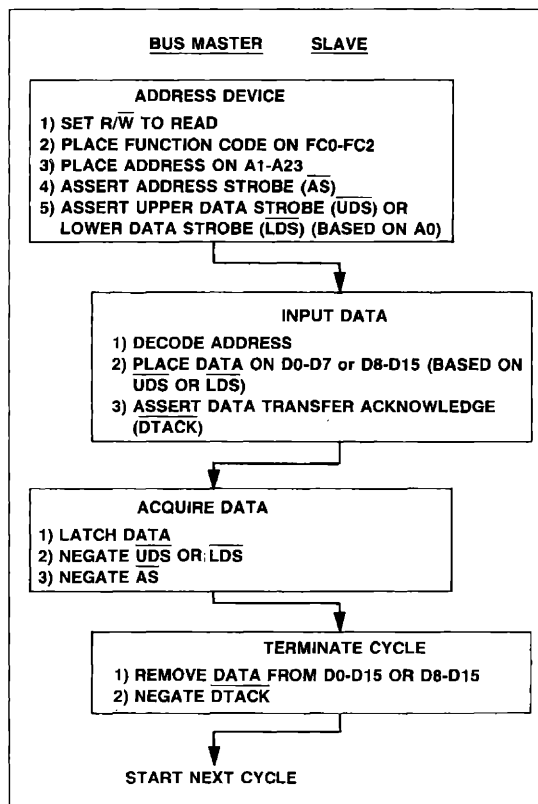


Figure 5. Byte Read Cycle Flow Chart

Read-Modify-Write Cycle. The read-modify-write cycle performs a read, modifies the data in the arithmetic-logic unit, and writes the data back to the same address. In the R68000 this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. TAS is the only instruction that uses the read-modify-write cycles. Since the test and set instruction only operates on bytes, all read-modify-write cycles are byte operations. A read-modify-write cycle flow chart is given in Figure 11 and a timing diagram is given in Figure 12.

BUS ARBITRATION. Bus arbitration is a technique used by master-type devices to request, be granted, and knowledge bus mastership. In its simplest form, it consists of:

1. asserting a bus mastership request,
2. receiving a grant that the bus is available at the end of the current cycle, and
3. acknowledging that mastership has been assumed.

Figure 13 is a flow chart showing the detail involved in a request from a single device. Figure 14 is a timing diagram for the same operation. This technique allows processing of bus requests during data transfer cycles.

The timing diagram shows that the bus request is negated at the time that an acknowledge is asserted. This is true for a system consisting of the processor and one device capable of bus mastership. However, in systems having a number of devices capable of bus mastership, the bus request line from each device is ORed to the processor. In this system, it is easy to see that there could be more than one bus request being made. The timing diagram shows that the bus grant signals negate a few clock cycles after the transition of the acknowledge (BGACK) signal.

However, if the bus requests are still pending, the processor will assert another bus grant within a few clock cycles after negation. This additional assertion of bus grant allows external arbitration circuitry to select the next bus master before the current bus master has completed its requirements. The following paragraphs provide additional information about the three steps in the arbitration process.

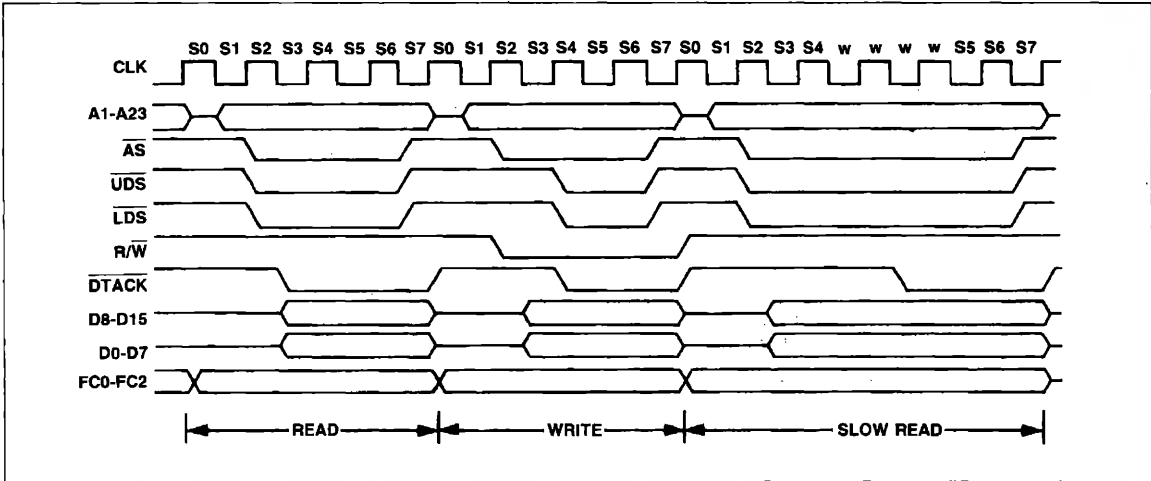


Figure 6. Read and Write Cycle Timing Diagram

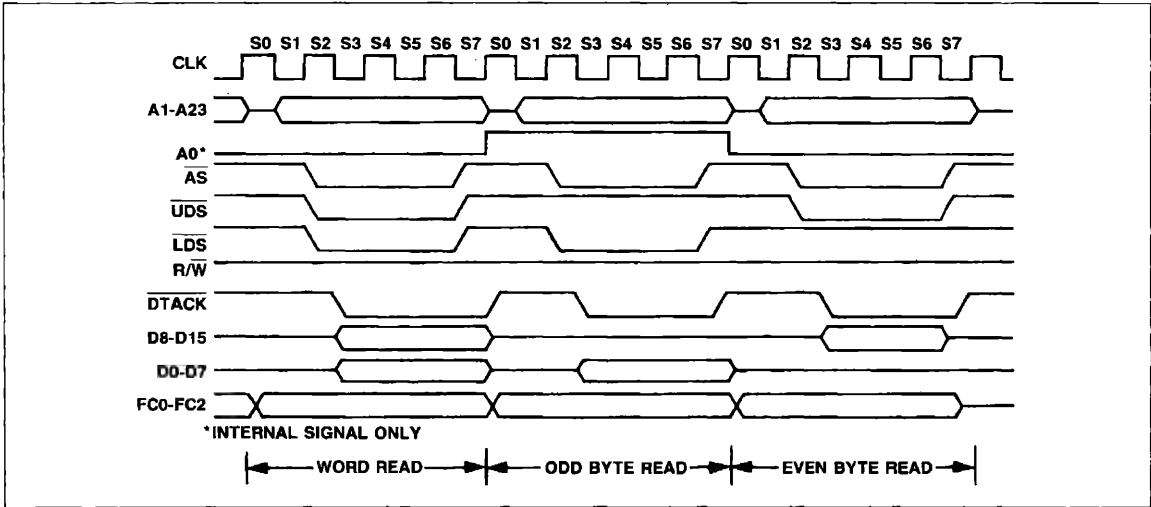


Figure 7. Word and Byte Read Cycle Timing Diagram

Requesting the Bus. External devices capable of becoming bus masters request the bus by asserting the bus request (BR) signal. This ORed signal (although it need not be constructed from open collector devices) indicates to the processor that some external device requires control of the external bus. The processor, at a lower bus priority level than the external device, will relinquish the bus after it has completed the last bus cycle it has started. If no acknowledge is received before the bus request signal goes inactive, the processor will continue processing when it detects that the bus request is inactive. This allows ordinary processing to continue if the arbitration circuitry inadvertently responded to noise.

Receiving the Bus Grant. Normally the processor asserts bus grant (BG) as soon as possible after internal synchronization. The only exception occurs when the processor has made an internal decision to execute the next bus cycle but has not progressed far enough into the cycle to have asserted the address strobe (AS) signal. In this case, bus grant will not be asserted until one clock after address strobe is asserted to indicate to external devices that a bus cycle is being executed.

The bus grant signal may be routed through a daisy-chained network or through a specific priority-encoded network. The processor is not affected by the external method of arbitration as long as the protocol is obeyed.

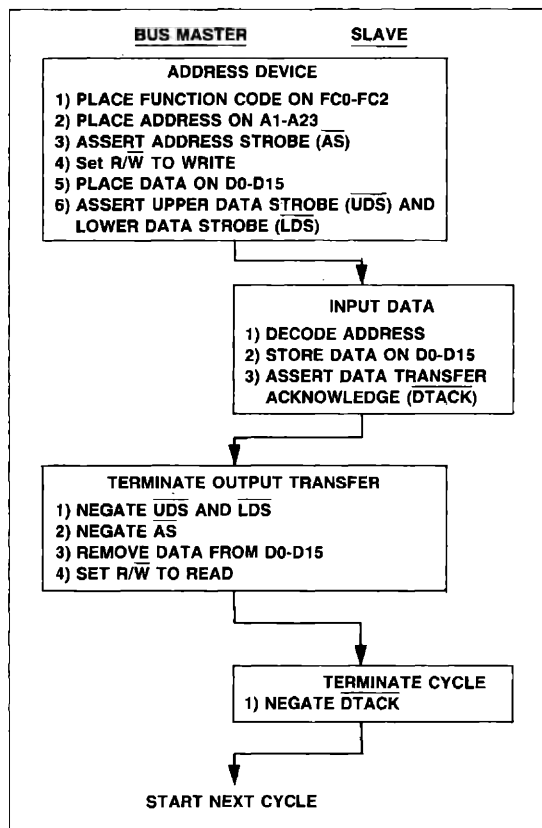


Figure 8. Word Write Cycle Flow Chart

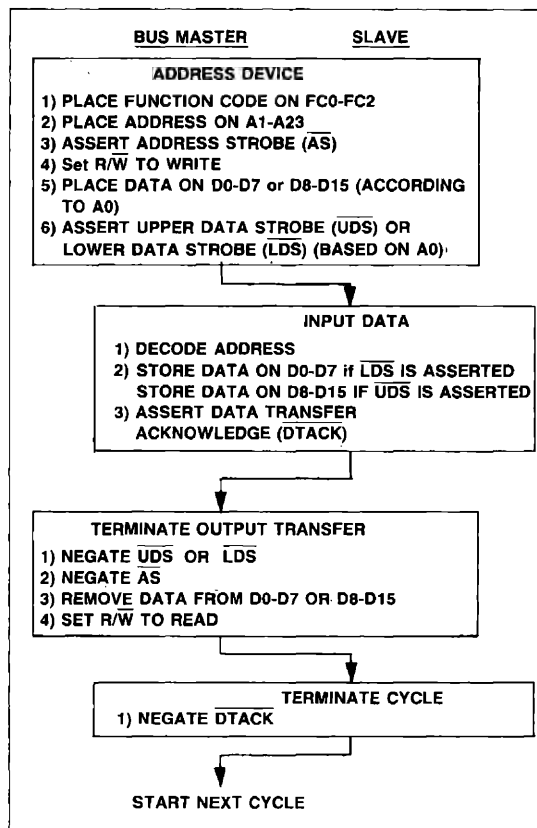


Figure 9. Byte Write Cycle Flow Chart

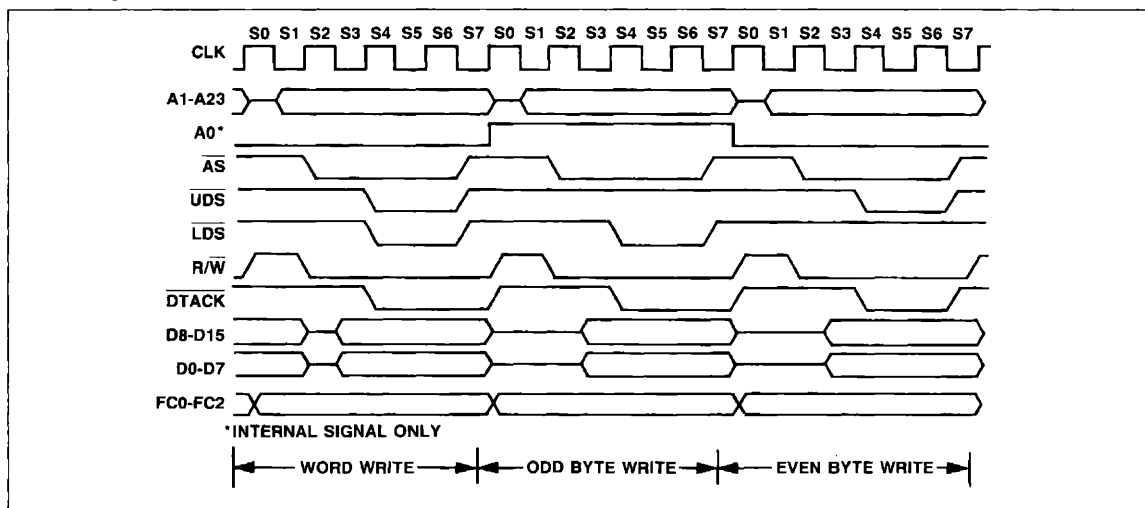


Figure 10. Word and Byte Write Cycle Timing Diagram

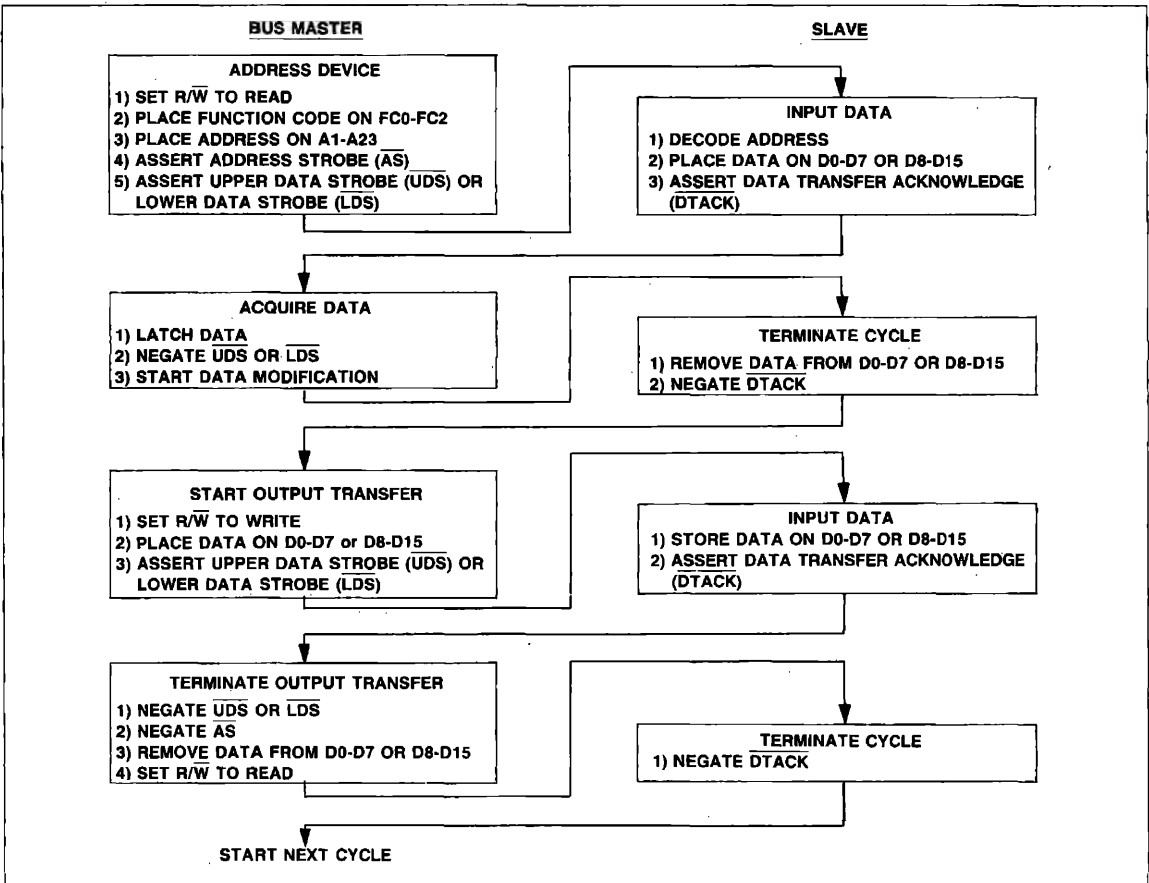


Figure 11. Read-Modify-Write Cycle Flow Chart

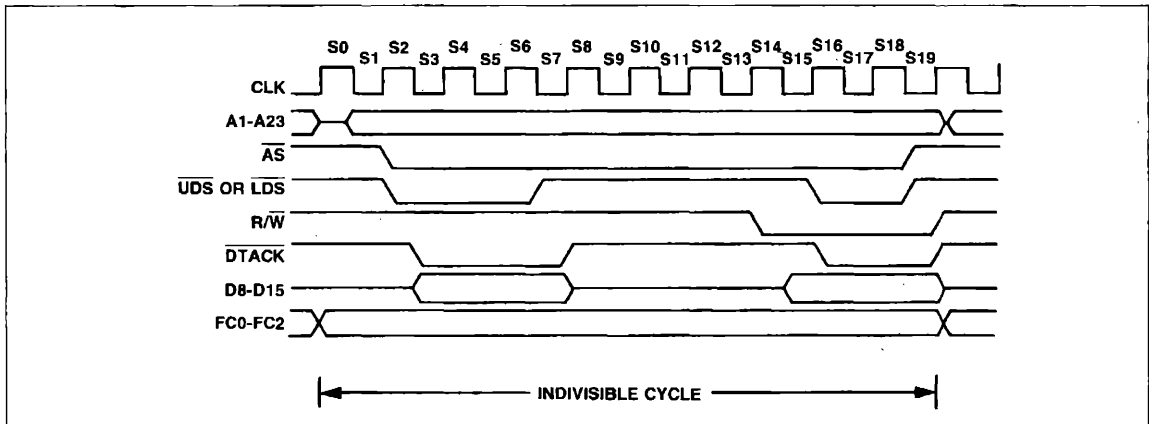


Figure 12. Read-Modify-Write Cycle Timing Diagram

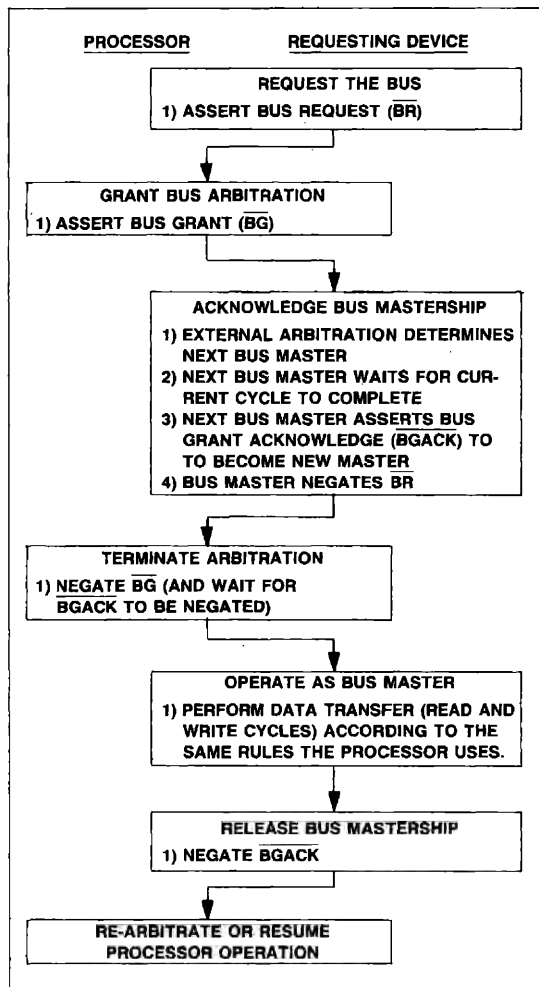


Figure 13. Bus Arbitration Cycle Flow Chart

Acknowledgment of Mastership. Upon receiving a bus grant (BG), the requesting device waits until address strobe (AS), data transfer acknowledge (DTACK), and bus grant acknowledge (BGACK) are negated before issuing its own BGACK. The negation of the address strobe indicates that the previous master has completed its cycle, while the negation of bus grant acknowledge indicates that the previous master has released the bus. (If address strobe is asserted no device is allowed to "break into" a cycle.) The negation of data transfer acknowledge indicates the previous slave has terminated its connection to the previous master. In some applications data transfer acknowledge may not be required. In this case the devices would use the address strobe. When bus grant acknowledge is issued the device is bus master. Only after the bus cycle(s) is (are) completed should bus grant acknowledge be negated to terminate bus mastership.

The bus request from the granted device should be dropped after bus grant acknowledge is asserted. If a bus request is still pending, another bus grant will be asserted within a few clocks of the negation of bus grant. Refer to Bus Arbitration Control section. The processor does not perform any external bus cycles before it reasserts bus grant.

BUS ARBITRATION CONTROL. The bus arbitration control unit in the R68000 is implemented with a finite state machine. A state diagram of this machine is shown in Figure 15. All asynchronous signals to the R68000 are synchronized before being used internally. This synchronization is accomplished in a maximum of one cycle of the system clock, assuming that the asynchronous input setup time (#47) has been met (see Figure 16). The input signal is sampled on the falling edge of the clock and is valid internally after the next falling edge. If \overline{BR} and \overline{BGACK} meet the asynchronous set-up time tASI (#47), then tBGKBR (#37A) can be ignored. If \overline{BR} and \overline{BGACK} are asserted asynchronously with respect to the clock, \overline{BGACK} has to be asserted before \overline{BR} is negated.

As shown in Figure 15, input signals labeled R and A are internally synchronized on the bus request and bus grant acknowledge pins respectively. The bus grant output is labeled G and the internal three-state control signal T. If T is true, the address, data, and control buses are placed in a high-impedance state when AS is negated. All signals are shown in positive logic (active high) regardless of their true active voltage level.

State changes (valid outputs) occur on the next rising clock edge after the internal signal is valid.

A timing diagram of the bus arbitration sequence during a processor bus cycle is shown in Figure 17. The bus arbitration sequence while the bus is inactive (i.e., executing internal operations such as a multiply instruction) is shown in Figure 18.

If a bus request (\overline{BR}) is made at a time when the MPU has already begun a bus cycle but AS has not been asserted (bus state S0), BG will not be asserted on the next rising edge. Instead BG will be delayed until the second rising edge following its internal assertion. This sequence is shown in Figure 19.

BUS ERROR AND HALT OPERATION. In a bus architecture that requires a handshake from an external device, the possibility exists that the handshake might not occur. Since different systems will require a different maximum response time, a bus error input is provided.

External circuitry must be used to determine the duration between address strobe and data transfer acknowledge before issuing a bus error signal. When a bus error signal is received, the processor has two options: initiate a bus error exception sequence or try running the bus cycle again.

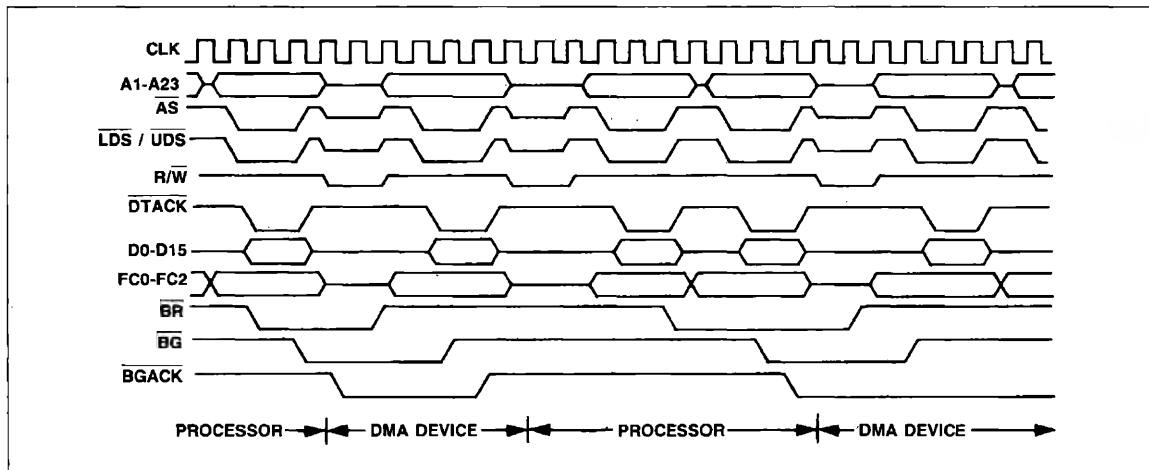


Figure 14. Bus Arbitration Cycle Timing Diagram

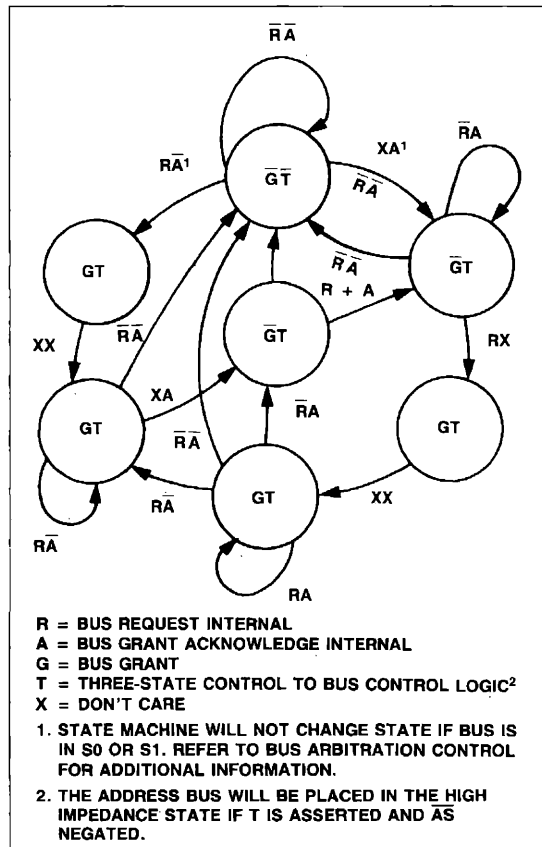


Figure 15. State Diagram of R68000 Bus Arbitration Unit

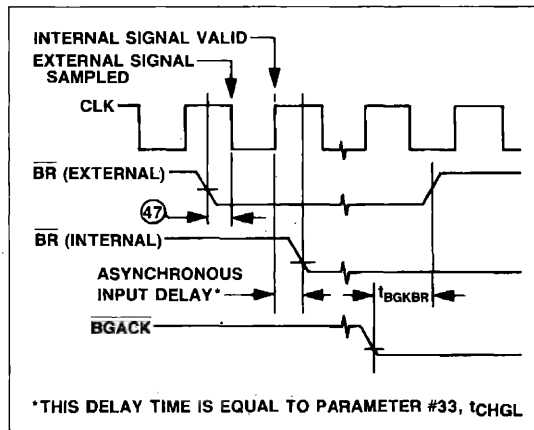


Figure 16. Timing Relationship of External Asynchronous Inputs to Internal Signals

Bus Error Operation. When \overline{BERR} is asserted, the current bus cycle is terminated. If \overline{BERR} is asserted before the falling edge of S2, AS will be negated in S7 in either a read or write cycle. As long as \overline{BERR} remains asserted, the data and address buses will be in the high-impedance state. When \overline{BERR} is negated, the processor will begin stacking for exception processing. Figure 20 is a timing diagram for the exception sequence. The sequence is composed of the following elements:

1. stacking the program counter and status register,
2. stacking the error information,
3. reading the bus error vector table entry, and
4. executing the bus error handler routine.

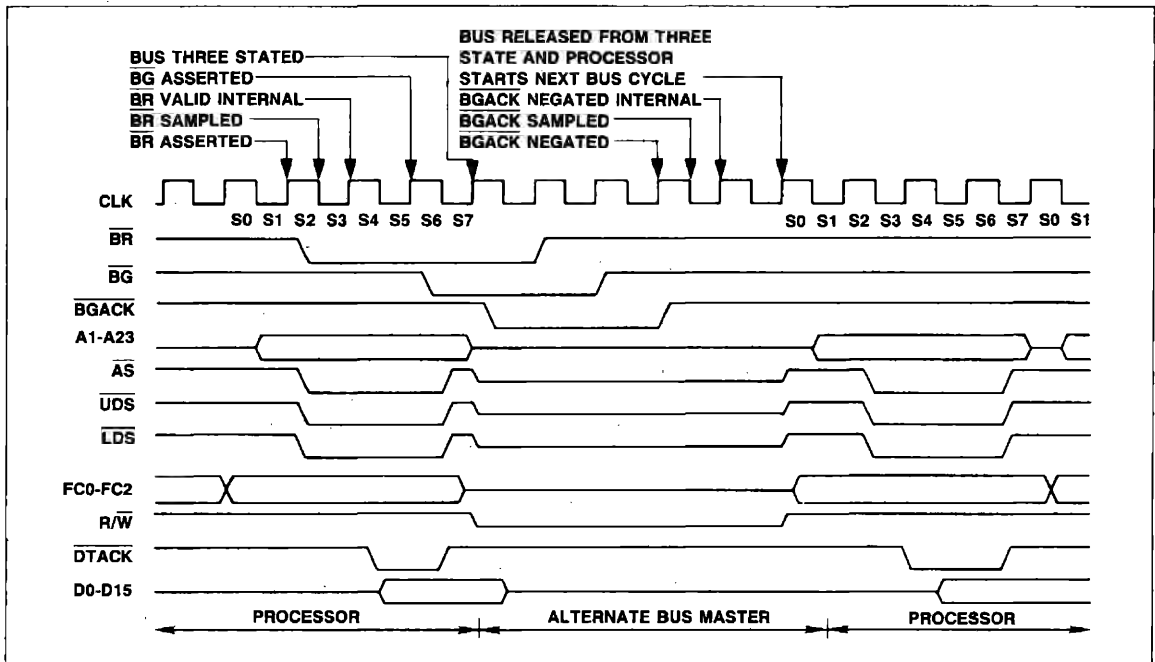


Figure 17. Bus Arbitration During Processor Bus Cycle

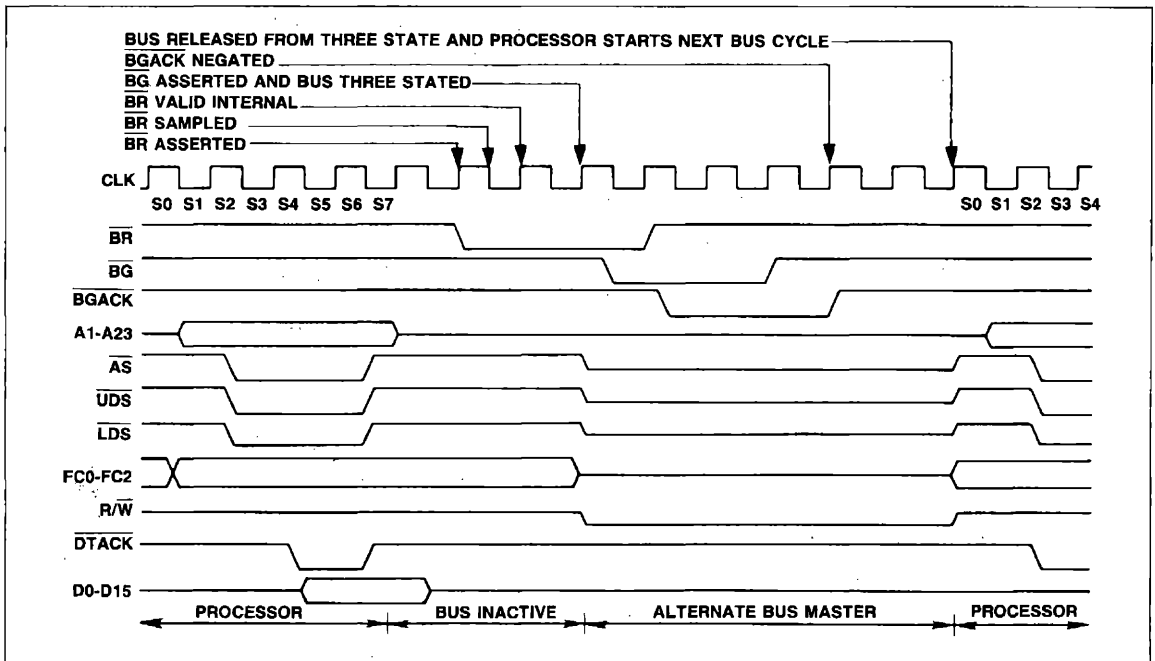


Figure 18. Bus Arbitration with Bus Inactive

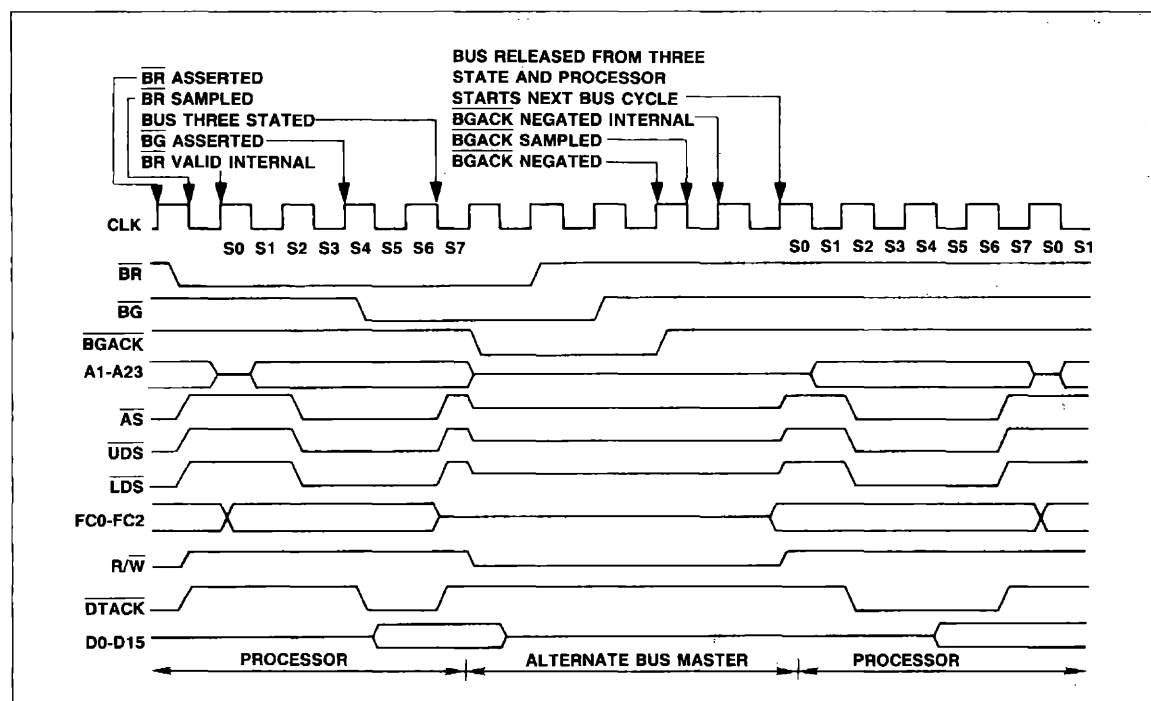


Figure 19. Bus Arbitration During Processor Bus Cycle Special Case

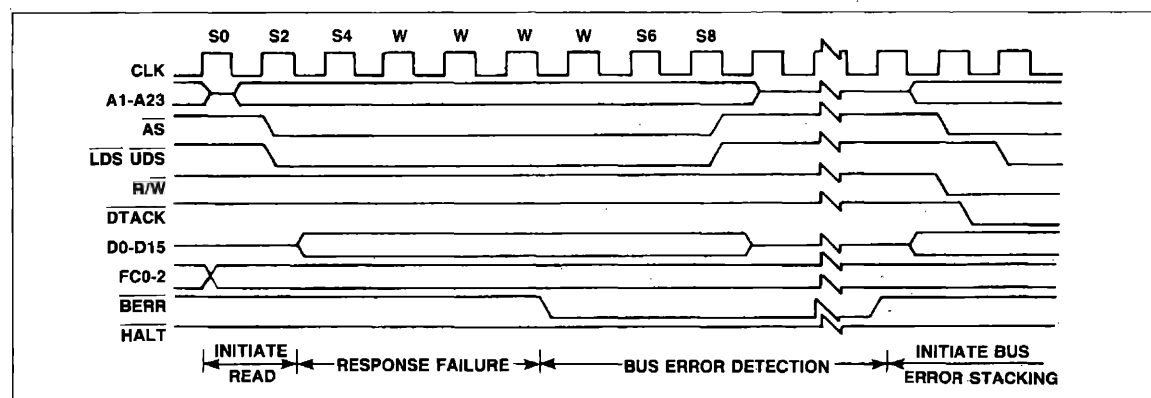


Figure 20. Bus Error Timing Diagram

The stacking of the program counter and the status register is identical to the interrupt sequence. Several additional items are stacked when a bus error occurs. These items are used to determine the nature of the error and correct it, if possible. The bus error vector is vector number two located at address \$000008. The processor loads the new program counter from this location. A software bus error handler routine is then executed by the processor. Refer to EXCEPTION PROCESSING for additional information.

Re-Running the Bus Cycle. When, during a bus cycle, the processor receives a $\overline{\text{BERR}}$, and $\overline{\text{HALT}}$ is being driven by an external device, the processor enters the re-run sequence. Figure 21 is a timing diagram for re-running the bus cycle.

The processor terminates the bus cycle, then puts the address and data output lines in the high-impedance state. The processor remains "halted" and will not run another bus cycle until external logic negates $\overline{\text{HALT}}$. Then the processor will re-run the previous bus cycle using the same address, the same function codes, the same data (for a write operation), and the same controls. $\overline{\text{BERR}}$ should be negated at least one clock cycle before $\overline{\text{HALT}}$ is negated.

Note

The processor will not re-run a read-modify-write cycle. This restriction is made to guarantee that the entire cycle runs correctly and that the write operation of a Test-and-Set operation is performed without ever releasing AS. If $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ are asserted during a read-modify-write bus cycle, a bus error operation results.

Halt Operation with No Bus Error. The $\overline{\text{HALT}}$ input signal to the R68000 performs a Halt/Run/Single-Step function in a similar fashion to the R6500 halt functions. When the $\overline{\text{HALT}}$ signal is constantly active the processor "halts" (does nothing) and when the $\overline{\text{HALT}}$ signal is constantly inactive the processor "runs" (does something).

The single-step mode, derived from correctly timed transitions on the $\overline{\text{HALT}}$ signal input, forces the processor to execute a single bus-cycle by entering the "run" mode until the processor starts a bus cycle then changing to the "halt" mode. Thus, the single-step mode allows the user to proceed through (and therefore debug) processor operations one bus cycle at a time.

Figure 22 details the timing required for correct single-step operations. Some care must be exercised to avoid harmful interactions between $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ when using the single cycle mode as a debugging tool. This is also true of interactions between the $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ lines since these can reset the machine.

When the processor completes a bus cycle after recognizing that $\overline{\text{HALT}}$ is active, most three-state signals are put in the high-impedance state. These include:

1. address lines, and
2. data lines.

This is required for correct performance of the re-run bus cycle operation.

Honoring the halt request has no effect on bus arbitration. Only the bus arbitration function removes the control signals from the bus.

Total debugging flexibility is derived from the software debugging package, the halt function, and the hardware trace capability. These processor capabilities allow the hardware debugger to trace single bus cycles or single instructions at a time.

Double Bus Faults. When a bus error exception occurs, the processor will attempt to stack several words containing information about the state of the machine. If a bus error exception occurs during the stacking operation, there have been two bus errors in a row, or a double bus fault. A double bus fault causes the processor to halt. Once a bus error exception has occurred, any bus error exception occurring before the execution of the next instruction constitutes a double bus fault.

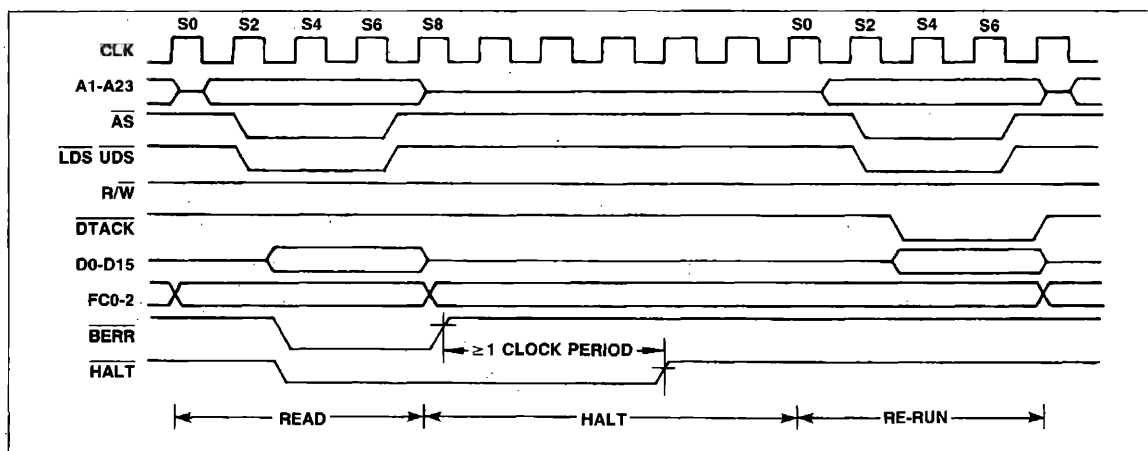


Figure 21. Re-Run Bus Cycle Timing Diagram

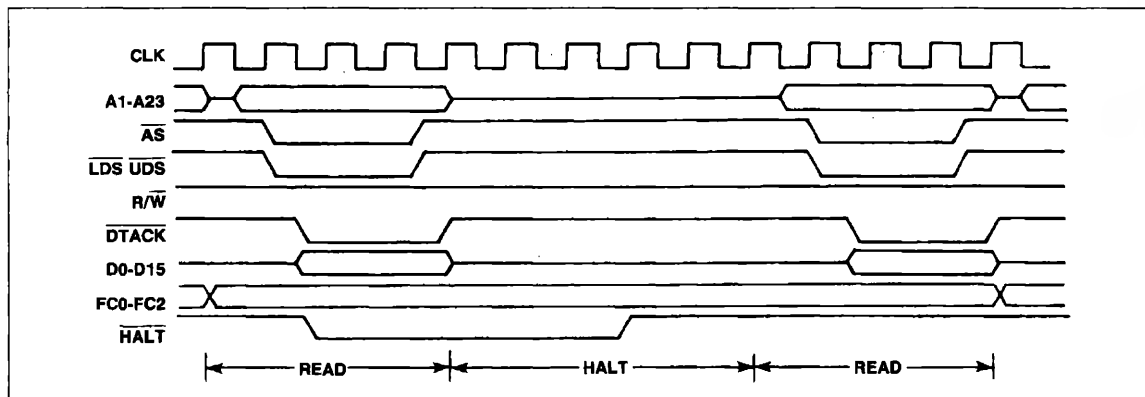


Figure 22. Halt Signal Timing Waveforms

Note that a bus cycle which is re-run does not constitute a bus error exception, and does not contribute to a double bus fault. This means that as long as the external hardware requests it, the processor will continue to re-run the same bus cycle.

The bus error ($\overline{\text{BERR}}$) pin also has an effect on processor operation after the processor receives an external reset input. The processor reads the vector table after a reset to determine the address to start program execution. If a bus error occurs while reading the vector table (or at any time before the first instruction is executed), the processor reacts as if a double bus fault has occurred and it halts. Only an external reset will start a halted processor.

RESET OPERATION. The reset signal is a bidirectional signal that allows either the processor or an external signal to reset the system. Figure 23 is a timing diagram for reset operations. Both $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ must be applied to ensure total reset of the processor.

When the $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ are driven by an external device the entire system, including the processor, is reset. The processor responds by reading the reset vector table entry (vector number zero, address \$0000000) and loads it into the supervisor stack pointer (SSP). Vector table entry number one at address \$0000004 is read next and loaded into the program counter. The processor initializes the status register to an interrupt level of seven, with no other register being affected.

Execution of the RESET instruction drives the reset pin low for 124 clock periods. In this case, the processor is trying to reset the rest of the system. The internal state of the processor, including the processor's internal registers and the status register, is unaffected by the execution of a RESET instruction. All external devices connected to the reset line will be reset at the completion of the RESET instruction.

Asserting $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ for 10 clock cycles will cause a processor reset, except when V_{cc} is initially applied to the processor. In this case, an external reset must be applied for 100 milliseconds.

THE RELATIONSHIP OF $\overline{\text{DTACK}}$, $\overline{\text{BERR}}$, AND $\overline{\text{HALT}}$

In order to properly control termination of a bus cycle for a re-run or a bus error condition, $\overline{\text{DTACK}}$, $\overline{\text{BERR}}$, and $\overline{\text{HALT}}$ should be asserted and negated on the rising edge of R68000 clock. This will assure that when two signals are asserted simultaneously, the required setup time (#47) for both of them will be met during the same bus state.

This, or some equivalent precaution, should be designed external to the R68000. Parameter #48 is intended to ensure this operation in a totally asynchronous system, and may be ignored if the above conditions are met.

The preferred bus cycle terminations may be summarized as follows (case numbers refer to Table 4):

Normal Termination: $\overline{\text{DTACK}}$ occurs first (case 1).

Halt Termination: $\overline{\text{HALT}}$ is asserted at same time, or precedes $\overline{\text{DTACK}}$ (no $\overline{\text{BERR}}$) cases 2 and 3.

Bus Error Termination: $\overline{\text{BERR}}$ is asserted in lieu of, at same time, or preceding $\overline{\text{DTACK}}$ (case 4); $\overline{\text{BERR}}$ negated at same time, or after $\overline{\text{DTACK}}$.

Re-Run Termination: $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ asserted in lieu of, at the same time, or before $\overline{\text{DTACK}}$ (cases 6 and 7); $\overline{\text{HALT}}$ must be negated at least one cycle after $\overline{\text{BERR}}$. (Case 5 indicates $\overline{\text{BERR}}$ may precede $\overline{\text{HALT}}$ which allows fully asynchronous assertion).

Table 4 details the resulting bus cycle termination under various combinations of control signal sequences. The negation of these same control signals under several conditions is shown in Table 5. ($\overline{\text{DTACK}}$ is assumed to be negated normally in all cases; for best results, both $\overline{\text{DTACK}}$ and $\overline{\text{BERR}}$ should be negated when address strobe is negated).

Example A: A system uses a watch-dog timer to terminate accesses to unpopulated address space. The timer asserts $\overline{\text{DTACK}}$ and $\overline{\text{BERR}}$ simultaneously after timeout (case 4).

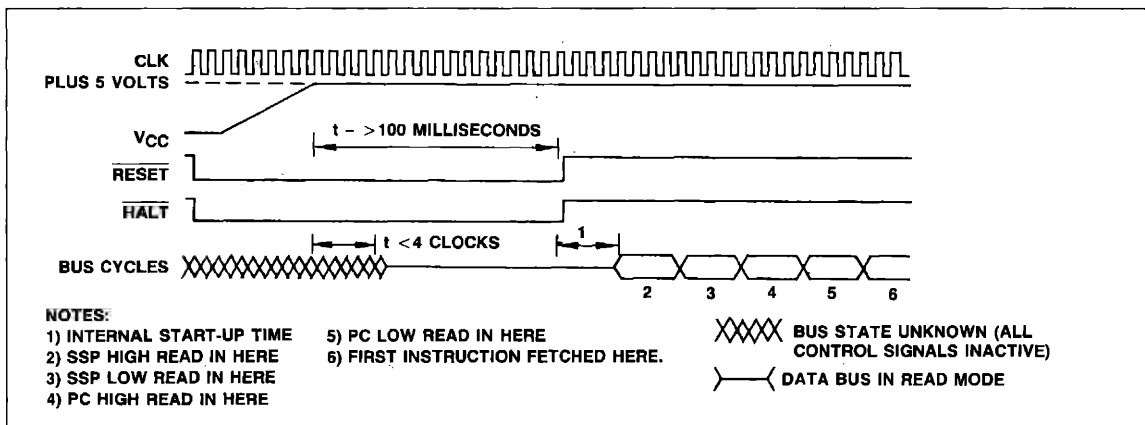


Figure 23. Reset Operation Timing Diagram

Example B: A system uses error detection on RAM contents. Designer may (a) delay DTACK until data verified, and return BERR and HALT simultaneously to re-run error cycle (case 6), or if valid, return DTACK (case 1); (b) delay DTACK until data verified and return BERR at same time as DTACK if data in error (case 4).

The BERR signal is allowed to be asserted after the DTACK signal is asserted. BERR must be asserted within the time given as parameter #48 after DTACK is asserted in any asynchronous system to insure proper operation. If this maximum delay time is violated, the processor may exhibit erratic behavior.

ASYNCHRONOUS VERSUS SYNCHRONOUS OPERATION

Asynchronous Operation

To achieve clock frequency independence at a system level, the R68000 can be used in an asynchronous manner. This entails using only the bus handshake lines (AS, UDS, LDS, DTACK, BERR, HALT, and VPA) to control the data transfer. Using this method, AS signals the start of a bus cycle and the data strobes are used as a condition for valid data on a write cycle. The slave device (memory or peripheral) then responds by placing the requested data on the data bus for a read cycle or latching data on a write cycle and asserting the data transfer acknowledge signal (DTACK) to terminate the bus cycle. If no slave responds or the access is invalid, external control logic asserts the BERR, or BERR and HALT, signal to abort or rerun the bus cycle.

The DTACK signal is allowed to be asserted before the data from a slave device is valid on a read cycle. The length of time that DTACK may precede data is given as parameter #31 (See Figure 45) and it must be met in any asynchronous system to insure that valid data is latched into the processor. Notice that there is no maximum time specified from the assertion of AS to the assertion of DTACK. This is because the MPU will insert wait cycles of one clock period each until DTACK is recognized.

Synchronous Operation

To allow for those systems which use the system clock as a signal to generate DTACK and other asynchronous inputs, the asynchronous inputs setup time is given as parameter #47. If this setup is met on an input, such as DTACK, the processor is guaranteed to recognize that signal on the next falling edge of the system clock. However, the converse is not true—if the input signal does not meet the setup time it is not guaranteed not to be recognized. In addition, if DTACK is recognized on a falling edge, valid data will be latched into the processor (on a read cycle) on the next falling edge provided that the data meets the setup time given as parameter #27. Given this, parameter #31 may be ignored. Note that if DTACK is asserted, with the required setup time, before the falling edge of S4, no wait states will be incurred and the bus cycle will run at its maximum speed of four clock periods.

In order to assure proper operation in a synchronous system when BERR is asserted after DTACK, the following conditions must be met. Within one clock cycle after DTACK was recognized, BERR must meet the setup time parameter #27A prior to the falling edge of the next clock. The setup time is critical to proper operation, and the R68000 may exhibit erratic behavior if it is violated.

Note

During an active bus cycle, VPA and BERR are sampled on every falling edge of the clock starting with S0. DTACK is sampled on every falling edge of the clock starting with S4 and data is latched on the falling edge of S6 during a read. The bus cycle will then be terminated in S7 except when BERR is asserted in the absence of DTACK, in which case it will terminate one clock cycle later in S9.

Table 4. \overline{DTACK} , \overline{BERR} , \overline{HALT} Assertion Results

Case No.	Control Signal	Asserted on Rising Edge of State		Result
		N	N + 2	
1	\overline{DTACK} \overline{BERR} \overline{HALT}	A NA NA	S X X	Normal cycle terminate and continue.
2	\overline{DTACK} \overline{BERR} \overline{HALT}	A NA A	S X S	Normal cycle terminate and halt. Continue when \overline{HALT} removed.
3	\overline{DTACK} \overline{BERR} \overline{HALT}	NA NA A	A NA S	Normal cycle terminate and halt. Continue when \overline{HALT} removed.
4	\overline{DTACK} \overline{BERR} \overline{HALT}	X A NA	X S NA	Terminate and take bus error trap.
5	\overline{DTACK} \overline{BERR} \overline{HALT}	NA A NA	X S A	Terminate and re-run.
6	\overline{DTACK} \overline{BERR} \overline{HALT}	X A A	X S S	Terminate and re-run when \overline{HALT} removed.
7	\overline{DTACK} \overline{BERR} \overline{HALT}	NA NA A	X A S	Terminate and re-run when \overline{HALT} removed.

Legend:
N — the number of the current even bus state (e.g., S4, S6, etc.)
A — signal is asserted in this bus state
NA — signal is not asserted in this state
X — don't care
S — signal was asserted in previous state and remains asserted in this state

Table 5. \overline{BERR} AND \overline{HALT} Negation Results

Conditions of Termination in Table 4-4	Control Signal	Negated on Rising Edge of State		Results — Next Cycle
		N	N + 2	
Bus Error	\overline{BERR} \overline{HALT}	● or ● ● or ●	●	Takes bus error trap.
Re-run	\overline{BERR} \overline{HALT}	● or ● ●	●	Illegal sequence; usually traps to vector number 0.
Re-run	\overline{BERR} \overline{HALT}	●	●	Re-runs the bus cycle.
Normal	\overline{BERR} \overline{HALT}	● or ●	●	May lengthen next cycle.
Normal	\overline{BERR} \overline{HALT}	● or ●	● or none	If next cycle is started it will be terminated as a bus error.

● = Signal is negated in this bus state.

PROCESSING STATES

The following paragraphs describe the actions of the R68000 which are outside the normal processing associated with the execution of instructions. The functions of the bits in the supervisor portion of the status register are covered: the supervisor/user bit, the trace enable bit, and the processor interrupt priority mask. The sequence of memory references and actions taken by the processor on exception conditions are detailed.

The R68000 is always in one of three processing states: normal, exception, or halted. The normal processing state associated with instruction execution; the memory references are to fetch instructions and operands, and to store results. A special case of the normal state is the stopped state which the processor enters when a STOP instruction is executed. In this state, no further references are made.

The exception processing state is associated with interrupts, trap instructions, tracing and other exceptional conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

The halted processing state is an indication of a catastrophic hardware failure. For example, if during the exception processing of a bus error another bus error occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

PRIVILEGE STATES

The processor operates in one of two states of privilege: the "user" state or the "supervisor" state. The privilege state determines legal operations. It is used to choose between the supervisor stack pointer and the user stack pointer in instruction references, and by the external memory management device to control and translate accesses.

The privilege state is a mechanism for providing security in a computer system by allowing most programs to execute in user state. In this state, the accesses are controlled, and the effects on other parts of the system are limited. Programs should access only their own code and data areas, and ought to be restricted from accessing information.

The operating system which executes in the supervisor state, has access to all resources and performs the overhead tasks for the user state programs.

SUPERVISOR STATE. The supervisor state is the higher state of privilege. For instruction execution, the supervisor state is determined by asserting (high) the S-bit of the status register. All instructions can be executed in the supervisor state. The bus cycles generated by instructions executed in the supervisor state are classified as supervisor references. While the processor is in the supervisor privilege state, those instructions which use either the system stack pointer implicitly or address register seven explicitly access the supervisor stack pointer.

All exception processing is done in the supervisor state, regardless of the setting of the S-bit. The bus cycles generated during exception processing are classified as supervisor references. All stacking operations during exception processing use the supervisor stack pointer.

USER STATE. The user state is the lower state of privilege. For instruction execution, the user state is determined by negating (low) the S-bit of the status register.

Most instructions execute the same in user state as in the supervisor state. However, some instructions which have important system effects are made privileged. User programs are not permitted to execute the STOP instruction, or the RESET instruction. To ensure that a user program cannot enter the supervisor state except in a controlled manner, the instructions which modify the whole state register are privileged. To aid in debugging programs which are to be used as operating systems, the move to user stack pointer (MOVE to USP) and move from user stack pointer (MOVE from USP) instructions are also privileged.

The bus cycles generated by an instruction executed in user state are classified as user state references. This allows an external memory management device to translate the address and to control access to protected portions of the address space. While the processor is in user privilege state, those instructions which use either the system stack pointer implicitly or address register seven explicitly, access the user stack pointer.

PRIVILEGE STATE CHANGES. Once the processor is in the user state and executing instructions, only exception processing can change the privilege state. During exception processing, the current setting of the S-bit of the status register is saved and the S-bit is asserted, putting the processing in the supervisor state. Therefore, when instruction execution resumes to process the exception, the processor is in the supervisor privilege state.

REFERENCE CLASSIFICATION. When the processor makes a reference, it classifies the kind of reference being made by using the encoding on the three function code output lines. This allows external translation of addresses, control of access, and differentiation of special processor states, such as interrupt acknowledge. Table 6 lists the classification of references.

Table 6. Reference Classification

Function Code Output			Reference Class
FC2	FC1	FC0	
0	0	0	(Unassigned)
0	0	1	User Data
0	1	0	User Program
0	1	1	(Unassigned)
1	0	0	(Unassigned)
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	Interrupt Acknowledge

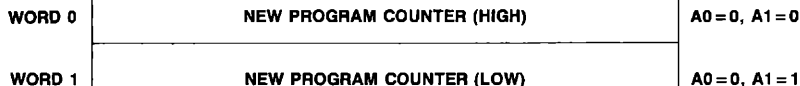
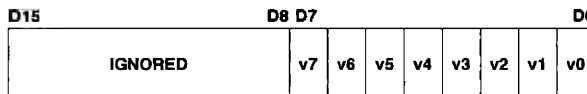


Figure 24. Exception Vector Format



WHERE:
v7 IS THE MSB OF THE VECTOR NUMBER
v0 IS THE LSB OF THE VECTOR NUMBER

Figure 25. Peripheral Vector Number Format

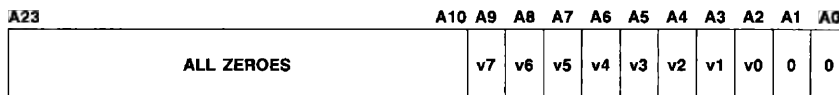


Figure 26. Address Translated From 8-Bit Vector Number

EXCEPTION PROCESSING

Before discussing the details of interrupts, traps, and tracing, a general description of exception processing is in order. The processing of an exception occurs in four steps, with variations for different exception causes. During the first step, a temporary copy of the status register is made, and the status register is set for exception processing. In the second step the exception vector is determined, and the third step is the saving of the current processor contents. In the fourth step a new context is obtained, and the processor switches to instruction processing.

EXCEPTION VECTORS. Exception vectors are memory locations from which the processor fetches the address of a routine which will handle that exception. All exception vectors are two words in length (Figure 24), except for the reset vector, which is four words. All exception vectors lie in the supervisor data space, except for the reset vector which is in the supervisor program space. A vector number is an eight-bit number which, when multiplied by four, gives the address of an exception vector. Vector numbers are generated internally or externally, depending on the cause of the exception. In the case of interrupts, during the interrupt acknowledge bus cycle, a peripheral provides an 8-bit vector number (Figure 25) to the processor on data bus lines D0 through D7. The processor translates the vector number into a full 24-bit address, as shown in Figure 26. The memory layout for exception vectors is given in Table 7.

As shown in Table 7, the memory layout is 512 words long (1024 bytes). It starts at address 0 and proceeds through

address 1023. This provides 255 unique vectors; some of these are reserved for TRAPS and other system functions. Of the 255, there are 192 reserved for user interrupt vectors. However, there is no protection on the first 64 entries, so user interrupt vectors may overlap at the discretion of the systems designer.

KINDS OF EXCEPTIONS. Exceptions can be generated either internally or externally. Externally generated exceptions include interrupts (IRQ), bus error (BERR), and reset (RESET) requests. Interrupts are requests from peripheral devices for processor action while BERR and RESET inputs are used for access control and processor restart. Internally generated exceptions come from instructions, from address errors, or from tracing. The trap (TRAP), trap on overflow (TRAPV), check register against bounds (CHK) and divide (DIV) instructions can all generate exceptions as part of their instruction execution. In addition, illegal instructions, word fetches from odd addresses and privilege violations cause exceptions. Tracing behaves like a very high priority, internally generated interrupt after each instruction execution.

EXCEPTION PROCESSING SEQUENCE. Exception processing occurs in four identifiable steps. In the first step, an internal copy is made of the status register. After the copy is made, the S-bit is asserted, putting the processor into the supervisor privilege state. Also, the T-bit is negated which will allow the exception handler to execute unhindered by tracing. For the reset and interrupt exceptions, the interrupt priority mask is also updated.

Table 7. Exception Vector Assignment

Vector Number(s)	Address			Assignment
	Dec	Hex	Space	
0	0	000	SP	Reset: Initial SSP
—	4	004	SP	Reset: Initial PC
2	8	008	SD	Bus Error
3	12	00C	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Divide
6	24	018	SD	CHK Instruction
7	28	01C	SD	TRAPV Instruction
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator
11	44	02C	SD	Line 1111 Emulator
12*	48	030	SD	(Unassigned, reserved)
13*	52	034	SD	(Unassigned, reserved)
14*	56	038	SD	(Unassigned, reserved)
15	60	03C	SD	Uninitialized Interrupt Vector
16-23*	64	04C	SD	(Unassigned, reserved)
	95	05F		—
24	96	060	SD	Spurious Interrupt
25	100	064	SD	Level 1 Interrupt Autovector
26	104	068	SD	Level 2 Interrupt Autovector
27	108	06C	SD	Level 3 Interrupt Autovector
28	112	070	SD	Level 4 Interrupt Autovector
29	116	074	SD	Level 5 Interrupt Autovector
30	120	078	SD	Level 6 Interrupt Autovector
31	124	07C	SD	Level 7 Interrupt Autovector
32-47	128	080	SD	TRAP Instruction Vectors
	191	0BF		—
48-63*	192	0C0	SD	(Unassigned, reserved)
	255	0FF		—
64-255	256	100	SD	User Interrupt Vectors
	1023	3FF		—

*Vector numbers 12, 13, 14, 16 through 23, and 48 through 63 are reserved for future enhancements. No user peripheral devices should be assigned these numbers.

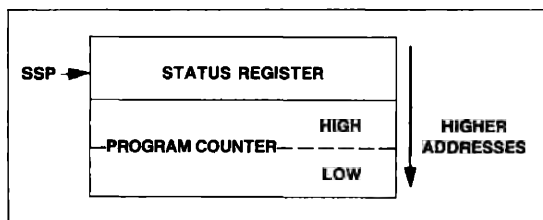


Figure 27. Exception Stack Order (Groups 1 and 2)

In the second step, the vector number of the exception is determined. For interrupts, the vector number is obtained by a processor fetch, classified as an interrupt acknowledge. For all other exceptions, internal logic provides the vector number. This vector number is then used to generate the address of the exception vector.

The third step is to save the current processor status except for the reset exception. The current program counter value and the saved copy of the status register are stacked using the supervisor stack pointer as shown in Figure 27. The program counter value stacked usually points to the next unexecuted instruction; however, for bus error and address error, the value stacked for the program counter is unpredictable, and may be incremented from the address of the instruction which caused the error. Additional information defining the current context is stacked for the bus error and address error exceptions.

The last step is the same for all exceptions. The new program counter value is fetched from the exception vector. The processor then resumes instruction execution. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execution is started.

MULTIPLE EXCEPTIONS. These paragraphs describe the processing which occurs when multiple exceptions arise simultaneously. Exceptions can be grouped according to their occurrence and priority. The Group 0 exceptions are reset, bus error, and address error. These exceptions cause the instruction currently being executed to be aborted, and the exception processing to commence within two clock cycles. The Group 1 exceptions are trace and interrupt, as well as the privilege violations and illegal instructions. These exceptions allow the current instruction to execute to completion, but preempt the execution of the next instruction by forcing exception processing to occur (privilege violations and illegal instructions are detected when they are the next instruction to be executed). The Group 2 exceptions occur as part of the normal processing of instructions. The TRAP, TRAPV, CHK, and zero divide exceptions are in this group. For these exceptions, the normal execution of an instruction may lead to exception processing.

Group 0 exceptions have highest priority, while Group 2 exceptions have lowest priority. Within Group 0, reset has highest priority, followed by address error and then bus error. Within Group 1, trace has priority over external interrupts, which in turn takes priority over illegal instruction and privilege violation. Since only one instruction can be executed at a time, there is no priority relation within Group 2.

Table 8. Exception Grouping and Priority

Group	Exception	Processing
0	Reset Address Error Bus Error	Exception processing begins within two clock cycles.
1	Trace Interrupt Illegal Instruction Privilege Violation	Exception processing begins before the next instruction.
2	TRAP, TRAPV, CHK, Zero Divide	Exception processing is started by normal instruction execution

The priority relation between two exceptions determines which is taken first if the conditions for both arise simultaneously. Therefore, if a bus error occurs during a TRAP instruction, the bus error takes precedence, and the TRAP instruction processing is aborted. In another example, if an interrupt request occurs during the execution of an instruction while the T-bit is asserted, the trace exception has priority, and is processed first. Before instruction processing resumes, however, the interrupt exception is also processed, and instruction processing commences finally in the interrupt handler routine. Table 8 gives a summary of exception grouping and priority.

EXCEPTION PROCESSING DETAILED DISCUSSION

Exceptions have a number of sources, and each exception has a unique processing sequence. The following paragraphs detail the sources of exceptions, how each arises, and how each is processed.

RESET. The reset input provides the highest exception level. The processing of the reset signal is designed for system initiation, and recovery from catastrophic failure. Any processing in progress at the time of the reset is aborted and cannot be recovered: The processor is forced into the supervisor state and the trace state is forced off. The processor interrupt priority mask is set at level seven. The vector number is internally generated to reference the reset exception vector at location 0 in the supervisor program space. Because no assumptions can be made about the validity of register contents, in particular the supervisor stack pointer, neither the program counter nor the status register is saved. The address contained in the first two words of the reset exception vector is fetched as the initial supervisor stack pointer, and the address in the last two words of the reset exception vector is fetched as the initial program counter. Finally, instruction execution is started at the address in the program counter. The powerup/restart code should be pointed to by the initial program counter.

The RESET instruction does not cause loading of the reset vector, but does assert the reset line to reset external devices. This allows the software to reset the system to a known state and then continue processing with the next instruction.

INTERRUPTS. Seven levels of interrupt priorities are provided. Devices may be chained externally within interrupt priority levels, allowing an unlimited number of peripheral devices to interrupt the processor. Interrupt priority levels are numbered from one to seven, level seven being the highest priority. The status register contains a three-bit mask which indicates the current processor priority. Interrupts are inhibited for all priority levels less than or equal to the current processor priority.

An interrupt request is made to the processor by encoding the interrupt request level on the interrupt request lines; a zero indicates no interrupt request. Interrupt requests arriving at the processor do not face immediate exception processing, but are made pending. Pending interrupts are detected between instruction executions. If the priority of the pending interrupt is lower than or equal to the current processor priority, execution continues with the next instruction and the interrupt exception processing is postponed. (The recognition of level seven is slightly different, as explained in a following paragraph.)

If the priority of the pending interrupt is greater than the current processor priority, the exception processing sequence is started. First a copy of the status register is saved, and the privilege state is set to supervisor, then tracing is suppressed, and the processor priority level is set to the level of the interrupt being acknowledged. The processor fetches the vector number from the interrupting device, classifying the reference as an interrupt acknowledge and displaying the level number of the interrupt being acknowledged on the address bus. If external logic requests an automatic vectoring, the processor internally generates a vector number which is determined by the interrupt level number. If external logic indicates a bus error, the interrupt is taken to be spurious, and the generated vector number references the spurious interrupt vector. The processor then proceeds with the usual exception processing, saving the program counter and status register on the supervisor stack. The saved value of the program counter is the address of the instruction which would have been executed had the interrupt not been present. The content of the interrupt vector whose vector number was previously obtained is fetched and loaded into the program counter, and normal instruction execution commences in the interrupt handling routine. A flow chart for the interrupt acknowledge sequence is given in Figure 28, a timing diagram is given in Figure 29, and the interrupt exception timing sequence is shown in Figure 30.

Priority level seven is a special case. Level seven interrupts cannot be inhibited by the interrupt priority mask, thus providing a "non-maskable interrupt" capability. An interrupt is generated each time the interrupt request level changes from some lower level to level seven. Note that a level seven interrupt may still be caused by the level comparison if the request level is a seven and the processor priority is set to a lower level by an instruction.

UNINITIALIZED INTERRUPT. An interrupting device asserts VPA or provides an interrupt vector during an interrupt acknowledge cycle to the R68000. If the vector register has not been initialized, the responding R68000 Family peripheral will provide vector 15, the uninitialized interrupt vector. This provides a uniform way to recover from a programming error.

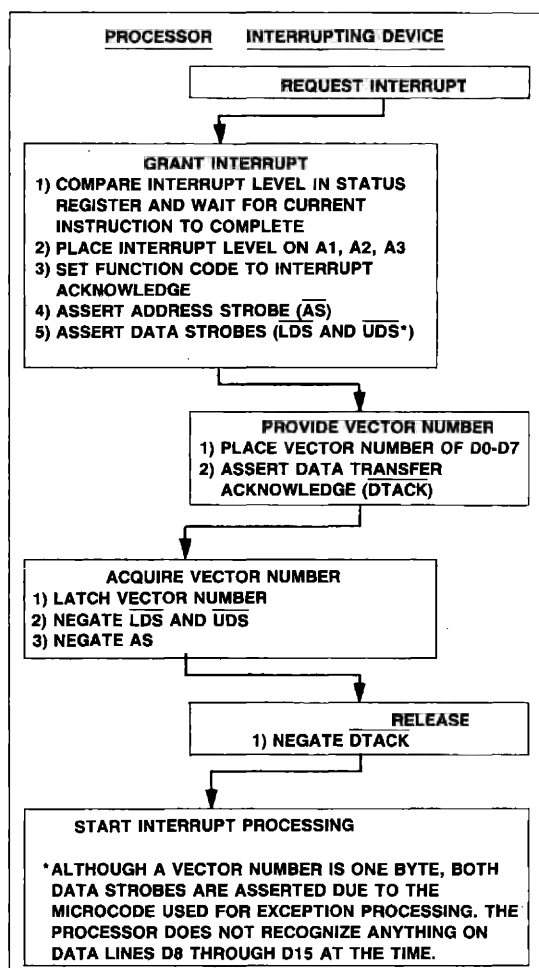


Figure 28. Interrupt Acknowledge Sequence Flow Chart

SPURIOUS INTERRUPT. If during the interrupt acknowledge cycle no device responds by asserting DTACK or VPA, the bus error line should be asserted to terminate the vector acquisition. The processor separates the processing of this error from bus error by fetching the spurious interrupt vector instead of the bus error vector. The processor then proceeds with the usual exception processing.

INSTRUCTION TRAPS. Traps are exceptions caused by instructions. They arise either from processor recognition of abnormal conditions during instruction execution, or from use of instructions whose normal behavior is trapping.

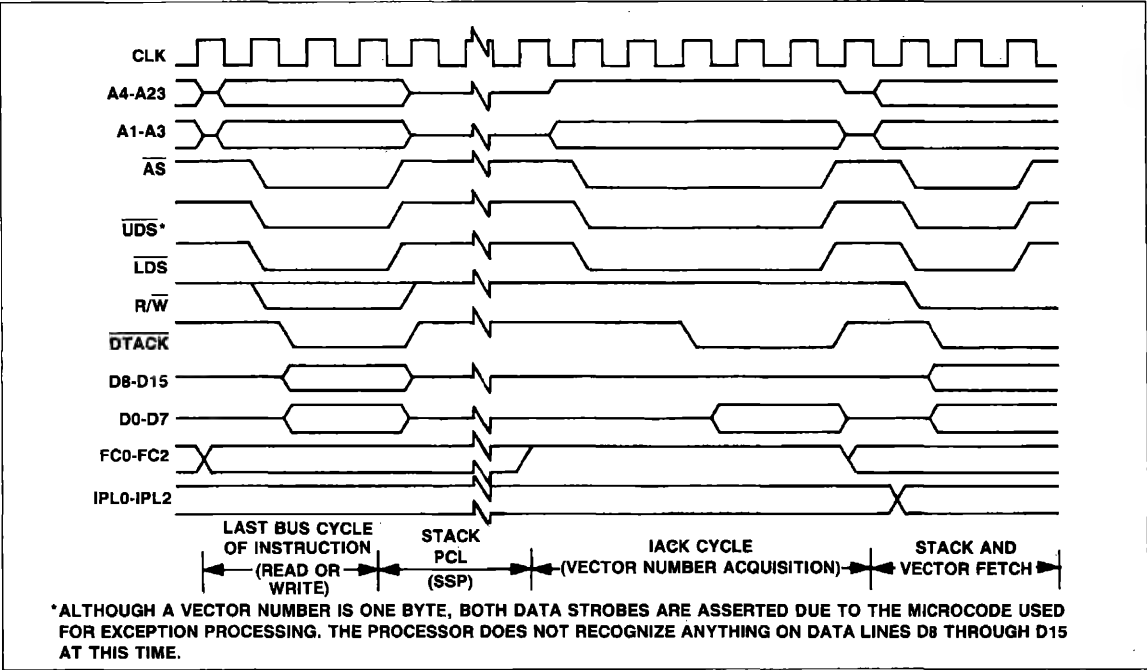


Figure 29. Interrupt Acknowledge Sequence Timing Diagram

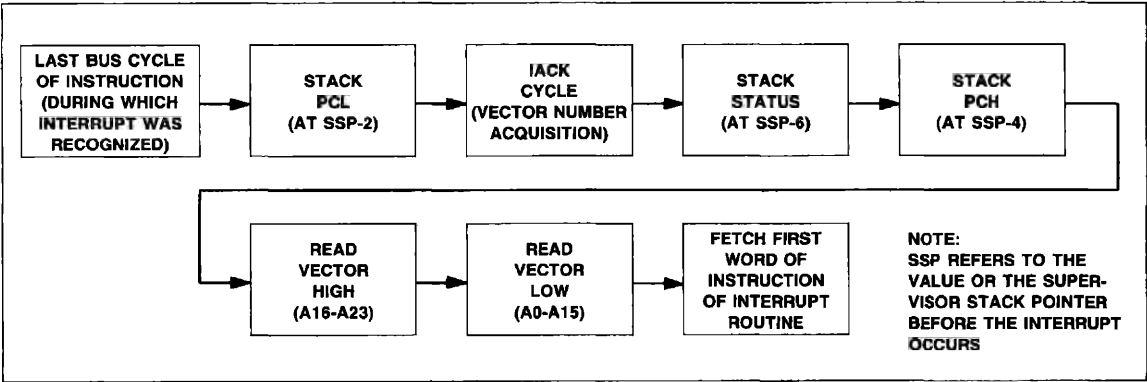


Figure 30. Interrupt Exception Timing Sequence

Some instructions are used specifically to generate traps. The TRAP instruction always forces an exception, and is useful for implementing system calls for user programs. The TRAPV and CHK instructions force an exception if the user program detects a runtime error, which may be an arithmetic overflow or a subscript out of bounds.

The signed divide (DIVS) and unsigned divide (DIVU) instructions will force an exception if a division operation is attempted with a divisor of zero.

ILLEGAL AND UNIMPLEMENTED INSTRUCTIONS. Illegal instruction refers to any of the word bit patterns which are not the bit pattern of the first word of a legal instruction. During instruction execution, if such an instruction is fetched, an illegal instruction exception occurs. Rockwell reserves the right to define instructions whose opcodes may be any of the illegal instructions. Three bit patterns will always force an illegal instruction trap on all R68000 Family compatible microprocessors. They are: \$4AFA, \$4AFB, and \$4AFC. Two of the patterns, \$4AFA and \$4AFB, are reserved for Rockwell system products. The third pattern, \$4AFC, is reserved for customer use.

Word patterns with bits 15 through 12 equaling 1010 or 1111 are distinguished as unimplemented instructions and separate exception vectors are given to these patterns to permit efficient emulation. This facility allows the operating system to detect program errors, or to emulate unimplemented instructions in software.

PRIVILEGE VIOLATIONS. In order to provide system security, various instructions are privileged. An attempt to execute one of the privileged instructions while in the user state will cause an exception. The privileged instructions are:

STOP	AND Immediate to SR
RESET	EOR Immediate to SR
RTE	OR Immediate to SR
MOVE USP	MOVE to SR

TRACING. To aid in program development, the R68000 includes a facility to allow instruction by instruction tracing. In the trace state, after each instruction is executed an exception is forced, allowing a debugging program to monitor the execution of the program under test.

The trace facility uses the T-bit in the supervisor portion of the status register. If the T-bit is negated (off), tracing is disabled, and instruction execution proceeds from instruction to instruction as normal. If the T-bit is asserted (on) at the beginning of the execution of an instruction, a trace exception will be generated after the execution of that instruction is completed. If the instruction is not executed, either because an interrupt is taken, or the instruction is illegal or privileged, the trace exception does not occur. The trace exception also does not occur if the instruction is aborted by a reset, bus error, or address error exception. If the instruction is indeed executed and an interrupt

is pending on completion, the trace exception is processed before the interrupt exception. If, during the execution of the instruction, an exception is forced by that instruction, the forced exception is processed before the trace exception.

As an extreme illustration of the above rules, consider the arrival of an interrupt during the execution of a TRAP instruction while tracing is enabled. First the trap exception is processed, then the trace exception, and finally the interrupt exception. Instruction execution resumes in the interrupt handler routine.

BUS ERROR. Bus error exceptions occur when the external logic requests that a bus error be processed by an exception. The current bus cycle which the processor is making is then aborted. Whether the processor was doing instruction or exception processing, that processing is terminated, and the processor immediately begins exception processing.

Exception processing for bus error follows the usual sequence of steps. The status register is copied, the supervisor state is entered, and the trace state is turned off. The vector number is generated to refer to the bus error vector. Since the processor was not between instructions when the bus error exception request was made, the context of the processor is more detailed. To save more of this context, additional information is saved on the supervisor stack. The program counter and the copy of the status register are of course saved. The value saved for the program counter is advanced by some amount, two to ten bytes beyond the address of the first word of the instruction which made the reference causing the bus error. If the bus error occurred during the fetch of the next instruction, the saved program counter has a value in the vicinity of the current instruction, even if the current instruction is a branch, a jump, or a return instruction. Besides the usual information, the processor saves its internal copy of the first word of the instruction being processed, and the address which was being accessed by the aborted bus cycle. Specific information about the access is also saved: whether it was a read or a write, whether the processor was processing an instruction or not, and the classification displayed on the function code outputs when the bus error occurred. The processor is processing an instruction if in the normal state or processing a Group 2 exception; the processor is not processing an instruction when processing a Group 0 or a Group 1 exception. Figure 31 illustrates how the information is organized on the supervisor stack. Although this information is not sufficient to effect full recovery from the bus error, it does allow software diagnosis. Finally, the processor commences instruction processing at the address contained in the vector. It is the responsibility of the error handler routine to clean up the stack and determine where to continue execution.

If a bus error occurs during the exception processing for a bus error, address error, or reset, the processor is halted, and all processing ceases. This simplifies the detection of catastrophic system failure, since the processor removes itself from the system rather than destroy all memory contents. Only the RESET pin can restart a halted processor.

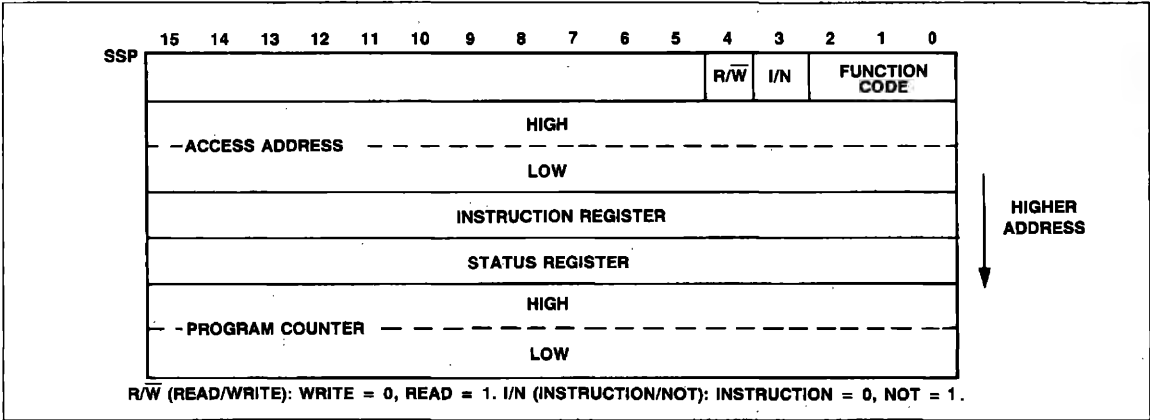


Figure 31. Supervisor Stack Order (Group 0)

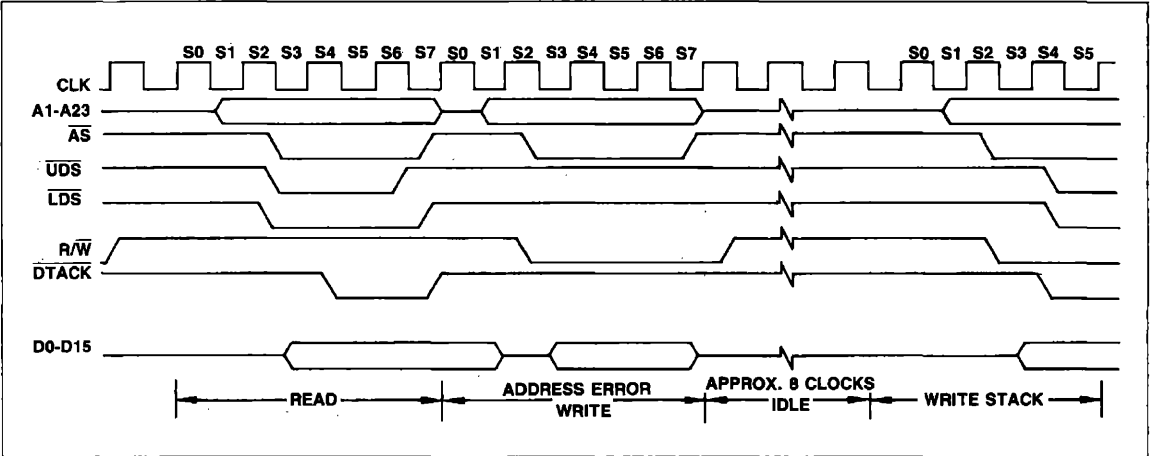


Figure 32. Address Error Timing

ADDRESS ERROR. Address error exceptions occur when the processor attempts to access a word or a long word operand or an instruction at an odd address. The effect is much like an internally generated bus error, so that the bus cycle is aborted, and the processor ceases whatever processing it is currently doing and begins exception processing. After exception processing commences, the sequence is the same as that for bus error including the information that is stacked, except that the vector number refers to the address error vector instead. Likewise, if an address error occurs during the exception processing for a bus error, address error, or reset, the processor is halted. As shown in Figure 32, an address error will execute a short bus cycle followed by an exception processing.

INTERFACE WITH R6500 PERIPHERALS

Rockwell's line of R6500 peripherals are directly compatible with the R68000. Some of these devices that are particularly useful are:

R6520	Peripheral Interface Adapter (PIA)
R6522	Versatile Interface Adapter (VIA)
R6545	CRT Controller (CRTC)
R6551	Asynchronous Communication Interface Adapter (ACIA)

To interface the synchronous R6500 peripherals with the asynchronous R68000, the processor modifies its bus cycle to meet the R6500 cycle requirements whenever an R6500 device address is detected. This is possible since both processors use memory mapped I/O. Figure 33 is a flow chart of the interface operation between the processor and R6500 devices. R6800 peripherals are also compatible with the R68000 processor.

DATA TRANSFER OPERATION

Three signals on the processor provide the R6500 interface. They are: enable (E), valid memory address (VMA), and valid Peripheral address (VPA). Enable corresponds to the E or $\Phi 2$ signal in existing R6500 systems. The bus frequency is one tenth of the incoming R68000 clock frequency. The timing of E allows 1 MHz peripherals to be used with an 8 MHz R68000. Enable has a 60/40 duty cycle; that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive VPA accesses on successive E pulses.

Figures 34 and 35 give a general R6500 to R68000 interface timing, while Figures 36 and 37 detail the specific timing parameters involved in the interface. At state zero (S0) in the cycle, the address bus is in the high-impedance state. A function code is asserted on the function code output lines. One-half clock later, in state 1, the address bus is released from the high-impedance state.

During state 2, the address strobe (\overline{AS}) is asserted to indicate that there is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write (R/W) signal is switched to a low (write) during state 2. One-half clock later, in state 3, the write data is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus. The processor now inserts wait states until it recognizes the assertion of VPA.

The VPA input signals the processor that the address on the bus is the address of an R6500 device (or an area reserved for R6500 devices) and that the bus should conform to the $\Phi 2$ transfer characteristics of the R6500 bus. Valid peripheral address (VPA) is derived by decoding the address bus, conditioned by address strobe (\overline{AS}). Chip select for the R6500 peripherals should be derived by decoding the address bus conditioned by VMA.

After the recognition of VPA, the processor assures that the Enable (E) is low, by waiting if necessary, and subsequently asserts VMA. Valid memory address is then used as part of the

chip select equation of the peripheral. This ensures that the R6500 peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the E signal. Figures 34 and 35 depict the best and worst case R6500 cycle timing. This cycle length is dependent strictly upon when VPA is asserted in relationship to the E clock.

If we assume that external circuitry asserts \overline{VPA} as soon as possible after the assertion of \overline{AS} , then VPA will be recognized as being asserted on the falling edge of S4. In this case, no "extra" wait cycles will be inserted prior to the recognition of VPA assertion and only the wait cycles inserted to synchronize with the E clock will determine the total length of the cycle. In any case, the synchronization delay will be some integral number of clock cycles within the following two extremes:

1. Best Case— \overline{VPA} is recognized as being asserted on the falling edge three clock cycles before E rises (or three clock cycles after E falls).
2. Worst Case— \overline{VPA} is recognized as being asserted on the falling edge two clock cycles before E rises (or four clock cycles after E falls).

Near the end of a read cycle, the processor latches the peripheral's data in state 6. For all cycles, the processor negates the address and data strobes one half clock cycle later in state 7, and the Enable signal goes low at this time. Another half clock later, the address bus is put in the high-impedance state. Upon write cycle completion, the data bus is put in the high-impedance state and the read/write signal is switched high. The peripheral logic must remove VPA within one clock after address strobe is negated.

\overline{DTACK} should not be asserted while \overline{VPA} is asserted. Note that the R68000 VMA is active low. This allows the processor to put its buses in the high-impedance state on DMA requests without inadvertently selecting peripherals.

INTERRUPT OPERATION

During an interrupt acknowledge cycle while the processor is fetching the vector, if \overline{VPA} is asserted, the R68000 will assert VMA and complete a normal R6500 read cycle as shown in Figure 38. The processor will then use an internally generated vector, called an autovector, that is a function of the interrupt being served. The seven autovectors are vector numbers 25 through 31 (decimal).

Autovectors operate in the same fashion (but are not restricted to) the R6500 interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with both the R6500 and the R68000's normal vectored interrupt, the interrupt service routine can be located anywhere in the address space. This is due to the fact that while the vector numbers are fixed, the contents of the vector table entries are assigned by the user.

Since \overline{VMA} is asserted during autovectored, the R6500 peripheral address decoding should prevent unintended accesses.

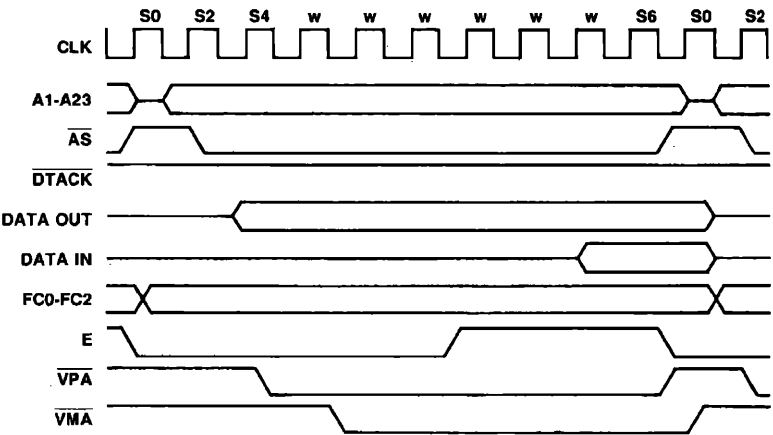


Figure 34. R68000 to R6500 Peripheral Timing—Best Case

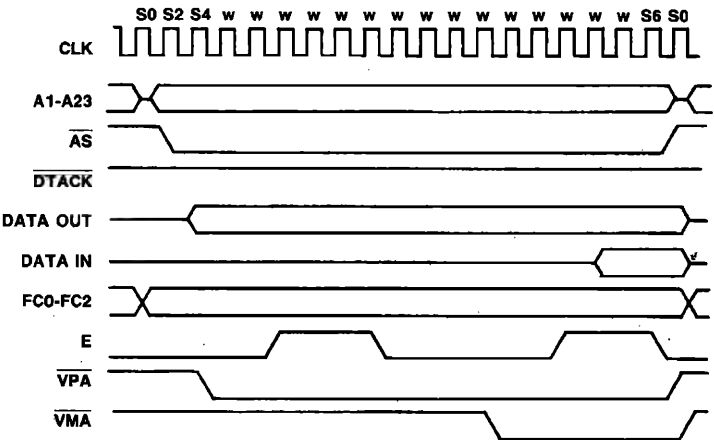
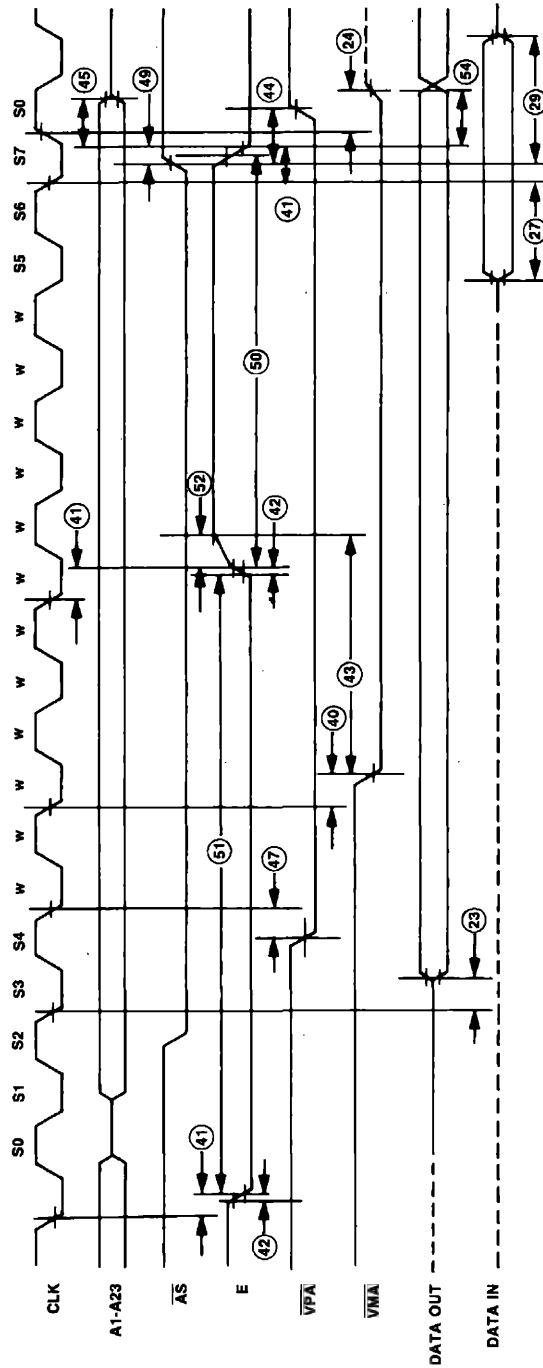


Figure 35. R68000 to R6500 Peripheral Timing—Worst Case



NOTES:
THIS FIGURE REPRESENTS THE BEST CASE R6500 TIMING WHERE \overline{VPA} FALLS BEFORE THE THIRD SYSTEM CLOCK CYCLE AFTER THE FALLING EDGE OF E.

THIS TIMING DIAGRAM IS INCLUDED FOR THOSE WHO WISH TO DESIGN THEIR OWN CIRCUIT TO GENERATE \overline{VMA} IT SHOWS THE BEST CASE POSSIBLY ATTAINABLE.

Figure 36. R6500 Timing—Best Case

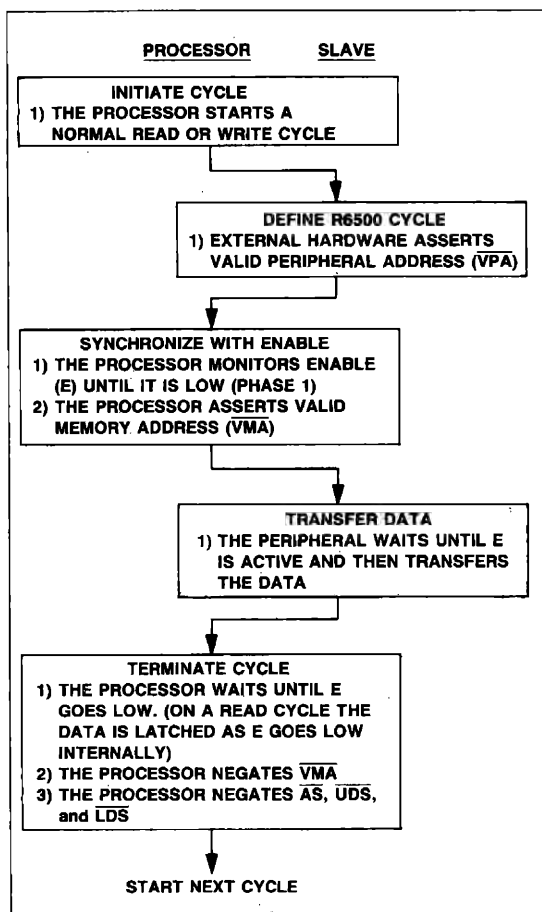


Figure 33. R6500 Interfacing Flow Chart

DATA TYPES AND ADDRESSING MODES

Five basic data types are supported. These data types are:

- Bits
- BCD Digits (4-bits)
- Bytes (8-bits)
- Word (16-bits)
- Long Words (32-bits)

In addition, operations on other data types such as memory addresses, status word data, etc., are provided for in the instruction set.

The 14 addressing modes, shown in Table 9, include six basic types:

- | | |
|-------------------|--------------------------|
| Register Direct | Program Counter Relative |
| Register Indirect | Implied |
| Absolute | Immediate |

Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting and indexing. Program counter relative mode can also be modified via indexing and offsetting.

Table 9. Addressing Modes

Mode	Generation
Register Direct Addressing Data Register Direct Address Register Direct	EA = Dn EA = An
Absolute Data Addressing Absolute Short Absolute Long	EA = (Next Word) EA = (Next Two Words)
Program Counter Relative Addressing Relative with Offset Relative with Index and Offset	EA = (PC) + d ₁₆ EA = (PC) + (Xn) + d ₈
Register Indirect Addressing Register Indirect Postincrement Register Indirect Predecrement Register Indirect Register Indirect with Offset Indexed Register Indirect with Offset	EA = (An) EA = (An), An ← An + N An ← An - N, EA = (An) EA = (An) + d ₁₆ EA = (An) + (Xn) + d ₈
Immediate Data Addressing Immediate Quick Immediate	DATA = Next Word(s) Inherent Data
Implied Addressing Implied Register	EA = SR, USP, SP, PC
NOTES: EA = Effective Address An = Address Register Dn = Data Register Xn = Address or Data Register used as Index Register SR = Status Register PC = Program Counter () = Contents of d ₈ = Eight-bit Offset (displacement) d ₁₆ = Sixteen-bit Offset (displacement) N = 1 for Byte, 2 for Words and 4 for Long Word. If An is the stack pointer and the operand size is byte, N = 2 to keep the stack pointer on a word boundary. ← = Replaces	

INSTRUCTION SET OVERVIEW

The R68000 instruction set is shown in Table 10. Some additional instructions are variations, or subsets, of these and they appear in Table 11. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned multiply and divide, "quick" arithmetic operations. BCD arithmetic and expanded operations (through traps).

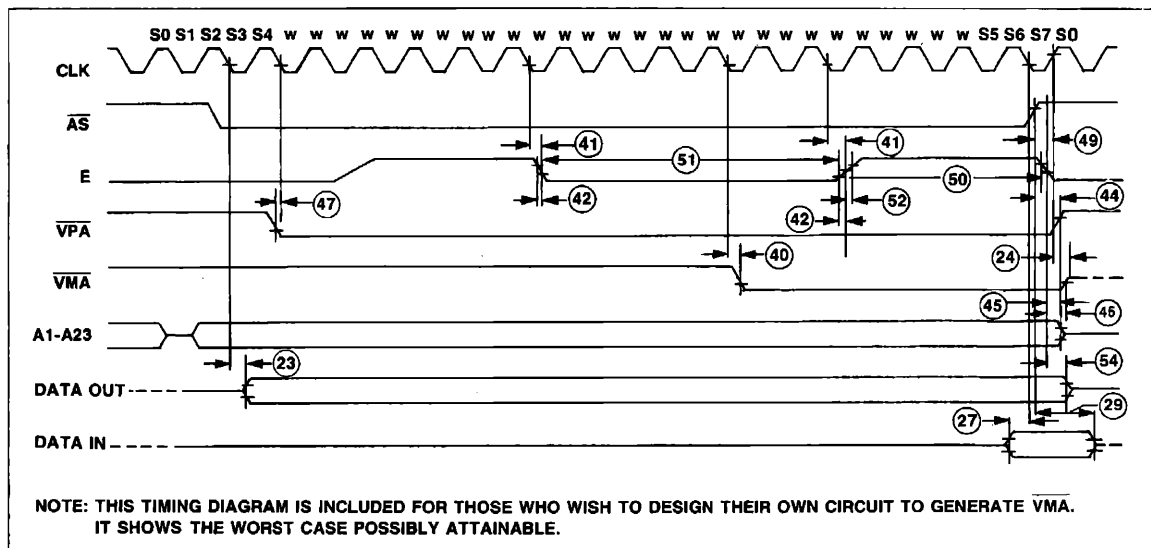


Figure 37. RC68000 to R6500 Peripheral Timing Diagram — Worst Case

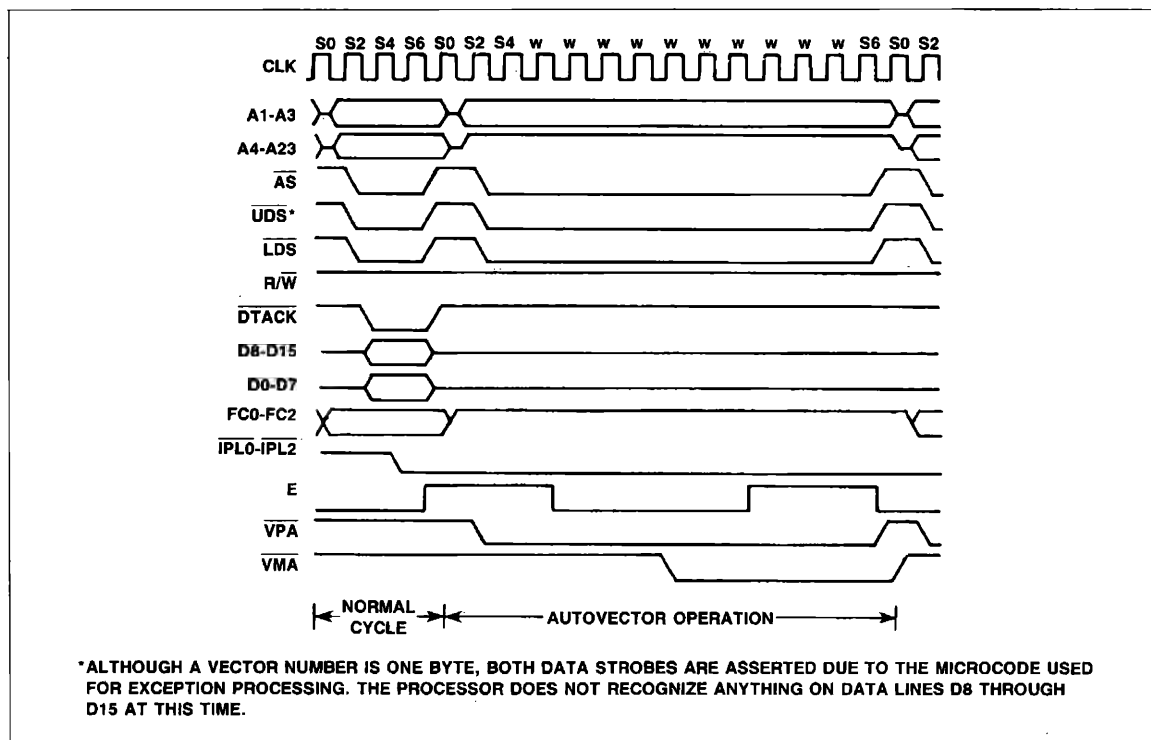


Figure 38. Autovector Operation Timing Diagram

Table 10. Instruction Set Summary

Mnemonic	Description	Mnemonic	Description	Mnemonic	Description
ADBC ADD AND ASL ASR	Add Decimal with Extend Add Logical And Arithmetic Shift Left Arithmetic Shift Right	EOR EXG EXT	Exclusive Or Exchange Registers Sign Extend	PEA	Push Effective Address
BCC BCHG BCLR BRA BSET BSR BTST*	Branch Conditionally Bit Test and Change Bit Test and Clear Branch Always Bit Test and Set Branch to Subroutine Bit Test	JMP JSR	Jump Jump to Subroutine	RESET ROL ROR ROXL ROXR RTE RTR RTS	Reset External Devices Rotate Left without Extend Rotate Right without Extend Rotate Left with Extend Rotate Right with Extend Return from Exception Return and Restore Return from Subroutine
CHK CLR CMP	Check Register Against Bounds Clear Operand Compare	LEA LINK LSL LSR	Load Effective Address Link Stack Logical Shift Left Logical Shift Right	SBCD SCC STOP SUB SWAP	Subtract Decimal with Extend Set Conditional Stop Subtract Swap Data Register Halves
DBCC DIVS DIVU	Test Condition, Decrement and Branch Signed Divide Unsigned Divide	MOVE MULS MULU	Move Signed Multiply Unsigned Multiply	TAS TRAP TRAPV TST	Test and Set Operand Trap Trap on Overflow Test
		NBCD NEG NOP NOT	Negate Decimal with Extend Negate No Operation One's Complement	UNLK	Unlink
		OR	Logical Or		

Table 11. Variations of Instruction Types

Instruction Type	Variation	Description	Instruction Type	Variation	Description
ADD	ADD ADDA ADDQ ADDI ADDX	Add Add Address Add Quick Add Immediate Add with Extend	MOVE	MOVE MOVEA MOVEM MOVEP MOVEQ MOVE from SR MOVE to SR MOVE to CCR MOVE USP	Move Move Address Move Multiple Registers Move Peripheral Data Move Quick Move from Status Register Move to Status Register Move to Condition Codes Move User Stack Pointer
AND	AND ANDI ANDI to CCR ANDI to SR	Logical And And Immediate And Immediate to Condition Codes And Immediate to Status Register	NEG	NEG NEGX	Negate Negate with Extend
CMP	CMP CMPA CMPM CMPI	Compare Compare Address Compare Memory Compare Immediate	OR	OR ORI ORI to CCR ORI to SR	Logical Or Or Immediate Or Immediate to Condition Codes Or Immediate to Status Register
EOR	EOR EORI EORI to CCR EORI to SR	Exclusive Or Exclusive Or Immediate Exclusive Or Immediate to Condition Codes Exclusive Or Immediate to Status Register	SUB	SUB SUBA SUBI SUBQ SUBX	Subtract Subtract Address Subtract Immediate Subtract Quick Subtract with Extend

The following paragraphs contain an overview of the form and structure of the R68000 instruction set. The instructions form a set of tools that include all the machine functions to perform the following operations:

- Data Movement
- Integer Arithmetic
- Logical
- Shift and Rotate
- Bit Manipulation
- Binary Coded Decimal
- Program Control
- System Control

The complete range of instruction capabilities combined with the flexible addressing modes described previously provide a very flexible base for program development.

ADDRESSING

Instructions for the R68000 contain two kinds of information: the type of function to be performed, and the location of the operand(s) on which to perform that function. The methods used to locate (address) the operand(s) are explained in the following paragraphs.

Instructions specify an operand location in one of three ways:

- Register Specification — the number of the register is given in the register field of the instruction.
- Effective Address — use of the different effective address modes.
- Implicit Reference — the definition of certain instructions implies the use of specific registers.

DATA MOVEMENT OPERATIONS

The move (MOVE) instruction provides a means for data acquisition (transfer and storage). The move instruction and the effective addressing modes allow both address and data manipulation. Data move instructions allow byte, word, and long word operands to be transferred from memory to memory, memory to register, register to memory, and register to register. Address move instructions allow word and long word operand transfers and ensure that only legal address manipulations are executed. In addition to the general move instruction there are several special data movement instructions: move multiple registers (MOVEM), move peripheral data (MOVEP), exchange registers (EXG), load effective address (LEA), push effective address (PEA), link stack (LINK), unlink stack (UNLK), and move quick (MOVEQ). Table 12 summarizes the data movement operations.

INTEGER ARITHMETIC OPERATIONS

The arithmetic operators include the four basic operations of add (ADD), subtract (SUB), multiply (MUL), and divide (DIV) as well as arithmetic compare (CMP), clear (CLR), and negate (NEG). The add and subtract instructions are available for both address and data operations, and with data operations accepting all

Table 12. Data Movement Operations

Instruction	Operand Size	Operation
EXG	32	$R_x \leftrightarrow R_y$
LEA	32	$EA \rightarrow An$
LINK	—	$An \rightarrow -(SP)$ $SP \rightarrow An$ $SP + displacement \rightarrow SP$
MOVE	8, 16, 32	$s \rightarrow d$
MOVEM	16, 32	$(EA) \rightarrow An, Dn$ $An, Dn \rightarrow EA$
MOVEP	16, 32	$(EA) \rightarrow Dn$ $Dn \rightarrow (EA)$
MOVEQ	8	$\#xxx \rightarrow Dn$
PEA	32	$EA \rightarrow -(SP)$
SWAP	32	$Dn[31:16] \leftrightarrow Dn[15:0]$
UNLK	—	$An \rightarrow Sp$ $(SP) + \rightarrow An$
NOTES: s = source $-()$ = indirect with predecrement d = destination $() +$ = indirect with postdecrement $[]$ = bit number $\#$ = immediate data		

operand sizes. Address operations are limited to legal address size operands (16 or 32 bits). Data, address, and memory compare operations are also available. The clear and negate instructions may be used on all sizes of data operands.

The multiply and divide operations are available for signed and unsigned operands using word multiply to produce a long word product, and a long word dividend with word divisor to produce a word quotient with a word remainder.

Multiprecision and mixed size arithmetic can be accomplished using a set of extended instructions. These instructions are: add extended (ADDX), subtract extended (SUBX), sign extend (EXT), and negate binary with extend (NEGX).

A text operand (TST) instruction that sets the condition codes as a result of a compare of the operand with zero is available. Test and set (TAS) is a synchronization instruction useful in multiprocessor systems. Table 13 summarizes the integer arithmetic operations.

INSTRUCTION FORMAT

Instructions, as shown in Figure 39, vary from one to five words in length. The first word of the instruction, called the operation word, specifies the length of the instruction and the operation to be performed. The remaining words further specify the operands. These words are either immediate operands or extensions to the effective address mode specified in the operation word.

Table 13. Integer Arithmetic Operations

Instruction	Operand Size	Operation
ADD	8, 16, 32	$Dn + (EA) \rightarrow Dn$ $(EA) + Dn \rightarrow (EA)$ $(EA) + \#xxx \rightarrow (EA)$
	16, 32	$An + (EA) \rightarrow An$
ADDX	8, 16, 32 16, 32	$Dx + Dy + X \rightarrow Dx$ $-(Ax) + -(Ay) + X \rightarrow (Ax)$
CLR	8, 16, 32	$0 \rightarrow EA$
CMP	8, 16, 32	$Dn - (EA)$ $(EA) - \#xxx$ $(Ax) - -(Ay) -$
	16, 32	$An - (EA)$
DIVS	$32 \div 16$	$Dn \div (EA) \rightarrow Dn$
DIVU	$32 \div 16$	$Dn \div (EA) \rightarrow Dn$
EXT	$8 \rightarrow 16$	$(Dn)_8 \rightarrow Dn_{16}$
	$16 \rightarrow 32$	$(Dn)_{16} \rightarrow Dn_{32}$
MULS	$16 \times 16 \rightarrow 32$	$Dn \times (EA) \rightarrow Dn$
MULU	$16 \times 16 \rightarrow 32$	$Dn \times (EA) \rightarrow Dn$
NEG	8, 16, 32	$0 - (EA) \rightarrow (EA)$
NEGX	8, 16, 32	$0 - (EA) - X \rightarrow (EA)$
SUB	8, 16, 32	$Dn - (EA) \rightarrow Dn$ $(EA) - Dn \rightarrow (EA)$ $(EA) - \#xxx \rightarrow (EA)$
	16, 32	$An - (EA) \rightarrow An$
SUBX	8, 16, 32	$Dx - Dy - X \rightarrow Dx$ $-(Ax) - -(Ay) - X \rightarrow (Ax)$
TAS	8	$[EA] - 0, 1 \rightarrow EA[7]$
TST	8, 16, 32	$(EA) - 0$

NOTES:
 [] = bit number
 -() = indirect with predecrement
 ()+ = indirect with postdecrement
 # = immediate data

PROGRAM/DATA REFERENCES

The R68000 separates memory references into two classes: program references, and data references. Program references reference that section of memory that contains the program being executed. Data references refer to that section of memory that contains data. Operand reads are from the data space, except in the case of the program counter relative addressing mode. All operand writes are to the data space.

REGISTER SPECIFICATION

The register field within an instruction specifies the register to be used. Other fields within the instruction specify whether the register selected is an address or data register and how the register is to be used.

EFFECTIVE ADDRESS

Most instructions specify the location of an operand by using the effective address field in the operation word. For example, Figure 40 shows the general format of the single effective address instruction operation word. The effective address is composed of two 3-bit fields: the mode field, and the register field. The value in the mode field selects the different address modes. The register field contains the number of a register.

The effective address field may require additional information to fully specify the operand. This additional information, called the effective address extension, is contained in the following word or words and is considered part of the instruction, as shown in Figure 39. The effective address modes are grouped into three categories: register direct, memory addressing, and special.

REGISTER DIRECT MODES. These effective addressing modes specify that the operand is in one of the 16 multifunction registers.

Data Register Direct. The operand is in the data register specified by the effective address register field.

Address Register Direct. The operand is in the address register specified by the effective address register field.

MEMORY ADDRESS MODES. These effective addressing modes specify that the operand is in memory and provide the specific address of that operand.

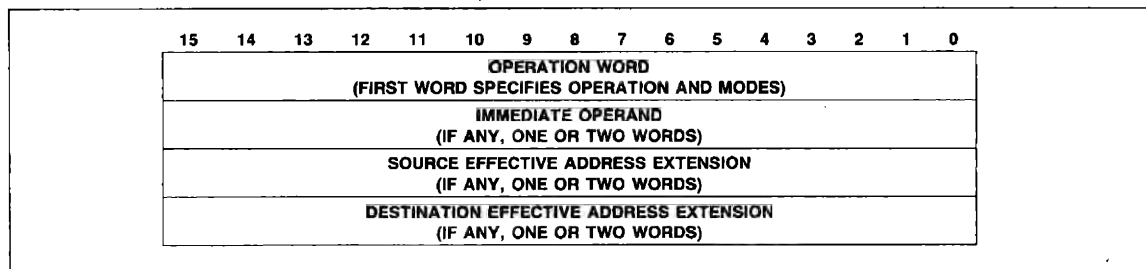


Figure 39. Instruction Format

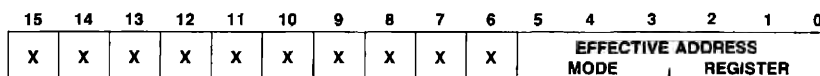


Figure 40. Single-Effective-Address Instruction Operation Word General Format

Address Register Indirect. The address of the operand is in the address register specified by the register field. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Address Register Indirect With Postincrement. The address of the operand is in the address register specified by the register field. After the operand address is used, it is incremented by one, two or four depending upon whether the size of the operand is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is incremented by two rather than one to keep the stack pointer on a word boundary. The reference classifies as a data reference.

Address Register Indirect With Predecrement. The address of the operand is in the address register specified by the register field. Before the operand address is used, it is decremented by one, two, or four depending upon whether the operand size is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is decremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

Address Register Indirect with Displacement. This address mode requires one word of extension. The address of the operand is the sum of the address in the address register and the sign-extended 16-bit displacement integer in the extension word. The reference classifies as a data reference with the exception of the jump to subroutine instructions.

Address Register Indirect With Index. This address mode requires one word of extension. The address of the operand sums the addresses in the address register, the sign-extended displacement integer in the low order eight bits of the extension word, and the contents of the index register. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

SPECIAL ADDRESS MODE. The special address modes use the effective address register field to specify the special addressing mode instead of a register number.

Absolute Short Address. This address mode requires one word of extension. The address of the operand is the extension word. The 16-bit address is sign extended before it is used. The reference classifies as a data reference with the exception of the jump and jump to subroutine instructions.

Absolute Long Address. This address mode requires two words of extension. The address of the operand is developed by the concatenation of the extension words. The high-order part of the address is the first extension word; the low-order part of the

address is the second extension word. The reference classifies as a data reference with the exception of the jump and jump to subroutine instructions.

Program Counter With Displacement. This address mode requires one word of extension. The address of the operand sums the addresses in the program counter and the sign-extended 16-bit displacement integer in the extension word. The value in the program counter is the address of the extension word. The reference classifies as a program reference.

Program Counter With Index. This address mode requires one word of extension. This address sums the addresses in the program counter, the sign-extended displacement integer in the lower eight bits of the extension word, and the contents of the index register. The value in the program counter is the address of the extension word. This reference classifies as a program reference.

Immediate Data. This address mode requires either one or two words of extension depending on the size of the operation.

- Byte Operation — operand is low order byte of extension word
- Word Operation — operand is extension word
- Long Word Operation — operand is in the two extension words, high-order 16 bits are in the first extension word, low-order 16 bits are in the second extension word.

IMPLICIT REFERENCE

Some instructions make implicit reference to the program counter (PC), the system stack pointer (SP), the supervisor stack pointer (SSP), the user stack pointer (USP), or the status register (SR).

A selected set of instructions may reference the status register by means of the effective address field. These are:

- ANDI to CCR
- ANDI to SR
- EORI to CCR
- EORI to SR
- MOVE to CCR
- MOVE to SR
- MOVE from SR
- ORI to CCR
- ORI to SR

EFFECTIVE ADDRESS ENCODING SUMMARY

Table 14 summarizes the effective addressing modes discussed in the previous paragraphs.

Table 14. Effective Address Encoding Summary

Addressing Mode	Mode	Register
Data Register Direct	000	register number
Address Register Direct	001	register number
Address Register Indirect	010	register number
Address Register Indirect with Postincrement	011	register number
Address Register Indirect with Predecrement	100	register number
Address Register Indirect with Displacement	101	register number
Address Register Indirect with Index	110	register number
Absolute Short	111	000
Absolute Long	111	001
Program Counter with Displacement	111	010
Program Counter with Index	111	011
Immediate	111	100

Table 15. Logical Operations

Instruction	Operand Size	Operation
AND	8, 16, 32	$Dn \wedge (EA) \rightarrow Dn$ $(EA) \wedge Dn \rightarrow (EA)$ $(EA) \wedge \#xxx \rightarrow (EA)$
OR	8, 16, 32	$Dn \vee (EA) \rightarrow Dn$ $(EA) \vee Dn \rightarrow (EA)$ $(EA) \vee \#xxx \rightarrow (EA)$
EOR	8, 16, 32	$(EA) \oplus Dy \rightarrow (EA)$ $(EA) \oplus \#xxx \rightarrow (EA)$
NOT	8, 16, 32	$\sim (EA) \rightarrow (EA)$
NOTES: \sim = invert $\#$ = immediate data \wedge = logical AND \vee = logical OR \oplus = logical exclusive OR		

Memory shifts and rotates are for word operands only and allow only single-bit shifts or rotates.

Table 16 summarizes the shift and rotate operations.

BIT MANIPULATION OPERATIONS

The following instructions provide bit manipulation operations: bit test (BTST), bit test and set (BSET), bit test and clear (BCLR), and bit test and change (BCHG). Table 17 is a summary of the bit manipulation operations. (Bit 2 of the status register is Z.)

SYSTEM STACK. The system stack is used implicitly by many instructions; user stacks and queues may be created and maintained through the addressing modes. Address register seven (A7) is the system stack pointer (SP). The system stack pointer is either the supervisor stack pointer (SSP) or the user stack pointer (USP), depending on the state of the S-bit in the status register. If the S-bit indicates supervisor state (High), SSP is the active system stack pointer, and the USP cannot be referenced as an address register. If the S-bit indicates user state (Low), the USP is the active system stack pointer, and the SSP cannot be referenced. Each system stack fills from high memory to low memory.

LOGICAL OPERATIONS

Logical operation instructions AND, OR, EOR, and NOT are available for all sizes of integer data operands. A similar set of immediate instructions (ANDI, ORI, and EORI) provide these logical operations with all sizes of immediate data. Table 15 summarizes the logical operations.

SHIFT AND ROTATE OPERATIONS

Shift operations in both directions are provided by arithmetic instructions ASR and ASL and logical shift instructions LSR and LSL. The rotate instructions (with and without extend) available are ROXR, ROXL, ROR, and ROL. All shift and rotate operations can be performed in either registers or memory. Register shifts and rotates support all operand sizes and allow a shift count specified in a data register.

Table 16. Shift and Rotate Operations

Instruction	Operand Size	Operation
ASL	8, 16, 32	
ASR	8, 16, 32	
LSL	8, 16, 32	
LSR	8, 16, 32	
ROL	8, 16, 32	
ROR	8, 16, 32	
ROXL	8, 16, 32	
ROXR	8, 16, 32	

Table 17. Bit Manipulation Operations

Instruction	Operand Size	Operation
BTST	8, 32	\sim bit of (EA) \rightarrow Z
BSET	8, 32	\sim bit of (EA) \rightarrow Z 1 \rightarrow bit of EA
BCLR	8, 32	\sim bit of (EA) \rightarrow Z 0 \rightarrow bit of EA
BCHG	8, 32	\sim bit of (EA) \rightarrow Z \sim bit of (EA) \rightarrow bit of EA

NOTE: \sim = invert

BINARY CODED DECIMAL OPERATIONS

The following instructions accomplish multiprecision arithmetic operations on binary coded decimal numbers: add decimal with extend (ABCD), subtract decimal with extend (SBCD), and negate decimal with extend (NBCD). Table 18 summarizes the binary coded decimal operations.

PROGRAM CONTROL OPERATIONS

Program control operations implementation requires a series of conditional and unconditional branch instructions and return instructions. These instructions are summarized in Table 19.

The conditional instructions provide setting and branching for the following conditions:

CC — carry clear
 CS — carry set
 EQ — equal
 F — never true
 GE — greater or equal
 GT — greater than
 HI — high
 LE — less or equal
 LS — low or same
 LT — less than
 MI — minus
 NE — not equal
 PL — plus
 T — always true
 VC — no overflow
 VS — overflow

Table 18. Binary Coded Decimal Operations

Instruction	Operand Size	Operation
ABCD	8	$Dx_{10} + Dy_{10} + X \rightarrow Dx$ $-(Ax)_{10} + -(Ay)_{10} + X \rightarrow (Ax)$
SBCD	8	$Dx_{10} - Dy_{10} - X \rightarrow Dx$ $-(Ax)_{10} - -(Ay)_{10} - X \rightarrow (Ax)$
NBCD	8	$0 - (EA)_{10} - X \rightarrow (EA)$

NOTE: $-()$ = indirect with predecrement

Table 19. Program Control Operations

Instruction	Operation
Conditional	
BCC	Branch conditionally (14 conditions) 8- and 16-bit displacement
DBCC	Test condition, decrement, branch 16-bit displacement
SCC	Set byte conditionally (16 conditions)
Unconditional	
BRA	Branch always 8- and 16-bit displacement
BSR	Branch to subroutine 8- and 16-bit displacement
JMP	Jump
JSR	Jump to subroutine
Returns	
RTR	Return and restore condition codes
RTS	Return from subroutine

SYSTEM CONTROL OPERATIONS

System control operations are accomplished by using privileged instructions, trap generating instructions, and instructions that use or modify the status register. These instructions are summarized in Table 20.

INSTRUCTION SET

The following paragraphs provide information about the addressing categories and instruction set of the R68000.

ADDRESSING CATEGORIES

Effective address modes may be categorized by the ways in which they may be used. The following classifications will be used in the instructions definitions.

Data	If an effective address mode may be used to refer to data operands, it is considered a data addressing effective address mode.
Memory	If an effective address mode may be used to refer to memory operands, it is considered a memory addressing effective address mode.
Alterable	If an effective address mode may be used to refer to alterable (writable) operands, it is considered an alterable addressing effective address mode.
Control	If an effective address mode may be used to refer to memory operands without an associated size, it is considered control addressing effective address mode.

Table 21 shows the various categories to which each of the effective address modes belong. Table 22 is the instruction set summary.

Table 20. System Control Operations

Instruction	Operation
Privileged	
ANDI to SR	Logical AND to Status Register
EORI to SR	Logical EOR to Status Register
MOVE EA to SR	Load New Status Register
MOVE USP	Move User Stack Pointer
ORI to SR	Logical OR to Status Register
RESET	Reset External Devices
RTE	Return from Exception
STOP	Stop Program Execution
Trap Generating	
CHK	Check Data Register Against Upper Bounds
TRAP	Trap
TRAPV	Trap on Overflow
Status Register	
ANDI to CCR	Logical AND to Condition Codes
EORI to CCR	Logical EOR to Condition Codes
MOVE EA to CCR	Load New Condition Codes
MOVE SR to EA	Store Status Register
ORI to CCR	Logical OR to Condition Codes

The status register addressing mode is not permitted unless it is explicitly mentioned as a legal addressing mode.

These categories may be combined, so that additional, more restrictive, classifications may be defined. For example, the instruction descriptions use such classifications as alterable memory or data alterable. The former refers to those addressing modes which are both alterable and memory addresses, and the latter refers to addressing modes which are both data and alterable.

INSTRUCTION PREFETCH

The R68000 uses a two-word tightly-coupled instruction prefetch mechanism to enhance performance. This mechanism is described in terms of the microcode operations involved. If the execution of an instruction is defined to begin when the microroutine for that instruction is entered, some features of the prefetch mechanism can be described.

- 1) When execution of an instruction begins, the operation word and the word following have already been fetched. The operation word is in the instruction decoder.
- 2) In the case of multi-word instructions, as each additional word of the instruction is used internally, a fetch is made to the instruction stream to replace it.
- 3) The last fetch from the instruction stream is made when the operation word is discarded and decoding is started on the next instruction.
- 4) If the instruction is a single-word instruction causing a branch, the second word is not used. But because this word is fetched by the preceding instruction, it is impossible to avoid this superfluous fetch.
- 5) In the case of an interrupt or trace exception, both words are not used.
- 6) The program counter usually points to the last word fetched from the instruction stream.

INSTRUCTION EXECUTION TIMES

The following paragraphs contain listings of the instruction execution times in terms of external clock (CLK) periods. In this timing data, it is assumed that both memory read and write cycle times are four clock periods. Any wait states caused by a longer memory cycle must be added to the total instruction time. The number of bus read and write cycles for each instruction is enclosed in parenthesis following the execution periods and is shown as (r/w) where r is the number of read cycles and w is the number of write cycles.

Table 21. Effective Addressing Mode Categories

Effective Address Modes	Mode	Register	Addressing Categories			
			Data	Memory	Control	Alterable
Dn	000	Register Number	X	—	—	X
An	001	Register Number	—	—	—	X
(An)	010	Register Number	X	X	X	X
(An) +	011	Register Number	X	X	—	X
— (An)	100	Register Number	X	X	—	X
d(An)	101	Register Number	X	X	X	X
d(An, ix)	110	Register Number	X	X	X	X
xxx.W	111	000	X	X	X	X
xxx.L	111	001	X	X	X	X
d(PC)	111	010	X	X	X	—
d(PC, ix)	111	011	X	X	X	—
#xxx	111	X	X	X	—	—

Table 22. Instruction Set

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ABCD	Add Decimal with Extend	$(\text{Destination})_{10} + (\text{Source})_{10} + X \rightarrow \text{Destination}$	*	U	*	U	*
ADD	Add Binary	$(\text{Destination}) + (\text{Source}) \rightarrow \text{Destination}$	*	*	*	*	*
ADDA	Add Address	$(\text{Destination}) + (\text{Source}) \rightarrow \text{Destination}$	—	—	—	—	—
ADDI	Add Immediate	$(\text{Destination}) + \text{Immediate Data} \rightarrow \text{Destination}$	*	*	*	*	*
ADDQ	Add Quick	$(\text{Destination}) + \text{Immediate Data} \rightarrow \text{Destination}$	*	*	*	*	*
ADDX	Add Extended	$(\text{Destination}) + (\text{Source}) + X \rightarrow \text{Destination}$	*	*	*	*	*
AND	AND Logical	$(\text{Destination}) \wedge (\text{Source}) \rightarrow \text{Destination}$	—	*	*	0	0
ANDI	AND Immediate	$(\text{Destination}) \wedge \text{Immediate Data} \rightarrow \text{Destination}$	—	*	*	0	0
ANDI to CCR	AND Immediate to Condition Codes	$(\text{Source}) \wedge \text{CCR} \rightarrow \text{CCR}$	*	*	*	*	*
ANDI to SR	AND Immediate to Status Register	$(\text{Source}) \wedge \text{SR} \rightarrow \text{SR}$	*	*	*	*	*
ASL, ASR	Arithmetic Shift	$(\text{Destination}) \text{ Shifted by } \langle \text{count} \rangle \rightarrow \text{Destination}$	*	*	*	*	*
BCC	Branch Conditionally	If CC then $\text{PC} + d \rightarrow \text{PC}$	—	—	—	—	—
BCHG	Test a Bit and Change	$\sim (\langle \text{bit number} \rangle \text{ OF Destination}) \rightarrow Z$ $\sim (\langle \text{bit number} \rangle \text{ OF Destination}) \rightarrow$ $\langle \text{bit number} \rangle \text{ OF Destination}$	—	—	*	—	—
BCLR	Test a Bit and Clear	$\sim (\langle \text{bit number} \rangle \text{ OF Destination}) \rightarrow Z$ $0 \rightarrow \langle \text{bit number} \rangle \rightarrow \text{OF Destination}$	—	—	*	—	—
BRA	Branch Always	$\text{PC} + d \rightarrow \text{PC}$	—	—	—	—	—
BSET	Test a Bit and Set	$\sim (\langle \text{bit number} \rangle \text{ OF Destination}) \rightarrow Z$ $1 \rightarrow \langle \text{bit number} \rangle \text{ OF Destination}$	—	—	*	—	—
BSR	Branch to Subroutine	$\text{PC} \rightarrow (\text{SP}); \text{PC} + d \rightarrow \text{PC}$	—	—	—	—	—
BTST	Test a Bit	$\sim (\langle \text{bit number} \rangle \text{ OF Destination}) \rightarrow Z$	—	—	*	—	—
CHK	Check Register Against Bounds	If $\text{Dn} < 0$ or $\text{Dn} > \langle \text{ea} \rangle$ then TRAP	—	*	U	U	U
CLR	Clear and Operand	$0 \rightarrow \text{Destination}$	—	0	1	0	0
CMP	Compare	$(\text{Destination}) - (\text{Source})$	—	*	*	*	*
CPMA	Compare Address	$(\text{Destination}) - (\text{Source})$	—	*	*	*	*
CMPI	Compare Immediate	$(\text{Destination}) - \text{Immediate Data}$	—	*	*	*	*
CMPM	Compare Memory	$(\text{Destination}) - (\text{Source})$	—	*	*	*	*
DBCC	Test Condition, Decrement and Branch	If $\sim \text{CC}$ then $\text{Dn} - 1 \rightarrow \text{Dn}$; if $\text{Dn} \neq -1$ then $\text{PC} + d \rightarrow \text{PC}$	—	—	—	—	—
DIVS	Signed Divide	$(\text{Destination})/(\text{Source}) \rightarrow \text{Destination}$	—	*	*	*	0
DIVU	Unsigned Divide	$(\text{Destination})/(\text{Source}) \rightarrow \text{Destination}$	—	*	*	*	0
EOR	Exclusive OR Logical	$(\text{Destination}) \oplus (\text{Source}) \rightarrow \text{Destination}$	—	*	*	0	0
EORI	Exclusive OR Immediate	$(\text{Destination}) \oplus \text{Immediate Data} \rightarrow \text{Destination}$	—	*	*	0	0
EORI to CCR	Exclusive OR Immediate to Condition Codes	$(\text{Source}) \oplus \text{CCR} \rightarrow \text{CCR}$	*	*	*	*	*

NOTES:
 \wedge = logical AND * = affected
 \vee = logical OR — = unaffected
 \oplus = logical exclusive OR 0 = cleared
 \sim = logical complement 1 = set
 U = undefined

Table 22. Instruction Set (Continued)

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
EORI to SR	Exclusive OR Immediate to Status Register	(Source) \oplus SR \rightarrow SR	*	*	*	*	*
EXG	Exchange Register	Rx \leftrightarrow Ry	—	—	—	—	—
EXT	Sign Extend	(Destination) Sign-Extended \rightarrow Destination	—	*	*	0	0
JMP	Jump	Destination \rightarrow PC	—	—	—	—	—
JSR	Jump to Subroutine	PC \rightarrow -(SP); Destination \rightarrow PC	—	—	—	—	—
LEA	Load Effective Address	<ea> \rightarrow An	—	—	—	—	—
LINK	Link and Allocate	An \rightarrow (SP); SP \rightarrow An; SP + Displacement \rightarrow SP	—	—	—	—	—
LSL, LSR	Logical Shift	(Destination) Shifted by <count> \rightarrow Destination	*	*	*	0	*
MOVE	Move Data from Source to Destination	(Source) \rightarrow Destination	—	*	*	0	0
MOVE to CCR	Move to Condition Code	(Source) \rightarrow CCR	*	*	*	*	*
MOVE to SR	Move to the Status Register	(Source) \rightarrow SR	*	*	*	*	*
MOVE from SR	Move from the Status Register	SR \rightarrow Destination	—	—	—	—	—
MOVE USP	Move User Stack Pointer	USP \rightarrow An; An \rightarrow USP	—	—	—	—	—
MOVEA	Move Address	(Source) \rightarrow Destination	—	—	—	—	—
MOVEM	Move Multiple Registers	Register \rightarrow Destination (Source) \rightarrow Registers	—	—	—	—	—
MOVEP	Move Peripheral Data	(Source) \rightarrow Destination	—	—	—	—	—
MOVEQ	Move Quick	Immediate Data \rightarrow Destination	—	*	*	0	0
MULS	Signed Multiply	(Destination)X(Source) \rightarrow Destination	—	*	*	0	0
MULU	Unsigned Multiply	(Destination)X(Source) \rightarrow Destination	—	*	*	0	0
NBCD	Negate Decimal with Extend	0 - (Destination) ₁₀ - X \rightarrow Destination	*	U	*	U	*
NEG	Negate	0 - (Destination) \rightarrow Destination	*	*	*	*	*
NEGX	Negate with Extend	0 - (Destination) - X \rightarrow Destination	*	*	*	*	*
NOP	No Operation	—	—	—	—	—	—
NOT	Logical Complement	\sim (Destination) \rightarrow Destination	—	*	*	0	0
OR	Inclusive OR Logical	(Destination) \vee (Source) \rightarrow Destination	—	*	*	0	0
ORI	Inclusive OR Immediate	(Destination) \vee Immediate Data \rightarrow Destination	—	*	*	0	0
ORI to CCR	Inclusive OR Immediate to Condition Codes	(Source) \vee CCR \rightarrow CCR	*	*	*	*	*
ORI to SR	Inclusive OR Immediate to Status Register	(Source) \vee SR \rightarrow SR	*	*	*	*	*
PEA	Push Effective Address	<ea> \rightarrow -(SP)	—	—	—	—	—
RESET	Reset External Device	—	—	—	—	—	—
ROL, ROR	Rotate (Without Extend)	(Destination) Rotated by <count> \rightarrow Destination	—	*	*	0	*

NOTES:

\wedge = logical AND	*
\vee = logical OR	—
\oplus = logical exclusive OR	0
\sim = logical complement	1
	U

Table 22. Instruction Set (Continued)

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ROXL, ROXR	Rotate with Extend	(Destination) Rotated by <count> \rightarrow Destination	*	*	*	0	*
RTE	Return from Exception	(SP) + \rightarrow SR; (SP) + \rightarrow PC	*	*	*	*	*
RTR	Return and Restore Condition Codes	(SP) + \rightarrow CC; (SP) + \rightarrow PC	*	*	*	*	*
RTS	Return from Subroutine	(SP) + \rightarrow PC	—	—	—	—	—
SBCD	Subtract Decimal with Extend	(Destination) ₁₀ - (Source) ₁₀ - X \rightarrow Destination	*	U	*	U	*
SCC	Set According to Condition	If CC then 1's \rightarrow Destination else 0's \rightarrow Destination	—	—	—	—	—
STOP	Load Status Register and Stop	Immediate Data \rightarrow SR; STOP	*	*	*	*	*
SUB	Subtract Binary	(Destination) - (Source) \rightarrow Destination	*	*	*	*	*
SUBA	Subtract Address	(Destination) - (Source) \rightarrow Destination	—	—	—	—	—
SUBI	Subtract Immediate	(Destination) - Immediate Data \rightarrow Destination	*	*	*	*	*
SUBQ	Subtract Quick	(Destination) - Immediate Data \rightarrow Destination	*	*	*	*	*
SUBX	Subtract with Extend	(Destination) - (Source) - X \rightarrow Destination	*	*	*	*	*
SWAP	Swap Register Halves	Register [31:16] \leftrightarrow Register [15:0]	—	*	*	0	0
TAS	Test and Set an Operand	(Destination) Tested \rightarrow CC; 1 \rightarrow [7] OF Destination	—	*	*	0	0
TRAP	Trap	PC \rightarrow - (SSP); SR \rightarrow - (SSP); (Vector) \rightarrow PC	—	—	—	—	—
TRAPV	Trap on Overflow	If ν then TRAP	—	—	—	—	—
TST	Test and Operand	(Destination) Tested \rightarrow CC	—	*	*	0	0
UNLK	Unlink	An \rightarrow SP; (SP) + \rightarrow An	—	—	—	—	—

NOTES:

[] = bit number * = affected
 \wedge = logical AND — = unaffected
 \vee = logical OR 0 = cleared
 \oplus = logical exclusive OR 1 = set
 \sim = logical complement U = undefined

Note

The number of periods includes instruction fetch and all applicable operand fetches and stores.

EFFECTIVE ADDRESS OPERAND CALCULATION TIMING

Table 23 lists the number of clock periods required to compute an instruction's effective address. It includes fetching of any extension words, the address computation, and fetching of the memory operand. The number of bus read and write cycles is shown in parenthesis as (r/w). Note there are no write cycles involved in processing the effective address.

MOVE INSTRUCTION CLOCK PERIODS

Tables 24 and 25 indicate the number of clock periods for the move instruction. This data includes instruction fetch, operand reads, and operand writes. The number of bus read and write cycles is shown in parenthesis as (r/w).

STANDARD INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 26 delineate the time required to perform the operations, store the results, and read the next instruction. The number of bus read and write cycles is shown in parenthesis as (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

In Table 26, the headings have the following meanings: An = address register operand, Dn = data register operand, ea = an operand specified by an effective address, and M = memory effective address operand.

IMMEDIATE INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 27 includes the time to fetch immediate operands, perform the operations, store the results, and read the next operation. The number of bus read and write cycles is shown in parenthesis as (r/w). The number

Table 23. Effective Address Calculation Timing

Addressing Mode		Byte, Word	Long
Dn An	Register		
	Data Register Direct Address Register Direct	0(0/0) 0(0/0)	0(0/0) 0(0/0)
(An) (An) +	Memory		
	Address Register Indirect Address Register Indirect with Postincrement	4(1/0) 4(1/0)	8(2/0) 8(2/0)
- (An) d(An)	Address Register Indirect with Predecrement Address Register Indirect with Displacement	6(1/0) 8(2/0)	10(2/0) 12(3/0)
d(An, ix)* xxx.W	Address Register Indirect with Index Absolute Short	10(2/0) 8(2/0)	14(3/0) 12(3/0)
xxx.L d(PC)	Absolute Long Program Counter with Displacement	12(3/0) 8(2/0)	16(4/0) 12(3/0)
d(PC, ix)* #xxx	Program Counter with Index Immediate	10(2/0) 4(1/0)	14(3/0) 8(2/0)

*The size of the index register (ix) does not affect execution time.

Table 24. Move Byte and Word Instruction Clock Periods

Source	Destination								
	Dn	An	(An)-	(An) +	- (An)	d(An)	d(An, ix)*	xxx.W	xxx.L
Dn	4(1/0)	4(1/0)	8(1/1)	8(1/1)	8(1/1)	12(2/1)	14(2/1)	12(2/1)	16(3/1)
An	4(1/0)	4(1/0)	8(1/1)	8(1/1)	8(1/1)	12(2/1)	14(2/1)	12(2/1)	16(3/1)
(An)	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)
(An) +	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)
- (An)	10(2/0)	10(2/0)	14(2/1)	14(2/1)	14(2/1)	18(3/1)	20(3/1)	18(3/1)	22(4/1)
d(An)	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
d(An, ix)*	14(3/0)	14(3/0)	18(3/1)	18(3/1)	18(3/1)	22(4/1)	24(4/1)	22(4/1)	26(5/1)
xxx.W	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
xxx.L	16(4/0)	16(4/0)	20(4/1)	20(4/1)	20(4/1)	24(5/1)	26(5/1)	24(5/1)	28(6/1)
d(PC)	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
d(PC, ix)*	14(3/0)	14(3/0)	18(3/1)	18(3/1)	18(3/1)	22(4/1)	24(4/1)	22(4/1)	26(5/1)
#xxx	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)

*The size of the index register (ix) does not affect execution time.

of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

In Table 27, the headings have the following meanings:
 # = immediate operand, Dn = data register operand,
 An = address register operand, M = memory operand, and
 SR = status register.

SINGLE OPERAND INSTRUCTION CLOCK PERIODS

Table 28 indicates the number of clock periods for the single operand instructions. The number of bus read and write cycles is shown in parenthesis as (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

Table 25. Move Long Instruction Clock Periods

Source	Destination								
	Dn	An	(An)	(An) +	-(An)	d(An)	d(An, ix)*	xxx.W	xxx.L
Dn	4(1/0)	4(1/0)	12(1/2)	12(1/2)	12(1/2)	16(2/2)	18(2/2)	16(2/2)	20(3/2)
An	4(1/0)	4(1/0)	12(1/2)	12(1/2)	12(1/2)	16(2/2)	18(2/2)	16(2/2)	20(3/2)
(An)	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)
(An) +	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)
-(An)	14(3/0)	14(3/0)	22(3/2)	22(3/2)	22(3/2)	26(4/2)	28(4/2)	26(4/2)	30(5/2)
d(An)	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(6/2)
d(An, ix)*	18(4/0)	18(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
xxx.W	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(6/2)
xxx.L	20(5/0)	20(5/0)	28(5/2)	28(5/2)	28(5/2)	32(6/2)	34(6/2)	32(6/2)	36(7/2)
d(PC)	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(5/2)
d(PC, ix)*	18(4/0)	18(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
#xxx	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)

*The size of the index register (ix) does not affect execution time.

Table 26. Standard Instruction Clock Periods

Instruction	Size	op <ea>, An†	op <ea>, Dn	op Dn, <M>
ADD	Byte, Word	8(1/0) +	4(1/0) +	8(1/1) +
	Long	6(1/0) + **	6(1/0) + **	12(1/2) +
AND	Byte, Word	—	4(1/0) +	8(1/1) +
	Long	—	6(1/0) + **	12(1/2) +
CMP	Byte, Word	6(1/0) +	4(1/0) +	—
	Long	6(1/0) +	6(1/0) +	—
DIVS	—	—	158(1/0) + *	—
DIVU	—	—	140(1/0) + *	—
EOR	Byte, Word	—	4(1/0)***	8(1/1) +
	Long	—	8(1/0)***	12(1/2) +
MULS	—	—	70(1/0) + *	—
MULU	—	—	70(1/0) + *	—
OR	Byte, Word	—	4(1/0) +	8(1/1) +
	Long	—	6(1/0) + **	12(1/2) +
SUB	Byte, Word	8(1/0) +	4(1/0) +	8(1/1) +
	Long	6(1/0) + **	6(1/0) + **	12(1/2) +

NOTES:

+ add effective address calculation time

† word or long only

* indicates maximum value

** The base time of six clock periods is increased to eight if the effective address mode is register direct or immediate (effective address time should also be added).

*** Only available effective address mode is data register direct

DIVS, DIVU The divide algorithm used by the R68000 provides less than 10% difference between the best and worst case timings.

MULS, MULU The multiply algorithm requires $38 + 2n$ clocks where n is defined as:MULU: n = the number of ones in each <ea>MULU: n = concatenate the <ea> with a zero as the LSB; n is the resultant number of 10 or 01 patterns in the 17-bit source; i.e., worst case happens when the source is \$5555.

Table 27. Immediate Instruction Clock Periods

Instruction	Size	op #, Dn	op #, An	op #, M
ADDI	Byte, Word	8(2/0)	—	12(2/1) +
	Long	16(3/0)	—	20(3/2) +
ADDQ	Byte, Word	4(1/0)	8(1/0)*	8(1/1) +
	Long	8(1/0)	8(1/0)	12(1/2) +
ANDI	Byte, Word	8(2/0)	—	12(2/1) +
	Long	16(3/0)	—	20(3/1) +
CMPI	Byte, Word	8(2/0)	—	8(2/0) +
	Long	14(3/0)	—	12(3/0) +
EORI	Byte, Word	8(2/0)	—	12(2/1) +
	Long	16(3/0)	—	20(3/2) +
MOVEQ	Long	4(1/0)	—	—
ORI	Byte, Word	8(2/0)	—	12(2/1) +
	Long	16(3/0)	—	20(3/2) +
SUBI	Byte, Word	8(2/0)	—	12(2/1) +
	Long	16(3/0)	—	20(3/2) +
SUBQ	Byte, Word	4(1/0)	8(1/0)*	8(1/1) +
	Long	8(1/0)	8(1/0)	12(1/2) +

+ add effective address calculation time
* word only

Table 28. Single Operand Instruction Clock Periods

Instruction	Size	Register	Memory
CLR	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NBCD	Byte	6(1/0)	8(1/1) +
NEG	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NEGX	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NOT	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
SCC	Byte, False	4(1/0)	8(1/1) +
	Byte, True	6(1/0)	8(1/1) +
TAS	Byte	4(1/0)	10(1/1) +
TST	Byte, Word	4(1/0)	4(1/0) +
	Long	4(1/0)	4(1/0) +

+ add effective address calculation time

SHIFT/ROTATE INSTRUCTION CLOCK PERIODS

Table 29 delineates the number of clock periods for the shift and rotate instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

BIT MANIPULATION INSTRUCTION CLOCK PERIODS

Table 30 indicates the number of clock periods required for the bit manipulation instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

CONDITIONAL INSTRUCTION CLOCK PERIODS

Table 31 delineates the number of clock periods required for the conditional instructions. The number of bus read and write cycles is indicated in parenthesis as: (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

JMP, JSR, LEA, PWA, MOVEM INSTRUCTION CLOCK PERIODS

Table 32 indicates the number of clock periods required for the jump, jump to subroutine, load effective address, push effective address, and move multiple registers instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w).

Table 29. Shift/Rotate Instruction Clock Periods

Instruction	Size	Register	Memory
ASR, ASL	Byte, Word	$6 + 2n(1/0)$	$8(1/1) +$
	Long	$8 + 2n(1/0)$	—
LSR, LSL	Byte, Word	$6 + 2n(1/0)$	$8(1/1) +$
	Long	$8 + 2n(1/0)$	—
ROR, ROL	Byte, Word	$6 + 2n(1/0)$	$8(1/1) +$
	Long	$8 + 2n(1/0)$	—
ROXR, ROXL	Byte, Word	$6 + 2n(1/0)$	$8(1/1) +$
	Long	$8 + 2n(1/0)$	—

+ add effective address calculation time
n is shift or rotate count

Table 30. Bit Manipulation Instruction Clock Periods

Instruction	Size	Dynamic		Static	
		Register	Memory	Register	Memory
BCHG	Byte	—	$8(1/1) +$	—	$12(2/1) +$
	Long	$8(1/0)^*$	—	$12(2/0)^*$	—
BCLR	Byte	—	$8(1/1) +$	—	$12(2/1) +$
	Long	$10(1/0)^*$	—	$14(2/0)^*$	—
BSET	Byte	—	$8(1/1) +$	—	$12(2/1) +$
	Long	$8(1/0)^*$	—	$12(2/0)^*$	—
BTST	Byte	—	$4(1/0) +$	—	$8(2/0) +$
	Long	$6(1/0)$	—	$10(2/0)$	—

+ add effective address calculation time
* indicates maximum value

Table 31. Conditional Instruction Clock Periods

Instruction	Displacement	Branch Taken	Branch Not Taken
BCC	Byte	10(2/0)	8(1/0)
	Word	10(2/0)	12(2/0)
BRA	Byte	10(2/0)	—
	Word	10(2/0)	—
BSR	Byte	18(2/2)	—
	Word	18(2/2)	—
DBCC	CC true	—	12(2/0)
	CC false	10(2/0)	14(3/0)

Table 32. JMP, JSR, LEA, PEA, MOVEM INSTRUCTION CLOCK PERIODS

Instr	Size	(An)	(An) +	— (An)	d(An)	d(An, ix)* +	xxx.W	xxx.L	d(PC)	d(PC, ix)*
JMP	—	8(2/0)	—	—	10(2/0)	14(3/0)	10(2/0)	12(3/0)	10(2/0)	14(3/0)
JSR	—	16(2/2)	—	—	18(2/2)	22(2/2)	18(2/2)	20(3/2)	18(2/2)	22(2/2)
LEA	—	4(1/0)	—	—	8(2/0)	12(2/0)	8(2/0)	12(3/0)	8(2/0)	12(2/0)
PEA	—	12(1/2)	—	—	16(2/2)	20(2/2)	16(2/2)	20(3/2)	16(2/2)	20(2/2)
MOVEM M → R	Word	12 + 4n (3 + n/0)	12 + 4n (3 + n/0)	—	16 + 4n (4 + n/0)	18 + 4n (4 + n/0)	16 + 4n (4 + n/0)	20 + 4n (5 + n/0)	16 + 4n (4 + n/0)	18 + 4n (4 + n/0)
	Long	12 + 8n (3 + 2n/0)	12 + 8n (3 + 2n/0)	—	16 + 8n (4 + 2n/0)	18 + 8n (4 + 2n/0)	16 + 8n (4 + 2n/0)	20 + 8n (5 + 2n/0)	16 + 8n (4 + 2n/0)	18 + 8n (4 + 2n/0)
MOVEM R → M	Word	8 + 4n (2/n)	—	8 + 4n (2/n)	12 + 4n (3/n)	14 + 4n (3/n)	12 + 4n (3/n)	16 + 4n (4/n)	—	—
	Long	8 + 8n (2/2n)	—	8 + 8n (2/2n)	12 + 8n (3/2n)	14 + 8n (3/2n)	12 + 8n (3/2n)	16 + 8n (4/2n)	—	—

n is the number of registers to move
 * The size of the index register (ix) does not affect the instruction's execution time

Table 33. Multi-Precision Instruction Clock Periods

Instruction	Size	op Dn, Dn	op M, M
ADDX	Byte, Word	4(1/0)	18(3/1)
	Long	8(1/0)	30(5/2)
CMPM	Byte, Word	—	12(3/0)
	Long	—	20(5/0)
SUBX	Byte, Word	4(1/0)	18(3/1)
	Long	8(1/0)	30(5/2)
ABCD	Byte	6(1/0)	18(3/1)
SBCD	Byte	6(1/0)	18(3/1)

MULTI-PRECISION INSTRUCTION CLOCK PERIODS

Table 33 delineates the number of clock periods for the multi-precision instructions. The number of clock periods includes the time to fetch both operands, perform the operations, store the results, and read the next instructions. The number of read and write cycles is shown in parenthesis as: (r/w).

In Table 33, the headings have the following meanings: Dn = data register operand and M = memory operand.

MISCELLANEOUS INSTRUCTION CLOCK PERIODS

Table 34 and 35 indicate the number of clock periods for the following miscellaneous instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

Table 34. Miscellaneous Instruction Clock Periods

Instruction	Size	Register	Memory	Instruction	Size	Register	Memory
ANDI to CCR	Byte	20(3/0)	—	LINK	—	16(2/2)	—
ANDI to SR	Word	20(3/0)	—	MOVE from USP	—	4(1/0)	—
CHK	—	10(1/0) +	—	MOVE to USP	—	4(1/0)	—
EORI to CCR	Byte	20(3/0)	—	NOP	—	4(1/0)	—
EORI to SR	Word	20(3/0)	—	RESET	—	132(1/0)	—
ORI to CCR	Byte	20(3/0)	—	RTE	—	20(5/0)	—
ORI to SR	Word	20(3/0)	—	RTR	—	20(5/0)	—
MOVE from SR	—	6(1/0)	8(1/1) +	RTS	—	16(4/0)	—
MOVE to CCR	—	12(2/0)	12(2/0) +	STOP	—	4(0/0)	—
MOVE to SR	—	12(2/0)	12(2/0) +	SWAP	—	4(1/0)	—
EXG	—	6(1/0)	—	TRAPV	—	4(1/0)	—
EXT	Word	4(1/0)	—	UNLK	—	12(3/0)	—
	Long	4(1/0)	—				

+ add effective address calculation time

EXCEPTION PROCESSING CLOCK PERIODS

Table 36 delineates the number of clock periods for exception processing. The number of clock periods includes the time for all stacking, the vector fetch, and the fetch of the first instruction of the handler routine. The number of bus read and write cycles is shown in parenthesis as (r/w).

Table 35. Move Peripheral Instruction Execution Times

Instruction	Size	Register → Memory	Memory → Register
MOVEP	Word	16(2/2)	16(4/0)
	Long	24(2/4)	24(6/0)

Table 36. Exception Processing Clock Periods

Exception	Periods
Address Error	50(4/7)
Bus Error	50(4/7)
CHK Instruction	44(5/4) +
Divide by Zero	42(5/4)
Illegal Instruction	34(4/3)
Interrupt	44(5/3)*
Privilege Violation	34(4/3)
RESET**	40(6/0)
Trace	34(4/3)
TRAP Instruction	38(4/4)
TRAPV Instruction	34(4/3)

+ add effective address calculation time
 * The interrupt acknowledge cycle is assumed to take four clock periods.
 ** Indicates the time from when RESET and HALT are first sampled as negated to when instruction execution starts.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0	V
Input Voltage	V _{IN}	-0.3 to +7.0	V
Operating Temperature Range	T _A	T _L to T _H 0 to 70	°C
Storage Temperature	T _{STG}	-56 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance 64-Pin Ceramic	θ _{JA}	30	°C/W
64-Pin Plastic Dip		55 ± 5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = P_{INT} + P_{I/O}

P_{INT} = I_{CC} · V_{CC}, Watts—Chip Internal Power

P_{I/O} = Power Dissipation on Input and Output Pins—User Determined

For most applications P_{I/O} ≪ P_{INT} and can be neglected.

An approximate relationship between P_D and T_J (if P_{I/O} is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \cdot (T_A + 273^\circ\text{C}) + \theta_{JA} \cdot P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = T_L to T_H °C. See Figures 41, 42, and 43.

Characteristic	Symbol	Min	Max	Unit	Test Conditions
Input High Voltage	V _{IH}	2.0	V _{CC}	V	
Input Low Voltage	V _{IL}	V _{SS} - 0.3	0.8	V	
Input Leakage Current BERR, BGACK, BR, DTACK, CLK, IPL0-IPL2 VPA, HALT, RESET	I _{IN}	—	2.5 20	μA μA	V _{IN} = 5.25 V _{CC} = 0V
Three-State (Off State) Input Current AS, A1-A23, D0-D15, FC0-FC2, LDS, R/W, UDS, VMA	I _{TSI}	—	20	μA	V _{IN} = 0.4V to 2.4V V _{CC} = 5.25V
Output High Voltage E* E, AS, A1-A23, BG, D0-D15, FC0-FC2, LDS, R/W, UDS, VMA	V _{OH}	V _{CC} - 0.75 2.4	— —	V V	V _{CC} = 4.75V I _{OH} = -400 μA
Output Low Voltage HALT BG, FC0-FC2, A1-A23 RESET AS, D0-D15, LDS, R/W, UDS, VMA	V _{OL}	— — — —	0.6 0.5 0.5 0.5	V V V V	V _{CC} = 4.75V (I _{OL} = 1.6 mA) (I _{OL} = 3.2 mA) (I _{OL} = 5.0 mA) (I _{OL} = 5.3 mA)
Power Dissipation	P _{D***}	—	1.5	W	
Input Capacitance	C _{IN}	—	20.0	pF	V _{CC} = 5.0V, V _{IN} = 0V f = 1 MHz, T _A = 25°C

*With external pullup resistor of 1.1 kΩ

**Capacitance is periodically sampled rather than 100% tested.

***During normal operation instantaneous V_{CC} current requirements may be as high as 1.5A.

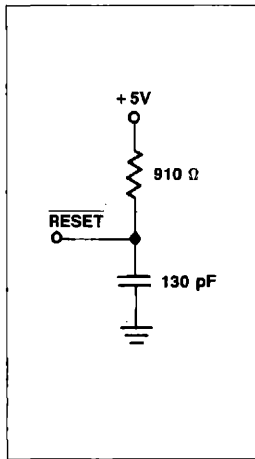


Figure 41. RESET Test Load

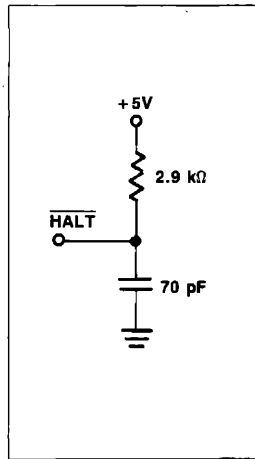


Figure 42. HALT Test Load

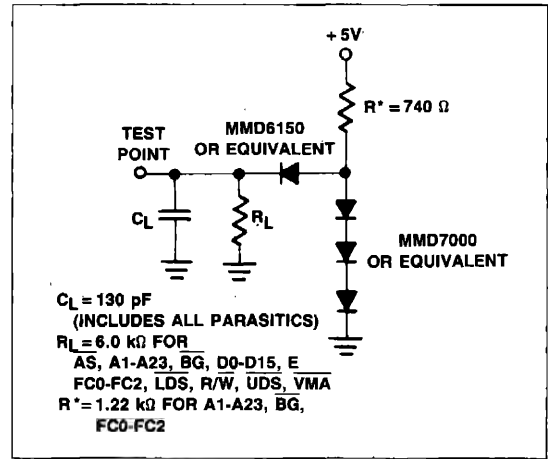


Figure 43. Test Loads

CLOCK TIMING (See Figure 44)

Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency of Operation	F	2.0	4.0	2.0	6.0	2.0	8.0	2.0	10.0	4.0	12.5	MHz
Cycle Time	t_{cyc}	250	500	167	500	125	500	100	500	80	250	ns
Clock Pulse Width	t_{CL}	115	250	75	250	55	250	45	250	35	125	ns
	t_{CH}	115	250	75	250	55	250	45	250	35	125	
Rise and Fall Times	t_{Cr}	—	10	—	10	—	10	—	10	—	5	ns
	t_{Cf}	—	10	—	10	—	10	—	10	—	5	

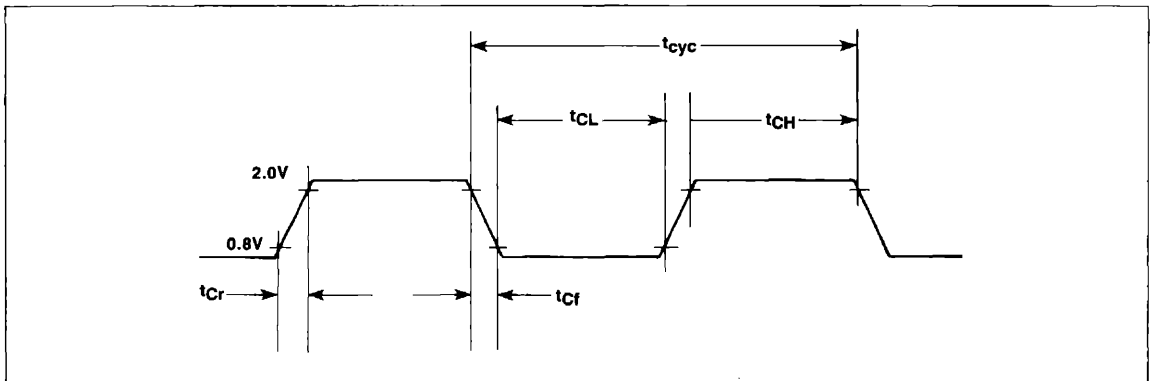


Figure 44. Input Clock Waveform

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

(VCC = 5.0 Vdc \pm 5%, VSS = 0 Vdc; TA = TL to TH, see Figures 45 and 46)

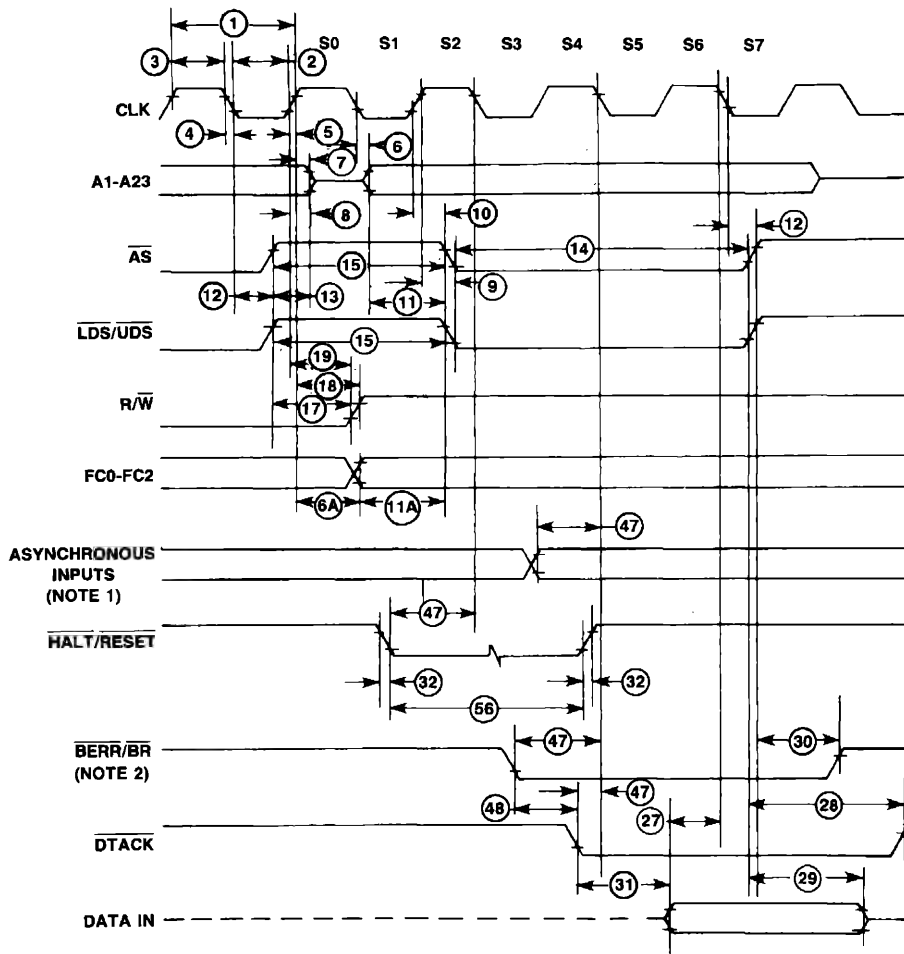
Num.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		12.5 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
1	Clock Period	t _{cyc}	250	500	167	500	125	500	100	500	80	250	ns
2	Clock Width Low	t _{CL}	115	250	75	250	55	250	45	250	35	125	ns
3	Clock Width High	t _{CH}	115	250	75	250	55	250	45	250	35	125	ns
4	Clock Fall Time	t _{Cf}	—	10	—	10	—	10	—	10	—	5	ns
5	Clock Rise Time	t _{Cr}	—	10	—	10	—	10	—	10	—	5	ns
6	Clock Low to Address	t _{CLAV}	—	90	—	80	—	70	—	60	—	55	ns
6A	Clock High to FC Valid	t _{CHFCV}	—	90	—	80	—	70	—	60	—	55	ns
7	Clock High to Address Data High Impedance (Maximum)	t _{CHAZx}	—	120	—	100	—	80	—	70	—	60	ns
8	Clock High to Address/FC Invald (Minimum)	t _{CHAZn}	0	—	0	—	0	—	0	—	0	—	ns
9 ¹	Clock High to \overline{AS} , \overline{DS} Low (Maximum)	t _{CHSLx}	—	80	—	70	—	60	—	55	—	55	ns
10	Clock High to \overline{AS} , \overline{DS} Low (Minimum)	t _{CHSLn}	0	—	0	—	0	—	0	—	0	—	ns
11 ²	Address to \overline{AS} , \overline{DS} (Read) Low/ \overline{AS} Write	t _{AVSL}	55	—	35	—	30	—	20	—	0	—	ns
11A ²	FC Valid to \overline{AS} , \overline{DS} (Read) Low/ \overline{AS} Write	t _{FCVSL}	80	—	70	—	60	—	50	—	40	—	ns
12 ¹	Clock Low to \overline{AS} , \overline{DS} High	t _{CLSH}	—	90	—	80	—	70	—	55	—	50	ns
13 ²	\overline{AS} , \overline{DS} High to Address/FC Invald	t _{SHAZ}	60	—	40	—	30	—	20	—	10	—	ns
14 ²	\overline{AS} , \overline{DS} Width Low (Read)/ \overline{AS} Write	t _{SL}	535	—	337	—	240	—	195	—	160	—	ns
14A ²	\overline{DS} Width Low (Write)	t _{DWPW}	285	—	170	—	115	—	95	—	80	—	ns
15 ²	\overline{AS} , \overline{DS} Width High	t _{SH}	285	—	180	—	150	—	105	—	65	—	ns
16	Clock High to \overline{AS} , \overline{DS} High	t _{CHSZ}	—	120	—	100	—	80	—	70	—	60	ns
17 ²	\overline{AS} , \overline{DS} High to R/W High	t _{SHRH}	60	—	50	—	40	—	20	—	10	—	ns
18 ¹	Clock High to R/W High (Maximum)	t _{CHRHx}	—	90	—	80	—	70	—	60	—	60	ns
19	Clock High to R/W High (Minimum)	t _{CHRHn}	0	—	0	—	0	—	0	—	0	—	ns
20 ¹	Clock High to R/W Low	t _{CHRL}	—	90	—	80	—	70	—	60	—	60	ns
20A ⁶	\overline{AS} Low to R/W Valid	t _{ASRV}	—	20	—	20	—	20	—	20	—	20	ns
21 ²	Address Valid to R/W Low	t _{AVRL}	45	—	25	—	20	—	0	—	0	—	ns
21A ²	FC Valid to R/W Low	t _{FCVRL}	80	—	70	—	60	—	50	—	30	—	ns
22 ²	R/W Low to \overline{DS} Low (Write)	t _{RSL}	200	—	140	—	80	—	50	—	30	—	ns
23	Clock Low to Data Out Valid	t _{CLDO}	—	90	—	80	—	70	—	55	—	55	ns
24	Clock High to R/W, VMA High Impedance	t _{CHRZ}	—	120	—	100	—	80	—	70	—	60	ns
25 ²	\overline{DS} High to Data Out Invald	t _{SHDO}	60	—	40	—	30	—	20	—	15	—	ns
26 ²	Data Out Valid to \overline{DS} Low (Write)	t _{DOSL}	55	—	35	—	30	—	20	—	15	—	ns
27 ⁶	Data In to Clock Low (Setup Time)	t _{DICL}	30	—	25	—	15	—	10	—	10	—	ns
27A	Late \overline{BERR} Low to Clock Low (Setup Time)	t _{BELCL}	45	—	45	—	45	—	45	—	45	—	ns
28 ²	\overline{AS} , \overline{DS} High to \overline{DTACK} High	t _{SHDAH}	0	490	0	325	0	245	0	190	0	150	ns

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (CONTINUED)

Num.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		12.5 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
29	\overline{DS} High to Data Invalid (Hold Time)	t_{SHDI}	0	—	0	—	0	—	0	—	0	—	ns
30	\overline{AS} , \overline{DS} High to $BERR$ High	t_{SHBEH}	0	—	0	—	0	—	0	—	0	—	ns
31 ²	\overline{DTACK} Low to Data In (Setup Time)	t_{DALDI}	—	180	—	120	—	90	—	65	—	50	ns
32	\overline{HALT} and \overline{RESET} Input Transition Time	$t_{RHr,f}$	0	200	0	200	0	200	0	200	0	200	ns
33	Clock High to \overline{BG} Low	t_{CHGL}	—	90	—	80	—	70	—	60	—	50	ns
34	Clock High to \overline{BG} High	t_{CHGH}	—	90	—	80	—	70	—	60	—	50	ns
35	\overline{BR} Low to \overline{BG} Low	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Cik. Per.
36	\overline{BR} High to \overline{BG} High	t_{BRHGH}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Cik. Per.
37	\overline{BGACK} Low to \overline{BG} High	t_{GALGH}	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	Cik. Per.
37A	\overline{BGACK} Low to \overline{BR} High (to Prevent Rearbitration)	t_{BGKBR}	30	—	25	—	20	—	20	—	20	—	ns
38	\overline{BG} Low to Bus High Impedance (with \overline{AS} High)	t_{GLZ}	—	120	—	100	—	80	—	70	—	60	ns
39	\overline{BG} Width High	t_{GH}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Cik. Per.
40	Clock Low to \overline{VMA} Low	t_{CLVML}	—	90	—	80	—	70	—	70	—	70	ns
41	Clock Low to E Transition	t_{CLC}	—	100	—	85	—	70	—	55	—	45	ns
42	E Output Rise and Fall Time	$t_{Er,f}$	—	25	—	25	—	25	—	25	—	25	ns
43	\overline{VMA} Low to E High	t_{VMLEH}	325	—	240	—	200	—	150	—	90	—	ns
44	\overline{AS} , \overline{DS} High to \overline{VPA} High	t_{SHVPH}	0	240	0	160	0	120	0	90	0	70	ns
45	E Low to Address/ \overline{VMA}/FC Invalid	t_{ELAI}	55	—	35	—	30	—	10	—	10	—	ns
46	\overline{BGACK} Width	t_{BGL}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Cik. Per.
47 ⁵	Asynchronous Input Setup Time	t_{ASI}	30	—	25	—	20	—	20	—	20	—	ns
48 ³	$BERR$ Low to \overline{DTACK} Low	t_{BELDAL}	30	—	25	—	20	—	20	—	20	—	ns
49	E Low to \overline{AS} , \overline{DS} Invalid	t_{ELSI}	—80	—	—80	—	—80	—	—80	—	—80	—	ns
50	E Width High	t_{EH}	900	—	600	—	450	—	350	—	280	—	ns
51	E Width Low	t_{EL}	1400	—	900	—	700	—	550	—	440	—	ns
52	E Extended Rise Time	t_{CIEHX}	—	80	—	80	—	80	—	80	—	80	ns
53	Data Hold from Clock High	t_{CHDO}	0	—	0	—	0	—	0	—	0	—	ns
54	Data Hold from E Low (Write)	t_{ELDOZ}	60	—	40	—	30	—	20	—	15	—	ns
55	R/W to Data Bus Impedance Change	t_{RLDO}	55	—	35	—	30	—	20	—	10	—	ns
56 ⁴	$\overline{HALT}/\overline{RESET}$ Pulse Width	t_{HRPW}	10	—	10	—	10	—	10	—	10	—	Cik. Per.

Notes:

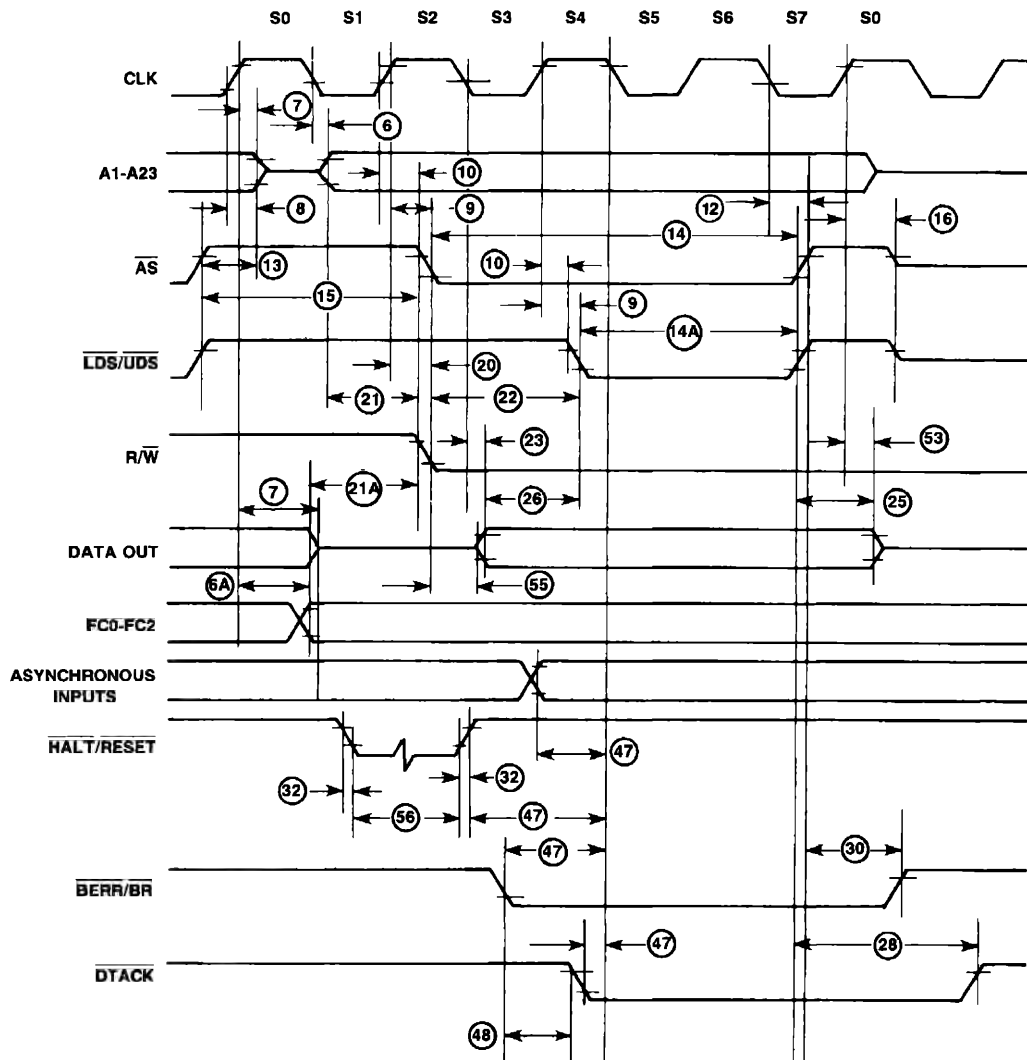
- For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in these columns.
- Actual value depends on clock period.
- If #47 is satisfied for both \overline{DTACK} and $BERR$, #48 may be 0 nanoseconds.
- For power up, the MPU must be held in \overline{RESET} state for 100 ms to stabilize all on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the system.
- If the asynchronous setup time (#47) requirements are satisfied the \overline{DTACK} low-to-data setup time (#31) requirement can be ignored. The data must only satisfy the data-in clock-low setup time (#27) for the following cycle.
- When \overline{AS} and R/W are equally loaded ($\pm 20\%$), subtract 10 nanoseconds from the value given in these columns.



NOTES:

1. SETUP TIME FOR THE ASYNCHRONOUS INPUTS \overline{BGACK} , $\overline{IPL0-IPL2}$, AND \overline{VPA} GUARANTEES THEIR RECOGNITION AT THE NEXT FALLING EDGE OF THE CLOCK.
2. \overline{BR} NEEDS FALL AT THIS TIME ONLY IN ORDER TO INSURE BEING RECOGNIZED AT THE END OF THIS BUS CYCLE.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 45. Read Cycle Timing



NOTES:

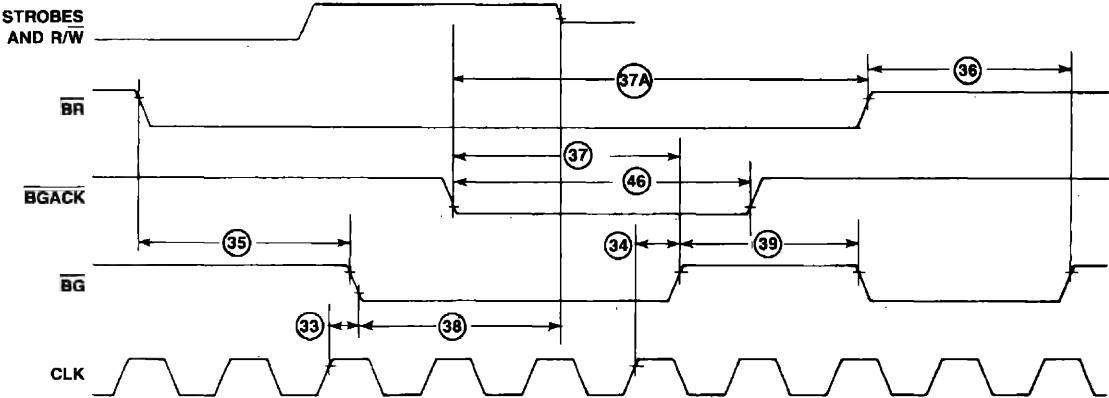
1. BECAUSE OF LOADING VARIATIONS, $\overline{R/W}$ MAY BE VALID AFTER \overline{AS} EVEN THOUGH BOTH ARE INITIATED BY THE RISING EDGE OF S2 (SPECIFICATION 20A).
2. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 46. Write Cycle Timing

AC ELECTRICAL SPECIFICATIONS — BUS ARBITRATION
(VCC = 5.0 Vdc ±5%, VSS = 0 Vdc, TA = 0° to 70°C. See Figure 47.)

Num.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		12.5 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
33	Clock High to $\overline{\text{BG}}$ Low	t_{CHGL}	—	90	—	80	—	70	—	60	—	50	ns
34	Clock High to $\overline{\text{BG}}$ High	t_{CHGH}	—	90	—	80	—	70	—	60	—	50	ns
35	$\overline{\text{BR}}$ Low to $\overline{\text{BG}}$ Low	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
36	$\overline{\text{BR}}$ High to $\overline{\text{BG}}$ High	t_{BRHGH}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37	$\overline{\text{BGACK}}$ Low to $\overline{\text{BG}}$ High	t_{GALGH}	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	Clk. Per.
37A	$\overline{\text{BGACK}}$ Low to $\overline{\text{BR}}$ High (to Prevent Rearbitration)	t_{BGKBR}	30	—	25	—	20	—	20	—	20	—	ns
38	$\overline{\text{BG}}$ Low to Bus High Impedance (with AS High)	t_{GLZ}	—	120	—	100	—	80	—	70	—	60	ns
39	$\overline{\text{BG}}$ Width High	t_{GH}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clk. Per.
46	$\overline{\text{BGACK}}$ Width	t_{BGL}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clk. Per.

THESE WAVEFORMS SHOULD ONLY BE REFERENCED IN REGARD TO THE EDGE-TO-EDGE MEASUREMENT OF THE TIMING SPECIFICATIONS. THEY ARE NOT INTENDED AS A FUNCTIONAL DESCRIPTION OF THE INPUT AND OUTPUT SIGNALS. REFER TO OTHER FUNCTIONAL DESCRIPTIONS AND THEIR RELATED DIAGRAMS FOR DEVICE OPERATION.



- NOTES:
1. SETUP TIME FOR THE ASYNCHRONOUS INPUTS $\overline{\text{BERR}}$, $\overline{\text{BGACK}}$, $\overline{\text{BR}}$, $\overline{\text{DTACK}}$, $\overline{\text{IPL0-IPL2}}$, AND $\overline{\text{VPA}}$ GUARANTEES THEIR RECOGNITION AT THE NEXT FALLING EDGE OF THE CLOCK.
 2. WAVEFORM MEASUREMENTS FOR ALL INPUTS AND OUTPUTS ARE SPECIFIED AT: LOGIC HIGH = 2.0 VOLTS, LOGIC LOW = 0.8 VOLTS

Figure 47. AC ELECTRICAL Waveforms — Bus Arbitration



R68465 DOUBLE-DENSITY FLOPPY DISK CONTROLLER (DDFDC)

PRELIMINARY

DESCRIPTION

The R68465 Double-Density Floppy Disk Controller (DDFDC) interfaces up to four floppy disk drives to a 68000/68008 microprocessor-based system. The DDFDC simplifies the system design by minimizing both the number of external hardware components and software steps needed to implement the floppy disk drive (FDD) interface. Control signals supplied by the DDFDC reduce the number of components required in external phase locked loop and write precompensation circuitry. Memory-mapped registers containing commands, status and data simplify the software interface. Built-in functions reduce the software overhead needed to control the FDD interface. The DDFDC supports both the IBM 3740 Single-Density (FM) and IBM System 34 Double-Density (MFM) formats.

The DDFDC interfaces directly to the 68000/68008 asynchronous microprocessor bus and operates with 8-bit byte length data transferred on the bus. The DDFDC will operate in either DMA or non-DMA mode. In DMA mode, the MPU need only load the command into the DDFDC and all data transfers occur under DMA control. The DDFDC is directly compatible with the MC68440 Dual Direct Memory Access Controller (DDMAC). In non-DMA mode, the DDFDC generates an interrupt to the MPU indicating that a byte of data is available.

Controller commands, command or device status, and data are transferred between the DDFDC and the MPU via six internal registers. The Main Status Register (MSR) stores the DDFDC status information while four additional status registers provide result information to the MPU following each controller command. The Data Register (DR) stores actual disk data, parameters, controller commands and FDD status information for use by the MPU.

The R68465 executes 15 separate multi-byte commands:

Read Data	Specify
Write Data	Format a Track
Read Deleted Data	Scan Equal
Write Deleted Data	Scan High or Equal
Read a Track	Scan Low or Equal
Read ID	Sense Interrupt Status
Seek	Sense Drive Status
Recalibrate (Restore to Track 0)	

FEATURES

- Address mark detection circuitry
- Software control of
 - Track stepping rate
 - Head load time
 - Head unload time
- IBM compatible in both single- and double-density recording formats
- Programmable data record lengths: 128, 256, 512, 1024, 2048, 4096 or 8192 bytes/sector
- Multi-sector and multi-track transfer capability
- Controls up to four floppy disk drives
- Data scan capability—will scan a single sector or an entire track of data fields, comparing on a byte-by-byte basis data in the processor's memory with data read from the disk
- Data transfers in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Directly compatible with 68000 16-bit and 68008 8-bit asynchronous microprocessor bus
- Single phase 8 MHz Clock
- Single +5 Volt Power Supply

ORDERING INFORMATION

Part Number	CLK Frequency	Temperature Range
R68465	8 MHz	0°C to 70°C
Package: C = Ceramic P = Plastic		

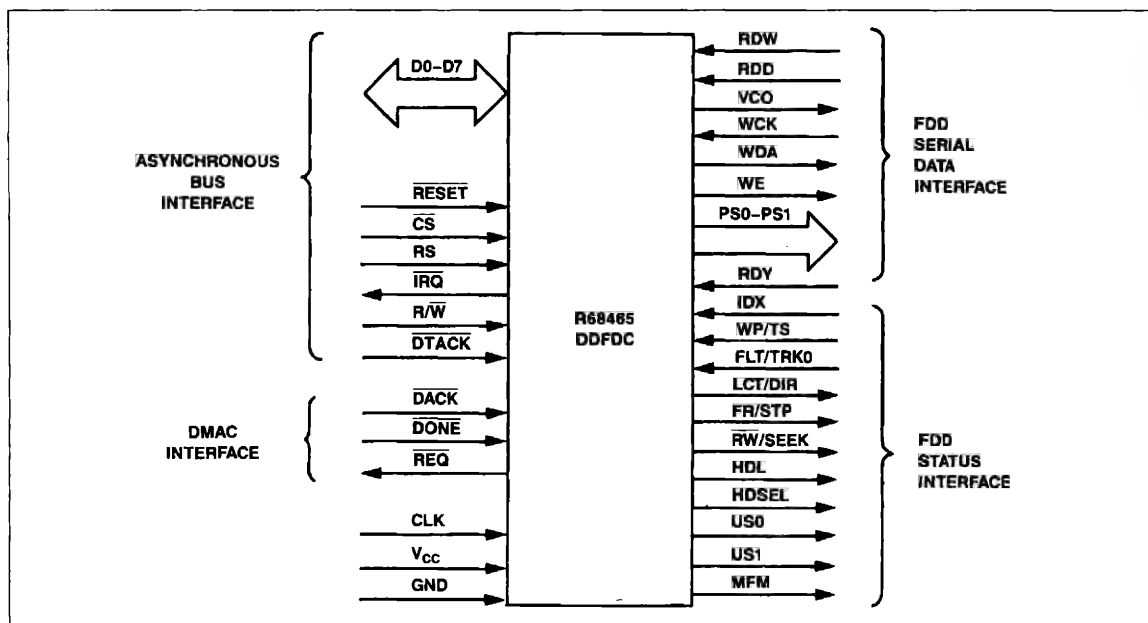


Figure 1. DDFDC Input and Output Signals

PIN DESCRIPTION

Throughout this document signals are presented using the terms active and inactive, or asserted and negated, independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar. For example, $\overline{R/W}$ indicates read is active high and a write is active low.

BUS INTERFACE

D0-D7—Data Lines. The bidirectional data lines transfer data between the DDFDC and the 8-bit data bus.

CLK—CLOCK. The clock is a TTL compatible 8 MHz square wave signal.

\overline{RESET} —RESET. This active high input places the DDFDC in the idle state and resets the output lines to the floppy disk drives to the low state.

\overline{CS} —Chip Select. The DDFDC is selected when the \overline{CS} input is low.

RS—Data/Status Register Select. This input selects the Data or Status Register for reading from or writing to. When RS = high, the Data Register is selected and the state of $\overline{R/W}$ determines whether it is a read ($\overline{R/W}$ = high) or a write ($\overline{R/W}$ = low) operation. When RS = low, the Status Register is selected. This register may only be read ($\overline{R/W}$ = high); the state \overline{RW} = low is invalid when the Status Register is selected.

\overline{IRQ} —Interrupt Request. This active low output is the interrupt request generated by the DDFDC to the MPU. \overline{IRQ} is asserted upon completion of some DDFDC commands and before a data byte is transferred between the DDFDC and the data bus (in the Non-DMA mode).

$\overline{R/W}$ —Read/Write. This input defines the data bus transfer as a read or write cycle. When high (read), the data transfer is from the DDFDC to the data bus. When low (write), the data transfer is from the data bus to the DDFDC.

DTACK—Data Transfer Acknowledge. This signal is the asynchronous handshake line for information transfer on the 68000 system bus. It is generated by the DDFDC as an acknowledge to the CS signal in an asynchronous transfer. A low output indicates that valid data is on the bus (read cycle) or that data has been written (write cycle). Except when being asserted, this signal is normally in the high impedance state.

The output characteristics of \overline{DTACK} are the same as other system interface signals with allowances for an external pull-up resistor such that the output is driven to the high level first and then to the high impedance state.

DIRECT MEMORY ACCESS CONTROLLER (DMAC) INTERFACE

\overline{DACK} —DMA Acknowledge. The DMA transfer acknowledge signal is a TTL compatible input generated by the DMA controller (DMAC) controlling the DDFDC. The DMA cycle is active when \overline{DACK} is low and the DDFDC is performing a DMA transfer.

\overline{REQ} —Data DMA Request. The transfer request signal is a TTL compatible output generated by the DDFDC to request a data transfer operation under control of the DMAC (in the DMA mode). The request is active when \overline{REQ} = low. The signal is reset inactive when DMA Acknowledge (\overline{DACK}) is asserted (low).

\overline{DONE} —DMA Transfer Complete. This input signal is issued to the DDFDC when the DMA transfer for a channel is complete. The signal is active low concurrent with the \overline{DACK} input when the DMA operation is complete as a result of that transfer.

FDD SERIAL DATA INTERFACE

RDD—Read Data. Read Data input from the floppy disk drive (FDD) containing clock and data bits.

RDW—Read Data Window. Data Window input generated by the Phase Locked Loop (PLL) and used to sample data from the FDD.

VCO—Variable Frequency Oscillator Sync. This output signal inhibits the VCO in the PLL circuit when low and enables the VCO in the PLL circuit when high. This inhibits RDD and RDW from being generated until valid data is detected from the FDD.

WCK—Write Clock. This input clock determines the Write Data rate to the FDD. The data rate is 500 KHz in the FM mode (MFM = low) and 1 MHz in the MFM mode (MFM = high). The pulse width is 250 ns (typical) in both modes.

WDA—Write Data. Serial write data output to the FDD containing both clock and data bits.

WE—Write Enable. This output signal enables the Write Data into the FDD when high.

PS0—PS1—Preshift. These outputs are encoded to convey write compensation status during the MFM mode to determine early, late or normal times as follows:

Write Precompensation Status	Preshift Outputs	
	PS0	PS1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

0 = Low, 1 = High

FDD STATUS INTERFACE

RDY—Ready. An active high input signal indicates the FDD is ready to send data to, or receive data from, the DDFDC.

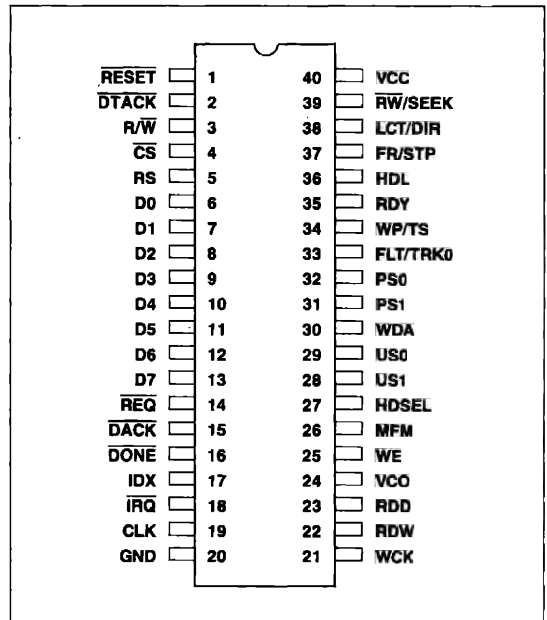
IDX—Index. An active high input signal from the FDD indicates the index hole is under the index sensor. Index is used to synchronize DDFDC timing.

$\overline{RW/SEEK}$ —Read Write/Seek. Mode selection signal to the FDD which controls the multiplexer from the multiplexed signals. When $\overline{RW/SEEK}$ is low, the Read/Write mode is commanded; when $\overline{RW/SEEK}$ is high, the Seek mode is commanded.

$\overline{RW/SEEK}$	Mode	Active FDD Interface Signals
Low	Read/Write	WP, FLT, LCT, FR
High	Seek	TS, TRK0, DIR, STP

WP/TS—Write Protect/Two Side. An active high multiplexed input signal from the FDD. In the Read/Write mode, WP/TS high indicates the media is write-protected. In the Seek mode, WP/TS high indicates the media is two-sided.

FLT/TRK0—Fault/Track Zero. An active high multiplexed input from the FDD. In the Read/Write mode ($\overline{RW/SEEK}$ = low), FLT/TRK0 high indicates an FDD fault. In the Seek mode, FLT/TRK0 high indicates that the read/write head is positioned over track zero.



R68465 Pin Diagram

LCT/DIR—Low Current/Direction. A multiplexed output to the FDD. In the Read/Write mode, LCT/DIR is low when the read/write head is to be positioned over the inner tracks and the LCT/DIR is high when the head is to be positioned over the outer tracks. In the Seek mode, LCT/DIR controls the head direction. When LCT/DIR is high, the head steps to the outside of the disk; when LCT/DIR is low, the head steps to the inside of the disk.

FR/STP—Fault Reset/Step. A multiplexed output to the FDD. In the Read/Write mode, FR/STP high resets the fault indicator in the FDD. An FR pulse is issued at the beginning of each read or write command prior to issuing HDL. In the Seek mode, FR/STP provides the step pulses to move the read/write head to another track in the direction indicated by the LCT/DIR signal.

HDL—Head Load. An active high output to notify the FDD that the read/write head should be loaded (placed in contact with the media). A low level indicates the head should be unloaded.

HD—Head Select. An output to the FDD to select the proper read/write head. Head One is selected when HD = high and Head Zero is selected when HD = low.

US0-US1—Unit Select. Output signals for floppy disk drive selection as follows:

Unit Select		Floppy Disk Drive Select
US0	US1	
0	0	0
0	1	1
1	0	2
1	1	3

0 = Low, 1 = High

MFM—MFM Mode. Output signal to the FDD to indicate MFM or FM mode. Selects the MFM mode when MFM = high and the FM mode when MFM = low.

VCC—Power. +5V dc.

GND—Ground (V_{ss}).

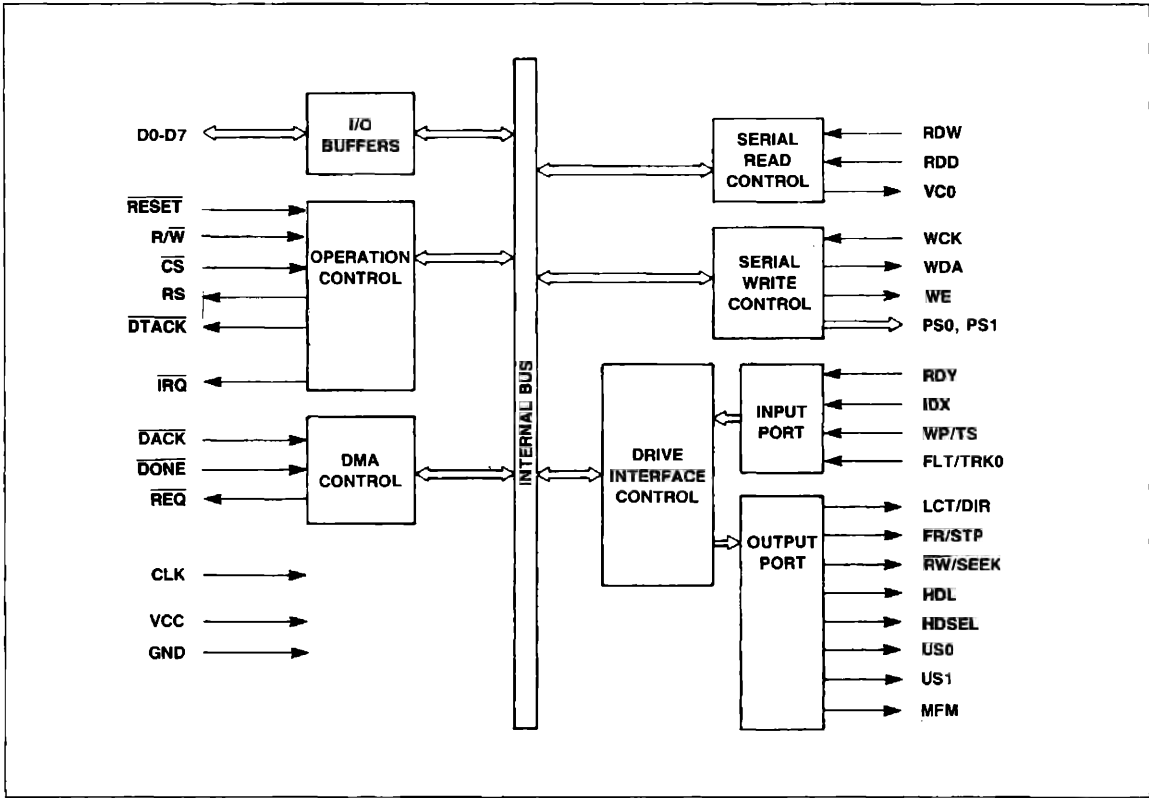


Figure 2. DDFDC Block Diagram

DDFDC REGISTERS

The DDFDC contains six registers which may be accessed by the processor or DMA controller via the system (i.e., micro-processor) bus: a Main Status Register, a Data Register, and four Result Status Registers. The 8-bit Main Status Register (MSR) contains the status information of the DDFDC, and may be accessed at any time. The 8-bit Data Register, consisting of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, parameters and FDD status information. Bytes of data are read out of, or written into, the Data Register in order to initiate a command or to obtain the results of a command execution.

The read-only Main Status Register facilitates the transfer of data between the system and the DDFDC. The other Status Registers (ST0, ST1, ST2 and ST3) are only available during the result phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The relationship between the status/data registers and the R/W and RS signals is shown below.

RS	R/W	Function
0	0	Read Main Status Register
0	0	Illegal
1	1	Read from Data Register
1	0	Write into Data Register
0 = Low, 1 = High		

Table 1 shows each of the status registers used by the DDFDC and each bit assignment within the individual registers. Table 2 defines the symbols used throughout the command definitions. Each register bit symbol is defined in the register definition that follows Table 2.

REGISTER DEFINITIONS

Main Status Register (MSR)

7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B

The Main Status Register (MSR) contains the status information of the DDFDC, and must be read by the processor before each byte is written to, or read from, the Data Register during the command or result phase. MSR reads are not required during the execution phase. The Data Input/Output (DIO) and Request for Master (RQM) bits in the MSR indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last R/W during command or result phases and the DIO and RQM getting set or reset is 12 μ s. For this reason, every time the MSR is read the processor should wait 12 μ s. The maximum time from the end of the last read in the result phase to when bit 4 (DDFDC Busy) goes low is also 12 μ s.

The DIO and RQM timing chart is shown in Figure 3.

MSR

- 7 RQM —Request for Master.
0 Data Register is not ready.
1 Data Register is ready.

MSR

- 6 DIO —Data Input/Output.
0 Data transfer is from system to the Data Register.
1 Data transfer is from Data Register to the system.

MSR

- 5 EXM —Execution Mode. (Non-DMA mode only).
0 Execution phase ended, result phase begun.
1 Execution phase started.

MSR

- 4 CB —Controller (DDFDC) Busy.
0 DDFDC is not busy, will accept a command.
1 DDFDC is busy, will not accept a command.

MSR

- 3 D3B —Floppy Disk Drive (FDD) 3 Busy.
0 FDD 3 is not busy, DDFDC will accept read or write command.
1 FDD 3 is busy, DDFDC will not accept read or write command.

MSR

- 2 D2B —FDD 2 Busy.
0 FDD 2 is not busy, DDFDC will accept read or write command.
1 FDD 2 is busy, DDFDC will not accept read or write command.

MSR

- 1 D1B —FDD 1 Busy.
0 FDD 1 is not busy, DDFDC will accept read or write command.
1 FDD 1 is busy, DDFDC will not accept read or write command.

MSR

- 0 D0B —FDD 0 Busy.
0 FDD 0 is not busy, DDFDC will accept read or write command.
1 FDD 0 is busy, DDFDC will not accept read or write command.

Status Register 0 (ST0)

7	6	5	4	3	2	1	0
IC	SE	EC	NR	HD	US		
					US1	US0	

The Status Register 0 (ST0) as well as the other status registers (ST1-ST3), are available only during the result phase, and may be read only after completing a command. The particular command executed determines which status registers are used and may be read.

Table 1. DDFDC Status Register Bit Assignments

Bit Number							
7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B
IC		SE	EC	NR	HD	US	
EN	0	DE	OR	0	ND	NW	MA
0	CM	DD	WT	SH	SN	BT	MD
FLT	WP	RDY	TRK0	TS	HD	US1	US0

Main Status Register (MSR)

Status Register 0 (ST0)

Status Register 1 (ST1)

Status Register 2 (ST2)

Status Register 3 (ST3)

Table 2. Command Symbol Description

Symbol	Name	Description
D	Data	The data pattern which is going to be written into a sector.
D0-D7	Data Bus	8-bit data bus, where D0 is the least significant data line and D7 is the most significant data line.
DTL	Data Length	When N is defined as 00, DTL is the number of data bytes to read from or write into the sector.
EOT	End of Track	The final sector number on a track. During read or write operation, the DDFDC stops data transfer after reading from or writing to the sector equal to EOT.
GPL	Gap Length	The length of Gap 3. During read/write commands this value determines the number of bytes that the VCO will stay low after two CRC bytes. During the Format a Track command it determines the size of Gap 3.
H	Head Address	Head number 0 or 1, as specified in ID field.
HD (H)	Head	A selected head number 0 or 1 which controls the polarity of pin 27. (H = HD in all command words).
HLT	Head Load Time	The head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	The head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	When MF = 0, FM mode is selected; and when MF = 1, MFM mode is selected.
MT	Multi-Track	When MT = 1, a multi-track operation is to be performed. After finishing a read/write operation on side 0, the DDFDC will automatically start searching for sector 1 on side 1.
N	Bytes/Sector	The number of data bytes written in a sector.
ND	Non-DMA Mode	When ND = 1, operation is in the Non-DMA mode; when ND = 0, operation is in the DMA mode.
NTN	New Track Number	A new track number, which will be reached as a result of the Seek command. Desired head position.
PTN	Present Track Number	The track number at the completion of Sense Interrupt Status command. Present head position.
R	Record (Sector)	The sector number to be read or written.
RS	Register Select	Controls selection of Main Status Register (RS = low) or Data Register (RS = high).
R/W	Read/Write	Either read (R) or write (W) signal
ST	Sectors/Track	The number of sectors per track.
SK	Skip	Skip Deleted Data Address Mark.
SRT	Step Rate Time	The stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by RS = low). ST0-ST3 may be read only after a command has been executed and contain information relevant to that particular command.
STP	Sector Test Process	During a Scan command, if STP = 01, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA controller); and if STP = 02, then alternate sectors are read and compared.
T	Track Number	The current/selected track number of the medium (0-255).
US0,US1	Unit Select	A selected drive number (0-3).

ST0

7 6 IC —Interrupt Code.
 0 0 Normal Termination (NT). Command was properly executed and completed.
 0 1 Abnormal Termination (AT). Command execution was started, but was not successfully completed.
 1 0 Invalid Command (IC). Received command was invalid.
 1 1 Abnormal Termination (AT). The Ready (RDY) signal from the FDD changed state during command execution.

ST0

5 SE —Seek End.
 0 Seek command is not completed.
 1 Seek command completed by DDFDC.

ST0

4 EC —Equipment Check.
 0 No error.
 1 Either a fault signal is received from the FDD or the track 0 signal failed to occur after 256 step pulses (Recalibrate Command).

ST0

3 NR —Not Ready.
 0 FDD is ready.
 1 FDD is not ready at issue of read or write command. If a read or write command is issued to side 1 of a single-sided drive, this bit is also set.

ST0

2 HD —Head Address. (At Interrupt).
 0 Head Select 0.
 1 Head Select 1.

ST0

1 0 US —Unit Select. (At Interrupt).
 0 0 FDD 0 selected.
 0 1 FDD 1 selected.
 1 0 FDD 2 selected.
 1 1 FDD 3 selected.

Status Register 1 (ST1)

7	6	5	4	3	2	1	0
EN	0	DE	OR	0	ND	NW	MA

ST1

7 EN —End of Track.
 0 No error.
 1 DDFDC attempted to access a sector beyond the last sector of a track.

ST1

6 —Not Used. Always Zero.

ST1

5 DE —Data Error.
 0 No error.
 1 DDFDC detected a CRC error in ID field or the Data field.

ST1

4 OR —Over Run.
 0 No error.
 1 DDFDC was not serviced by the system during data transfers, within a predetermined time interval.

ST1

3 —Not Used. Always Zero.

ST1

2 ND —No Data.
 0 No error.
 1 3 possible errors.
 1. DDFDC cannot find sector specified in ID Register during execution of Read Data, Write Deleted Data or Scan commands.
 2. DDFDC cannot read ID field without an error during Read ID command.
 3. DDFDC cannot find starting sector during execution of Read a Track command.

ST1

1 NW —Not Writable.
 0 No error.
 1 DDFDC detected a write protect signal from FDD during execution of Write Data, Write Deleted Data or Format a Track commands.

ST1

0 MA —Missing Address Mark.
 0 No error.
 1 2 possible errors.
 1. DDFDC cannot detect the ID Address Mark after encountering the index hole twice.
 2. DDFDC cannot detect the Data Address Mark or Deleted Data Address Mark. The MD (Missing Address Mark in Data field) of Status Register 2 is also set.

Status Register 2 (ST2)

7	6	5	4	3	2	1	0
0	CM	DD	WT	SH	SN	BT	MD

ST2

7 —Not Used. Always Zero.

ST2

6 CM —Control Mark.
 0 No error.
 1 DDFDC encountered a sector which contained a Deleted Data Address Mark during execution of a Read Data, Read a Track, or Scan command, or the DDFDC encountered a sector which contained a Data Address Mark during execution of a Read Deleted Data command.

ST2

- 5 DD —Data Error in Data Field.**
 0 No error.
 1 DDFDC detected a CRC error in the Data field.

ST2

- 4 WT —Wrong Track.**
 0 No error.
 1 Contents of T on the disk is different from that stored in IDR. Bit is related to ND (Bit 2) of Status Register 1.

ST2

- 3 SH —Scan Equal Hit.**
 0 No "equal" condition during a scan command.
 1 "Equal" condition satisfied during a scan command.

ST2

- 2 SN —Scan Not Satisfied.**
 0 No error.
 1 DDFDC cannot find a sector on the track which meets the scan command condition.

ST2

- 1 BT —Bad Track.**
 0 No error.
 1 Contents of T on the disk is different from that stored in the IDR and T = FF. Bit is related to ND (Bit 2) of Status Register 1.

ST2

- 0 MD —Missing Address Mark in Data Field.**
 0 No error.
 1 DDFDC cannot find a Data Address Mark or Deleted Data Address Mark during a data read from the disk.

Status Register 3 (ST3)

7	6	5	4	3	2	1	0
FLT	WP	RDY	TRK0	TS	HD	US1	US0

Status Register 3 (ST3) holds the results of the Sense Drive Status command.

ST3

- 7 FLT —Fault.**
 0 Fault (FLT) signal from the FDD is low.
 1 Fault (FLT) signal from the FDD is high.

ST3

- 6 WP —Write Protect.**
 0 Write Protect (WP) signal from the FDD is low.
 1 Write Protect (WP) signal from the FDD is high.

ST3

- 5 RDY —Ready.**
 0 Ready (RDY) signal from the FDD is low.
 1 Ready (RDY) signal from the FDD is high.

ST3

- 4 TRK0 —Track 0.**
 0 Track 0 (TRK0) signal from the FDD is low.
 1 Track 0 (TRK0) signal is from the FDD is high.

ST3

- 3 TS —Two Side.**
 0 Two Side (TS) signal from the FDD is low.
 1 Two Side (TS) signal from the FDD is high.

ST3

- 2 HD —Head Select.**
 0 Head Select (HD) signal to the FDD is low.
 1 Head Select (HD) signal to the FDD is high.

ST3

- 1 US1 —Unit Select 1.**
 0 Unit Select 1 (US1) signal to the FDD is low.
 1 Unit Select 1 (US1) signal to the FDD is high.

ST3

- 0 US0 —Unit Select 0.**
 0 Unit Select 0 (US0) signal to the FDD is low.
 1 Unit Select 0 (US1) signal to the FDD is high.

COMMAND SEQUENCE

The DDFDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer of data from the system. After command execution, the result of the command may be a multi-byte transfer of data back to the system. Because of this multi-byte transfer of information between the DDFDC and the system, each command consists of three phases:

Command Phase—The DDFDC receives all information required to perform a particular operation from the system.

Execution Phase—The DDFDC performs the instructed operation.

Result Phase—After completion of the operation, status and other housekeeping information are made available to the system.

The bytes of data sent to the DDFDC to form a command, and read out of the DDFDC in the result phase, must occur in the order shown for each command sequence. That is, the command Code byte must be sent first followed by the other bytes in the specified sequence. All command bytes must be written and all result bytes must be read in each phase. After the last byte of data in the command phase is received by the DDFDC, the execution phase starts. Similarly, when the last byte of data is read out in the Result Phase, the command is ended and the DDFDC is ready to accept a new command. A command can be terminated by asserting the **DONE** signal to the DDFDC. This ensures that the processor can always get the DDFDC's attention even if the command in process hangs up in an abnormal manner.

COMMAND DESCRIPTION

READ DATA

A command set of nine bytes places the DDFDC into the Read Data mode. After the Read Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID Address Marks and ID fields from the disk. When the current sector number (R) stored in the ID Register (IDR) matches the sector number read from the disk, the DDFDC transfers data from the disk Data field to the data bus.

After completion of the read operation from the current sector, the DDFDC increments the Sector Number (R) by one, and the data from the next sector is read and output to the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Command terminates after reading the last data byte from sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The Read Data command can also be terminated by a low DONE signal. DONE should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of TC, the DDFDC stops outputting data to the data bus, but continues to read data from the current sector, checks CRC (Cyclic Redundancy Count) bytes, and then at the end of that sector terminates the Read Data command and sets bits 7 and 6 in ST0 to 0. The amount of data which can be handled with a single command to the DDFDC depends upon MT (Multi-Track), MF (MFM/FM), and N (Number of Bytes/Sector) values. Table 3 shows the transfer capacity.

The multi-track function (MT) allows the DDFDC to read data from both sides of the disk. For a particular track, data is transferred starting at sector 1, side 0 and completed at sector L, side 1 (sector L = last sector on the side). This function pertains to only one track (the same track) on each side of the disk.

When N = 0 in command byte 6 (FM mode), the Data Length (DTL) in command byte 9 defines the data length that the DDFDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond the DTL is not sent to the data bus. The DDFDC reads (internally) the complete sector, performs the CRC check, and depending upon the manner of command termination, may perform a multi-sector Read operation. When N is non-zero (MFM mode), DTL has no meaning and should be set to FF.

At the completion of the Read Data command, the head is not unloaded until the Head Unload Time (HUT) interval defined in the Specify command has elapsed. The head settling time may be avoided between subsequent reads if the processor issues another command before the head unloads. This time savings is considerable when disk contents are copied from one drive to another.

If the DDFDC detects the Index Hole twice in succession without finding the right sector (indicated in R), then the DDFDC sets the No Data (ND) flag in Status Register 1 (ST1) to a 1, sets Status Register 0 (ST0) bits 7 and 6 to 0 and 1, respectively, and terminates the Read Data command.

After reading the ID and Data fields in each sector, the DDFDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the DDFDC sets the Data Error (DE) flag in ST1 to a 1, sets the Data Error in Data Field (DD) flag in ST2 to a 1 if a CRC error occurs in the Data field, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the DDFDC reads a Deleted Data Address Mark from the disk, and the Skip Deleted Data Address Mark bit in the first command byte is not set (SK = 0), then the DDFDC reads all the data in the sector, sets the Control Mark (CM) flag in ST2 to a 1, and terminates the command. If SK = 1, the DDFDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

Table 3. DDFDC Transfer Capacity

Multi-Track (MT)	MFM/FM (MF)	Bytes/Sector (N)	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Disk
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

During disk data transfers from the DDFDC to the system, the DDFDC must be serviced by the system within 27 μ s in the FM mode, and within 13 μ s in the MFM mode, otherwise the DDFDC sets the Over Run (OR) flag in ST1 to a 1, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the processor terminates a read (or write) operation in the DDFDC, then the ID information in the result phase is dependent upon the state of the MT bit in the first command byte and the End of Track (EOT) byte. Table 4 shows the values for Track Number (T), Head Number (H), Sector Number (R), and Number of Data Bytes/Sector (N), when the processor terminates the command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	0	1	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DATA

A command set of nine bytes places the DDFDC in the Write Data mode. After the Write Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID fields from the disk. When the four bytes (T, H, R, N) loaded during the command match the four bytes of the ID field from the disk, the DDFDC transfers data from the data bus to the disk Data field.

After writing data into the current sector, the DDFDC increments the sector number (R) by one, and writes into the Data field in the next sector. The DDFDC continues this multi-sector write operation until the last byte is written to sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The command can also be terminated by a low on DONE. If DONE is sent to the DDFDC while writing into the current sector, then the remainder of the Data field is filled with 00 (zeros). In this case, ST0 bits 7 and 6 are set to 0 and the command is terminated.

The DDFDC reads the ID field of each sector and checks the CRC bytes. If the DDFDC detects a read error (incorrect CRC) in one of the ID fields, it terminates the Write Data command, sets the DE flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

The Write Data command operates in much the same manner as the Read Data command. Refer to the Read Data command for the handling of the following items:

- Transfer Capacity
- End of Track (EN) flag
- No Data (ND) flag
- Head Unload Time (HUT) interval
- ID information when the processor terminates command (see Table 4)
- Definition of Data Length (DTL) when N = 0 and when N \neq 0

Table 4. DDFDC Command Termination Values

Command Phase ID		Final Sector Transferred to/from Data Bus	Result Phase ID			
Multi-Track (MT)	Head Number (HD)		Track Number (T)	Head Number (H)	Sector Number (R)	No. of Data Bytes (N)
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	T + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	LSB	01	NC
Notes:						
1. NC (No Change): The same value as the one at the beginning of command execution.						
2. LSB (Least Significant Bit): The least significant bit of H is complemented.						

In the Write Data mode, data transfers from the data bus to the DDFDC must occur within 27 μ s in the FM mode, and within 13 μ s in the MFM mode. If the time interval between data transfers is longer than this, then the DDFDC terminates the Write Data command, sets the Over Run (OR) flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	0	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)							
	2	Status Register 1 (ST1)							
	3	Status Register 2 (ST2)							
	4	Track Number (T)							
	5	Head Number (H)							
	6	Sector Number (R)							
	7	Number of Data Bytes per Sector (N)							

WRITE DELETED DATA

The Write Deleted Data command is the same as the Write Data command except a Deleted Data Address Mark is written at the beginning of the Data field instead of the normal Data Address Mark.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ DELETED DATA

The Read Deleted Data command is the same as the Read Data command except that if SK = 0 when the DDFDC detects a **Data Address Mark** at the beginning of a Data field, it reads all the data in the sector and sets the CM flag in ST2 to a 1, and then terminates the command. If SK = 1, then the DDFDC skips the sector with the **Data Address Mark** and reads the next sector.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	1	1	0	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ A TRACK

The Read a Track command is similar to the Read Data command except that this is a continuous read operation where all Data fields from each of the sectors on a track are read and transferred to the data bus. Immediately after encountering the Index Hole, the DDFDC starts reading the Data fields as continuous blocks of data. This command terminates when the number of sectors read is equal to EOT. Multi-track operations are not allowed with this command.

If the DDFDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The DDFDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag in ST1 to a 1 if there is no match.

If the DDFDC does not find an ID Address Mark on the disk after it encounters the Index Hole for the second time it terminates the command, sets the Missing Address Mark (MA) flag in ST1 to a 1, and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	SK	0	0	0	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ ID

The two-byte Read ID command returns the present position of the read/write head. The DDFDC obtains the value from the first ID field it is able to read, sets bits 7 and 6 in ST0 to 0 and terminates the command.

If no proper ID Address Mark is found on the disk before the Index Hole is encountered for the second time then the Missing Address Mark (MA) flag in ST1 is set to a 1, and if no data is found then the ND flag to a 1 is also set in ST1. Bits 7 and 6 in ST0 are set to 0 and 1, respectively and the command is terminated.

During this command there is no data transfer between DDFDC and the data bus except during the result phase.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	0	1	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

FORMAT A TRACK

The six-byte Format a Track command formats an entire track. After the Index Hole is detected, data is written on the disk: Gaps, Address Marks, ID fields and Data fields; all are recorded in either the double-density IBM System 34 format (MF = 1) or the single-density IBM 3740 format (MF = 0). The particular format written is also controlled by the values of Number of Bytes/Sector (N), Sectors/Track (ST), Gap Length (GPL) and Data Pattern (D) which are supplied by the processor during the command phase. The Data field is filled with the data pattern stored in D.

The ID field for each sector is supplied by the processor in response to four data requests per sector issued by the DDFDC. The type of data request depends upon the Non-DMA flag (ND) in the Specify command. In the DMA mode (ND = 0), the DDFDC asserts the DMA Request (DRQ) output four times per sector. In the Non-DMA mode (ND = 1), the DDFDC asserts Interrupt Request (IRQ) output four times per sector.

The processor must write one data byte in response to each request, sending (in the consecutive order) the Track Number (T), Head Number (H), Sector Number (R) and Number of Bytes/Sector (N). This allows the disk to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for T, H, R, and N to the DDFDC for each sector on the track. For sequential formatting R is incremented by one after each sector is formatted, thus, R contains the total numbers of sectors formatted when it is read during the result phase. This incrementing and formatting continues for the whole track until the DDFDC, upon encountering the Index Hole for the second time, terminates the command and sets bits 7 and 6 in ST0 to 0.

If the Fault (FLT) signal is high from the FDD at the end of a write operation, the DDFDC sets the Equipment Check (EC) flag in ST0 to a 1, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command. Also, a low (RDY) signal at the beginning of a command execution phase causes bits 7 and 6 of ST0 to be set to 0 and 1, respectively.

Table 5 shows the relationship between N, ST, and GPL for various disk and sector sizes.

Table 5. Standard Floppy Disk Sector Size Relationship

Disk Size	Mode	Sector Size Bytes/Sector	No. of Data Bytes/Sector (N)	No. of Sectors/Tracks (ST)	Gap Length (GPL) ⁴		Remarks
					Read/Write Command ¹	Format Command ²	
8"	FM	128	00	1A	07	1B	IBM Disk 1
		256	01	0F	0E	2A	IBM Disk 2
		512	02	08	1B	3A	
		1024	03	04	47	8A	
		2048	04	02	C8	FF-	
		4096	05	01	C8	FF	
	MFM ³	256	01	1A	0E	36	IBM Disk 2D
		512	02	0F	1B	54	
		1024	03	08	35	74	IBM Disk 2D
		2048	04	04	99	FF	
		4096	05	02	C8	FF	
		8192	06	01	C8	FF	
5¼"	FM	128	00	12	07	09	
		128	00	10	10	19	
		256	01	08	18	30	
		512	02	04	46	87	
		1024	03	02	C8	FF	
		2048	04	01	C8	FF	
	MFM ³	256	01	12	0A	0C	
		256	01	10	20	32	
		512	02	08	2A	50	
		1024	03	04	80	F0	
		2048	04	02	C8	FF	
		4096	05	01	C8	FF	

Notes:

1. Suggested values of GPL in Read or Write commands to avoid overlapping between Data field and ID field of contiguous sections.
2. Suggested values of GPL in Format a Track command.
3. In MFM mode the DDFDC cannot perform a read/write/format operation with 128 bytes/sector (N = 00).
4. Values of ST and GPL are in hexadecimal.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	1	0	1
	2	X	X	X	X	X	HD	US ¹	US ⁰
	3	Number of Bytes per Sector (N)							
	4	Sectors per Track (ST)							
	5	Gap Length (GPL)							
	6	Data Pattern (D)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)*
	5	Head Number (H)*
	6	Sector Number (R)*
	7	Number of Data Bytes per Sector (N)*

* The ID information has no meaning in this command.

SCAN COMMANDS

The scan commands compare data read from the disk to data supplied from the data bus. The DDFDC compares the data, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{BUS}$, $D_{FDD} \leq D_{BUS}$, or $D_{FDD} \geq D_{BUS}$ (D = the data pattern in hexadecimal). A magnitude comparison is performed (FF = largest number, 00 = smallest number). The hexadecimal byte of FF either from the bus or from FDD can be used as a mask byte because it always meets the condition of the compare. After a whole sector of data is compared, if the conditions are not met, the sector number is incremented ($R + STP - R$), and the scan operation is continued. The scan operation continues until one of the following events occur: the conditions for scan are met (equal, low or equal, or high or equal), the last sector on the track is reached (EOT), or DONE is received.

If conditions for scan are met, the DDFDC sets the Scan Hit (SH) flag in ST2 to a 1, and terminates the command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the track (EOT), then the DDFDC sets the Scan Not Satisfied (SN) flag in ST2 to a 1, and terminates the command. The receipt of DONE from the processor or DMA controller during the scan operation will cause the DDFDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6 shows the status of bits SH and SN under various conditions of scan.

Table 6. Scan Status Codes

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	D _{FDD} = D _{BUS}
	1	0	D _{FDD} ≠ D _{BUS}
Scan Low or Equal	0	1	D _{FDD} = D _{BUS}
	0	0	D _{FDD} < D _{BUS}
	1	0	D _{FDD} > D _{BUS}
Scan High or Equal	0	1	D _{FDD} = D _{BUS}
	0	0	D _{FDD} > D _{BUS}
	1	0	D _{FDD} < D _{BUS}

If SK = 0 and the DDFDC encounters a Deleted Data Address Mark on one of the sectors, it regards that sector as the last sector of the track, sets the Control Mark (CM) bit in ST2 to a 1 and terminates the command. If SK = 1, the DDFDC skips the sector with the Deleted Data Address Mark, sets the CM flag to a 1 in order to show that a Deleted Sector has been encountered, and reads the next sector.

When either the STP sectors are read (contiguous sectors = 01, or alternate sectors = 02) or MT (Multi-Track) is set, the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and the scan command starts reading at sector 21. Sectors 21, 23, and 25 are read, then the next sector (26) is skipped and the Index Hole is encountered before the EOT value of 26 can be read. This results in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the scan command would be completed in a normal manner.

During a scan command data is supplied from the data bus for comparison against the data read from the disk. In order to avoid having the Over Run (OR) flag set in ST1, data must be available from the data bus in less than 27 μs (FM mode) or 13 μs (MFM mode). If an OR occurs, the DDFDC terminates the command and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

The following tables specify the command bytes and describe the result bytes for the three scan commands.

SCAN EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	0	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN LOW OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN HIGH OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SEEK

The three-byte Seek command steps the FDD read/write head from track to track. The DDFDC has two independent Present Track Registers for each drive. They are cleared only by the Recalibrate command. The DDFDC compares the Present Track Number (PTN) which is the current head position with the New Track Number (NTN), and if there is a difference, performs the following operation:

If PTN < NTN: Sets the direction output (LCT/DIR) high and issues step pulses (FR/STP) to the FDD to cause the read/write head to step in.

If PTN > NTN: Sets the direction output (LCT/DIR) low and issues step pulses to the FDD to cause the read/write head to step out.

The rate at which step pulses are issued is controlled by the Step Rate Time (SRT) in the Specify command. After each step pulse is issued, NTN is compared against PTN. When NTN = PTN, then the Seek End (SE) flag in ST0 is set to a 1, bits 7 and 6 in ST0 are set to 0, and the command is terminated. At this point DDFDC asserts IRQ.

The FDD Busy flag (bit 0-3) in the Main Status Register (MSR) corresponding to the FDD performing the Seek operation is set to a 1.

After command termination, all FDD Busy bits set are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the DDFDC sets the Controller Busy (CB) flag in the MSR to 1; but during the execution phase the CB flag is set to 0 to indicate DDFDC non-busy. While the DDFDC is in the non-busy state, another Seek command may be issued, and in this manner parallel seek operations may be performed on all drives at once.

No command other than Seek will be accepted while the DDFDC is sending step pulses to any FDD. If a different command type is attempted, the DDFDC will set bits 7 and 6 in ST0 to a 1 and 0, respectively, to indicate an invalid command.

If the FDD is in a not ready state at the beginning of the command execution phase or during the seek operation, then the DDFDC sets the Not Ready (NR) flag in ST0 to a 1, sets ST0 bits 7 and 6 to 0 and 1, respectively, and terminates the command.

If the time to write the three bytes of the Seek command exceeds 150 μ s, the time between the first two step pulses may be shorter than the Step Rate Time (SRT) defined by the Specify command by as much as 1 ms.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	1	1	1
	2	X	X	X	X	X	0	US1	US0
	3	New Track Number (NTN)							

Result Phase: None.

RECALIBRATE

This two-byte command retracts the FDD read/write head to the Track 0 position. The DDFDC clears the contents of the PTN counters, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal (TRK0) is low, the direction signal (LCT/DIR) output remains low and step pulses are issued on FR/STP. When TRK0 goes high the DDFDC sets the Seek End (SE) flag in ST0 to a 1 and terminates the command. If the TRK0 is still low after 256 step pulses have been issued, the DDFDC sets Seek End (SE) and Equipment Check (EC) flags in ST0 to 1s, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the RDY signal, as described in the Seek command, also applies to the Recalibrate command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	1	1
	2	X	X	X	X	X	0	US1	US0

Result Phase: None.

SENSE INTERRUPT STATUS

Interrupt request (\overline{IRQ}) is asserted by the DDFDC when any of the following conditions occur:

- Upon entering the result phase of:
 - Read Data command
 - Read a Track command
 - Read ID command
 - Read Deleted Data command
 - Write Data command
 - Format a Track command
 - Write Deleted Data command
 - Scan commands
- Ready (RDY) line from the FDD changes state
- Seek or Recalibrate command termination
- During execution phase in the Non-DMA mode

\overline{IRQ} caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in Non-DMA mode, bit 5 in the MSR is set to 1. Upon entering result phase this bit is set to 0. Reasons 1 and 4 do not require the Sense Interrupt Status command. The interrupt is cleared by reading or writing data to DDFDC. Interrupts caused by reasons 2 and 3 are identified with the aid of the Sense Interrupt Status command. This command resets \overline{IRQ} and sets/resets bits 5, 6, and 7 of ST0 to identify the cause of the interrupt. Table 7 defines the seek and interrupt codes.

Neither the Seek or Recalibrate command has a result phase. Therefore, it is mandatory to use the Sense Interrupt Status command after these commands to effectively terminate them and to verify where the head is positioned by checking the Present Track Number (PTN).

Issuing a Sense Interrupt Status command without an interrupt pending is treated as an invalid command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	0	0	0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Present Track Number (PTN)

SPECIFY

The three-byte Specify command sets the initial values for each of the three internal timers. The Head Unload Time (HUT) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (1 = 16 ms, 2 = 32 ms, ... F = 240 ms).

The Step Rate Time (SRT) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, ... 0 = 16 ms).

The Head Load Time (HLT) defines the time between the Head Load (HDL) signal going high and the start of the read/write operation. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms, ... 7F = 254 ms).

The time intervals are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock. If the clock is reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of two.

The choice of DMA or Non-DMA operation is made by the Non-DMA mode (ND) bit. When this bit = 1 the Non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	0	1	1
	2	SRT				HUT			
	3	HLT							ND

SRT — Step Rate Time
HUT — Head Unload Time
HLT — Head Load Time
ND — Non-DMA mode

Result Phase: None.

SENSE DRIVE STATUS

This two-byte command obtains and reports the status of the FDDs. Status Register 3 (ST3) is returned in the result phase and contains the drive status.

Table 7. ST0 Seek and Interrupt Code Definition for Sense Interrupt Status

Status Register 0 (ST0) Bits			
Interrupt Code (IC)		Seek End (SE)	Cause
7	6	5	
1	1	0	
0	0	1	
0	1	1	

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	0	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 3 (ST3)
---	---	-------------------------

INVALID COMMAND

If an invalid command (i.e., a command not previously defined) is received by the DDFDC, then the DDFDC terminates the command after setting bits 7 and 6 of ST0 to 1 and 0, respectively. The DDFDC does not generate an interrupt during this condition. Bits 6 and 7 (DIO and RQM) in the MSR are both set to a 1 indicating to the processor that the DDFDC is in the result phase and that ST0 must be read. A hex 80 in ST0 indicates an invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt, otherwise the DDFDC considers the next command to be an invalid command.

In some applications the user may wish to use this command as a No-Op command, to place the DDFDC in a standby or no operation state.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	Invalid Codes							

Result Phase:

R	1	Status Register 0 (ST0) = 80
---	---	------------------------------

PROCESSOR INTERFACE

During the command or result phases, the Main Status Register (MSR) must be read by the processor before each byte of information is transferred to, or from, the DDFDC Data Register. After each byte of data is written to, or read from, the Data Register, the processor should wait 12 μ s before reading the MSR. Bits 6 and 7 in the MSR must be a 0 and 1, respectively, before each command byte can be written to the DDFDC. During the result phase, bits 6 and 7 of the MSR must both be 1s prior to reading each byte from the Data Register onto the data bus. Note that this status reading of bits 6 and 7 of the MSR before each byte transfer to and from the DDFDC is required in only the command and result phases and not during the execution phase.

During the result phase all bytes shown in the result phase must be read by the processor. The Read Data command, for example, has seven bytes of data in the result phase. All seven

bytes must be read to successfully complete the Read Data command. The DDFDC will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

INTERRUPT REQUEST MODE

During the execution phase, the MSR need not be read. The receipt of each data byte from the FDD is indicated by $\overline{\text{IRQ}}$ low on pin 18. When the DDFDC is in Non-DMA mode, $\overline{\text{IRQ}}$ is asserted during the execution phase. When the DDFDC is in the DMA mode, $\overline{\text{IRQ}}$ is asserted at the result phase. The $\overline{\text{IRQ}}$ signal is reset by a read (R/W high) or write (R/W low) of data to the DDFDC. A further explanation of the $\overline{\text{IRQ}}$ signal is described in the Sense Interrupt Status command on page 16. If the system cannot handle interrupts fast enough (within 13 μ s for MFM mode or 27 μ s for FM mode), it should poll bit 7 (RQM) in the MSR. In this case, RQM in the MSR functions as an Interrupt Request ($\overline{\text{IRQ}}$). If the RQM bit is not set, the Over Run (OR) flag in ST1 will be set to a 1 and bits 7 and 6 of ST0 will be set to a 0 and 1, respectively.

DMA MODE

When the DDFDC is in the DMA mode (ND = 0 in the third command byte of the Specify command), DRQ (DMA Request) is asserted during the execution phase (rather than $\overline{\text{IRQ}}$) to request the transfer of a data byte between the data bus and the DDFDC.

During a read command, the DDFDC asserts $\overline{\text{REQ}}$ as each byte of data is available to be read. The DMA controller responds to this request with both $\overline{\text{DACK}}$ low (DMA Acknowledge) and R/W high (read). When $\overline{\text{DACK}}$ goes low the DMA Request is reset ($\overline{\text{REQ}}$ high). After the execution phase has been completed ($\overline{\text{DONE}}$ low or the EOT sector is read), $\overline{\text{IRQ}}$ is asserted to indicate the beginning of the result phase. When the first byte of data is read during the result phase, $\overline{\text{IRQ}}$ is reset high.

During a write command, the DDFDC asserts $\overline{\text{REQ}}$ as each byte of data is required. The DMA controller responds to this request with $\overline{\text{DACK}}$ low (DMA Acknowledge) and R/W low (write). When $\overline{\text{DACK}}$ goes low the DMA Request is reset ($\overline{\text{REQ}}$ high). After the execution phase has been completed ($\overline{\text{DONE}}$ low or the EOT sector is written), $\overline{\text{IRQ}}$ is asserted. This signals the beginning of the result phase. When the first byte of data is read during the result phase, the $\overline{\text{IRQ}}$ is reset high.

FDD POLLING

After the Specify command has been received by the DDFDC, the Unit Select lines (US0 and US1) begin the polling mode. Between commands (and between step pulses in the Seek Command) the DDFDC polls all the FDD's looking for a change in the RDY line from any of the drives. If the RDY line changes state (usually due to the door opening or closing) then the DDFDC asserts $\overline{\text{IRQ}}$. When Status Register 0 (ST0) is read (after Sense Interrupt Status command is issued), Not Ready (NR = 1) will be indicated. The polling of the RDY line by the DDFDC occurs continuously between commands, thus notifying the processor which drives are on- or off-line. Each drive is polled every 1.024 ms except during read/write commands.

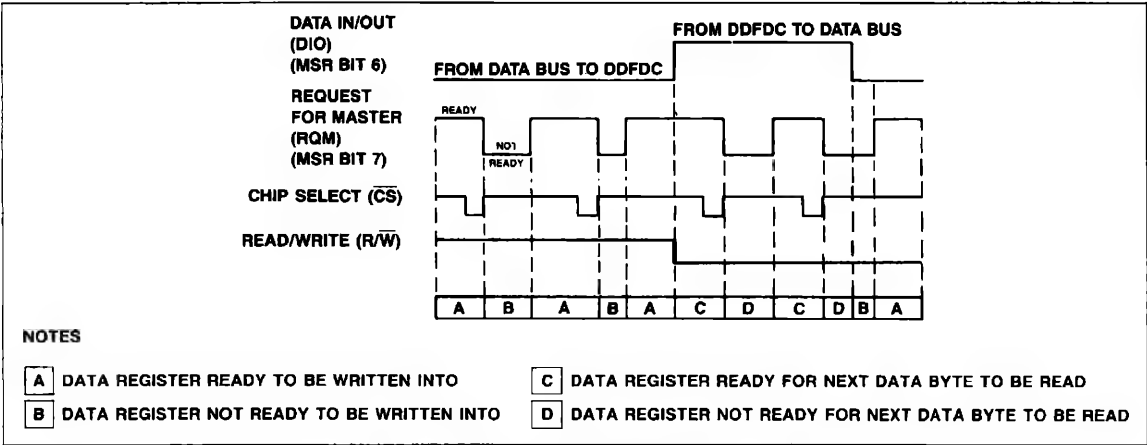


Figure 3. DDFDC and System Data Transfer Timing

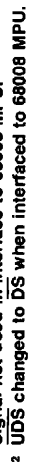


Figure 4. R68465 DDFDC Interface to R68000

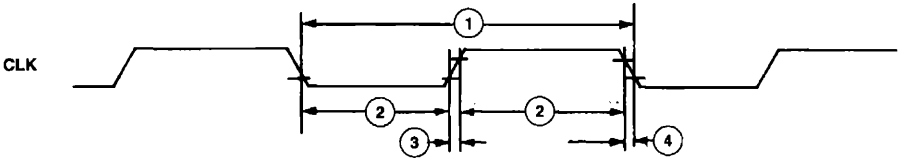


Figure 5. Clock Timing

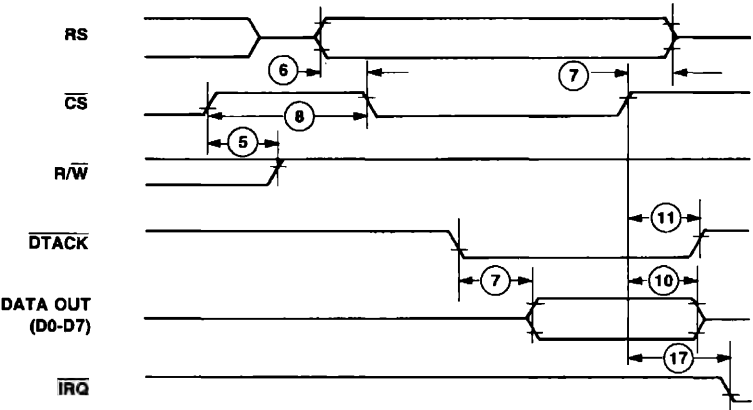


Figure 6. DDFDC Read Cycle Timing

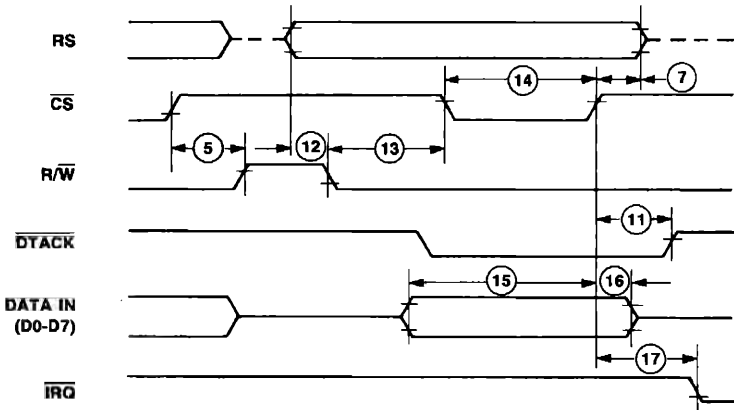


Figure 7. DDFDC Write Cycle Timing

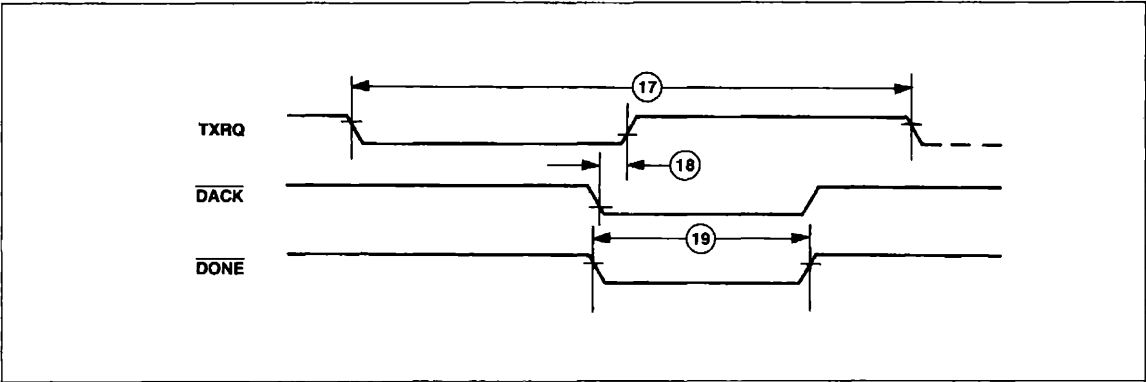


Figure 8. DMA Operation Timing

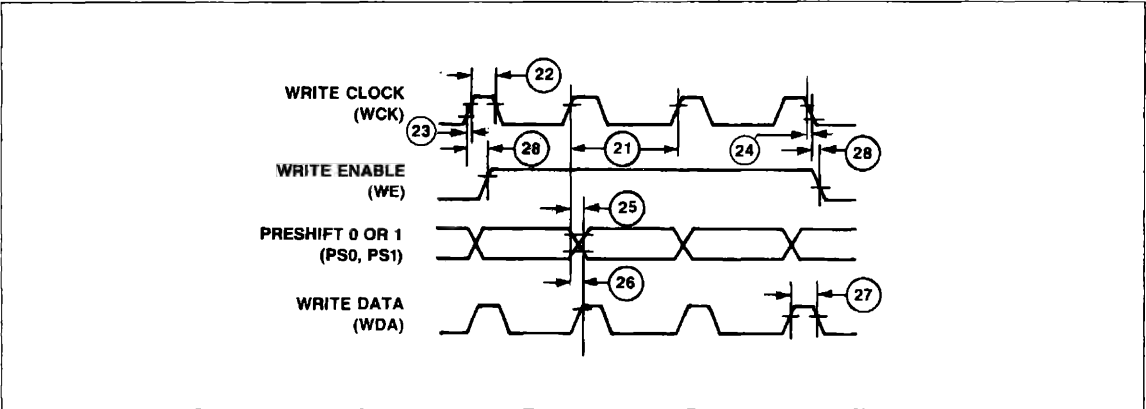


Figure 9. FDD Write Operation Timing

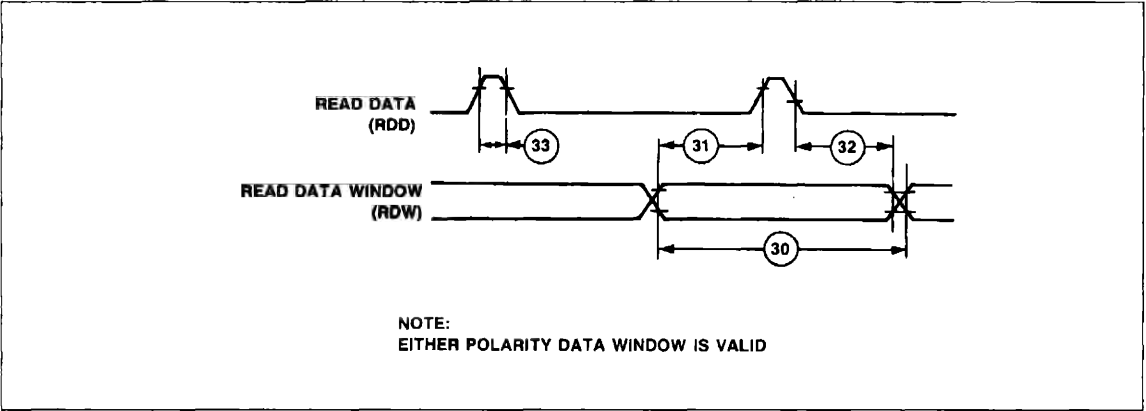


Figure 10. FDD Read Operation Timing

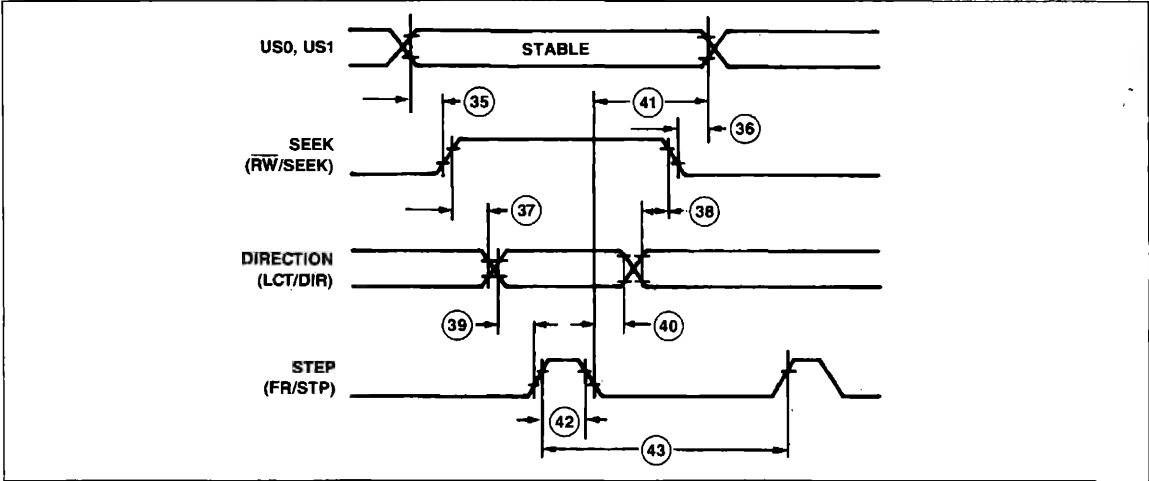


Figure 11. Seek Operation Timing

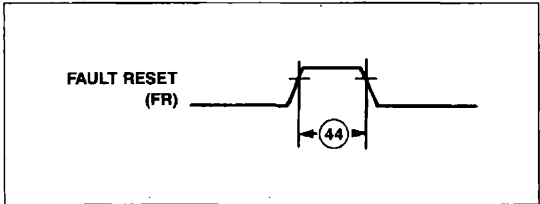


Figure 12. Fault Reset Timing

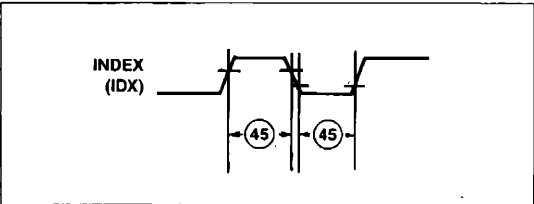


Figure 13. Index Timing

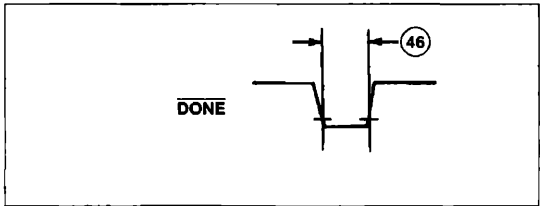


Figure 14. Terminal Count Timing

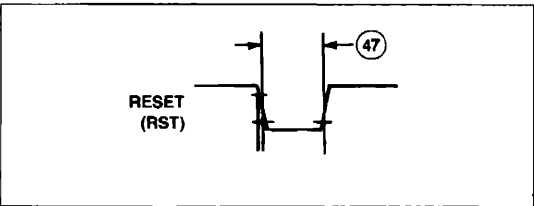


Figure 15. Reset Timing

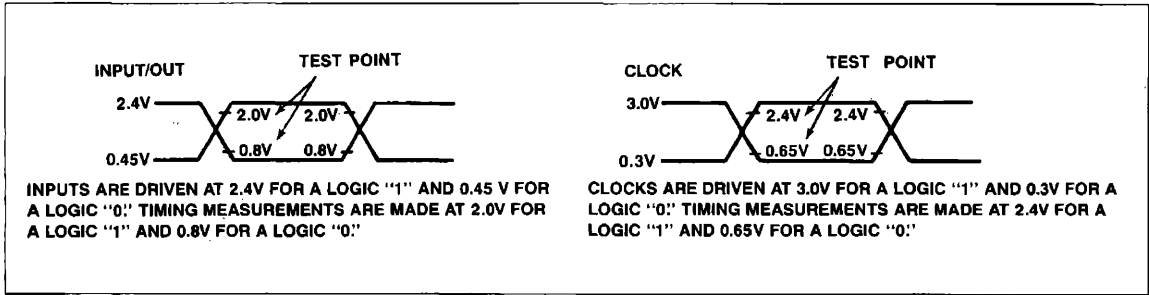


Figure 16. AC Timing Measurement Conditions

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Ref. Fig.	No.	Characteristic	Symbol	Alt. Sym.	Min.	Typ.	Max.	Unit	Test Conditions
5	1	Clock Period	t _{CY}	φ _{CY}	120	125	500	ns	CLK = 8 MHz
	2	Clock High, Low Width	t _{CA}	φ ₀	40	62.5	—	ns	
	3	Clock Rise Time	t _{CLCH}	φ _r	—	—	20	ns	
	4	Clock Fall Time	t _{CHCL}	φ _f	—	—	20	ns	
6 and 7	5	CS High to R/W High	t _{SHRH}	t _{SR}	40	—	—	ns	C _L = 100 pF
	6	Address Valid to CS Low	t _{AVSL}	t _{RA}	0	—	—	ns	
	7	CS High to Address Invalid	t _{SHAX}	t _{AH}	0	—	—	ns	
	8	CS High	t _{SHSL}	t _{SH}	150	—	—	ns	
	9	DTACK Low to Data Valid	t _{DLDV}	t _{RD}	—	—	90	ns	
	10	CS High to Output High Z	t _{SHDZ}	t _{DF}	20	—	—	ns	
	11	CS High to DTACK High	t _{SHDH}	t _{DTK}	—	—	120	ns	
	12	Address Valid to CS Low	t _{AVRL}	t _{WS}	20	—	—	ns	
	13	R/W Low to CS Low	t _{RLSL}	t _{WH}	80	—	—	ns	
	14	CS Low Pulse Width	t _{LSLH}	t _{SL}	250	—	—	ns	
	15	Data Valid to CS High	t _{DVSH}	t _{DSU}	150	—	—	ns	
	16	CS High to Data Invalid	t _{SHDZ}	t _{DHW}	5	—	—	ns	
8	17	IRQ Delay from CS High	t _{ILSH}	t _{IRQ}	—	—	500	μs	CLK = 8 MHz
	18	TXRQ Cycle Period	t _{TCY}	t _{TCY}	13	—	—	ns	
	19	ACK Low to TXRQ Low	t _{AKTH}	t _{ACK}	—	—	200	t _{CY}	
	20	DONE Low Width	t _{NLNL}	t _{DONE}	1	—	—	ns	
9	21	WCK Cycle Time	t _{KCY}	t _{CY}	—	note 1	—	μs	
	22	WCK High Width	t _{KHKL}	t ₀	80	250	350	ns	
	23	WCK Rise Time	t _{KLKH}	t _r	—	—	20	ns	
	24	WCK Fall Time	t _{KHKL}	t _f	—	—	20	ns	
	25	WCK High to PS0, PS1 Valid (Delay)	t _{KHPV}	t _{CP}	20	—	100	ns	
	26	PS0, PS1 Valid to WDA High (Delay)	t _{PVDH}	t _{CD}	20	—	100	ns	
	27	WDA High Width	t _{WDHL}	t _{WDD}	t _{WCH} - 50	—	—	ns	
	28	WE High to WCK High or WE Low to WCK Low	t _{EHKH}	t _{WE}	20	—	100	ns	
10	30	RDW Cycle Time	t _{WCY}	t _{WCY}	—	note 2	—	μs	
	31	RDW Valid to RDD High (Setup)	t _{WVRH}	t _{WRD}	15	—	—	ns	
	32	RDD Low to RDW Invalid (Hold)	t _{RLWI}	t _{RDW}	15	—	—	ns	
	33	RDD High Width	t _{RHRL}	t _{RDD}	40	—	—	ns	
11	35	US0, US1 Valid to SEEK High (Setup)	t _{UVSH}	t _{US}	12	—	—	μs	CLK = 8 MHz
	36	SEEK Low to US0, US1 Invalid (Hold)	t _{SLUI}	t _{SU}	15	—	—	μs	
	37	SEEK High to DIR Valid (Setup)	t _{SHDV}	t _{SD}	7	—	—	μs	
	38	DIR Invalid to SEEK Low (Hold)	t _{DSXL}	t _{DS}	30	—	—	μs	
	39	DIR Valid to STP High (Setup)	t _{DVTH}	t _{DST}	1	—	—	μs	
	40	STP Low to DIR Invalid (Hold)	t _{TLDX}	t _{STD}	24	—	—	μs	
	41	STP Low to US0, US1 Invalid (Hold)	t _{TLUX}	t _{STU}	5	—	—	μs	
	42	STP High Width	t _{THTL}	t _{STP}	6	7	—	μs	
12	44	FR High Width	t _{FHFL}	t _{FR}	8	—	10	μs	
13	45	IDX High Width	t _{IHIL}	t _{IDX}	10	—	—	t _{CY}	
14	46	DONE Low Width	t _{THTL}	t _{TC}	1	—	—	t _{CY}	
15	47	RESET Low Width	t _{RHRL}	t _{RST}	14	—	—	t _{CY}	

Notes:

1.	MFM	Mini	Standard
	0	4 μs	2 μs
	1	2 μs	1 μs

2. For MFM = 0: Typ. = 2 μs

For MFM = 1: Typ. = 1 μs

3. t_{SC} = 33 μs min. is for different drive units. In the case of the same unit, t_{SC} can be ranged from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Output Voltage	V_{OUT}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Range
V_{CC} Power Supply	5.0V \pm 5%
Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

($V_{CC} = 5.0$ Vdc \pm 5%, $V_{SS} = 0$ Vdc, $T_A = 0^\circ\text{C}$ to 70°C , unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Low Voltage Logic CLK and WCK	V_{IL}	-0.5 -0.5	0.8 0.65	V	
Input High Voltage Logic CLK and WCK	V_{IH}	2.0 2.4	$V_{CC} + 0.5$ $V_{CC} + 0.5$	V	
Output Low Voltage	V_{OL}		0.45	V	$V_{CC} = 4.75\text{V}$, $I_{OL} = 2.0$ mA
Output High Voltage	V_{OH}	2.4	V_{CC}	V	$V_{CC} = 4.75\text{V}$, $I_{OH} = -200$ μA
V_{CC} Supply Current	I_{CC}		150	mA	$V_{CC} = 4.75\text{V}$
Input Load Current All Inputs	I_{IL}		10	μA	$V_{IN} = V_{CC}$
			-10	μA	$V_{IN} = 0\text{V}$
High Level Output Leakage Current	I_{LOH}		10	μA	$V_{CC} = 0\text{V}$ to 5.25V, $V_{SS} = 0\text{V}$ $V_{OUT} = V_{CC}$
Low Level Output Leakage Current	I_{LOL}		-10	μA	$V_{CC} = 0\text{V}$ to 5.25V, $V_{SS} = 0\text{V}$ $V_{OUT} = +0.45\text{V}$
Internal Power Dissipation	P_{INT}	—	1.0	W	$T_A = 25^\circ\text{C}$

CAPACITANCE

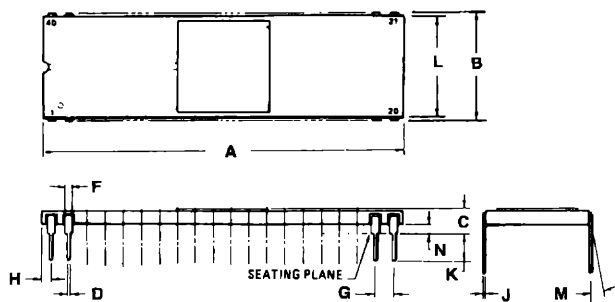
($T_A = 25^\circ\text{C}$; $f_c = 1$ MHz; $V_{CC} = 0\text{V}$)

Parameter	Symbol	Max Limit	Unit
Clock Input	$C_{IN(0)}$	20	pF
Input	C_{IN}	10	pF
Output	C_{OUT}	20	pF

Note: All pins except pin under test tied to ground.

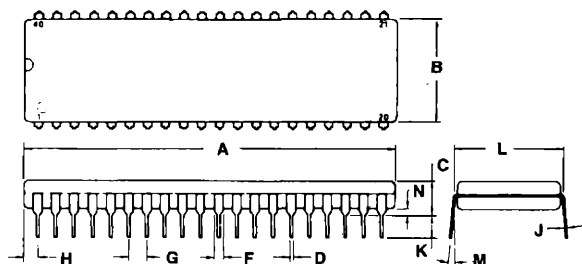
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	-0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040



R68560, R68561 MULTI-PROTOCOL COMMUNICATIONS CONTROLLER (MPCC)

1

PRELIMINARY

DESCRIPTION

The R68560, R68561 Multi-Protocol Communications Controller (MPCC) interfaces a single serial communications channel to a 68008/68000 microcomputer-based system using either asynchronous or synchronous protocol. High speed bit rate, automatic formatting, low overhead programming, eight character buffering, two channel DMA interface and three separate interrupt vector numbers optimize MPCC performance to take full advantage of the 68008/68000 processing capabilities and asynchronous bus structure.

In synchronous operation, the MPCC supports bit-oriented protocols (BOP), such as SDLC/HDLC, and character-oriented protocols (COP), such as IBM Bisync (BSC) in either ASCII or EBCDIC coding. Formatting, synchronizing, validation and error detection is performed automatically in accordance with protocol requirements and selected options. Asynchronous (ASYN) and isochronous (ISOC) modes are also supported. In addition, modem interface handshake signals are available for general use.

Control, status and data are transferred between the MPCC and the microcomputer bus via 22 directly addressable registers and a DMA interface. Two first-in first-out (FIFO) registers, addressable through separate receiver and transmitter data registers, each buffer up to eight characters at a time to allow more MPU processing time to service data received or to be transmitted and to maximize bus throughput, especially during DMA operation. The two-channel Direct Memory Access (DMA) interface operates with the MC68440/MC68450 DMA Controllers. Three prioritized interrupt vector numbers separately support receiver, transmitter and modem interface operation.

An on-chip oscillator drives the internal baud rate generator (BRG) and an external clock output with an 8 MHz input crystal or clock frequency. The BRG, in conjunction with two selectable prescalers and 16-bit programmable divisor, provides a data bit rate of DC to 4 MHz.

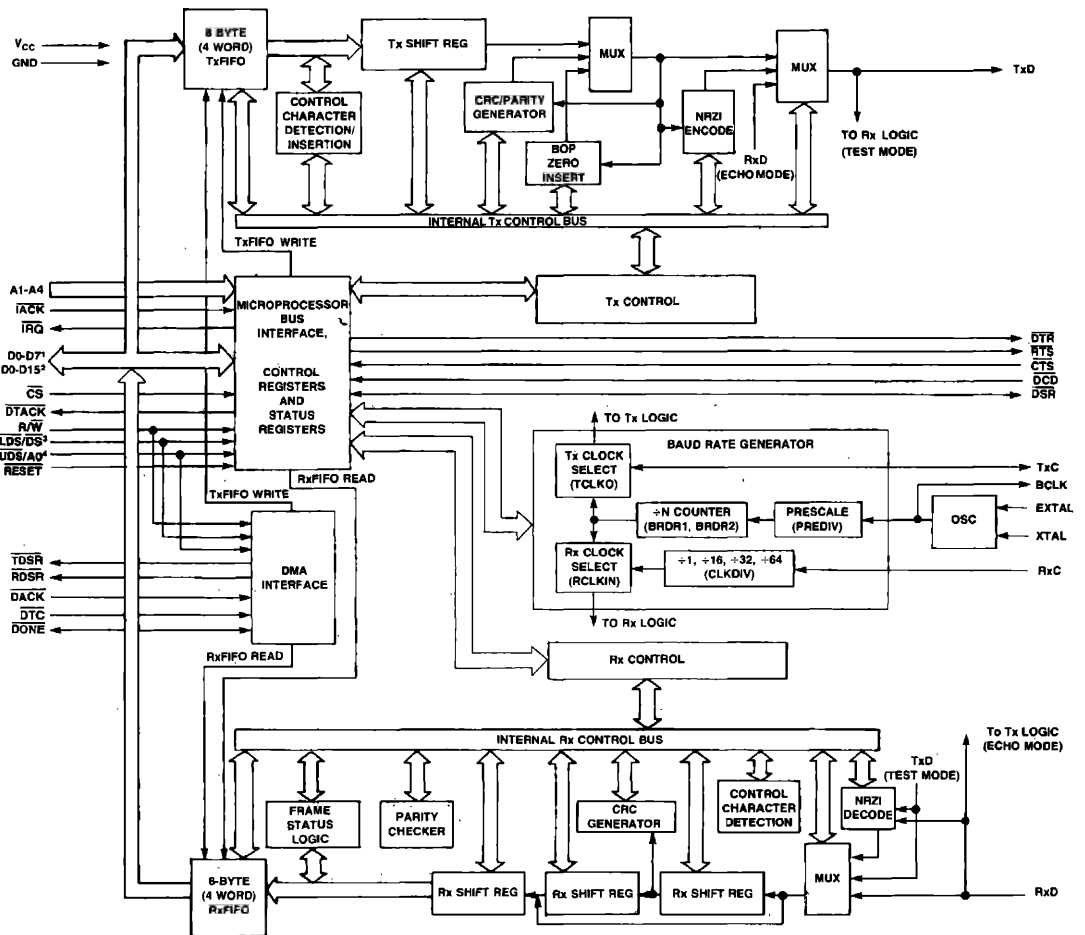
The 48-pin R68561 supports word-length (16-bit) operation when connected to the 68000 16-bit asynchronous bus, as well as byte-length (8-bit) operation when connected to the 68008 8-bit bus. The 40-pin R68560 supports byte-length operation on the 68008 bus.

FEATURES

- Full duplex synchronous/asynchronous receiver and transmitter
- Fully implements IBM Binary Synchronous Communications (BSC) in two coding formats: ASCII and EBCDIC
- Supports other synchronous character-oriented protocols (COP), such as six-bit BSC, X3.28, ISO IS1745, ECMA-16, etc.
- Supports synchronous bit-oriented protocols (BOP), such as SDLC, HDLC, X.25, etc.
- Asynchronous and isochronous modes
- Modem handshake interface
- High speed serial data rate (DC to 4 MHz)
- Internal oscillator and Baud Rate Generator (BRG) with programmable data rate
- Crystal or TTL level clock input and buffered clock output (8 MHz)
- Direct interface to 68008/68000 asynchronous bus
- Eight-character receiver and transmitter buffer registers
- 22 directly addressable registers for flexible option selection, complete status reporting, and data transfer
- Three separate programmable interrupt vector numbers for receiver, transmitter and serial interface
- Maskable interrupt conditions for receiver, transmitter and serial interface
- Programmable microprocessor bus data transfer: polled, interrupt and two-channel DMA transfer compatible with MC68440/MC68450
- Clock control register for receiver clock divisor and receiver and transmitter clock routing
- Selectable full/half duplex, autoecho and local loop-back modes
- Selectable parity (enable, odd, even) and CRC (control field enable, CRC-16, CCITT V.41, VRC/LRC)

ORDERING INFORMATION

Part Number	Frequency	Temperature Range
R6856	4 MHz	0°C to 70°C
Package: C = Ceramic P = Plastic		
Number of pins: 0 = 40 1 = 48		



NOTES:

1. R68560 ONLY.
2. R68561 ONLY.
3. UDS ON R68561 A0 ON R68560
4. LDS ON R68561 DS ON R68560

Figure 1. MPCC Block Diagram

PIN DESCRIPTION

Throughout the document, signals are presented using the terms active and inactive or asserted and negated independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar. R/W indicates a write is active low and a read active high.

Note: The R68561 interface is described for word mode operation only and the R68560 interface is described for byte mode operation only.

A1 – A4—Address Lines. A1 – A4 are active high inputs used in conjunction with the CS input to access the internal registers. The address map for these registers is shown in Table 1.

D0 – D15—Data Lines. The bidirectional data lines transfer data between the MPCC and the MPU, memory or other peripheral device. D0 – D15 are used when connected to the 16-bit 68000 bus and operating in the MPCC word mode. D0 – D7 are used when connected to the 16-bit 68000 bus or the 8-bit 68008 bus and operating in the MPCC byte mode. The data bus is three-stated when CS is inactive. (See exceptions in DMA mode.)

CS—Chip Select. CS low selects the MPCC for programmed transfers with the host. The MPCC is deselected when the CS input is inactive in non-DMA mode. CS must be decoded from the address bus and gated with address strobe (AS).

R/W—Read/Write. R/W controls the direction of data flow through the bidirectional data bus by indicating that the current bus cycle is a read (high) or write (low) cycle.

DTACK—Data Transfer Acknowledge. DTACK is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, DTACK is asserted by the MPCC after data has been provided on the data bus; during

write cycles it is asserted after data has been accepted at the data bus. DTACK is driven high after assertion prior to being tri-stated. A holding resistor is required to maintain DTACK high between bus cycles.

DS—Data Strobe (R68560). During a write (R/W low), the DS positive transition latches data on data bus lines D0 – D7 into the MPCC. During a read (R/W high), DS low enables data from the MPCC to data bus lines D0 – D7.

LDS—Lower Data Strobe (R68561). During a write (R/W low), the positive transition latches data on the data bus lines D0 – D7 (and on D8 – D15 if UDS is low) into the MPCC. During a read (R/W high), LDS low enables data from the MPCC to D0 – D7 (and to D8 – D15 if UDS is low).

A0—Address Line A0 (R68560). When interfacing to an 8-bit data bus system such as the 68008, address line A0 is used to access an internal register. A0 = 0 defines an even register and A0 = 1 defines an odd register. See Table 1b.

UDS—Upper Data Strobe (R68561). When interfacing to a 16-bit data bus system such as the 68000, a low on control bus signal UDS enables access to the upper data byte on D8 – D15. A high on UDS disables access to D8 – D15. Data is latched and enabled in conjunction with LDS.

IRQ—Interrupt Request. The active low IRQ output requests interrupt service by the MPU. IRQ is driven high after assertion prior to being tri-stated.

IACK—Interrupt Acknowledge. The active low IACK input indicates that the current bus cycle is an interrupt acknowledge cycle. When IACK is asserted the MPCC places an interrupt vector on the lower byte (D0 – D7) of the data bus.

TDSR—Transmitter Data Service Request. When Transmitter DMA mode is active, the low TDSR output requests DMA service.

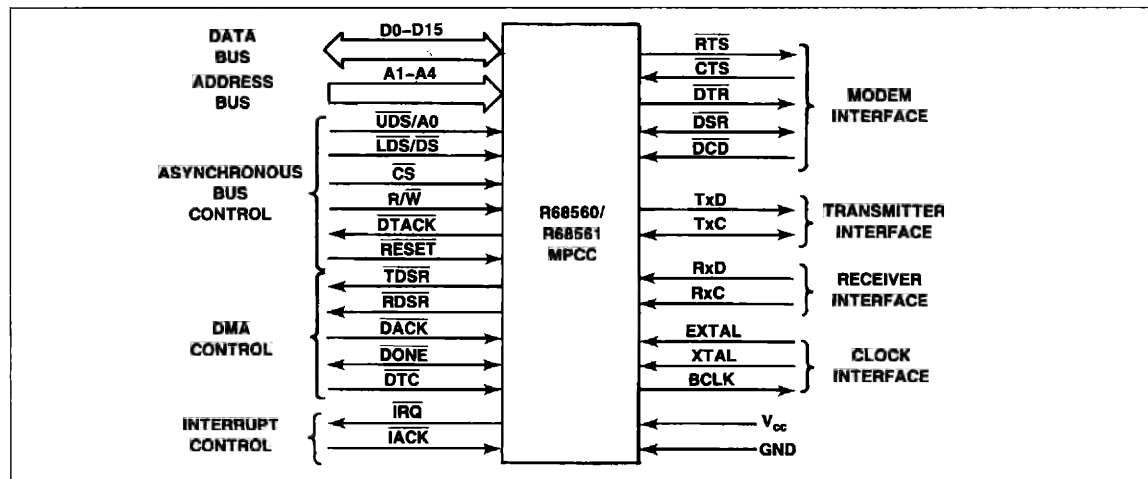


Figure 2. MPCC Input and Output Signals

RDSR—Receiver Data Service Request. When receiver DMA mode is active, the low $\overline{\text{RDSR}}$ output requests DMA service.

DACK—DMA Acknowledge. The $\overline{\text{DACK}}$ low input indicates that the data bus has been acquired by the DMAC and that the requested bus cycle is beginning.

DTC—Data Transfer Complete. The $\overline{\text{DTC}}$ low input indicates that a DMA data transfer is complete. $\overline{\text{DTC}}$ in response to a $\overline{\text{RDSR}}$ indicates that the data has been successfully stored in memory. $\overline{\text{DTC}}$ in response to a $\overline{\text{TDSR}}$ indicates that the data is present on the data bus for strobing into the MPCC. $\overline{\text{DTC}}$ is used in conjunction with R/W to increment the Tx FIFO or Rx FIFO pointer.

DONE—Done. $\overline{\text{DONE}}$ is a bidirectional active low signal. The $\overline{\text{DONE}}$ signal is asserted by the DMAC when the DMA transfer count is exhausted and there is no more data to be transferred, or asserted by the MPCC when the status byte following the last character of a frame (block) is being transferred in response to a $\overline{\text{RDSR}}$. The $\overline{\text{DONE}}$ signal asserted by the DMAC in response to a $\overline{\text{TDSR}}$ will be stored to track with the data byte (lower byte for word transfer) through the Tx FIFO.

RESET—Reset. $\overline{\text{RESET}}$ is an active low, high impedance input that initializes all MPCC functions. $\overline{\text{RESET}}$ must be asserted for at least 500 ns to initialize the MPCC.

DTR—Data Terminal Ready. The $\overline{\text{DTR}}$ active low output is general purpose in nature, and is controlled by the DTRLVL bit in the Serial Interface Control Register (SICR).

RTS—Request to Send. The $\overline{\text{RTS}}$ active low output is general purpose in nature, and is controlled by the RTSLVL bit in the SICR.

CTS—Clear to Send. The $\overline{\text{CTS}}$ active low input positive transition and level are reported in the CTST and CTSLVL bits in the Serial Interface Status Register (SISR), respectively.

DSR—Data Set Ready. The $\overline{\text{DSR}}$ active low input negative transition and level are reported in the DSRT and DSRLVL bits in the SISR, respectively. $\overline{\text{DSR}}$ is also an output for RSYN.

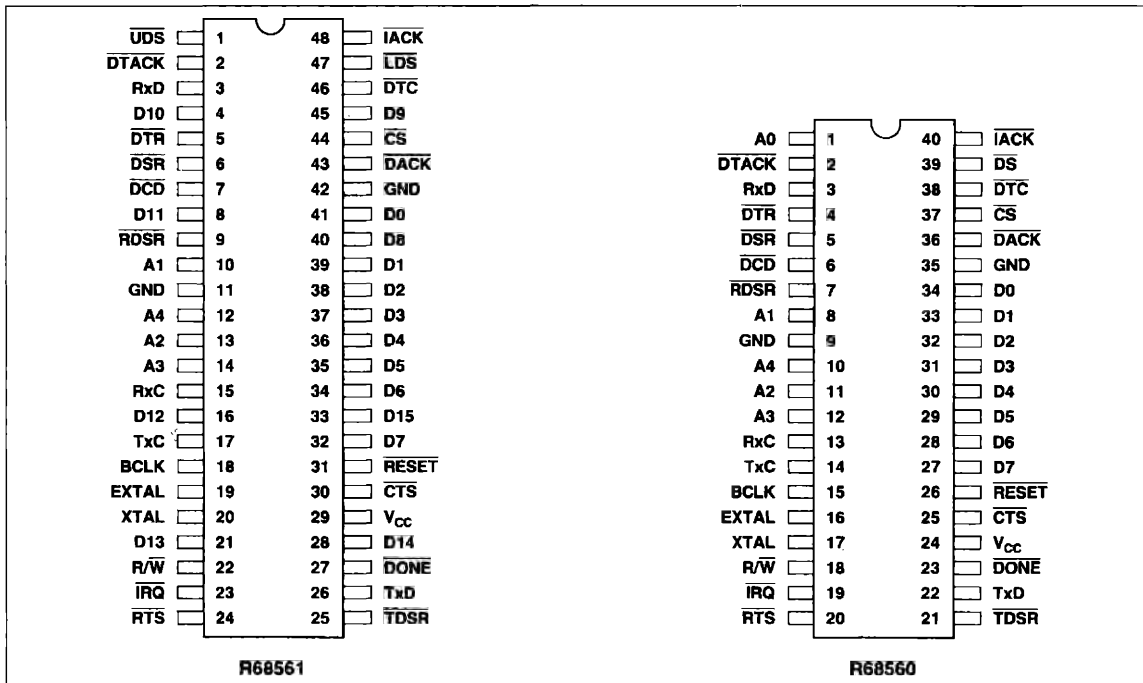
DCD—Data Carrier Detect. The $\overline{\text{DCD}}$ active low input positive transition and level are reported in the DCDT and DCDLVL bits in the SISR, respectively.

TxD—Transmitted Data. The MPCC transmits serial data on the TxD output. The TxD output changes on the negative going edge of Tx C.

RxD—Received Data. The MPCC receives serial data on the RxD input. The RxD input is shifted into the receiver with the negative going edge of Rx C.

TxC—Transmitter Clock. Tx C can be programmed to be an input or an output. When Tx C is selected to be an input, the transmitter clock must be provided externally. When Tx C is programmed to be an output, a clock is generated by the MPCC's internal baud rate generator. The low-to-high transition of the clock signal nominally indicates the center of a serial data present on the TxD output.

RxC—Receiver Clock. Rx C provides the MPCC receiver with received data timing information.



Pin Configuration

EXTAL—Crystal/External Clock Input.

XTAL Crystal Return. EXTAL and XTAL connect an 8 MHz external crystal to the MPCC internal oscillator. The pin EXTAL may also be used as a TTL level input to supply a DC to 8 MHz reference timing from an external clock source. XTAL must be tied to ground when applying an external clock to the EXTAL input.

BCLK—Buffered Clock. BCLK is the internal oscillator buffered output available to other MPCC devices eliminating the need for additional crystals.

Vcc—Power. 5V \pm 5%.

GND—Ground. Ground (V_{SS}).

MPCC REGISTERS

Twenty-two registers control and monitor the MPCC operation. The registers and their addresses are identified in Table 1a (R68561 operation in word mode) and in Table 1b (R68560 operation in byte mode). When the R68561 is operated in the word mode, two registers are read or written at a time starting at an even boundary. When the R68560 is operated in the byte mode, each register is explicitly addressed based on A0.

Table 2 summarizes the MPCC register bit assignments and their access. A read from an unassigned location results in a read from a "null register." A null register returns all ones for data and results in a normal bus cycle. Unused bits of a defined register are read as zeros unless otherwise noted.

Table 1a. R68561 Accessible Registers (Word Mode)

Register(s)		R/W	Addr (Hex.)	Address Lines			
				A4	A3	A2	A1
15	8 7	0					
Receiver Control Register (RCR)	Receiver Status Register (RSR)	R/W	00	0	0	0	0
Receiver Data Register (RDR)—16 bits ¹		R	02	0	0	0	1
Receiver Interrupt Enable Register (RIER)	Receiver Interrupt Vector Number Register (RIVNR)	R/W	04	0	0	1	0
Transmitter Control Register (TCR)	Transmitter Status Register (TSR)	R/W	08	0	1	0	0
Transmitter Data Register (TDR)—16 bits ²		W	0A	0	1	0	1
Transmitter Interrupt Enable Register (TIER)	Transmitter Interrupt Vector Number Register (TIVNR)	R/W	0C	0	1	1	0
Serial Interface Control Register (SICR)	Serial Interface Status Register (SISR)	R/W	10	1	0	0	0
Reserved ³	Reserved ³	R/W	12	1	0	0	1
Serial Interrupt Enable Register (SIER)	Serial Interrupt Vector Number Register (SIVNR)	R/W	14	1	0	1	0
Protocol Select Register 2 (PSR2)	Protocol Select Register (PSR1)	R/W	18	1	1	0	0
Address Register 2 (AR2)	Address Register 1 (AR1)	R/W	1A	1	1	0	1
Band Rate Divider Register 2 (BRDR2)	Baud Rate Divider Register 1 (BRDR1)	R/W	1C	1	1	1	0
Error Control Register (ECR)	Clock Control Register (CCR)	R/W	1E	1	1	1	1

Notes:

1. Accessible register of the four word Rx FIFO. The data is not initialized, however, $\overline{\text{RES}}$ resets the Rx FIFO pointer to the start of the first word.
2. Accessible register of the four word Tx FIFO. The data is not initialized, however, $\overline{\text{RES}}$ resets the Tx FIFO pointer to the start of the first word.
3. Reserved registers may contain random bit values.

Table 1b. R68560 Accessible Registers (Byte Mode)

Register(s)	R/W	Addr (Hex.)	Address Lines				
			A4	A3	A2	A1	A0
7		0					
Receiver Status Register (RSR)	R/W	00	0	0	0	0	0
Receiver Control Register (RCR)	R/W	01	0	0	0	0	1
Receiver Data Register (RDR)—8 bits ¹	R	02	0	0	0	1	0
Reserved ³		03	0	0	0	1	1
Receiver Interrupt Vector Number Register (RIVNR)	R/W	04	0	0	1	0	0
Receiver Interrupt Enable Register (RIER)	R/W	05	0	0	1	0	1
Transmitter Status Register (TSR)	R/W	08	0	1	0	0	0
Transmitter Control Register (TCR)	R/W	09	0	1	0	0	1
Transmitter Data Register (TDR) ² —8 bits	W	0A	0	1	0	1	0
Reserved ³		0B	0	1	0	1	1
Transmitter Interrupt Vector Number Register (TIVNR)	R/W	0C	0	1	1	0	0
Transmitter Interrupt Enable Register (TIER)	R/W	0D	0	1	1	0	1
Serial Interface Status Register (SISR)	R/W	10	1	0	0	0	0
Serial Interface Control Register (SICR)	R/W	11	1	0	0	0	1
Reserved ³		12	1	0	0	1	0
Reserved ³		13	1	0	0	1	1
Serial Interrupt Vector Number Register (SIVNR)	R/W	14	1	0	1	0	0
Serial Interrupt Enable Register (SIER)	R/W	15	1	0	1	0	1
Protocol Select Register 1 (PSR1)	R/W	18	1	1	0	0	0
Protocol Select Register 2 (PSR2)	R/W	19	1	1	0	0	1
Address Register 1 (AR1)	R/W	1A	1	1	0	1	0
Address Register 2 (AR2)	R/W	1B	1	1	0	1	1
Band Rate Divider Register 1 (BRDR1)	R/W	1C	1	1	1	0	0
Baud Rate Divider Register 2 (BRDR2)	R/W	1D	1	1	1	0	1
Clock Control Register (CCR)	R/W	1E	1	1	1	1	0
Error Control Register (ECR)	R/W	1F	1	1	1	1	1

Notes:

1. Accessible register of the eight byte Rx FIFO. The data is not initialized, however, $\overline{\text{RES}}$ resets the Rx FIFO pointer to the start of the first byte.
2. Accessible register of the eight byte Tx FIFO. The data is not initialized, however, $\overline{\text{RES}}$ resets the Tx FIFO pointer to the start of the first byte.
3. Reserved registers may contain random bit values.

Table 2. MPCC Register Bit Assignments

R/W Access	Bit Number								Reset ⁽¹⁾ Value	
	7	6	5	4	3	2	1	0		
R/W	RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE	00	Receiver Status Register (RSR)
R/W	0	RDSREN	DONEEN	RSYNEN	STRSYN	2ADCMP	RABTEN	RRES	01	Receiver Control Register (RCR)
R	RECEIVED DATA (RxFIFO) ²								— —	Receiver Data Register (RDR)
R/W	RECEIVER INTERRUPT VECTOR NUMBER (RIVN)								0F	Receiver Interrupt Vector Number Register (RIVNR)
R/W	RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0	00	Receiver Interrupt Enable Register (RIER)
R/W	TDRA	TFC	0	0	0	TUNRN	TFERR	0	80	Transmitter Status Register (TSR)
R/W	TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES	01	Transmitter Control Register (TCR)
W	TRANSMITTED DATA (TxFIFO) ²								— —	Transmitter Data Register (TDR)
R/W	TRANSMITTER INTERRUPT VECTOR NUMBER (TIVN)								0F	Transmitter Interrupt Vector Number Register (TIVNR)
R/W	TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	0	00	Transmitter Interrupt Enable Register (TIER)
R/W	CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0	00	Serial Interface Status Register (SISR)
R/W	RTSLVL	DTLVL	0	0	0	ECHO	TEST	NRZI	00	Serial Interface Control Register (SICR)
12	RANDOM BIT VALUES									(reserved)
13	RANDOM BIT VALUES									(reserved)
R/W	SERIAL INTERRUPT VECTOR NUMBER (SIVN)								0F	Serial Interrupt Vector Number Register (SIVNR)
R/W	CTS IE	DSR IE	DCD IE	0	0	0	0	0	00	Serial Interrupt Enable Register (SIER)
R/W	0	0	0	0	0	0	CTLEX	ADDEX	00	Protocol Select Register 1 (PSR1)
R/W	WD/BYT	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL			00	Protocol Select Register 2 (PSR2)
		SB2	SB1	CL2	CL1	PS3	PS2	PS1		
R/W	BOP ADDRESS/BSC & COP PAD								00	Address Register 1 (AR1)
R/W	BOP ADDRESS/BSC & COP SYN								00	Address Register 2 (AR2)
R/W	BAUD RATE DIVIDER (LSH)								01	Baud Rate Divider Register 1 (BRDR1)
R/W	BAUD RATE DIVIDER (MSH)								00	Baud Rate Divider Register 2 (BRDR2)
R/W	0	0	0	PSCDIV	TCLKO	RCLKIN	CLK SEL		00	Clock Control Register (CCR)
							CK2	CK1		
R/W	PAREN	ODDPAR	0	0	CTLCRC	CRCPRE	CRC SEL		04	Error Control Register (ECR)
							CR2	CR1		

Notes:

1. RESET = Register contents upon power up or RESET.
2. 16-bits for R68561 (word mode); 8-bits for R68560 (byte mode).

REGISTER DEFINITIONS

RECEIVER REGISTERS

Receiver Status Register (RSR)

7	6	5	4	3	2	1	0
RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE

Reset Value = \$00

The Receiver Status Register (RSR) contains the status of the receiver including error conditions. Status bits are cleared by writing a 1 into respective positions, by writing a 1 into the RCR RRES bit or by RESET. If an EOF, C/PERR, or FRERR is set in the RSR, the data reflecting the error (the first byte or word in the Rx FIFO) must be read prior to resetting the corresponding status bit in the RSR. The IRQ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the RIER is set.

The RSR format is the same as the frame status format (see below) except as noted.

RSR

- 7 RDA —Receiver Data Available. (RSR only).**
- 0 The Rx FIFO is empty (i.e., no received data is available).
 - 1 Received data is available in the Rx FIFO and can be read via the RDR.

RSR

- 6 EOF —End of Frame.**
- 0 No end of frame or block detected.
 - 1 End of frame or block detected (BOP and BSC).

RSR

- 5 RHW —Receive Half Word. (Frame Status only)***
- 0 The last word of the frame contains data on the upper half (D8–D15) and frame status on the lower half (D0–D7) of the data bus.
 - 1 The lower half of the data bus (D0–D7) contains the frame status but the upper half (D8–D15) is blank or invalid.

RSR

- 4 C/PERR —CRC/Parity Error.**
- 0 No CRC or parity error detected.
 - 1 CRC error detected (BOP, BSC), Parity error detected (ASYN, ISOC and COP).

RSR

- 3 FRERR —Frame Error.**
- 0 No frame error detected.
 - 1 Short Frame or a closing FLAG detected off boundary (BOP), Frame error (ASYN, ISOC) or receiver overrun.

RSR

- 2 ROVRN —Receiver Overrun.**
- 0 No receiver overrun detected.
 - 1 Receiver overrun detected. Indicates that receiver data was attempted to be transferred into the Rx FIFO when it was full, resulting in loss of received data. The data that is already in Rx FIFO are not affected and may be read by the processor.

RSR

- 1 RA/B —Receiver Abort/Break.**
- 0 Normal Operation.
 - 1 ABORT detected after an opening flag (BOP), ENQ detected in a block of text data (BSC), or BREAK detected (ASYN).

RSR

- 0 RIDLE —Receiver Idle. (RSR only).**
- 0 Receiver not idle.
 - 1 15 or more consecutive "1's" have been received and the receiver is in an inactive idle state.

*Frame Status (RSR)

7	6	5	4	3	2	1	0
0	EOF	RHW	C/PERR	FRERR	ROVRN	RA/B	0

For the BSC and BOP protocols which have defined message blocks or frames, a "frame status" byte will be loaded into the Rx FIFO following the last data byte of each block. The frame status contains all the status contained within the RSR with the exception of RDA and RIDLE. But, in addition to the RSR contents, the frame status byte has a RHW status in bit 5 which indicates either an even or odd boundary (applicable to word mode only).

If the MPCC is in word mode and the last data byte was on an even byte boundary (i.e., there was an even number of bytes in the message), a blank byte will be loaded into the Rx FIFO prior to loading the frame status byte in order to force the "frame status" byte and the next frame to be on an even boundary. When RHW = 0, the last word of the frame contains data on the upper half and status on the lower half of the data bus. If RHW = 1, the lower half of the bus contains status but the upper half is a blank or invalid byte.

In the byte mode, the status byte will always immediately follow the last data byte of the block/frame (see Figure 3). The EOF status in the RSR is then set when the byte/word containing the frame status is the next byte/word to be read from the Rx FIFO.

In the receiver DMA mode, when the EOF status in the RSR is set, DONE is asserted to the DMAC. Thus the last byte accessed by the DMAC is always a status byte, which the processor may read to check the validity of entire frame.

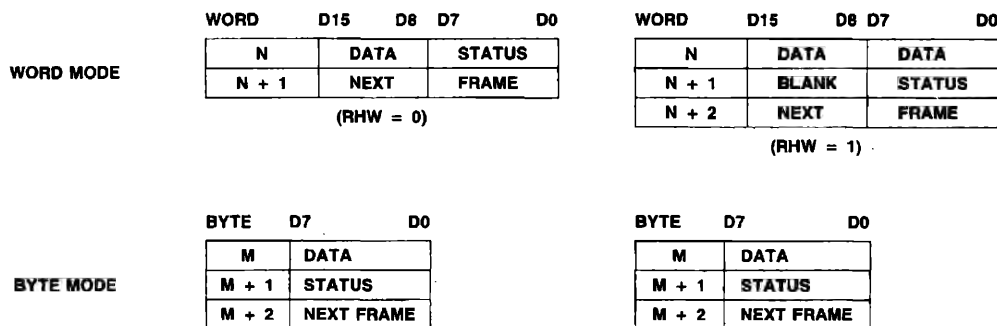


Figure 3. BSC/BOP Block/Frame Status Location

Receiver Control Register (RCR)

7	6	5	4	3	2	1	0
—	RDSREN	DONEEN	RSYNEN	STRSYN	2ADCMP	RABEN	RRES

Reset value = \$01

The Receiver Control Register (RCR) selects receiver control options.

RCR

7 —Not used.

RCR

6 **RDSREN** —Receiver Data Service Request Enable.
 0 Disable receiver DMA mode.
 1 Enable receiver DMA mode.

RCR

5 **DONEEN** —**DONE** Output Enable.
 0 Disable **DONE** output.
 1 Enable **DONE** output. (When the receiver is in the DMA mode, i.e., RDSREN = 1).

RCR

4 **RSYNEN** —**RSYNEN** Output Enable. Selects the DSR signal input or the RSYN SYNC signal output on the DSR pin.
 0 Input DSR on DSR.
 1 Output RSYN on DSR.

RCR

3 **STRSYN** —Strip SYN Character (COP only).
 0 Do not strip SYN character.
 1 Strip SYN character.

RCR

2 **2ADCMP** —One/Two Address Compare (BOP only).
 0 Compare one address byte with the contents of AR1.
 1 Compare two address bytes with the contents of AR1 and AR2.

RCR

1 **RABTEN** —Receiver Abort Enable (BOP only).
 0 Do not abort frame upon error detection.
 1 Abort frame upon Rx FIFO overrun (ROVRN bit = 1 in the RSR) or CFCRC error detection (C/PERR bit = 1 in the RSR). If either error occurs, the MPCC ignores the remainder of the current frame and searches for the beginning of the next frame.

RCR

0 **RRES** —Receiver Reset Command.
 0 Enable normal receiver operation.
 1 Reset receiver. Resets the receiver section including the Rx FIFO and the RSR (but not the RCR). RRES is set by RESET or by writing a 1 into this bit for one write cycle and is cleared by writing a 0 into this bit. RRES requires clearing after RESET.

Receiver Data Register (RDR)**R68561 (Word Mode)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
MSB				Byte 1				LSB				MSB				Byte 0				LSB			

R68560 (Byte Mode)

7	6	5	4	3	2	1	0	
MSB			Byte 0				LSB	

The receiver has an 8-byte (or 4-word) First In First Out (FIFO) register file (Rx FIFO) where received data are stored before being transferred to the bus. The received data is transferred out of the Rx FIFO via the RDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. When the Rx FIFO has a data byte/word ready to be transferred, the RDA status bit in the RSR is set to 1.

Receiver Interrupt Vector Number Register (RIVNR)

7	6	5	4	3	2	1	0
Receiver Interrupt Vector Number (RIVN)							

Reset value = \$0F

If a receiver interrupt condition occurs (as reported by status bits in the RSR that correspond to interrupt enable bits in the RIER) and the corresponding bit is set in the RIER, IRQ output is asserted to request MPU receiver interrupt service. When the IACK input is asserted from the bus, the Receiver Interrupt Vector Number (RIVN) from the Receiver Interrupt Vector Number Register (RIVNR) is placed on the data bus.

Receiver Interrupt Enable Register (RIER)

7	6	5	4	3	2	1	0
RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0

Reset value = \$00

The Receiver Interrupt Enable Register (RIER) contains interrupt enable bits for the Receiver Status Register (RSR). When enabled, the IRQ output is asserted when the corresponding condition is detected and reported in the RSR.

RIER

7 RDA IE —Receiver Data Available Interrupt Enable.

- 0 Disable RDA Interrupt.
- 1 Enable RDA Interrupt.

RIER

6 EOF IE —End of Frame Interrupt Enable.

- 0 Disable EOF Interrupt.
- 1 Enable EOF Interrupt.

RIER

5 —Not used.

RIER

4 C/PERR IE —CRC/Parity Error Interrupt Enable.

- 0 Disable C/PERR Interrupt.
- 1 Enable C/PERR Interrupt.

RIER

3 FRERR IE —Frame Error Interrupt Enable.

- 0 Disable FRERR Interrupt.
- 1 Enable FRERR Interrupt.

RIER

2 ROVRN IE —Receiver Overrun Interrupt Enable.

- 0 Disable ROVRN Interrupt.
- 1 Enable ROVRN Interrupt.

RIER

1 RA/B IE —Receiver Abort/Break Interrupt Enable.

- 0 Disable RA/B Interrupt.
- 1 Enable RA/B Interrupt.

RIER

0 —Not used.

TRANSMITTER REGISTERS**Transmitter Status Register (TSR)**

7	6	5	4	3	2	1	0
TDR	TFC	0	0	0	TUNRN	TFERR	0

Reset value = \$80

The Transmitter Status Register (TSR) contains the transmitter status including error conditions. The transmitter status bits are cleared by writing a 1 into their respective positions, by writing a 1 into the TCR TRES bit, or by RESET. The IRQ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the TIER is set.

TSR

7 TDR —Transmitter Data Register Available.

- 0 The Tx FIFO is full.
- 1 The Tx FIFO is not full (i.e., available) and data to transmit can be loaded via the TDR.

TSR

6 TFC —Transmitted Frame Complete. (BOP, BSC and COP only).

- 0 Frame not complete.
- 1 Closing FLAG or ABORT character has been transmitted (BOP), Trailing PAD has been transmitted (BSC), or the last character of a frame or block as defined by TLAST (TCR bit 3) has been transmitted (COP).

TSR

5-3 —Not used.

TSR

2 TUNRN —Transmitter Underrun (BOP, BSC and COP only). A transmitter underrun occurs when the transmitter runs out of data during a transmission. For BOP, the underrun condition is treated as an abort. For BSC and COP, SYN characters are transmitted until more data is available in the Tx FIFO.

- 0 No transmitter underrun occurred.
- 1 Transmitter underrun occurred.

TSR

1 TFERR —Transmit Frame Error (BOP only).

- 0 No frame error has occurred.
- 1 No control field was present (short frame).

Transmitter Control Register (TCR)

7	6	5	4	3	2	1	0
TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES

Reset value = \$01

The Transmitter Control Register (TCR) selects transmitter control function.

TCR

7 TEN —Transmitter Enable.

- 0 Disable transmitter. Tx output is idled. The Tx FIFO may be loaded while the transmitter is disabled.
- 1 Enable transmitter.

TCR

- 6 TDSREN** —Transmitter Data Service Request Enable.
- 0 Disable transmitter DMA mode.
- 1 Enable transmitter DMA mode.

TCR

- 5 TICS** —Transmitter Idle Character Select. Selects the idle character to be transmitted when the transmitter is in an active idle mode (transmitter enabled or disabled).
- 0 Mark Idle (TxD output is held high).
- 1 Content of AR2 (BSC and COP), BREAK condition (ASYN and ISOC), or FLAG character (BOP).

TCR

- 4 THW** —Transmit Half Word. (R68561, word mode only). This bit is used when the frame or block ends on an odd boundary in conjunction with the TLAST bit and indicates that the last word in the Tx FIFO contains valid data in the upper byte only. This bit must always be 0 in byte mode (R68560).
- 0 Transmit full word (16 bits) from the Tx FIFO.
- 1 Transmit upper byte (8 bits) from the Tx FIFO.

TCR

- 3 TLAST** —Transmit Last Character (BOP, BSC and COP only).
- 0 The next character is not the last character in a frame or block.
- 1 The next character to be written into the TDR is the last character of the message. The TLAST bit automatically returns to a 0 when the associated word/byte is written to the Tx FIFO. If the transmitter DMA mode is enabled, TLAST is set to a 1 by DONE from the DMAC. In this case the character written into the TDR in the current cycle is the last character.

TCR

- 2 TSYN** —Transmit SYN (BSC and COP only).
- 0 Do not transmit SYN characters.
- 1 Transmit SYN characters. Causes a pair of SYN characters to be transmitted immediately following the current character. If BSC transparent mode is active, a DLE SYN sequence is transmitted. The TSYN bit automatically returns to a 0 when the SYN character is loaded into the Transmitter Shift Register.

TCR

- 1 TABT** —Transmit ABORT (BOP only).
- 0 Enable normal transmitter operation.
- 1 Causes an abort by sending eight consecutive 1's. A data word/byte must be loaded into the Tx FIFO after setting this bit in order to complete the command. The TABT bit clears automatically when the subsequent data word/byte is loaded into the Tx FIFO.

TCR

- 0 TRES** —Transmitter Reset Command.
- 0 Enable normal transmitter operation.
- 1 Reset transmitter. Clears the transmitter section including the Tx FIFO and the TSR (but not the TCR). The TxD output is held in "Mark" condition. TRES is set by RESET or by writing a 1 into this bit for one write cycle and is cleared by writing a 0 into this bit. TRES requires clearing after RESET.

Transmit Data Register (TDR)

R68561 (Word Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
MSB				Byte 1				LSB		MSB				Byte 0		LSB	

R68560 (Byte Mode)

7	6	5	4	3	2	1	0
MSB		Byte 0				LSB	

The transmitter has an 8-byte (or 4-word) FIFO register file (Tx FIFO). Data to be transmitted is transferred from the bus into the Tx FIFO via the TDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. The TDRA status bit in the TSR is set to 1 when the Tx FIFO is ready to accept another data word/byte.

Transmitter Interrupt Vector Number Register (TIVNR)

7	6	5	4	3	2	1	0
Transmitter Interrupt Vector Number (TIVN)							

Reset value = \$0F

If a transmitter interrupt condition occurs (as reported by status bits in the TSR that correspond to interrupt enable bits in the TIER) and the corresponding bit in the TIER is set, the IRQ output is asserted to request MPU transmitter interrupt service. When the IACK input is asserted from the bus, the Transmitter Interrupt Vector Number (TIVN) from the Transmitter Interrupt Vector Number Register (TIVNR) is placed on the data bus.

Transmitter Interrupt Enable Register (TIER)

7	6	5	4	3	2	1	0
TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	—

Reset value = \$00

The Transmitter Interrupt Enable Register (TIER) contains interrupt enable bits for the Transmitter Status Register. When enabled, the IRQ output is asserted when the corresponding condition is detected and reported in the TSR.

TIER

- 7 TDRA IE** —Transmitter Data Register (TDR) Available Interrupt Enable.
- 0 Disable TDRA Interrupt.
- 1 Enable TDRA Interrupt.

TIER

- 6 TFC IE** —Transmit Frame Complete (TFC) Interrupt Enable.
 0 Disable TFC Interrupt.
 1 Enable TFC Interrupt.

TIER

5-3 —Not used.

TIER

- 2 TUNRN IE** —Transmitter Underrun (TUNRN) Interrupt Enable.
 0 Disable TUNRN Interrupt.
 1 Enable TUNRN Interrupt.

TIER

- 1 TFERR IE** —Transmit Frame Error (TFERR) Interrupt Enable.
 0 Disable TFERR Interrupt.
 1 Enable TFERR Interrupt.

TIER

0 —Not used.

SERIAL INTERFACE REGISTERS

Serial Interface Status Register (SISR)

7	6	5	4	3	2	1	0
CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0

Reset value = \$00

The Serial Interface Status Register (SISR) contains the serial interface status information. The transition status bits (CTST, DSRT and DCDT) are cleared by writing a 1 into their respective positions, or by RESET. The level status bits (CTSLVL, DSRLVL and DCDLVL) reflect the state of their respective inputs and cannot be cleared internally. The IRQ output is asserted if any of the conditions reported by the transition status bits occur and the corresponding interrupt enable bit in the SIER is set.

SISR

- 7 CTST** —Clear to Send Transition Status.
 1 CTS has transitioned positive (from active to inactive). (TRES must be zero).
 0 CTS has not transitioned positive.

SISR

- 6 DSRT** —Data Set Ready Transition Status.
 1 DSR has transitioned negative (from inactive to active).
 0 DSR has not transitioned negative.

SISR

- 5 DCDT** —Data Carrier Detect Transition Status.
 1 DCD has transitioned positive (from active to inactive).
 0 DCD has not transitioned positive.

SISR

- 4 CTSLVL** —Clear to Send Level.
 0 CTS input level is negated (high).
 1 CTS input level is asserted (low).

SISR

- 3 DSRLVL** —Data Set Ready Level.
 0 DSR input level is negated (high).
 1 DSR input level is asserted (low).

SISR

- 2 DCDLVL** —Data Carrier Detect Level.
 0 DCD input level is negated (high).
 1 DCD input level is asserted (low).

SISR

1-0 —Not used.

Serial Interface Control Register (SICR)

7	6	5	4	3	2	1	0
RTSLVL	DTRLVL	0	0	0	ECHO	TEST	NRZI

Reset value = \$00

The Serial Interface Control Register (SICR) controls various serial interface signals and test functions.

SICR

- 7 RTSLVL** —Request to Send Level.
 0 Negate RTS output (high).
 1 Assert RTS output (low).

NOTE

In BOP, BSC, or COP, when the RTSLVL bit is cleared in the middle of data transmission, the RTS output remains asserted until the end of the current frame or block has been transmitted. In ASYNC or ISOC, the RTS output is negated when the Tx FIFO is empty. If the transmitter is idling when the RTSLVL bit is reset, the RTS output is negated within two bit times.

SICR

- 6 DTRLVL** —Data Terminal Ready Level.
 0 Negate DTR output (high).
 1 Assert DTR output (low).

SICR

5-3 —Not used. These bits are initialized to 0 by RESET and must not be set to 1.

SICR

- 2 ECHO** —Echo Mode Enable.
 0 Disable Echo mode (enable normal operation).
 1 Enable Echo mode. Received data (RxD) is routed back through the transmitter to Tx D. The contents of the Tx FIFO is undisturbed. This mode may be used for remote test purposes.

SICR

- 1 TEST** —Self-test Enable.
 0 Disable self-test (enable normal operation).
 1 Enable self-test. The transmitted data (Tx D) and clock (Tx C) are routed back through to the receiver through RxD and RxC, respectively (DCD and CTS are ignored). This "loopback" self-test may be used for all protocols. RxC is external regardless of the state of CCR bit 2. CCR bit 3 may be a 0 or a 1.

SICR

- 0 NRZI** —NRZI Data Format Select. Selects the transmit and receive data format to be NRZ or NRZI.
- 0** Select NRZ data format. NRZ coding—high = 1 and low = 0.
- 1** Select NRZI data format. The serial data remains in the same state to send a binary 1 and switches to the opposite state to send a binary 0. A 1 bit delay is added to the Tx/D output to allow for encoding.

Serial Interrupt Vector Number Register (SIVNR)

7	6	5	4	3	2	1	0
Serial Interrupt Vector Number (SIVN)							

Reset value = \$0F

If a serial interface interrupt condition occurs (as reported by status bits in the SISR that correspond to interrupt enable bits in the SIER) and the corresponding bit in the SIER is set, the IRQ output is asserted to request MPU serial interface interrupt service. When the IACK input is asserted from the bus, the Serial Interrupt Vector Number (SIVN) from the Serial Interrupt Vector Number Register (SIVNR) is placed on the data bus.

Serial Interrupt Enable Register (SIER)

7	6	5	4	3	2	1	0
CTS IE	DSR IE	DCD IE	0	0	0	0	0

Reset value = \$00

The Serial Interrupt Enable Register (SIER) contains interrupt enable bits for the Serial Interface Status Register. When an interrupt enable bit is set, the IRQ output is asserted when the corresponding condition occurs as reported in the SISR.

SIER

- 7 CTS IE** —Clear to Send (CTS) Interrupt Enable.
- 0** Disable CTS Interrupt.
- 1** Enable CTS Interrupt.

SIER

- 6 DSR IE** —Data Set Ready (DSR) Interrupt Enable.
- 0** Disable DSR Interrupt.
- 1** Enable DSR Interrupt.

SIER

- 5 DCD IE** —Data Carrier Detect (DCD) Interrupt Enable.
- 0** Disable DCD Interrupt.
- 1** Enable DCD Interrupt.

SIER

- 4-0** —Not used.

GLOBAL REGISTERS

The global registers contain command information applying to different modes of operation and protocols. After changing global register data, TRES in the TCR and RRES in the RCR should be set then cleared prior to performing normal mode processing.

Protocol Select Register 1 (PSR1)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CTLEX	ADDEX

Reset value = \$00

Protocol Select Register 1 (PSR1) selects BOP protocol related options.

PSR1

- 7-2** —Not used.

PSR1

- 1 CTLEX** —Control Field Extend (BOP only).
- 0** Select 8-bit control field.
- 1** Select 16-bit control field.

PSR1

- 0 ADDEX** —Address Extend (BOP only).
- 0** Disable address extension. All eight bits of the address byte are utilized for addressing.
- 1** Enable address extension. When bit 0 in the address byte is a 0 the address field is extended by one byte. An exception to the address field extension occurs when the first address byte is all 0's (null address).

Protocol Select Register 2 (PSR2)

7	6	5	4	3	2	1	0
WD/BYT	STOP BIT SEL	CHAR LEN SEL	PROTOCOL SEL				
	SB2	SB1	CL2	CL1	PS3	PS2	PS1

Reset value = \$00

Protocol Select Register 2 (PSR2) selects protocols, character size, the number of stop bits, and word/byte mode.

PSR2

- 7 WD/BYT** —Data Bus Word/Byte Mode.
- 0** Select byte mode. Selects the number of data bits to be transferred from the Rx/FIFO and the registers to the data bus and to be transferred from the data bus to the Tx/FIFO and the registers. The MPCC is initialized by RESET to the byte mode.
- 1** Select word mode. For operation with the 16-bit bus, select the word mode by sending \$80 on D7 – D0 to address \$19 prior to transferring subsequent data between the MPCC and the data bus.

PSR2

- 6-5 STOP BIT SEL** —Number of Stop Bits Select.
- Selects the number of stop bits transmitted at the end of the data bins in ASYNC and ISOC modes.

No. of Stop Bits			
6	5	ASYNC	ISOC
SB2	SB1		
0	0	1	1
0	1	1-1/2	2
1	0	2	2

PSR2

4-3 CHAR LEN SEL — **Character Length Select.** Selects the character length except in BOP and BSC where the character length is always eight bits. Parity is not included in the character length.

4 CL2	3 CL1	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

PSR2

2-0 PROTOCOL SEL — **Protocol Select.** Selects protocol and defines the protocol dependent control bits.

2 PS3	1 PS2	0 PS1	Protocol
0	0	0	BOP (Primary)
0	0	1	BOP (Secondary)
0	1	0	Reserved
0	1	1	COP
1	0	0	BSC EBCDIC
1	0	1	BSC ASCII
1	1	0	ASYN
1	1	1	ISOC

Address Register 1 (AR1)

7	6	5	4	3	2	1	0
BOP ADDRESS/BSC & COP PAD							

Reset value = \$00

Address Register 2 (AR2)

7	6	5	4	3	2	1	0
BOP ADDRESS/BSC & COP SYN							

Reset value = \$00

The protocol selected in PSR2 (BOP, BSC and COP only) determines the function of the two 8-bit Address Registers (AR1 and AR2). As a secondary station in BOP, the contents of the address registers are used for address matching depending on the 2 ADCMP selection in the RCR. In BSC and COP, AR1 and AR2 contain programmable leading PAD and programmable SYN characters, respectively.

Address Register (AR) Contents

Protocol Selected	2ADCMP	AR1	AR2
BOP (Primary)	X	X	X
BOP (Secondary)	0	Address	X
	1	Address	Address
BSC EBCDIC	X	Leading PAD	SYN
BSC ASCII	X	Leading PAD	SYN
COP	X	Leading PAD	SYN
*X = Not used			

Baud Rate Divider Register 1 (BRDR1)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (LSH)							

Reset value = \$01

Baud Rate Divider Register 2 (BRDR2)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (MSH)							

Reset value = \$00

The two 8-bit Baud Rate Divider Registers (BRDR1 and BRDR2) hold the divisor of the Baud Rate Divider circuit. BRDR1 contains the least significant half (LSH) and BRDR2 contains the most significant half (MSH). With an 8.064 MHz EXTAL input, standard bit rates can be selected using the combination of Prescaler Divider (in the CCR) and Baud Rate Divider values shown in Table 3. For isochronous or synchronous protocols, the Baud Rate Divider value must be multiplied by two for the same Prescaler Divider value.

The Baud Rate Divider (BRD) value can be computed for other crystal frequency, prescaler divider and desired baud rate values as follows:

$$BRD = \frac{\text{Crystal Frequency}}{(\text{Prescaler Divider}) (\text{Baud Rate}) (K)}$$

where: K = 1 for isochronous or synchronous
2 for asynchronous

Clock Control Register (CCR)

7	6	5	4	3	2	1	0
0	0	0	PSCDIV	TCLKO	RCLKIN	CLK SEL	
						CK2	CK1

Reset value = \$00

The CCR selects various clock options.

CCR

7-5 — Not used.

CCR

4 PSCDIV — **Prescaler Divider.** The Prescaler Divider network reduces the external/oscillator frequency to a value for use by the internal Baud Rate Generator.

- 0 Divide by 2.
- 1 Divide by 3.

CCR

3 TCLKO — **Transmitter Clock Output Select.**

- 0 Select TxC to be an input.
- 1 Select TxC to be an output.

Table 3. Standard Baud Selection (8.064 MHz Crystal)

Desired Baud Rate (Bit Rate)	Prescaler Divider		Baud Rate Divider					
			Asynchronous			Isochronous and Synchronous		
	Decimal Value	PSCDIV (0 to 1)	Decimal Value	Hexadecimal Value		Decimal Value	Hexadecimal Value	
				BRDR2 (MSH)	BRDR1 (LSH)		BRDR2 (MSH)	BRDR1 (LSH)
50	3	1	26,880	69	00	53,760	D2	00
75	2	0	26,880	69	00	53,760	D2	00
110	3	1	12,218	2F	BA	24,436	5F	74
135	2	0	14,933	3A	55	29,866	74	AA
150	3	1	8,960	23	00	17,920	46	00
300	2	0	6,720	1A	40	13,440	34	80
1200	3	1	1,120	04	60	2,240	08	C0
1800	2	0	1,120	04	60	2,240	08	C0
2400	2	0	840	03	48	1,680	06	90
3600	2	0	560	02	30	1,120	04	60
4800	3	1	280	01	18	560	02	30
7200	2	0	280	01	18	560	02	30
9600	3	1	140	00	8C	280	01	18
19200	3	1	70	00	46	140	00	8C
38400	3	1	35	00	23	70	00	46

CCR**2 RCLKIN** —Receiver Clock Internal Select (ASYNC only).

- 0 Select External RxC.
1 Select Internal RxC.

CCR**1-0 CLK DIV** —External Receiver Clock Divider. Selects the divider of the external RxC to determine the receiver data rate.

CK2	CK1	Divider
0	0	1 (ISOC)
0	1	16
1	0	32
1	1	64

Error Control Register (ECR)

7	6	5	4	3	2	1	0
PAREN	ODDPAR	—	—	CRCCTL	CRCPRE	CRCSEL	
						CR2	CR1

Reset value = \$04

The Error Control Register (ECR) selects the error detection method used by the MPCC.

ECR**7 PAREN** —Parity Enable. (ASYNC, ISOC and COP only).

- 0 Disable parity generation/checking.
1 Enable parity generation/checking.

ECR**6 ODDPAR** —Odd/Even Parity Select (Effective only when PAREN = 1).

- 0 Generate/check even parity.
1 Generate/check odd parity.

ECR**5-4** —Not used.**ECR****3 CFCRC** —Control Field CRC Enable.

- 0 Disable control field CRC. Enables an intermediate CRC remainder to be appended after the address/control field in transmitted BOP frames and checked in received frames. The CRC generator is reset after control field CRC calculation.

ECR**2 CRCPRE** —CRC Generator Preset Select.

- 0 Preset CRC Generator to 0.
1 Preset CRC Generator to 1 and transmit the 1's complement of the resulting remainder.

ECR**1-0 CRCSEL** —CRC Polynomial Select. Selects one of the RC polynomials.

1	0	
CR2	CR1	Polynomial
0	0	$x^{16} + x^{12} + x^5 + 1$ (CCITT V.41)
0	1	$x^{16} + x^{15} + x^2 + 1$ (CRC-16)
1	0	$x^8 + 1$ (VRC/LRC)*
1	1	Not used.

*VRC: Odd-parity check is performed on each character including the LRC character.

INPUT/OUTPUT FUNCTIONS

MPU INTERFACE

Transfer of data between the MPCC and the system bus involves the following signals:

	R68561	R68560
Address Lines	A1–A4	A0–A4
Data Lines	D0–D15	D0–D7
Read/Write	R/W	R/W
Data Transfer Acknowledge	DTACK	DTACK
Chip Select	CS	CS
Data Strokes	UDS and LDS	DS

Figures 10 and 11 show typical interface connections.

Read/Write Operation

The R/W input controls the direction of data flow on the data bus. CS (Chip Select) enables the MPCC for access to the internal registers and other operations. When CS is asserted, the data I/O buffer acts as an output driver during a read operation and as an input buffer during a write operation. CS must be decoded from the address bus and gated with address strobe (AS).

When the R68561 is connected to the 16-bit bus for operation in the word mode (WD/BYT = 1 in the PSR2), address lines A1–A4 select the internal register(s) (the 8-bit control/status registers are accessed two at a time and the 16-bit data registers are accessed on even address boundaries). When the MPCC is selected (CS low) during a read (R/W high), 16 bits of register data are placed on the data bus when the data strobes (LDS and UDS) are asserted. LDS strobes the eight data bits from the even numbered registers to the lower data bus lines (D0–D7) and UDS strobes the eight data bits from the odd numbered registers to the upper data bus lines (D8–D15). The MPCC asserts Data Transfer Acknowledge (DTACK prior to placing data on the data bus. Conversely, when the MPCC is selected (CS low) during a write (R/W low) LDS and UDS strobe data from the D0–D7 and D8–D15 data bus lines into the addressed even and odd numbered registers, respectively, and the MPCC asserts DTACK. DTACK is negated when CS is negated. Figures 12 and 13 show the read and write timing relationships.

When the R68560 is connected to the 8-bit bus for operation in the byte mode (WD/BYT = 0 in the PSR2), address lines A0–A4 select one internal 8-bit register. When the MPCC is selected (CS low) during a read (R/W high), eight bits of register data are placed on data bus lines D0–D7 when the data strobe (DS) is asserted. When the MPCC is selected (CS low) for a write (R/W low), DS strobes data from the D0–D7 data lines into the selected register.

DMA INTERFACE

The MPCC is capable of providing DMA data transfers up to 2 Mbytes per second when used with the MC68440 or MC68450 DMAC in the single address mode. Based on 4 Mb/s serial data rate and 5 bits/character, the maximum DMA required transfer rate is 800 Kbytes per second.

The MPCC has separate DMA enable bits for the transmitter and receiver, each of which requires a DMA channel. Both the transmitter and receiver data are implicitly addressed (TDR or RDR) therefore addressing of the data register is not required before data may be transferred. Communication between the

MPCC and the DMAC is accomplished by a two-signal request/acknowledge handshake. Since the MPCC has only one acknowledge input (DACK) for its two DMA request lines, an external OR function must be provided to combine the two DMA acknowledge signals. The MPCC uses the R/W input to distinguish between the Transmitter Data Service Request (TDSR) acknowledge and the Receiver Data Service Request (RDSR) acknowledge.

Receiver DMA Mode

The receiver DMA mode is enabled when the RDSREN bit in the RCR is set to 1. When data is available in the Rx FIFO, Receiver Data Service Request (RDSR) is asserted for one receiver clock period to initiate the MPCC to memory DMA transfer. The next RDSR cycle may be initiated as soon as the current RDSR cycle is completed (i.e., a full sequence of DACK, DS, and DTC).

In response to RDSR assertion, the DMAC sets the R/W line to write, asserts the memory address, address strobe, and DMA acknowledge. The MPCC outputs data from the Rx FIFO to the data bus and the DMAC asserts the data strobes. The memory latches the data and asserts DTACK to complete the data transfer. The DMAC asserts DTC to indicate to the MPCC that data transfer is complete. Figure 13 shows the timing relationships for the receiver DMA mode.

RDSR is inhibited when either RDSREN is reset to 0 or RRES is set to 1 (both in the RCR), or when RESET is asserted.

Transmitter DMA Mode

The transmitter DMA mode is enabled when the TDSREN bit in the TCR is set to 1. When the Tx FIFO is available, Transmitter Data Service Request (TDSR) is asserted for one transmitter clock period to initiate the memory to MPCC DMA transfer. The next TDSR cycle may be initiated as soon as the current TDSR cycle is completed.

In the transmitter DMA mode, the Tx FIFO is implicitly addressed. That is, when the transfer is from memory to the Tx FIFO, only the memory is addressed. In response to TDSR assertion, the DMAC sets the R/W line to read, asserts the memory address, the address strobe, the data strobes and DMA acknowledge. The memory places data on the data bus and asserts DTACK. Data is valid at this time and will remain valid until the data strobes are negated. The DMAC asserts DTC to indicate to the MPCC that data is available. The MPCC loads the data into the Tx FIFO on the negation (rising edge) of DS and the transfer is complete. A timing diagram for the transmitter DMA Mode is shown in Figure 15.

TDSR is inhibited when either TDSREN is reset to 0 or TRES is set to 1 (both in the TCR), or when RESET is asserted.

DONE Signal

When the DMA transfer count is exhausted in transmitter DMA mode, the DMAC asserts DONE which sets the TLAST bit in the TCR to indicate that the last word/byte has been transferred. In the receiver DMA mode, DONE is asserted by the MPCC when the last character of the frame/block is being transferred from the Rx FIFO to the data bus if the DONEEN bit is set to a 1 in the RCR.

INTERRUPTS

If an interrupt generating status occurs and the interrupt is enabled, the MPCC asserts the $\overline{\text{IRQ}}$ output. Upon receiving $\overline{\text{IACK}}$ for the pending interrupt request, the MPCC places an interrupt vector on D0–D7 data bus and asserts $\overline{\text{DTACK}}$.

The MPCC has three vector registers: Receiver Interrupt Vector Number Register (RIVNR), Transmitter Interrupt Vector Number Register (TIVNR), and Serial Interrupt Vector Number Register (SIVNR). The receiver interrupt has higher priority over the transmitter interrupt, and the transmitter interrupt has priority over the serial interface interrupt. For example, if a pending interrupt request has been generated simultaneously by the receiver and the transmitter, the Receiver Interrupt Vector Number (RIVN) is placed on D0–D7 when acknowledged by the MPU. Upon completion of the first interrupt request cycle (which clears the receiver interrupt), $\overline{\text{IRQ}}$ will remain low to start the transmitter interrupt cycle. $\overline{\text{IRQ}}$ is negated by clearing all bits set in a status register that could have caused the interrupt.

A timing diagram for the interrupt acknowledge sequence is shown in Figure 15.

SERIAL INTERFACE

The MPCC is a high speed, high performance device supporting the more popular bit and character oriented data protocols. The lower speed asynchronous (ASYNC) and isochronous (ISOCH) modes are also supported. An on-chip clock oscillator and baud rate generator provide an output data clock at a frequency of DC to 4 MHz. The clock can also be used in the ASYNC mode to provide a receive clock for the incoming data. The serial interface consists of the following signals:

RTS (Request to Send) Output

The RTS output to the DCE is controlled by the RTSLVL bit in the SICR in conjunction with the state of the transmitter section. When the RTSLVL bit is set to 1, the RTS output is asserted. When the RTSLVL bit is reset to 0, the RTS output remains asserted until the Tx FIFO becomes empty or the end of the message (or frame), complete with CRC code if any, has been transmitted. RTS also is negated when the RTSLVL bit is reset during transmitter idle, or when the RESET input is asserted.

CTS (Clear to Send) Input

The CTS input signal is normally generated by the DCE to indicate whether or not the data set is ready to transmit data. The CTST bit in the SISR reflects the transition status of the CTS input while the CTSLVL bit in the SISR reflects the current level. A positive transition on the CTS pin asserts $\overline{\text{IRQ}}$ if the CTS IE bit in the SIER is set. The CTS input in an inactive state disables the start of transmission.

DCD (Data Carrier Detect) Input

The DCD input signal is normally generated by the DCE and indicates that the DCE is receiving a data carrier signal suitable for demodulation. The DCDT bit in the SISR reports the transition status of the DCD input while the DCDLVL bit in the SISR contains the current level. A positive transition on the DCD pin asserts the $\overline{\text{IRQ}}$ output if the DCD IE bit in the SIER is set. A negated DCD input disables the start of the receiver.

DSR (Data Set Ready) Input/RSYN Output

The DSRT input from the DCE indicates the status of the local set. The DSRT bit in the SISR contains the transition status of the DSR input while the DSRLVL bit in the SISR reports the current level. A negative transition on the DSR pin asserts the $\overline{\text{IRQ}}$ output if the DSR IE bit in the SIER is set.

When the RSYN bit in the RCR is set to 1, the frame synchronization signal (RSYN) in the receiver is output on the DSR pin. In this mode, DSR output low indicates detection of SYN in BSC or COP, or an address match in BOP.

DTR (Data Terminal Ready) Output

The DTR output is general purpose in nature and can be used to control switching of the DCE. The DTR output is controlled by the DTRLVL bit in the SICR.

TxC (Transmitter Clock) Input/Output

The transmitter clock (TxC) may be programmed to be input or an output. When the TCLKO control bit in the CCR is set to a 1, the TxC pin becomes an output and provides the DCE with a clock whose frequency is determined by the internal baud rate generator. When the TCLKO control bit is reset, TxC is an input and the transmitter shift timing must be provided externally. The TxD output changes state on the negative-going edge of the transmitter clock. In the asynchronous mode when TCLKO = 0 in the CCR, the TxC input frequency must be two times the desired baud rate.

TxD (Transmitted Data) Output

The serial data transmitted from the MPCC is coded in NRZ or NRZI (zero complement) data format as selected by the NRZI control bit in the SICR.

RxC (Receiver Clock) Input

The receiver latches data on the negative transition of the RxC.

RxD (Received Data) Input

The serial data received by the MPCC can be coded in NRZ or NRZI data format. The MPCC will decode the received data in accordance with the NRZI control bit setting in the SICR.

Serial Interface Timing

The timing for the serial interface clock and data lines is shown in Figure 18. The MPCC supports high speed synchronous operation. As shown, the TxD output changes with the negative-going edge of TxC and the received data on RxD is latched on the negative edge of RxC. This assures high speed two-way operation between two MPCCs connected as shown in Figure 17.

For low speed operation between the MPCC and a modem or RS-232C Data Communications Equipment (DCE), an inverter can be used in the TxC output lines as shown in Figure 17. RS-232 and RS-423 (covering serial data interface up to 100K baud) require that data be centered $\pm 25\%$ about the negative-going edge of the RxC. This criteria is met for frequencies up to 1.25 MHz using the inverter. Use of the inverter also allows MPCC to MPCC operation up to 2.17 MHz.

SERIAL COMMUNICATION MODES AND PROTOCOLS

ASYNCHRONOUS AND ISOCRONOUS MODES

Asynchronous and isochronous data are transferred in frames. Each frame consists of a start bit, 5 to 8 data bits plus optional even or odd parity, and 1, 1½, or 2 stop bits. The data character is transmitted with the least significant bit (LSB) first. The data line is normally held high (MARK) between frames; however, a BREAK (minimum of one frame length for which the line is held low) is used for control purposes. Figure 4 illustrates the frame format supported by the MPCC.

Asynchronous Receive

In the asynchronous (ASYN) mode, data received on RxD occurs in three phases: (1) detection of the start bit and bit synchronization, (2) character assembly and optional parity check, and (3) stop bit detection. The receiver bit stream may be synchronized by the internal baud rate generator clock or by an external clock on RxC. When RCLKIN in the CCR is set to 0, an external clock with a frequency of 16, 32, or 64 times the data rate establishes the data bit midpoint and maintains bit synchroniza-

tion. The character assembly process does not start if the start bit is less than one-half bit time. Framing and parity errors are detected and buffered along with the character on which errors occurred. They are passed on to the Rx FIFO and set appropriate status bits in the RSR when the character with an error reaches the last Rx FIFO register where it is ready to be transferred onto the data bus via the RDR.

Isochronous Receive

In the isochronous (ISOC) mode, a 1 times clock on RxC is required with the data on RxD and the serial data bit is latched on the falling edge of each clock pulse. The requirement for the detection of a valid start bit, or the beginning of a break, is satisfied by the detection of a high-to-low transition on the serial data input line. Error detection and status indication are the same as the asynchronous mode.

Asynchronous and Isochronous Transmit

In asynchronous and isochronous transmit modes, output data transmission on TxD begins with the start bit. This is followed by the data character which is transmitted LSB first. If parity generation is enabled, the parity bit is transmitted after the MSB of the character.

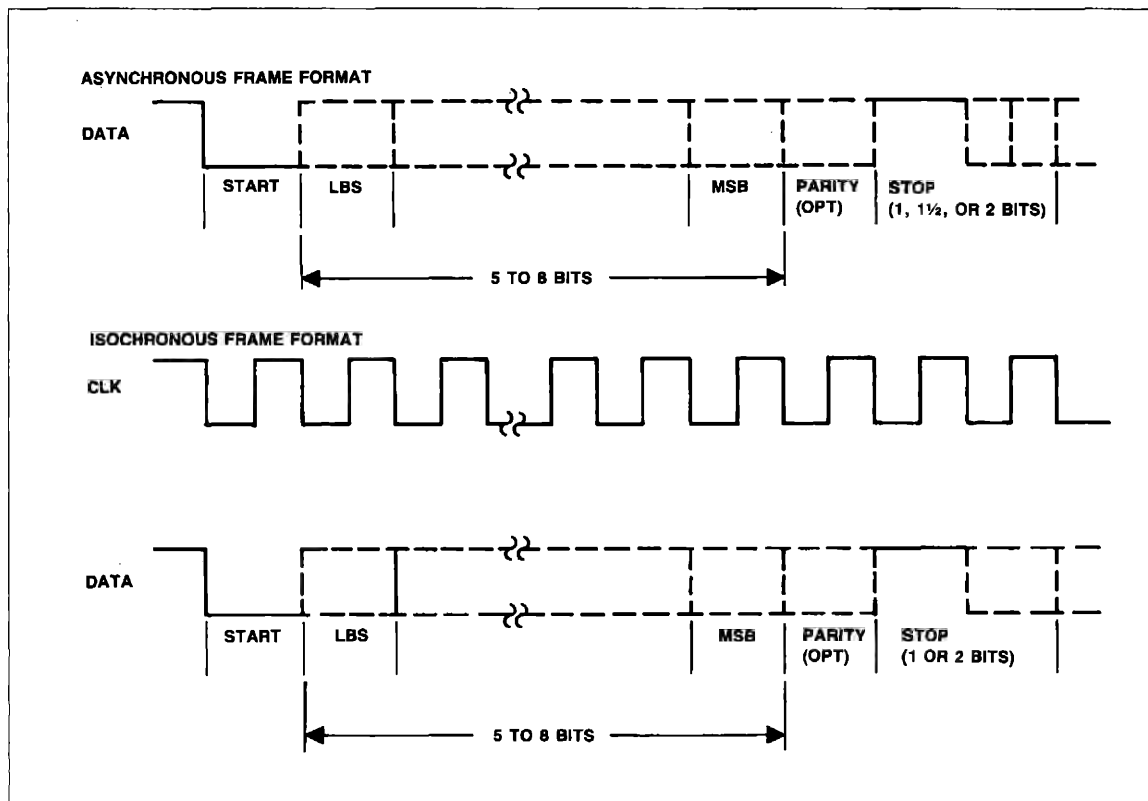


Figure 4. Asynchronous and Isochronous Frame Format

SYNCHRONOUS MODES

In synchronous modes, a one-times clock is provided along with the data. Serial output data is shifted out and input data is latched on the falling edge of the clock.

BIT ORIENTED PROTOCOLS (BOP)

In bit oriented protocols (BOP), messages (data) are transmitted and received in frames. Each frame contains an opening flag, address field, control field, frame check sequence, and a closing flag. A frame may also contain an information field. (See Figure 5).

The opening flag is a special character whose bit pattern is 01111110. It marks the frame boundaries and is the interframe fill character. The address field of a frame contains the address of the secondary station which is receiving or responding to a command. The address field may be one or more bytes long. The address field can be extended by setting the ADDEX bit to a 1 in PSR1. In this case, the address field will be extended until the occurrence of an address byte with a 1 in bit 0. Up to two bytes of the address field may be automatically checked when the MPCC is programmed to be a secondary station in BOP. An automatic check for global (11111111) or null (00000000) address is also made. The control field of one or two bytes is transparent to the MPCC and sent directly to the host without interpretation.

The optional information field consists of 8-bit characters. Cyclic redundancy checking is used for error detection and the CRC remainder resulting from the calculation is transmitted as the frame check sequence field. For BOP, the polynomial $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) should be used, i.e., selected in the CRC SEL bits in the ECR. The registers representing the CRC-CCITT polynomial are generally preset to all 1s, and the 1s complement of the resulting remainder is transmitted. (See X.25 Recommendation.)

Zero insertion/deletion is employed to prevent valid frame data from being confused with the special characters. A 0 is inserted by the transmitter after every fifth consecutive 1 in the data stream. These inserted zeros are removed by the receiver to restore the data to its original form. The inserted zeros are not included in the CRC calculation.

The end of the frame is determined by the detection of the closing Flag special character which is the same as the opening Flag.

With the control options offered by the MPCC, commonly used bit oriented protocols such as SDLC, HDLC and X.25 standards can be supported. Figure 6 compares the requirements of these options.

BOP Receiver Operation

In BOP, the receiver starts assembling characters and accumulating CRC immediately after the detection of a Flag. The receiver also continues to search for additional Flag, or Abort, characters on a bit-by-bit basis. Zero deletion is implemented in the Receiver Shift Register after the Flag detection logic and before the CRC circuitry. The receiver recognizes the shared flag (the closing flag for one frame serves as the opening flag for the next frame) and the shared zero (the ending 0 of a closing flag serves as the beginning 0 of an opening flag forming the pattern "011111101111110").

Character assembly and CRC accumulation are stopped when a closing Flag or Abort is detected. The CRC accumulation includes all the characters between the opening Flag and the closing Flag. The contents of the CRC register are checked at the close of a frame and the C/PERR bit in the RSR is updated. The FCS and the Flag are not passed on to the RxFIFO.

If the Flag is a closing flag, checks for short frame (no control field) and CRC error conditions are made and the appropriate status is updated. When an Abort (seven 1s) is detected, the remaining frame is discarded and the R/A/B bit is set in the RSR. When a link idle (15 or more consecutive 1s) is detected, the R/DLE status bit is set in the RSR. The zeros that have been inserted to distinguish data from special characters are detected and deleted from the data stream before characters are assembled. The MPCC programmed as a secondary station provides automatic address matching of up to two bytes. If there is no address match, the receiver (secondary station) ignores the remainder of the frame by searching for the Flag. If there is a match, the address bytes are transferred to the RxFIFO as they are assembled.

FLAG 01111110	ADDRESS 1 OR N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES (OPTIONAL)	FCS 2 BYTES	FLAG 01111110
------------------	----------------------------	----------------------------	--------------------------------------	----------------	------------------

Figure 5. Bit Oriented Protocol (BOP) Frame Format

IBM SDLS FRAME FORMAT

FLAG 01111110	ADDRESS 1 BYTE	CONTROL 1 BYTE	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110
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ADCCP/HDLC FRAME FORMAT

FLAG 01111110	ADDRESS N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110
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Figure 6. Implemented Bit Oriented Protocols

For the control field, one or two bytes are assembled and passed on to the Rx FIFO depending on the state of the extended control field bit.

If the CFCRC bit in the ECR is set to 1, an intermediate CRC check will be made after the address and control field. The Frame Check Sequence is still calculated over the remainder of the frame.

BOP Transmitter Operation

In BOP, the Tx FIFO can be preloaded through the TDR while the transmitter is disabled (TEN = 0 in the TCR). When the transmitter is enabled (TEN = 1 in the TCR), the leading Flag is automatically sent prior to transmitting data from the Tx FIFO. The TDRA bit is set to 1 in the TSR as long as Tx FIFO is not full. If an underrun occurs, the TUNRN bit in the TSR is set to a 1 and an Abort (11111111) is transmitted followed by continuous Flags or marks until a new sequence is initiated.

The TLAST bit in the TCR must be set prior to loading the last character of the message to signal the transmitter to append the two-byte Frame Check Sequence (FCS) following the last character. If the transmitter DMA mode is selected (the TDSREN bit set to 1 in the TCR) the TLAST bit is set by the DONE signal from the DMAC.

A message may be terminated at any time by setting the TABT bit in the TCR to 1. This causes the transmitter to send an Abort character followed by the remainder of the current frame data in the Tx FIFO.

The serial data from the Transmitter Shift Register is continuously monitored for five consecutive 1s, and a 0 is inserted in the data stream each time this condition occurs (excluding Flag and Abort characters).

CRC accumulation begins with the first non-Flag character and includes all subsequent characters. The CRC remainder is transmitted as the FCS following the last data character. If the CTCRC bit in the ECR is set to 1, an intermediate CRC remainder is appended after the Address and Control field. The final Frame Check Sequence is calculated over the balance of the frame.

BISYNC (BSC)

The structure of messages utilizing the IBM Binary Synchronous Communications (BSC) protocol, commonly called Bisync, is shown in Figure 7. The MPCC can process both transparent and nontransparent messages using either the EBCDIC or the ASCII codes. The CRC-16 polynomial should be selected by setting the appropriate CRCSEL bits in the ECR for both transparent and

non-transparent EBCDIC and for transparent ASCII coded messages. VRC/LRC should be selected for non-transparent ASCII coded messages. BSC messages are formatted using defined data-link control characters. Data-link control characters generated and recognized by the MPCC are listed in Table 4.

Table 4. BSC Control Sequences—Inclusion in CRC Accumulation

ASCII			EBCDIC		
Command	Byte 1	Byte 2	Command	Byte 1	Byte 2
SYN	16*	—	SYN	32*	—
SOH	01	—	SOH	01	—
STX	02	—	STX	02	—
ETB	17	—	EOB (ETB)	26	—
ETX	03	—	ETX	03	—
ENQ	05	—	ENQ	2D	—
DLE	10	—	DLE	10	—
ITB	1F	—	ITB	1F	—
EOT	04	—	EOT	37	—
ACK N*	10	30-37	ACK 0	10	70
NAK	15	—	ACK 1	10	61
WACK	10	3B	NAK	3D	—
RVI	10	3C	WACK	10	6B
			RVI	10	7C

Note: *Programmable

A heading is a block of data starting with an SOH and containing one or more characters that are used for message control (e.g., message identification, routing, and priority). The SOH initiates the block-check-character (BCC) accumulation, but is not included in the accumulation. The heading is terminated by STX when it is part of a block containing both heading and text. A block containing only a heading is terminated with an ITB or an ETB followed by the BCC. Only the first SOH or STX in a transmission block following a line turnaround causes the BCC to reset. All succeeding STX or SOH characters are included in the BCC. This permits the entire transmission (excluding the first SOH or STX) to be block-checked.

The text data is transmitted in complete units called messages, which are initiated by STX and concluded with ETX. A message can be subdivided into smaller blocks for ease in processing and more efficient error control. Each block starts with STX and ends with ETB (except for the last block of a message, which ends with ETX). A single transmission can contain any number of blocks (ending with ETB) or messages (ending with ETX). An EOT following the last ETX block indicates a normal end of transmission. Message blocking without line turnaround can be accomplished by using ITB (see the Additional Data Link Capabilities section, IBM GA 27-3004-2).

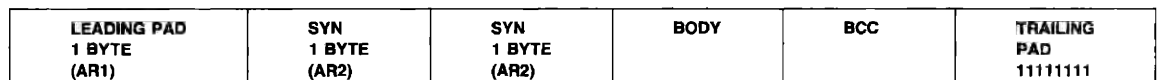


Figure 7. BSC Block Format

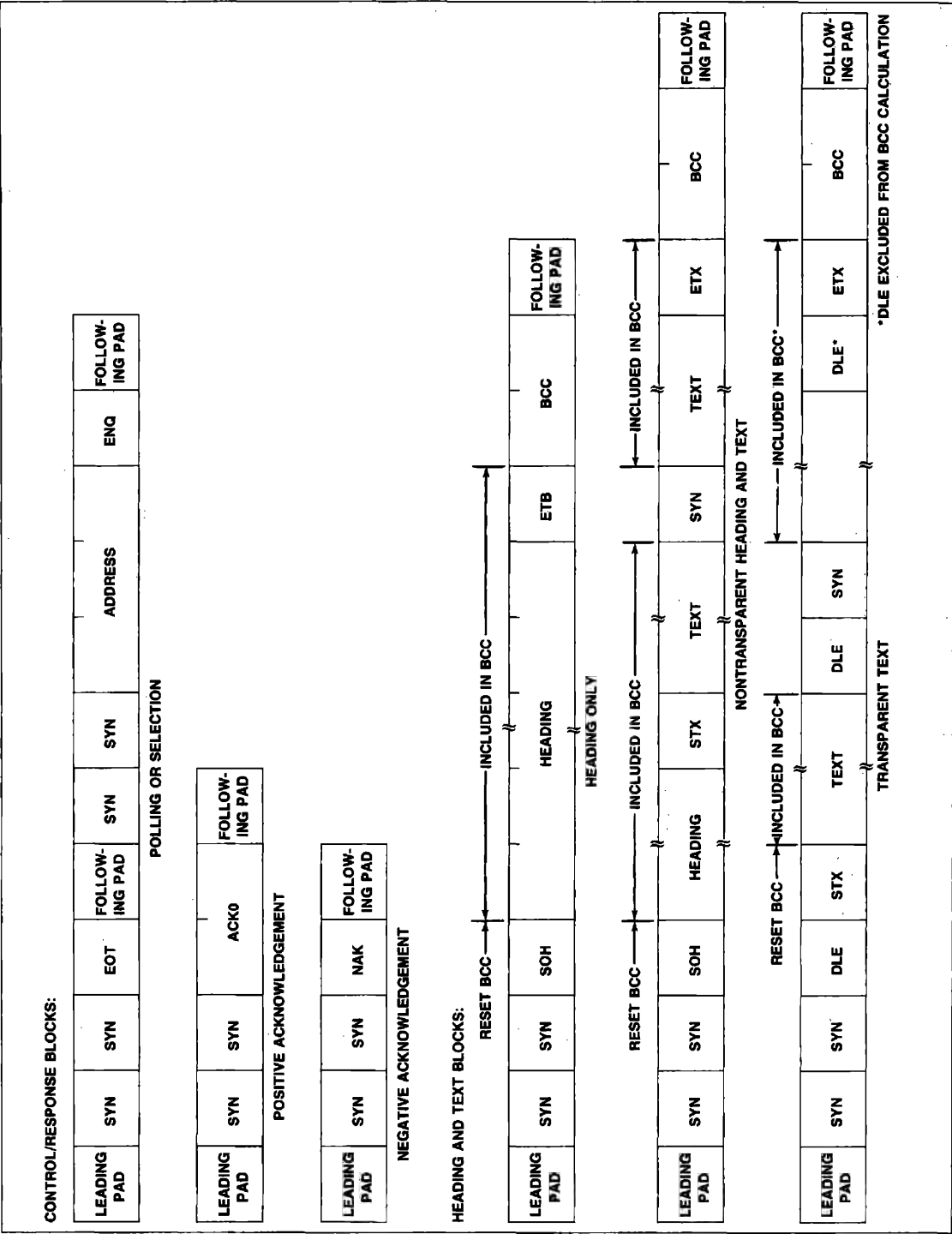


Figure 8. BSC Message Format Examples

Two modes of data transfers are used in BSC. In non-transparent mode, data link control characters may not appear as text data. In transparent mode, each control character is preceded by a data link escape (DLE) character to differentiate it from the text data. Table 5 indicates which control characters are excluded in the CRC generation. All characters not shown in the table are included in the CRC generation. Figure 8 shows various formats for Control/Response Blocks and Heading and Text Blocks.

Table 5. BSC Control Sequences — Inclusion in CRC Accumulation

Character of Sequence	Included in CRC Accumulation	
	Yes	No
TSYN	—	DLESYN
TSOH	—	DLESOH
TSTX*	—	DLESTX
TETB	ETB	DLE
TETX	ETX	DLE
TDLE	(DLE)DLE	DLE(DLE)

* If not preceded within the same block by transparent heading information.

BSC Receiver Operation

Character length defaults to eight bits in BSC mode. When ASCII is selected, the eighth bit is used for parity provided that VRC/LRC polynomial is selected. Character assembly starts after the receipt of two consecutive SYN characters. Serial data bits are shifted through the Receiver Shift Register into the Serial-to-Parallel Register and transferred to the Rx FIFO. The RDA status bit in the RSR is set to 1 each time data is transferred to the Rx FIFO. The SYN character in non-transparent mode and DLE-SYN pairs in transparent mode are discarded.

The receiver starts each block in the non-transparent mode. It switches to transparent mode if a block begins with a DLE-SOH or DLE-STX pair. The receiver remains in transparent mode until a DLE-ITB, DLE-ETB, DLE-ETX or DLE-ENQ pair is received. BCC accumulation begins after an opening SOH, STX, or DLE-STX. SYN characters in non-transparent mode or DLE-SYN pairs in transparent mode are excluded from the BCC accumulation. The first DLE of a DLE-DLE sequence is not included in the BCC accumulation and is discarded. The BCC is checked after receipt of an ITB, ETB, or ETX in non-transparent mode or DLE-ITB, DLE-ETB, DLE-ETX in transparent mode. If a CRC error is detected, the C/PERR and EOF bits in the RSR are set to 1. If no error

is detected only the EOF bit is set. If the closing character was an ITB, BCC accumulation and character assembly starts again on the first character following the BCC.

BSC Transmitter Operation

BSC transmission begins with the sending of an opening pad (PAD) and two sync (SYN) characters. These characters are programmable and stored in AR1(PAD) and AR2(SYN). SOH or STX initiates the block-check-character (BCC) accumulation. An initial SOH or STX is not included in the BCC accumulation. Should an underrun condition occur, the content of AR2 (normally SYN character) is transmitted until new characters become available. The message is terminated by the transmission of the BCC followed by a closing pad when an ETB, ITB, or ETX is fetched from the Tx FIFO. The closing PAD is generated by the MPCC.

In transparent mode, the BCC accumulation is initiated by DLE-STX and is terminated by the sequences DLE-ETX, DLE-ETB, or DLE-ITB. See Table 5 for character sequence and inclusion in CRC accumulation. If an underrun occurs, DLE-SYN characters will be transmitted until new characters are available in the Tx FIFO, ETC, ETX, ITB, or ENQ with a TLAST tag is treated as a control character and the MPCC automatically inserts a DLE immediately preceding these characters, DLE-ETB, DLE-ETX, DLE-ITB, or DLE-ENQ terminates a block of transparent text, and returns the data link to normal mode. BCC generation is not used for messages beginning with characters other than SOH, STX, DLE-SOH, or DLE-STX. On all message types, if the TSYN bit is set to 1 in the TCR, a SYN-SYN (DLE-SYN sequence on transparent messages) sequence is transmitted before the next character is fetched from the Tx FIFO.

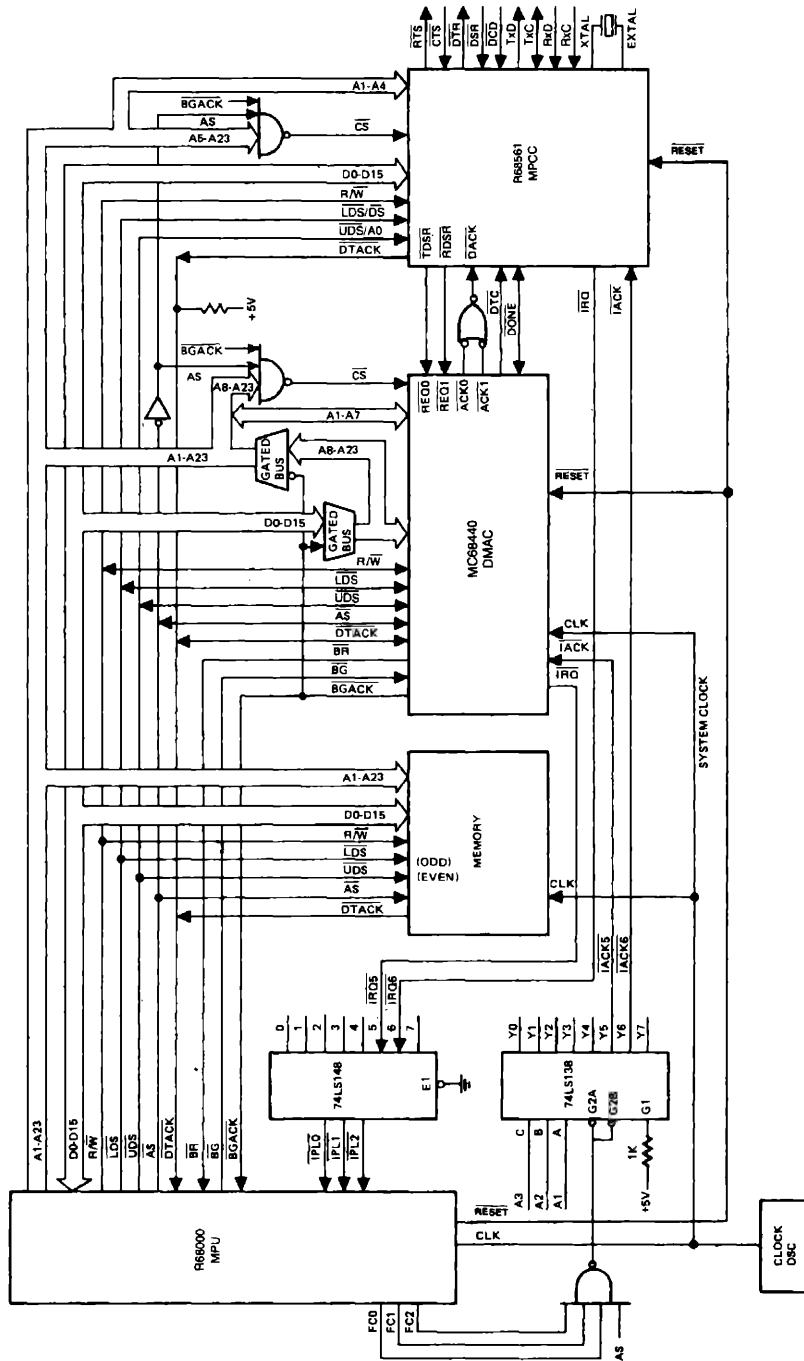
CHARACTER ORIENTED PROTOCOLS

The character oriented protocol (COP) option uses the format shown in Figure 9. It may be used for various character oriented protocols with 5-8 bit character sizes and optional parity checking. The input data is checked on a bit-by-bit basis for a pair of consecutive SYN characters to establish character synchronization. These SYN characters are discarded after detection. The PAD and SYN characters may be 5-8 bits long and are user programmable as stored in AR1 and AR2, respectively.

If parity checking is enabled the characters assembled after character sync are checked for parity errors. If STRSYN is set in the RCR, all SYN characters detected within the message will be discarded and will not be passed on to the Rx FIFO. If STRSYN is reset, SYNs detected within the message will be treated as data.



Figure 9. Character Oriented Protocol Format



NOTE: UDS MAY BE TIED LOW (GROUND).

Figure 10. Typical Interface to 68000-Based System

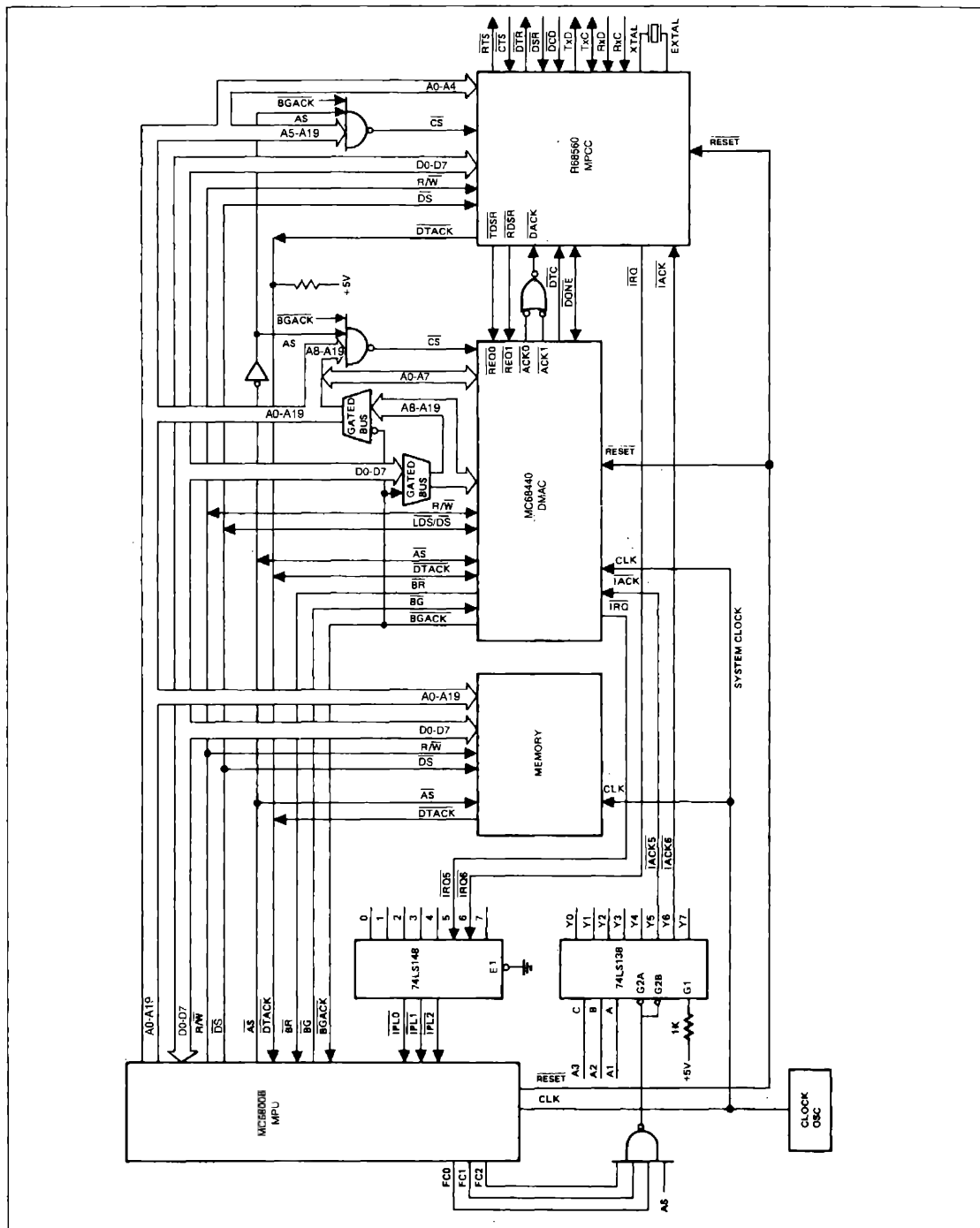
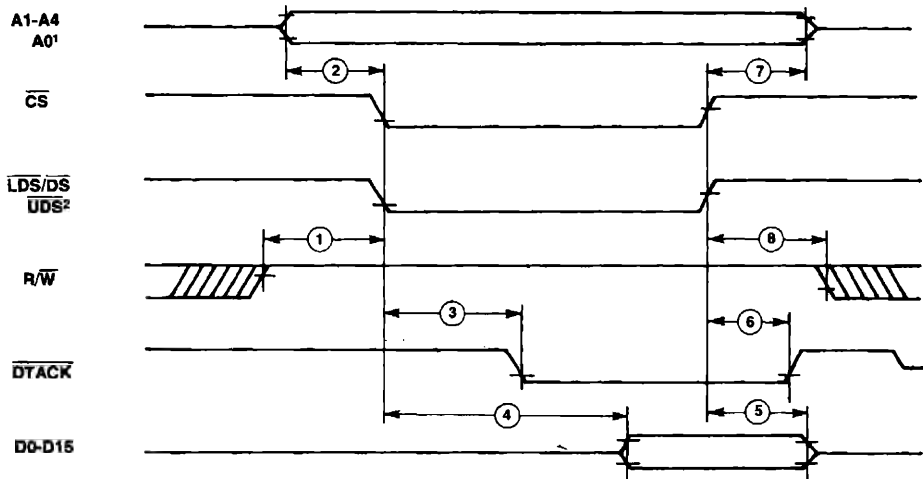


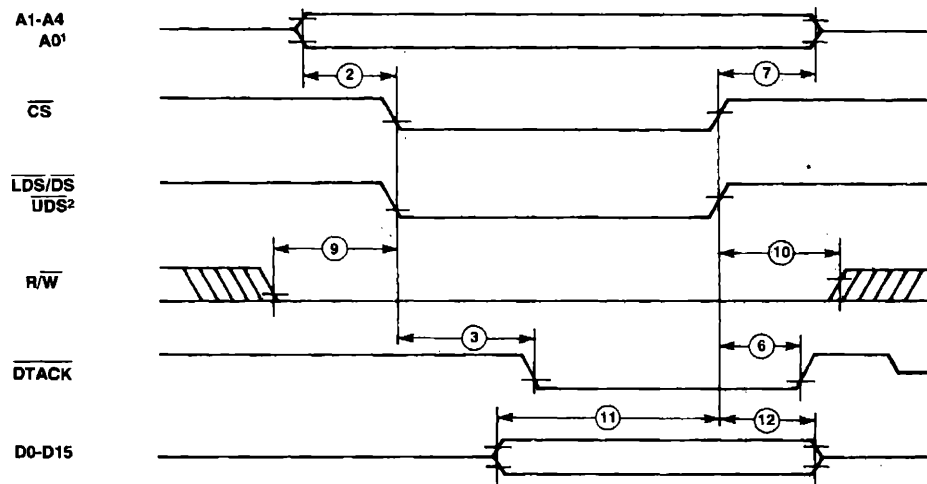
Figure 11. Typical Interface to 68008-Based System



NOTES:

1. BYTE MODE WHEN CONNECTED TO A0 ON 68008 BUS.
2. WORD MODE WHEN CONNECTED TO UDS ON 68000 BUS.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 12. MPCC Read Cycle Timing



NOTES:

1. BYTE MODE WHEN CONNECTED TO A0 ON 68008 BUS.
2. WORD MODE WHEN CONNECTED TO UDS ON 68000 BUS.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 13. MPCC Write Cycle Timing

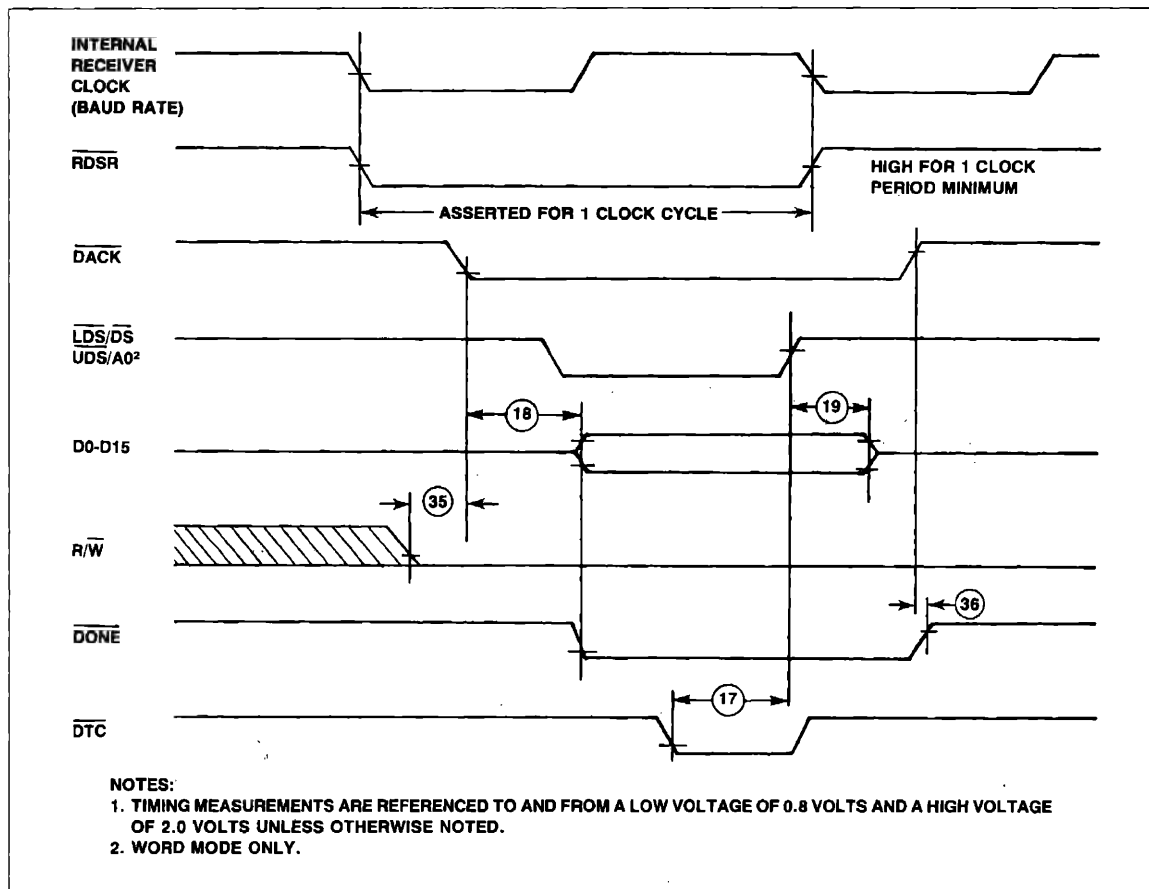


Figure 14. MPCC to Memory DMA Transfer Cycle Timing (Receiver DMA Mode)

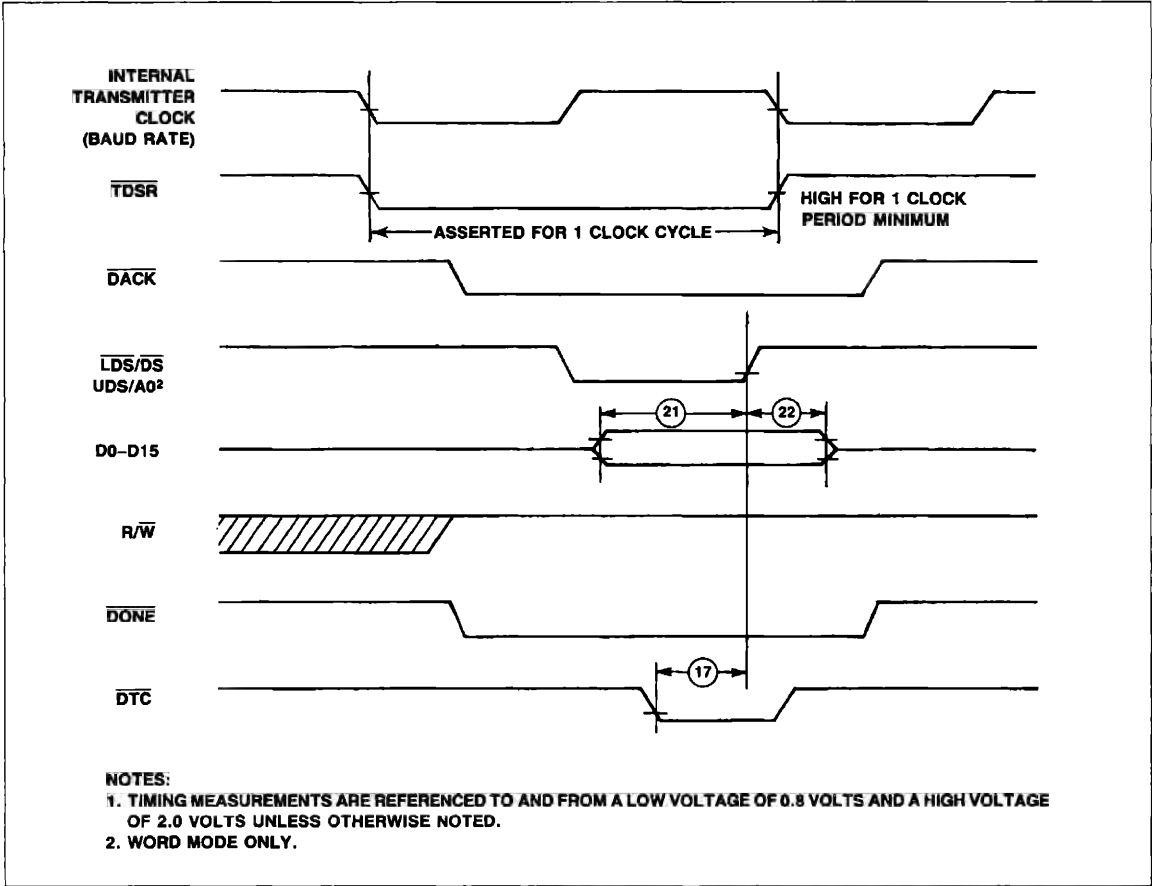
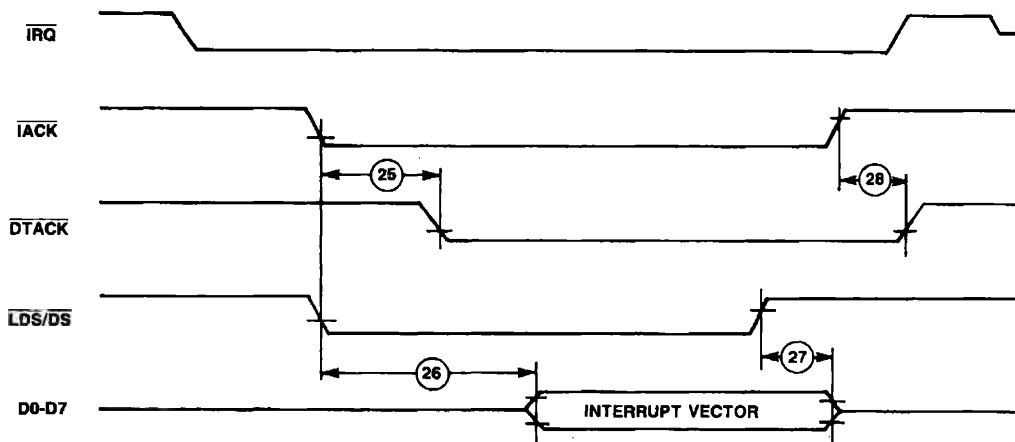


Figure 15. Memory to MPCC DMA Transfer Cycle Timing (Transmitter DMA Mode)

**NOTES:**

1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
2. $\overline{\text{IRQ}}$ IS NEGATED WHEN ALL BITS IN STATUS REGISTERS THAT COULD HAVE CAUSED THE INTERRUPT ARE CLEARED.

Figure 16. Interrupt Request Cycle Timing

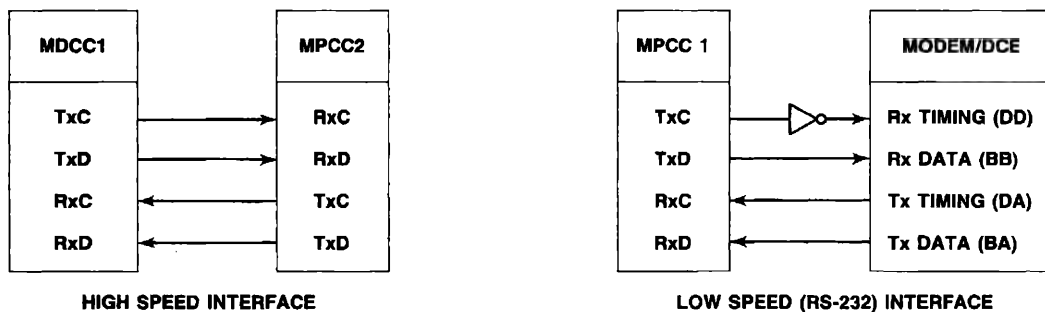
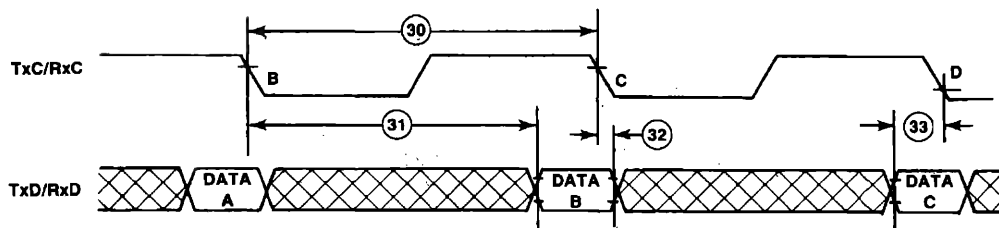


Figure 17. Serial Interface

HIGH SPEED APPLICATION



LOW SPEED APPLICATION (RS-232 COMPATIBLE)

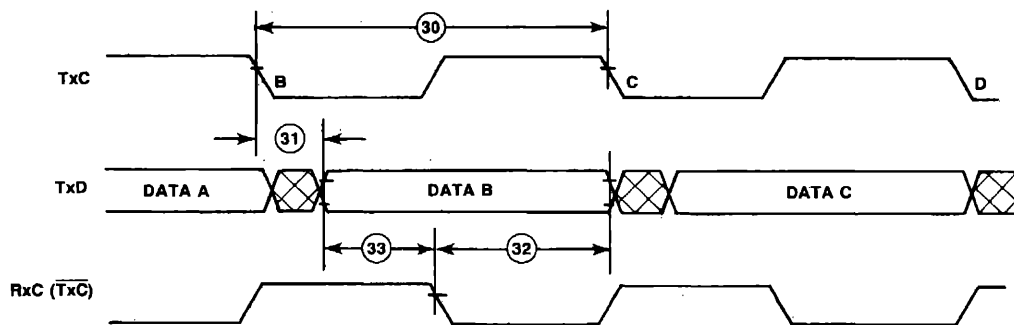
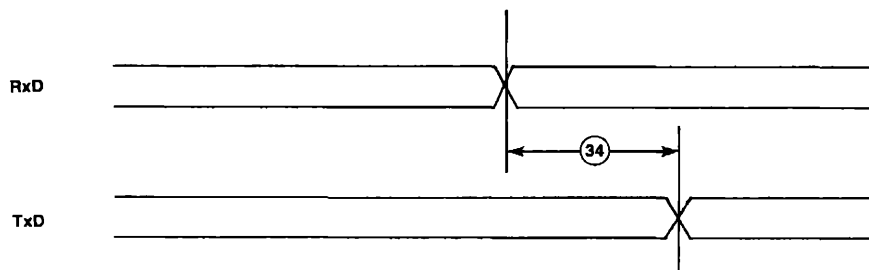


Figure 18. Serial Interface Timing



NOTE:

TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 19. Serial Interface Echo Mode Timing

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Number	Parameter	Symbol	Min	Max	Unit
1	R/W High to \overline{CS} , \overline{DS} Low	t_{RHSL}	0	—	ns
2	Address Valid to \overline{CS} , \overline{DS} Low	t_{AVSL}	30	—	ns
3 ⁽¹⁾	\overline{CS} Low to \overline{DTACK} Low	t_{CLDAL}	0	60	ns
4 ⁽¹⁾	\overline{CS} , \overline{DS} Low to Data Valid	t_{SLDV}	0	140	ns
5	\overline{CS} , \overline{DS} High to Data Invalid	t_{SHDXR}	10	150	ns
6	\overline{CS} , \overline{DS} High to \overline{DTACK} High	t_{SHDAT}	0	40	ns
7	\overline{CS} , \overline{DS} High to Address Invalid	t_{SHAI}	20	—	ns
8	\overline{CS} , \overline{DS} High to R/W Low	t_{SHRL}	20	—	ns
9	R/W Low to \overline{CS} , \overline{DS} Low	t_{RLSL}	0	—	ns
10	\overline{CS} High, \overline{DS} High to R/W High	t_{SHRH}	20	—	ns
11	Data Valid to \overline{CS} , \overline{DS} High	t_{DVSH}	60	—	ns
12	\overline{CS} , \overline{DS} High to Data Invalid	t_{SHDXW}	0	—	ns
17	\overline{DTC} Low to \overline{DS} High	t_{CLSH}	60	—	ns
18	\overline{DACK} Low to Data Valid, \overline{DONE} Low	t_{ALDV}	0	140	ns
19	\overline{DS} High to Data Invalid	t_{SHDXDR}	10	150	ns
21	Data Valid to \overline{DS} High	t_{DVSH}	60	—	ns
22	\overline{DS} High to Data Invalid	t_{SHDXDW}	0	—	ns
25	\overline{IACK} Low to \overline{DTACK} Low	t_{IALAL}	0	40	ns
26	\overline{IACK} , \overline{DS} Low to Data Valid	t_{IALDV}	0	140	ns
27	\overline{DS} High to Data Invalid	t_{SHDI}	10	150	ns
28	\overline{IACK} High to \overline{DTACK} High	$t_{IAHDTAT}$	0	40	ns
30	RxC and Tx C Period	t_{CP}	248	—	ns
31	TxC Low to Tx D Delay	t_{TCLTD}	0	200	ns
32	RxC Low to Rx D Transition (Hold)	t_{RCLRD}	0	—	ns
33	RxD Transition to Rx C Low (Setup)	t_{RDRCL}	30	—	ns
34	RxD to Tx D Delay (Echo Mode)	t_{RDTD}	—	200	ns
35	R/W Low to \overline{DTACK} Low (Setup)	t_{RLAL}	0	—	ns
36	\overline{DACK} High to \overline{DONE} High	t_{AHDH}	0	—	ns

Note:

- For read cycle timing, the MPCC asserts \overline{DTACK} within the MPU S4 clock low setup time requirement and establishes valid data (Data In) within the MPU S6 clock low setup time requirement.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Rating
Thermal Resistance Ceramic	θ_{JA}	50	°C/W
Plastic		68	

OPERATING CONDITIONS

Parameter	Range
V_{CC} Power Supply	5.0V $\pm 5\%$
Operating Temperature	0°C to 70°C

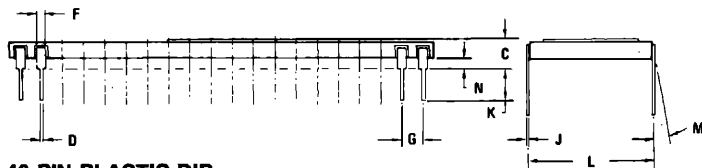
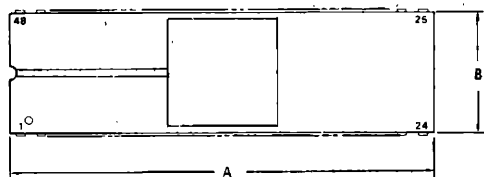
DC CHARACTERISTICS

($V_{CC} = 5.0 \text{ Vdc} \pm 5\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = 0^\circ\text{C}$ to 70°C unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input High Voltage All Inputs	V_{IH}	2.0	V_{CC}	V	
Input Low Voltage All Inputs	V_{IL}	-0.3	+0.8	V	
Input Leakage Current ($V_{IN} = 0$ to 5.25V) $\overline{R}/\overline{W}$, $\overline{\text{RESET}}$, $\overline{\text{CS}}$	I_{IN}	—	10.0	μA	$V_{IN} = 0$ to 5.25V $V_{CC} = 0$
Three-State (Off State) Input Current ($V_{IN} = 0.4$ to 2.4) $\overline{\text{IRQ}}$, $\overline{\text{DTACK}}$, $\overline{\text{D0-D15}}$	T_{ISI}	—	10.0	μA	$V_{IN} = 0.4$ to 2.4V $V_{CC} = 5.0\text{V}$
Output High Voltage $\overline{\text{RDSR}}$, $\overline{\text{TDSR}}$, $\overline{\text{IRQ}}$, $\overline{\text{DTACK}}$, $\overline{\text{D0-D15}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RTS}}$, TxD , TxC	V_{OH}	$V_{SS} + 2.4$	—	V	$V_{CC} = 4.75\text{V}$ $I_{LOAD} = -400\mu\text{A}$ $C_{LOAD} = 130 \text{ pF}$
$\overline{\text{BCLK}}$	V_{OH}	$V_{SS} + 2.4$	—	V	$V_{CC} = 4.75\text{V}$ $I_{LOAD} = 0$ $C_{LOAD} = 30 \text{ pF}$
Output Low Voltage $\overline{\text{RDSR}}$, $\overline{\text{TDSR}}$, $\overline{\text{IRQ}}$, $\overline{\text{DTACK}}$, $\overline{\text{D0-D15}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RTS}}$, TxD , TxC , $\overline{\text{BCLK}}$	V_{OL}	—	0.5	V	$V_{CC} = 4.75\text{V}$ $I_{LOAD} = 3.2 \text{ mA}$
$\overline{\text{DONE}}$					$V_{CC} = 4.75\text{V}$ $I_{LOAD} = 8.8 \text{ mA}$
Internal Power Dissipation	P_{INT}	—	1	W	$T_A = 25^\circ\text{C}$
Input Capacitance	C_{IN}	—	13	pF	$V_{IN} = 0\text{V}$ $T_A = 25^\circ\text{C}$ $f = 1 \text{ MHz}$

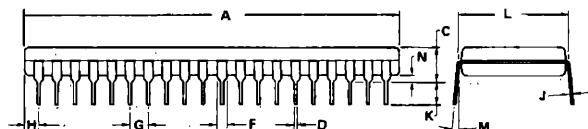
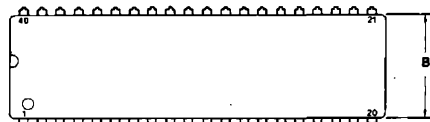
PACKAGE DIMENSIONS

48-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	60.35	61.57	2.376	2.424
B	14.63	15.34	0.576	0.604
C	3.05	4.32	0.120	0.160
D	0.381	0.533	0.015	0.021
E	0.762	1.397	0.030	0.055
F	2.54 BSC		0.100 BSC	
G	0.203	0.330	0.008	0.013
H	2.54	4.18	0.100	0.165
I	14.99	15.65	0.590	0.616
J	0"	10"	0"	10"
K	1.018	1.524	0.040	0.606

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
E	1.02	1.52	0.040	0.060
F	2.54 BSC		0.100 BSC	
G	1.65	2.16	0.065	0.085
H	0.20	0.30	0.008	0.012
I	3.05	3.56	0.120	0.140
J	15.24 BSC		0.600 BSC	
K	7"	10"	7"	10"
L	0.51	1.02	0.020	0.040



R68802 LOCAL NETWORK CONTROLLER (LNET)

1

PRELIMINARY

DESCRIPTION

The R68802^{*} Local Network Controller (LNET) implements the IEEE 802.3 CSMA/CD Access Method local network standard. More generally, it is designed to support a variety of local network designs with varying performance requirements.

The basic function of the LNET is to execute the CSMA/CD algorithm, perform parallel-to-serial and serial-to-parallel conversions of the 10M bps packet data stream, and assemble and disassemble the packet format. In addition, the LNET provides the necessary asynchronous handshake signals to the 68000 family processors, the required DMA interfaces, and the proper interface to the Manchester Interface (MI) component(s) used to connect the LNET to an IEEE 802.3 defined Media Attachment Unit (MAU).

The controller can interface data terminal equipment to local networks with differing performance requirements. At the high end, the R68802 meets the IEEE 802.3 10M bps specification and supports the implementation of ISO layers one and two. For low cost networks, the controller can be run at greatly reduced data rates and inexpensive system components (drivers, cables, etc.) may be selected.

The LNET controller implements a protocol known as Carrier Sense Multiple Access with Collision Detection (CSMA/CD), which allows multiple Data Terminal Equipment to share the same communication medium without the need for a central arbiter of medium utilization.

Ethernet nodes needing to transmit wait exactly 9.6 μ s before transmitting data to provide recovery time for other controllers and the cable itself. If a collision with another station is detected, the transmission is aborted and a jam signal transmitted to alert other nodes. Following a jam, the station waits a random amount of time based on a Binary Exponential Back-off algorithm before retransmitting. Repeated collisions result in repeated retries and an increase in the randomly selected time interval to improve trafficking.

ORDERING INFORMATION

Part Number

R68802 _ Temperature Range: 0°C to 70°C

Package:

C = Ceramic
P = Plastic

FEATURES

- Serial data rates as high as 10M bps
- Compatible with a variety of 8- or 16-bit processors and DMA controllers
- Meets the IEEE 802.3 (as well as Ethernet^{*}) specifications for local networks
- Interfaces to SEEQ 8002 Manchester Code Converter (MCC)
- Programmable interframe wait times for smaller topologies and lower data rates
- CSMA/CD algorithm:
 - Wait before transmit
 - Jam on collision
 - Binary exponential backoff
- Programmable 2- or 6-byte address recognition
- Supports three modes of node self-test
- Programmable disable on reception
- 32-bit CRC generation and reception
- Broadband applications
- TTL compatible I/O
- 40-pin DIP
- Single 5V power supply

^{*}R68802 is a trademark of the Rockwell International Corporation.

^{*}Ethernet is a trademark of the Xerox Corporation.

VCC	1	40	MAUREQ
R/W	2	39	MAUAVAIL
RESET	3	38	ISOLATE
D0	4	37	TXCLK
D1	5	36	TXDATA
D2	6	35	TXEN
D3	7	34	SIGQUAL
D4	8	33	SENSE
D5	9	32	RXCLK
D6	10	31	RXDATA
D7	11	30	MILLOOP
D8	12	29	TXREQ
D9	13	28	RXREQ
D10	14	27	DACK
D11	15	26	DONE
D12	16	25	IRQ
D13	17	24	DTACK
D14	18	23	DS
D15	19	22	IACK
CS	20	21	GND

R68802 Pin Assignments

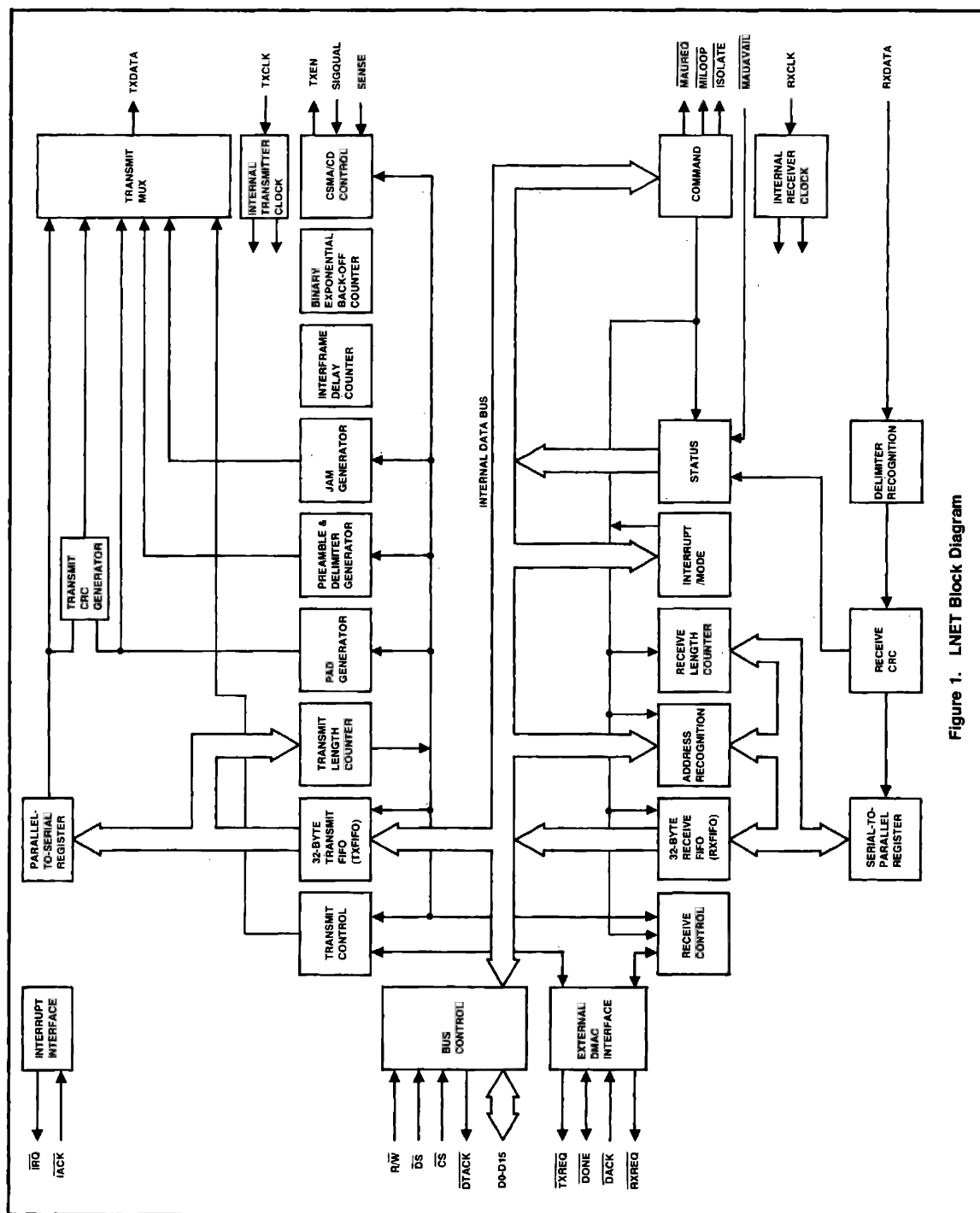


Figure 1. LNET Block Diagram

PIN DESCRIPTION

Throughout the document, signals are presented using the terms active and inactive or asserted and negated independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar. R/W indicates a write is active low and a read active high.

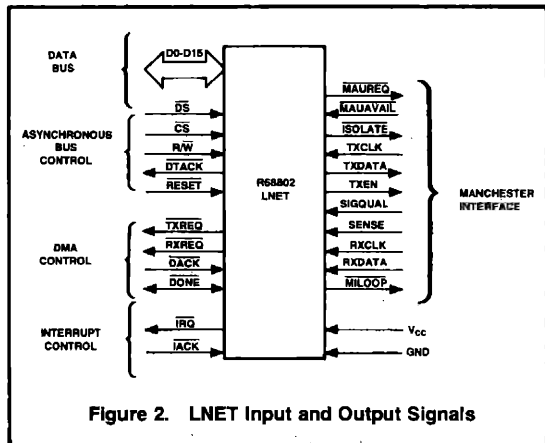


Figure 2. LNET Input and Output Signals

D0-D15—Data Lines. The bidirectional data lines transfer data between the LNET and the MPU, memory or other peripheral device. D0-D15 are used when connected to the 16-bit 68000 bus and operating in the word mode. D0-D7 are used when connected to the 16-bit 68000 bus or the 8-bit 68008 bus and operating in the byte mode. The data bus is tri-stated when \overline{CS} is inactive. (See exceptions in DMA mode.)

\overline{CS} —Chip Select. \overline{CS} low selects the LNET for programmed transfers with the host. The LNET is deselected when the \overline{CS} input is inactive in non-DMA mode. \overline{CS} must be decoded from the address bus and gated with address strobe (\overline{AS}).

R/W—Read/Write. R/W controls the direction of data flow through the bidirectional data bus by indicating that the current bus cycle is a read (high) or write (low) cycle.

\overline{DTACK} —Data Transfer Acknowledge. \overline{DTACK} is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, \overline{DTACK} is asserted by the LNET after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. A pull up resistor is required to maintain \overline{DTACK} high between bus cycles.

\overline{DS} —Data Strobe. During a write (R/W low), the \overline{DS} positive transition latches data from the external data bus lines into the LNET. During a read (R/W high), \overline{DS} low enables data from the LNET onto data bus lines.

\overline{IRQ} —Interrupt Request. The active low \overline{IRQ} output requests interrupt service by the MPU.

\overline{IACK} —Interrupt Acknowledge. The active low \overline{IACK} input indicates that the current bus cycle is an interrupt acknowledge cycle. When \overline{IACK} is asserted the LNET places an interrupt vector on the lower byte (D0-D7) of the data bus.

\overline{DACK} —DMA Acknowledge. The \overline{DACK} low input indicates that the data bus has been acquired by the DMAC and that the requested bus cycle is beginning.

\overline{DONE} —Done. \overline{DONE} is a bidirectional active low signal. The \overline{DONE} signal is asserted by the DMAC when the DMA transfer count is exhausted and there is no more data to be transferred, or is asserted by the LNET when either the last byte of receive data is transferred or a collision is detected during a transmission.

\overline{RESET} —Reset. The active low, high impedance \overline{RESET} input initializes all LNET functions. \overline{RESET} must be asserted for at least 500 TXCLKs to initialize the LNET.

\overline{RXREQ} —Receive DMA Request. When receive data becomes available in the RXFIFO, \overline{RXREQ} output is asserted and held low for 16 (single address burst mode) DMAC cycles (16 sequential \overline{DACK} pulses) or until the end of the receive block. When the last data byte of the receive block is transferred, \overline{DONE} is asserted by the LNET with the last \overline{DACK} strobe and the negation of \overline{RXREQ} .

\overline{TXREQ} —Transmit DMA Request. When the Transmitter Enable bit is set in Command Register 1, \overline{TXREQ} output is asserted and held low for 16 (single address burst mode) DMAC cycles (16 sequential \overline{DACK} pulses) or until the end of the transmit data block as signaled by the DMAC's assertion of \overline{DONE} .

\overline{MILOOP} —MI Loopback. With an active \overline{MILOOP} output, the MI shunts its LNET data-in path to its LNET data-out path, effectively routing the LNET TXDATA output into the LNET RXDATA input.

\overline{RXDATA} —Receive Data. The LNET receives serial data via the RXDATA input. The RXDATA input is shifted into the receiver on the positive going edge of RXCLK.

\overline{RXCLK} —Receive Clock. The free-running Receive Clock provides the LNET with received data timing information. The positive (low-to-high) clock transition enables an RXDATA bit into the LNET.

\overline{SENSE} —Carrier Sense. The active high \overline{SENSE} input indicates the presence of data on the RXDATA serial input line.

$\overline{SIGQUAL}$ —Signal Quality. The assertion of the active high $\overline{SIGQUAL}$ input by the MI indicates an error condition on the medium. During the transmission mode the LNET interprets this as a collision.

\overline{TXEN} —Transmit Enable. The active high TXEN output indicates to the MI that data is present on the TXDATA output.

TXDATA—Transmit Data. The LNET transmits serial data on the TXDATA line. The TXDATA output changes on the positive going edge of TXCLK.

TXCLK—Transmit Clock. The Transmit Clock input is a free-running clock supplied by the MI that provides both a system clock and a means of shifting out serial data bit on the TXDATA output line.

ISOLATE—Isolate MAU. The active low $\overline{\text{ISOLATE}}$ output is asserted when the Isolate bit in Command Register 1 is set to 1 to isolate the MAU from the medium. As long as $\overline{\text{ISOLATE}}$ is low, the MAU is unable to transmit or receive on the medium.

MAUAVAIL—MAU Available. When the active low $\overline{\text{MAUAVAIL}}$ input is asserted, the transmission algorithm can proceed.

MAUREQ—MAU Request. The active low $\overline{\text{MAUREQ}}$ output is asserted prior to transmission if $\overline{\text{MAUAVAIL}}$ is not asserted.

V_{CC}—Power. 5 V \pm 5%.

GND—Ground. Ground.

LNET REGISTERS

The LNET contains three groups of registers accessible from the MPU bus which initialize the LNET, control and monitor LNET operation, and transfer data between the LNET and the MPU bus. These register groups, specific registers within each group, and the size, access and mode of each register are listed in Table 1.

All registers, except the Mode Register, may be accessed either in the word or byte mode, depending on the MPU data bus length (8-bit or 16-bit) and the Word/Byte mode selected in bit 4 of the Mode Register during initialization. In the word mode, two registers are read or written during one cycle with the least significant byte (D0-D7) accessed first.

INITIALIZATION REGISTERS

The initialization registers contain command information to configure the LNET for normal operation. The registers are the one-byte Mode Register (MR), the one-byte Interrupt Vector Number Register (IVNR) and the two- or six-byte Station Address Register (SAR). These registers must be loaded upon RESET (either caused by power up or initiated during normal operation) or upon setting of the RESET bit in Command Register 1. Any of these conditions reset the LNET by clearing the Mode Register, Station Address Register, Command Registers and Status Registers. The Interrupt Vector Number Register is auto-initialized to its default value of \$0F.

All initialization registers must be written to by the MPU instruction sequence immediately after a reset in the manner described below even if no data is changed in a register. The number of bytes written depends upon the number of bytes in the Station Address as selected in bit 4 of the Mode Register.

After the proper number of write cycles have been completed, the LNET Initialized bit in Status Register 1 is set and further MPU writes to the LNET will address only Command Register 1 or Command Register 2. All MPU reads of the LNET after initialization is complete will access only Status Register 1 or Status Register 2.

Initialization Procedure for 16-Bit MPU Bus

Write cycle 1—write the Mode byte on the lower byte of the data bus D0-D7. The upper byte is not used and can contain any data.

Write cycle 2—write the Interrupt Vector Number on the lower byte of the data bus D0-D7. The upper byte is not used and can contain any data.

Write cycle 3 or write cycles 3 through 5—write the one- or three-word Station Address (depending on the Station Address Size loaded into the Mode Register), least significant words first.

Table 1. LNET MPU Bus Accessible Registers

Register Group	Register Name	Size (No. Bytes)	Access	Reset Value	Mode
Initialization Registers	Mode Register (MR)	1	$\overline{\text{CS}} = \text{L}, \text{R}/\overline{\text{W}} = \text{L}$ (write one byte ¹)	\$00	MPU Write
	Interrupt Vector Number Register (IVNR)	1	$\overline{\text{CS}} = \text{L}, \text{R}/\overline{\text{W}} = \text{L}$ (write one byte ²)	\$0F	
	Station Address Register (SAR)	2 or 6	$\overline{\text{CS}} = \text{L}, \text{R}/\overline{\text{W}} = \text{L}$ (write 1 or 3 sequential words or 2 or 6 sequential bytes)	\$00	
Operating Registers	Command Register 1 (CR1)	1	$\overline{\text{CS}} = \text{L}, \text{R}/\overline{\text{W}} = \text{L}$	\$00	MPU Write
	Command Register 2 (CR2)	1			
	Status Register 1 (SR1) Status Register 2 (SR2)	1 1	$\overline{\text{CS}} = \text{L}, \text{R}/\overline{\text{W}} = \text{H}$	\$00	MPU Read
Data Buffers	Transmit FIFO Register File (TXFIFO)	32	$\overline{\text{TXREQ}} = \text{L}$	\$XX	DMA Write
	Receive FIFO Register File (RXFIFO)	32	$\overline{\text{RXREQ}} = \text{L}$	\$XX	DMA Read

Notes:

1. Second byte of word ignored.

2. Second byte in word mode ignored.

Initialization Procedure for 8-Bit MPU Bus

Write cycle 1—write the Mode byte on the data bus.

Write cycle 2—write the Interrupt Vector Number on the data bus.

Write cycles 3 through 4 or 3 through 8—write the two- or six-byte Station Address (depending on the Station Address Size loaded into the Mode Register), least significant bytes first.

Mode Register (MR)

7	6	5	4	3	2	1	0
IFWT		BYTE		INTCOL	DISRX	NOLC	SAS

The Mode Register sets conditions during initialization for use during normal operations. It must be the first byte written during initialization. All mode bits are active high, i.e., = 1. All bits are cleared upon RESET or setting the RESET bit to 1 in Command Register 1.

MR IFWT —Interframe Wait Time**7-5 No. of TXCLKs**

000	16
001	32
010	48
011	64
100	80
101	96
110	112
111	128

MR**4 BYTE —Data Bus Byte Mode**

0	Select word mode (for use with 16-bit MPU bus).
1	Select byte mode (for use with 8-bit MPU bus).

MR**3 INTCOL —Interrupt on Collision**

0	Assert only DONE on collision.
1	Assert IRQ and DONE on collision.

MR**2 DISRX —Disable Receiver**

0	Enable receiver after each packet reception.
1	Disable receiver after each packet reception.

MR**1 NOLC —No Length Count**

0	Use length count in packet format.
1	Do not use length count in packet format.

MR**0 SAS —Station Address Size**

0	6-byte station address.
1	2-byte station address.

Interrupt Vector Number Register (IVNR)

7	6	5	4	3	2	1	0
Interrupt Vector Number (IVN)							

If an interrupt condition occurs (as reported by bits in Status Register 1 and Status Register 2), IRQ is asserted to request MPU interrupt service. Upon IACK input assertion, the Interrupt Vector Number (IVN) from the Interrupt Vector Number Register (IVNR) is placed on the data bus (D0-D7). The IVN must be the second byte initialized during LNET initialization. The IVN is set to \$0F upon RESET or setting the RESET bit to 1 in Command Register 1.

Station Address Register (SAR)

7	6	5	4	3	2	1	0
Station Address							

The Station Address Register holds the Station Address for the Receiver Address Recognition circuitry. The Station Address bytes must be written to the LNET following the Interrupt Vector Number during the initialization sequence. Either two or six bytes must be written, least significant bytes first, depending on the Station Address Size loaded into the Mode Register.

OPERATING REGISTERS

The command or status registers are addressed during an MPU write or read, respectively, after initialization is complete as indicated by the LNET Initialized bit in Status Register 1. In word mode, both command registers are written during one write cycle. Command Register 1 occupies the lower byte of the word. Likewise, while reading the status registers in word mode, Status Register 1 occupies the lower byte of the word.

COMMAND REGISTERS**Command Register 1 (CR1)**

Command Register 1 controls the operation of the LNET. All command bits are active high (i.e., = 1).

7	6	5	4	3	2	1	0
RESET	ENRX	RECALL	NOISOL	MILOOP	INLOOP	ODDND	ENMAU

CR1**7 RESET —Reset**

0	Enable LNET operation.
1	Reset LNET.

Note: The RESET bit is automatically cleared to 0 upon the completion of the reset sequence. This bit is unaffected by the RESET pin level.

CR1

6 ENRX —Enable Receiver after Packet Reception

- 0 Disable receiver after packet reception.
 1 Enable receiver after packet reception. This bit must be set after each packet is received to enable reception of the next packet only if bit 2 in the Mode Register is set at initialization. Reception of the packet clears this bit.

Note: This bit is not used if bit 2 in the Mode Register is not set at initialization.

CR1

5 RECALL—Receive All Packets

- 0 Receive only addressed packets. The address must correspond to the Station Address loaded into the Station Address Register upon initialization.
 1 Receive all packets (regardless of address).

CR1

4 NOISOL—No Isolate

- 0 Assert ISOLATE to the MI to request that the MAU isolate itself from the medium.
 1 Negate ISOLATE to the MI to request that the MAU connect itself to the medium.

CR1

3 MILOOP—Manchester Interface Loopback Test

- 0 Negate MILOOP to command MI normal operation.
 1 Assert MILOOP to command MI loopback operation.

CR1

2 INLOOP—Internal LNET Loopback Test

- 0 Enable LNET normal operation.
 1 Enable LNET internal loopback operation.

CR1

1 ODDNO—Odd Number of Bytes

- 0 Transmit even number of bytes in a block.
 1 Transmit odd number of bytes in a block.

CR1

0 ENMAU—Enable MAUREQ

- 0 Negate MAUREQ.
 1 Assert MAUREQ.

Command Register 2 (CR2)

7	6	5	4	3	2	1	0
Reserved for future use							

This register not presently in use. When programming, \$00 should be written to CR2 to assure future software compatibility. In byte mode, \$00 must be written to this register following the Command Register 1 write cycle.

STATUS REGISTERS

The two interrupt driven status registers report the status of the LNET receiver and transmitter operations. Status registers cannot be polled, they can *only* be read upon interrupt service by the MPU. Status is reported in either discrete or encoded bits. All discrete (or non-encoded) status bits are active high (i.e., = 1).

A change in any of these status bits causes IRQ to be asserted (except as noted). Reading of the status registers resets the individual bit or encoded field that caused the IRQ assertion and negates IRQ (except as noted). In the byte mode, both status registers must be read in consecutive read cycles.

Status Register 1 (SR1)

7	6	5	4	3	2	1	0
HRTBT	TXSTAT			ODD	RXSTAT		

SR1

7 HRTBT —Heartbeat Absent

- 0 Heartbeat present.
 1 Heartbeat absent (part of the transmission algorithm is to listen for the heartbeat before posting transmit status. Set concurrent with the transmitter status field.). The Heartbeat test checks the collision detection circuitry by listening for a "ping" within seven TXCLKs after the end of a transmission).

SR1

6-4 TXSTAT —Transmitter Status

- 000 Transmitter idle.
 001 Transmit successful.
 010 Collision (Assertion of SIGQUAL within the first 512 bit times causes DONE, or DONE and IRQ, to be asserted depending on the state of MR bit 3).
 011 Signal Quality error (SIGQUAL asserted after the first 512 bit times).
 100 Transmit retry count exceeded.
 101 Transmit buffer underflow during transmission (indicates the TXFIFO emptied between the 16th data byte delivered for transmission and the assertion of DONE).
 110 Transmit in progress (indicates the real time activity of the TXDATA pin. This state does not set the IRQ bit in SR2 nor cause IRQ to be asserted. This bit pattern is not reset to the transmitter idle pattern upon reading SR1).
 111 MAUAVAIL changed state during transmission.

SR1

3 ODD —Odd Number of Receive Bytes

- 0 Even number of bytes in the receive packet.
 1 Odd number of bytes in the receive packet.

SR1

2-0 RXSTAT —Receiver Status

- 000 Receiver idle.
 001 Receive successful.
 010 Minimum packet size error.
 011 Receive buffer overflow.
 100 Frame terminated on a non-byte boundary error.
 101 Frame Check Sequence (FCS) error.
 110 Receive in progress (indicates a valid address has been recognized and DONE has not been asserted. This state does not set the IRQ bit in SR2 nor cause IRQ to be asserted. This bit pattern is not reset to the receiver idle pattern upon reading SR1).
 111 Reserved

Status Register 2 (SR2)

7	6	5	4	3	2	1	0
IRQ	0	INIT	MAUAVAIL				COLCNT

SR2

7 IRQ —Interrupt Request

- 0 An interrupt condition has not occurred and $\overline{\text{IRQ}}$ has not been asserted.
- 1 An interrupt condition has occurred and $\overline{\text{IRQ}}$ has been asserted.

Note: This bit is cleared when SR2 is read and there is no pending interrupt condition.

SR2

6 —Not used

- 0 Always reads zero.

SR2

5 INIT —LNET Initialized

- 0 LNET initialization not complete.
- 1 LNET initialization complete (set after the last station address byte has been written).

Note: This bit is cleared upon $\overline{\text{RESET}}$ or RESET bit set in Command Register 1.

SR2

4 MAUAVAIL—MAU Available

- 0 MAU is not available.
- 1 MAU is available.

Note: This bit is not cleared when SR2 is read.

SR2

3-0 COLCNT—Collision Count

- 0000 Zero
- ...
- 1111 Fifteen

Note: Reset to zero when the enable $\overline{\text{MAUREQ}}$ bit is set in CR1. If Mode Register bit 3 is negated the changing count does not generate IRQ interrupts.

TRANSMIT DATA BUFFER (TXFIFO)

The Transmit data buffer is a 32-byte FIFO register file (TXFIFO) which can be loaded only by DMA service. One half of the TXFIFO loads data for transmission via the DMAC; the other half holds data currently being transmitted out serially on TXDATA. When the transmitting half is empty it becomes the loading half and the current loading buffer becomes the transmitting half. If the transmitting buffer empties before the loading buffer is fully loaded, $\overline{\text{IRQ}}$ is asserted and the transmitter buffer underflow bit pattern (101) is set in Status Register 1.

The time required to load half the transmitter buffer under DMAC control must be less than the time it takes to serialize out the

transmitting half on TXDATA. From the assertion of $\overline{\text{TXREQ}}$ to the end of the 16th DMAC bus cycle, no more than 128 TXCLKs can elapse.

RECEIVE DATA BUFFER (RXFIFO)

The Receive data buffer is a 32-byte FIFO register file (RXFIFO) which can be read only during DMA service. One half of the RXFIFO is a receiving buffer for the data from the Serial-to-Parallel Register; the other half is a reading buffer for the data ready to be transferred to the MPU bus. As soon as the receiving buffer is full, these two halves switched roles. If the receiving buffer is fully loaded before the reading buffer is empty, $\overline{\text{IRQ}}$ is asserted and the receive buffer overflow bit pattern (011) is set in Status Register 1.

The time it takes to unload the reading buffer under DMAC control must be less than the time it takes to load the receiving buffer from RXDATA. The loading time is 128 RXCLKs.

INPUT/OUTPUT FUNCTIONS

In addition to being directly compatible with the 68000 and the 68008 MPU's, the LNET supports DMA transfers when used with the 68440, 68450, AMZ9516, or AMZ8016 DMA controller. The LNET also provides the necessary synchronous signals for interfacing to the Manchester Interface device.

MPU INTERFACE

Transfer of data between the LNET and the system bus involves the following signals: Data Bus D0 through D15 and control signals consisting of R/W, $\overline{\text{DTACK}}$, $\overline{\text{CS}}$, $\overline{\text{IACK}}$, and $\overline{\text{DS}}$.

16-Bit MPU Interface

When connecting the LNET to the 16-bit 68000 MPU data bus, the LNET $\overline{\text{DS}}$ input is connected to the bus $\overline{\text{DS}}$ line and the LNET D0-D15 data lines are connected to the bus D0-D15 data lines (see Figure 4).

Bit 4 in the Mode Register, left in its default value of 0 during initialization, selects the word mode. In the word mode, a read of both status registers performed with one word read cycle transfers Status Register 1 on D0-D7 and Status Register 2 on D8-D15. A write to the command registers is also accomplished in one cycle which transfers Command Register 1 on D0-D7 and Command Register 2 on D8-D15.

8-Bit MPU Interface

When connecting the LNET to the 8-bit 68008 MPU data bus, the $\overline{\text{DS}}$ input is connected to the bus $\overline{\text{DS}}$ line and the LNET D0-D7 data lines are connected to the bus D0-D7 data lines (see Figure 5).

Bit 4 of the Mode Register set to 1 during initialization selects byte mode. In the byte mode, reading of the status registers is performed with two consecutive byte read cycles to enable first Status Register 1 and then Status Register 2 onto D0-D7. Writing to the command registers also requires two consecutive byte write cycles with Command Register 1 transferred first followed by Command Register 2.

Read/Write Operation

The R/\overline{W} input controls the direction of data flow on the data bus. \overline{CS} (Chip Select) enables the LNET for access to the internal registers and other operations. When \overline{CS} is asserted the data I/O buffer acts as an output driver during a read operation, and as an input buffer during a write operation. \overline{CS} must be decoded from the address bus and gated with address strobe (\overline{AS}).

If the LNET is selected ($\overline{CS} = \text{low}$) for a read ($R/\overline{W} = \text{high}$), data is placed on the data bus from the status register when the \overline{DS} is asserted. The LNET asserts Data Transfer Acknowledge (\overline{DTACK}) concurrent with the output data.

If the LNET is selected ($\overline{CS} = \text{low}$) for a write ($R/\overline{W} = \text{low}$), \overline{DS} strobes data into the selected register and the LNET asserts \overline{DTACK} immediately after \overline{DS} is asserted.

DMA INTERFACE

During receiving or transmitting data from the MPU bus, the LNET asserts a receive or transmit request (\overline{RXREQ} or \overline{TXREQ}) to the DMAC. A DMA acknowledge (\overline{DACK}) signal is asserted in response to \overline{RXREQ} or \overline{TXREQ} when the DMAC is ready to service the request. Both receive request and transmit request share the same \overline{DACK} pin; therefore, in the case of DMAC devices with a \overline{DACK} for each channel, they must be ORed together externally.

Transmit DMA Request

In servicing the \overline{TXREQ} , the DMAC writes to the TXFIFO a byte or a word at a time. The TXFIFO input pointer (TIP) is advanced and data latches on the rising edge of \overline{DS} .

Receive DMA Request

In servicing the \overline{RXREQ} , the DMAC reads from the RXFIFO a byte or word at a time. Data is enabled out on the falling edge of \overline{DACK} and the RXFIFO output pointer (ROP) is advanced on the rising edge of \overline{DACK} . The data lines are tri-stated following the rising edge of \overline{DACK} .

DONE

\overline{DONE} is a bidirectional signal line to or from the DMAC. With the AMZ8016 and the AMZ9516, \overline{DONE} auto-initializes the DMAC back to the start of the packet when a collision occurs during transmission. With the 68440, the \overline{DONE} output is routed to the 68440's PCL input after gating with \overline{TXREQ} line. For the 68450 it is necessary for the MPU to reinitialize the DMAC on collision.

INTERRUPTS

The \overline{IRQ} output asserts when there is status information available after the completion of a transmit or receive transaction. The MPU grants the interrupt by asserting an interrupt acknowledge (\overline{IACK}) signal and reads the interrupt vector when the LNET asserts data transfer acknowledge (\overline{DTACK}). The subsequent negation of \overline{IACK} and \overline{IRQ} precede MPU interrupt processing.

MANCHESTER INTERFACE (MI) SIGNALS

The abbreviation MI refers to the Manchester Interface component(s) necessary to interface the LNET to an IEEE 802.3 specified Media Access Unit (MAU).

SENSE (Sense Carrier) Input

The MI asserts SENSE when it has detected a change in Carrier Sense from no carrier present to carrier present. SENSE stays active as long as carrier is present and is negated when the carrier disappears.

ISOLATE (Isolate Message Request) Output

The LNET asserts $\overline{ISOLATE}$ to direct the MI to send an Isolate message to the MAU. When $\overline{ISOLATE}$ is negated, the MI sends a Normal message to the MAU unless the LNET requires that the MAU request message be sent to permit data output.

MAUREQ (MAU Request) Output

The LNET asserts \overline{MAUREQ} when CR 1 bit 0 is active. \overline{MAUREQ} stays active and a MAU request message is sent until the end of a packet transmission.

MAUAVAIL (MAU Available) Input

The MI asserts $\overline{MAUAVAIL}$ when an MAU available message from the MAU is received. $\overline{MAUAVAIL}$ is negated when an MAU not available message is received from the MAU.

SIGQUAL (Signal Quality) Input

SIGQUAL is asserted by MI when a Signal Quality Error Message is received from the MAU.

TXEN (Transmission Enable) Output

The LNET starts a transmission by asserting TXEN and outputs serial data on TXDATA which is Manchester encoded by the MI. TXEN is active until the end of the transmission.

RXCLK (Receive Clock) Input

RXCLK shifts receive data into the LNET and is free running at 10 MHz, or slower.

TXCLK (Transmitter Clock) Input

The TXCLK is a free running 10 MHz, or slower, clock used to clock data into the MI and perform operations in the transmitter.

MILOOP (MI Loopback) Output

The \overline{MILOOP} output signals the MI component(s) that the current data is a test frame and it is to be "looped back" to the LNET instead of being sent to the MAU.

LNET FUNCTIONAL DESCRIPTION

The LNET transmits and receives serial data on an IEEE 802.3 CSMA/CD Access Method defined communications medium and transfers parallel data to and from a host system under program or DMA control according to the IEEE 802.3 data link specification.

Frame Format

Serial data transfers synchronously between the LNET and the MI within the frame structure for data communications using local area network media access control (MAC) procedures. Each MAC frame, or packet, consists of eight fields: Preamble, Start Field Delimiter (SFD), Destination Address, Source Address, Length Count, Data, Pad and Frame Check Sequence (FSC). Figure 3 illustrates the frame format.

The Preamble consists of seven bytes of alternating 1's and 0's, i.e., 1010 . . . 1010.

The Start Field Delimiter (SFD) consists of one byte of bit pattern 10101011 immediately following the Preamble pattern which indicates the start of a valid frame.

The Destination and Source Addresses are either two or six bytes in length. Addresses may be any one of the following three types: Station Address, Logical Group, or Broadcast. Logical Group and Broadcast Addresses are identified by a 1 in the first bit position received. The first bit of a Station Address is 0.

The Length Count field is two bytes in length and specifies the Data field length (in an Ethernet application this field is the Type field and the Length Count field in the Mode Register must be initialized appropriately).

The Data field can have a variable number of bytes. If the Data field is less than 46 bytes (in a six-byte address mode), or less than 54 (in a two-byte address mode), pad bytes are added to the frame on transmission to bring the overall packet size up to the minimum size of 72 bytes. The maximum Data field length must be programmed into the DMAC operating with the LNET.

The Frame Check Sequence (FCS) field is four bytes in length.

Frame Reception

The Receiver consists of the following sections: Delimiter Recognition, Receive CRC, Serial-to-Parallel Register, Receive Length Counter, Address Recognition, and a 32-byte FIFO register file (RXFIFO). These registers are all driven or loaded by RXCLK or a derivative.

In the absence of serial input data from the network bus, the SENSE input from the MI is inactive. The Receive Clock (RXCLK) is free running and the Receiver front end is idling.

The assertion of SENSE defines the beginning of a frame. The rising edge of RXCLK enables SENSE and concurrently the first Preamble bit on RXDATA to the LNET. The falling edge of RXCLK shifts the first bit of the Preamble into the Delimiter Recognition logic and SENSE into the SENSE Detection logic. Delimiter Recognition is deferred for eight RXCLKs after the assertion of SENSE, to give the MI unit time to synchronize on the Preamble.

If sequential zeros are detected during the time the LNET is searching for the double ones delimiter, the packet's reception is aborted.

The Preamble bits are shifted through the Delimiter Recognition logic without result. As the last bit of the Delimiter is shifted in, an internal signal is asserted.

The data is then routed to the Receive CRC and the Serial-to-Parallel Register. The Byte Alignment and Odd/Even byte monitor is initialized, and a Byte Counter is started.

At the appropriate byte count, the first byte of Destination Address is converted to parallel data, and compared with the first byte of Station Address and loaded into the RXFIFO.

The RXFIFO Input Pointer (RIP) is then advanced by one. The next byte(s) of destination and source addresses are loaded in the same manner. As the two length count bytes are sent to the RXFIFO they are also loaded into the Length Counter. If this field is non-zero it is decremented on each succeeding byte of the packet.

The remainder of the first 16 bytes of the packet are loaded into the RXFIFO (unless the Length Counter reaches its terminal count or the packet terminates).

With 16 bytes buffered, the RXFIFO is half full. \overline{RXREQ} is now asserted, the receiving half of the buffer becomes the reading half, and the first 16 bytes of receive data are unloaded by advancing the RXFIFO Output Pointer (ROP) as a function of the DMAC's \overline{DACK} and \overline{DS} signals. Meanwhile the empty, receiving half, of the RXFIFO continues to fill.

As the 32nd byte of received data is loaded, \overline{RXREQ} is asserted again and RIP proceeds to the just emptied reading buffer while DMA bus cycles unload the new reading buffer.

The RXFIFO continues to load and unload in this manner throughout the duration of the packet's Data field.

The position of RIP indicates when to load the Length Counter from the data stream, when to check for a valid address, when to assert or negate \overline{RXREQ} and to flag an overrun of the receive DMA service.

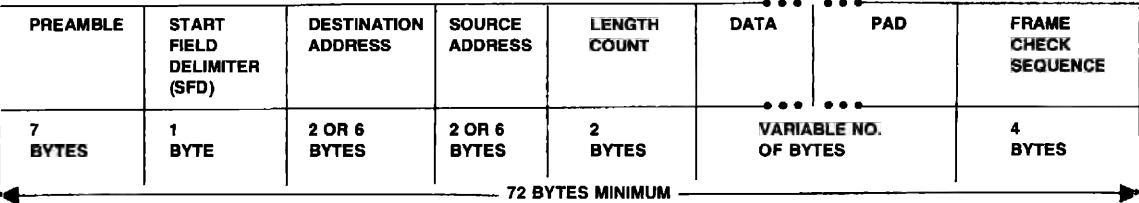


Figure 3. MAC Frame Format

The two-byte Length Counter is located either four or twelve bytes (depending on the address mode) after Valid Delimiter. The Length Counter is decremented every eight RXCLKs. When the Length Counter equals zero, indicating the end of the Data field, RIP is disabled and RXREQ asserts long enough to unload the last bytes.

In the case of a normal termination of the packet, after the last bytes are unloaded, the LNET asserts **DONE** concurrent with the last **DACK** strobe and negates **RXREQ**. The CRC Register continues to calculate over the Pad and Frame Check Sequence fields and the Byte Alignment Checker continues to run until packet end. The state of the Odd/Even byte checker is latched at the time of the Length Counter's terminal count.

The end of the packet is recognized as follows. The last FCS bit shifts in as RXCLK goes low in the normal manner. Two RXCLKs later the negated value of **SENSE** shifts in. At the next rising edge of RXCLK the CRC syndrome is compared and the result is posted to Status Register 1 and **IRQ** is asserted.

If, during the course of a reception, the Data byte count held by the system exceeds the maximum number (1500 bytes for Ethernet), a maximum frame size error is flagged by **DONE** from the DMAC. The LNET responds by negating **RXREQ** and clearing the status registers without generating an **IRQ**.

Frame Transmission

The Transmitter consists of the following: Parallel-to-Serial Register, Transmit Length Counter, 32-byte Transmitter FIFO register file (TXFIFO), Transmit CRC Generator, Preamble and Delimiter Generator, Jam Generator, Interframe Delay Counter, and the Binary Exponential Back-Off Counter. These sections are all driven by TXCLK or a derivation.

Frame transmission commences with a MPU write to Command Register 1 setting the Enable MAUREQ bit. The LNET responds by asserting Transmit DMA Request (TXREQ). Under DMA control, 16 bytes are loaded from the MPU bus into the TXFIFO by advancing the TXFIFO Input Pointer (TIP) as a function of **DACK** and **DS**. The LNET then negates **TXREQ** until the first byte of this data has been serialized out.

While the first 16 bytes are being loaded into the TXFIFO, the LNET is monitoring the **SENSE** input. Upon **SENSE** negation the Transmitter waits 96 TXCLKs (strict IEEE 802.3 or Ethernet application, otherwise the delay follows whatever is programmed into Mode Register bits 5-7) and then serializes out the first byte of data on TXDATA if the TXFIFO is half full (if it is not half full yet, the LNET returns to monitoring **SENSE**). If **SENSE** is active the LNET waits until it is negated and then starts the Interframe Delay Counter.

At the terminal count of the Interframe Delay Counter the first preamble bits are shifted out under TXCLK control and the transmitter begins to monitor the **SIGQUAL** input. At the same time **TXREQ** is asserted again and another 16-byte data burst is transferred into the empty half of the TXFIFO.

As the TXFIFO Output Pointer (TOP) advances to the first byte of the most recently filled half of the buffer, **TXREQ** is again asserted to reload the half just emptied.

Upon the assertion of the **DONE** input by the DMAC (at the time of the last byte or word transfer), the transmitter finishes serializing the last bytes out, zeros the TXFIFO Input Pointer (TIP) and serializes the contents of the CRC Register out on TXDATA.

If **SIGQUAL** is asserted by the MI during the first 512 TXCLKs, the LNET assumes there has been a collision between its own transmission and that of another node in the network. The response of the LNET at its MI interface is to abort the frame transmission after appending a Jam signal consisting of 48 alternating zeros and ones to it. The Jam signal is sent whenever the LNET has successfully contended for the medium and then has been interrupted in its transmission during the collision window.

DMA TRANSFER MODES

The response of the LNET at its MPU/DMAC interface to a collision is programmable to one of two modes in the Mode Register at initialization.

This allows for the LNET to be used with DMACs of differing capabilities. Specifically, some DMACs need to be reinitialized by the MPU if they are to restart a block transfer that has been aborted by a peripheral's assertion of a **DONE** and an **IRQ**. Others are capable of automatically re-starting a block by themselves if a **DONE** is detected during a transfer.

Mode One: Assert **IRQ** plus **DONE** On Collision.

Assertion of **SIGQUAL** during the first 512 TXCLKs after transmission begins sets the collision code (010) in the encoded Transmitter Status field in Status Register 1 and increments the Collision Count field in Status Register 2 by one. Next, **IRQ** is asserted, and the Interrupt Vector Number from the Interrupt Vector Number Register is output on the data bus when **IACK** is asserted.

The MPU processes the interrupt by reading the status registers to determine the cause of the interrupt and to clear the interrupt. The MPU then reinitializes the DMAC and reloads the first 16 bytes of the aborted data packet into the TXFIFO. Meanwhile the LNET is sending the Jam signal followed by a delay interval determined by the Binary Exponential Back-off Counter. At the end of this time interval the LNET begins to transmit the preamble and delimiter again if the TXFIFO has been reloaded with the first 16 bytes of the packet. If the TXFIFO has not been reloaded by the time the Jam signal and the back-off delay interval are over, the LNET will wait for data.

Mode Two: Assert only **DONE** On Collision.

Upon the assertion of **SIGQUAL** during the first 512 TXCLKs, the LNET zeros the TIP, asserts **DONE** to the DMAC concurrent with the next **DACK** signal, increments the retry count and remains in the transmit mode (**TXREQ** asserted, etc.), the Jam is sent, and the Back-off delay is observed. In the meantime, 16 bytes of data are loaded into the TXFIFO by the DMAC. The packet is then transmitted as before.

If the MI asserts **SIGQUAL** after the first 512 TXCLKs, **IRQ** is asserted and the Transmitter Status field in Status Register 2 is set to 011.

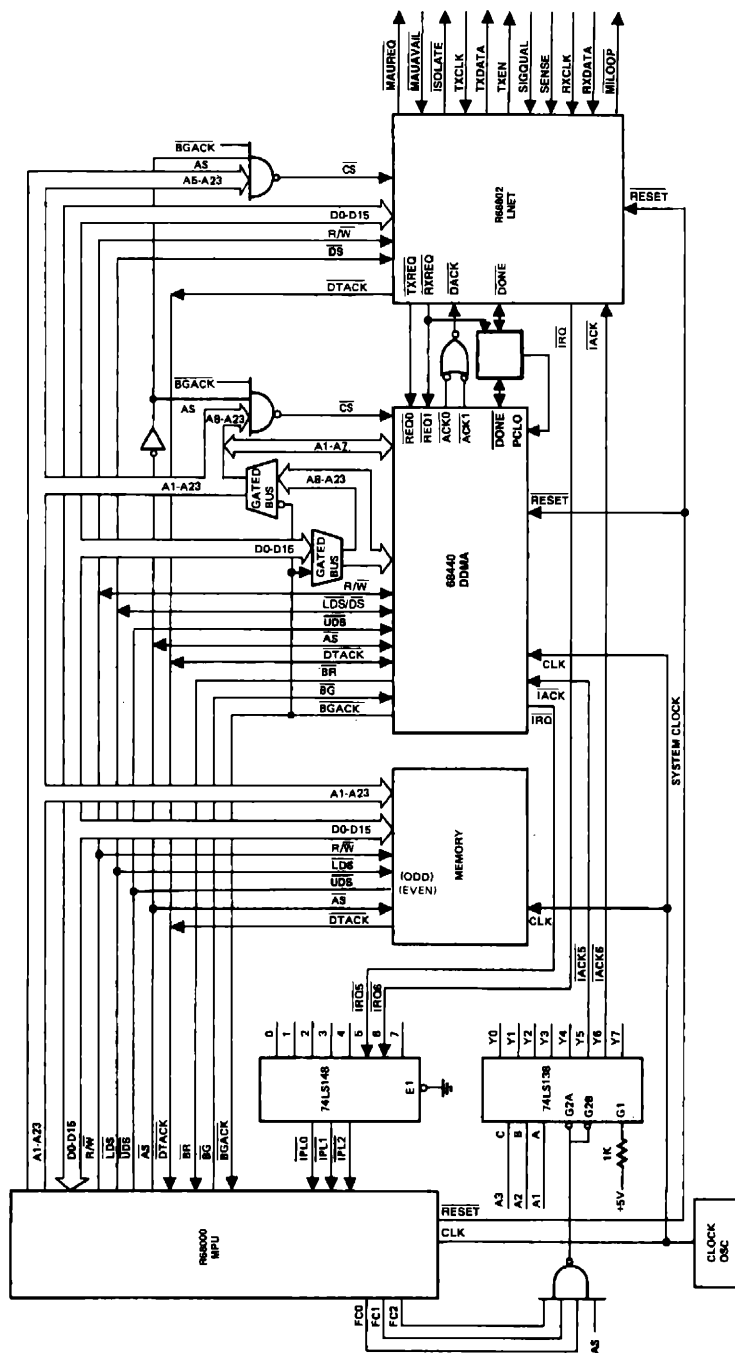


Figure 4. Typical Interface to 68000-Based System

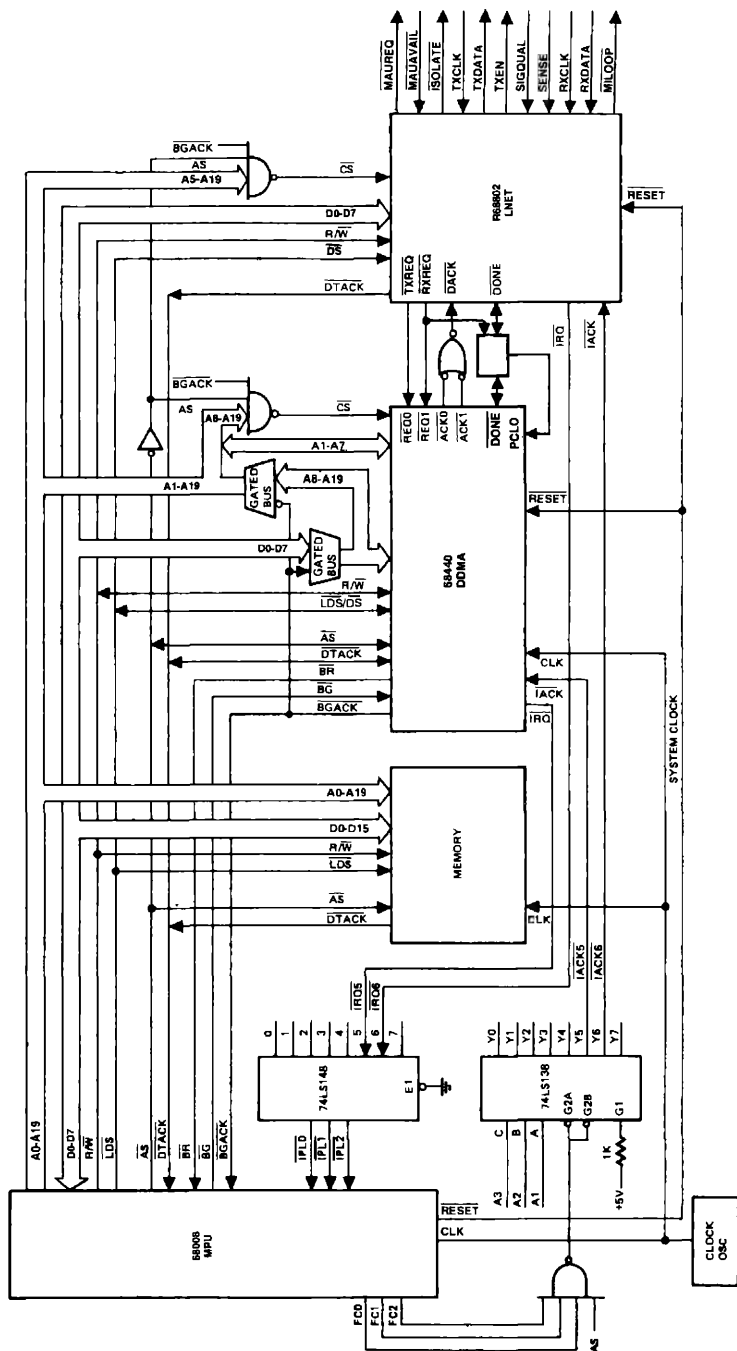
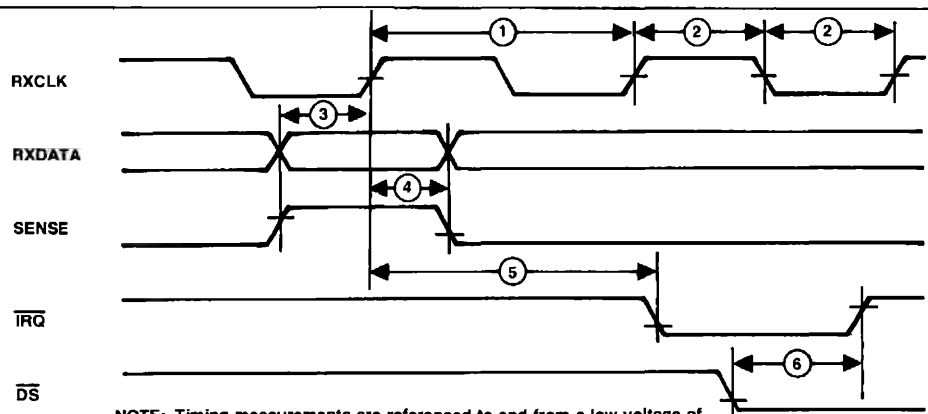
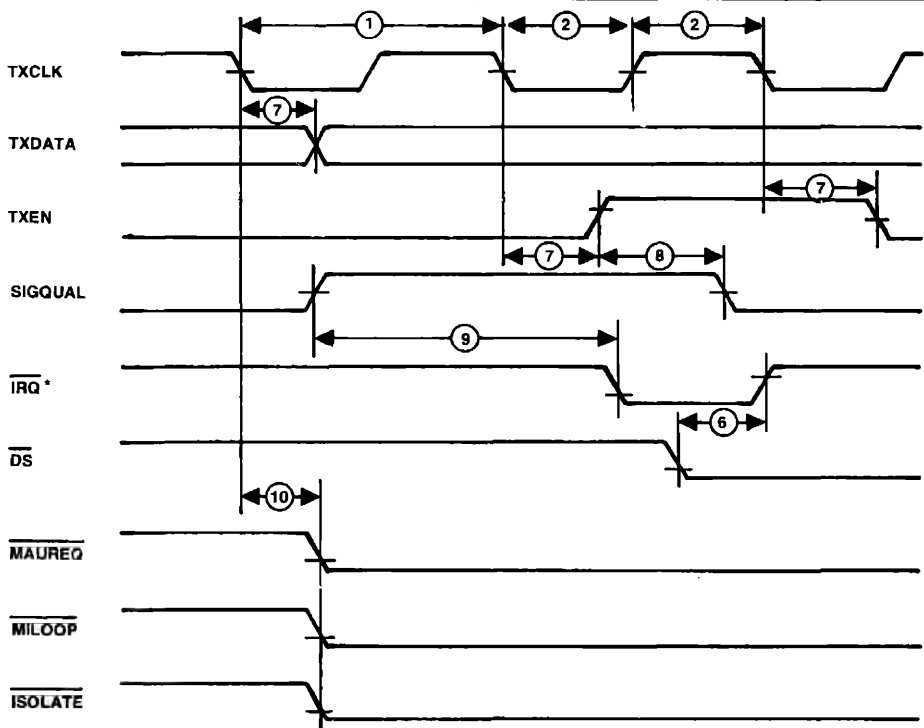


Figure 5. Typical Interface to 68008-Based System



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

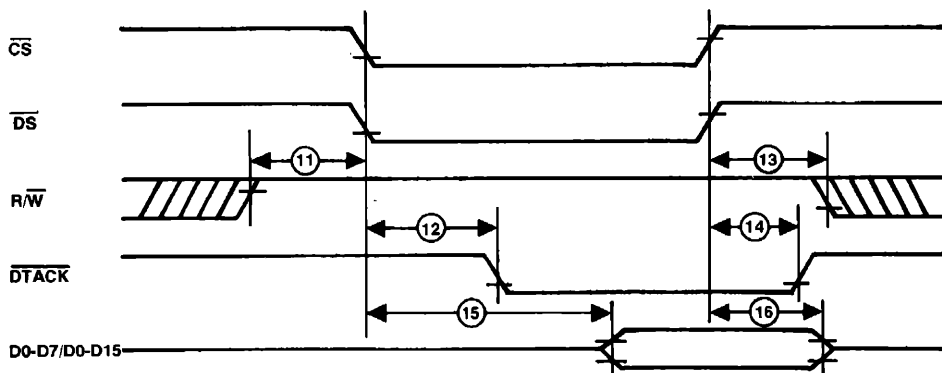
Figure 6. Manchester Interface Serial Receiver Timing



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

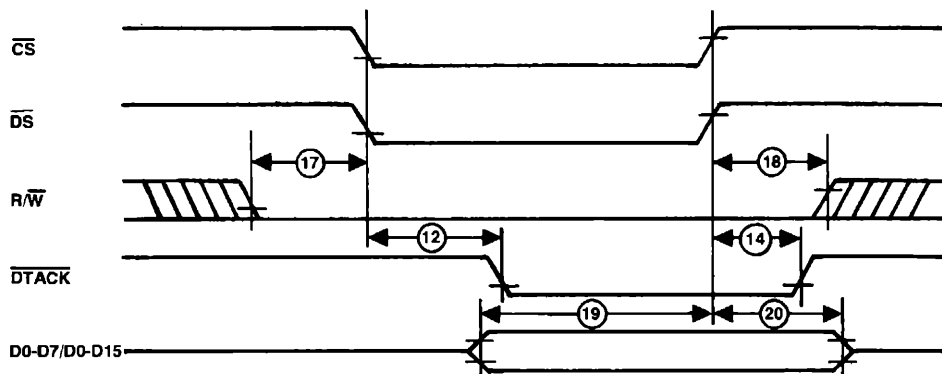
*IRQ assertion on collision not required—Bit 3 of the mode register (MR) determines whether or not IRQ asserts on collision.

Figure 7. Manchester Interface Serial Transmitter Timing

**NOTE:**

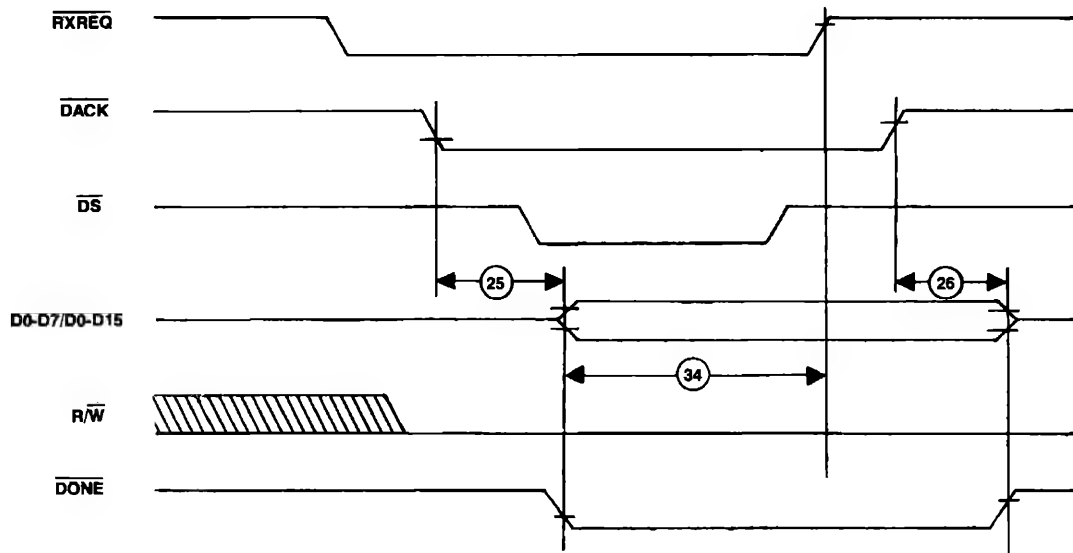
Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

Figure 8. LNET Read Cycle Timing

**NOTE:**

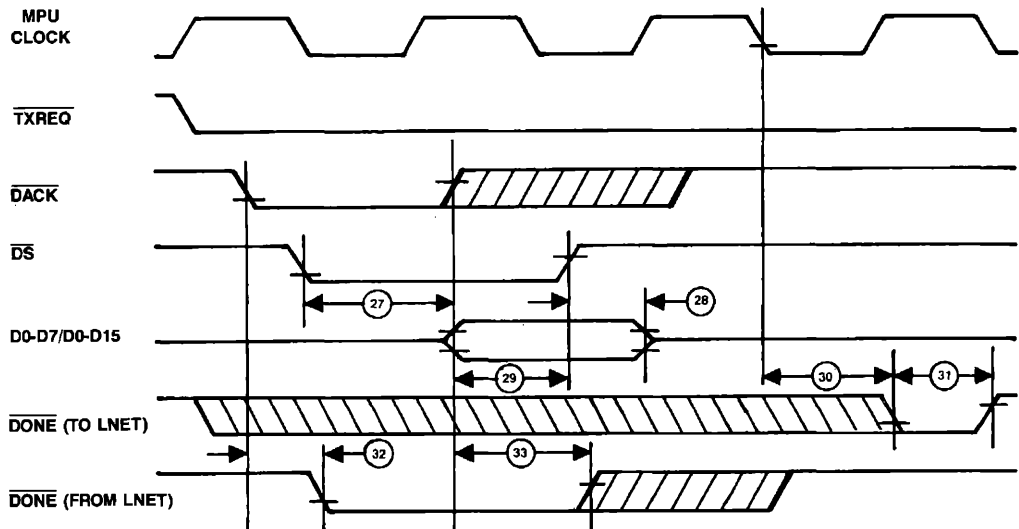
Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

Figure 9. LNET Write Cycle Timing



NOTES: 1. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.
 2. Word mode only.

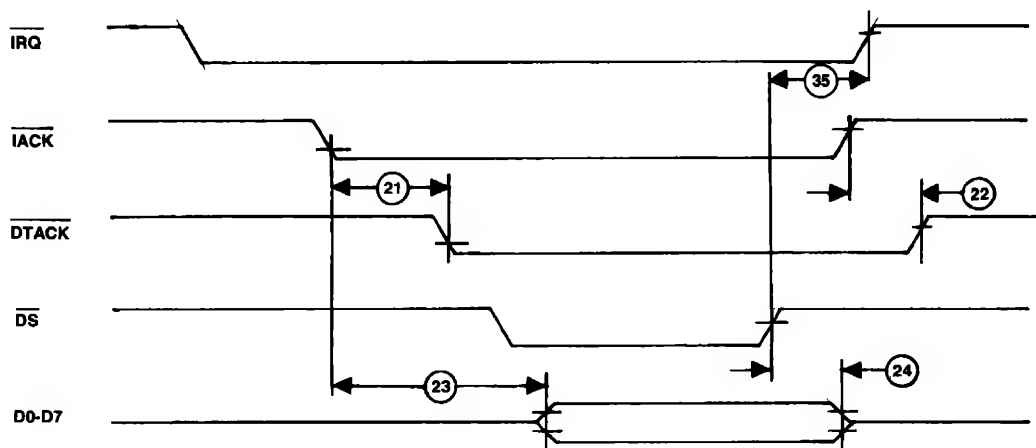
Figure 10. LNET to Memory DMA Transfer Cycle Timing



NOTES: 1. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

2. Word mode only.

Figure 11. Memory to LNET DMA Transfer Cycle Timing



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

Figure 12. Interrupt Request Cycle Timing

SPECIFICATIONS

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0Vdc \pm 5\%$, $V_S = 0Vdc$, $T_A = 0$ to $70^\circ C$)

Number	Characteristic	Symbol	Min	Typ	Max	Unit
1	Clock Period	t_{CP}	90		1000	ns
2	Receive Clock Pulse Width	t_{CFR}	45		—	ns
3	Receive Data/Sense Setup	t_{RXS}	30		—	ns
4	RXDATA, Sense Hold Time	t_{RXH}	20		—	ns
5	IRQ Delay from RXCLK	t_{RID}	0		80	ns
6	\overline{DS} to IRQ Clear (Status Read)	t_{DID}	50		—	ns
7	TXDATA/TXEN Delay ($C_L = 35pF$)	t_{TXD}	20		60	ns
8	SIGQUAL Hold Time	t_{CPH}	0		—	ns
9	IRQ Delay from SIGQUAL Edge (Optional)*	t_{ISD}	0		—	ns
10	MAU/MI Control Output Delay	t_{MOD}	0		80	ns
11	R/W High to \overline{CS} , \overline{DS} Low	$t_{RHS L}$	0		—	ns
12	\overline{CS} Low to \overline{DTACK} Low	t_{CLDAL}	20	40	80	ns
13	\overline{CS} , \overline{DS} High to R/W Low	t_{SHRL}	20		—	ns
14	\overline{CS} High to \overline{DTACK} Tristate	t_{SHDAT}	20	40	80	ns
15	\overline{CS} , \overline{DS} Low to Data Valid	t_{SLDV}	0		140	ns
16	\overline{CS} , \overline{DS} High to Data Invalid	t_{SHDI}	10		150	ns
17	R/W Low to \overline{CS} , \overline{DS} Low	t_{RLSL}	0		—	ns
18	\overline{CS} , \overline{DS} High to R/W High	t_{SHRH}	20		—	ns
19	Data Valid to \overline{CS} , \overline{DS} High	t_{DVSH}	100		—	ns
20	\overline{CS} , \overline{DS} High to Data Invalid	t_{SHDI}	10		—	ns
21	\overline{ACK} Low to \overline{DTACK} Low	t_{IALAL}	20	40	80	ns
22	\overline{ACK} High to \overline{DTACK} Tristate	t_{IAHDAT}	20	40	80	ns
23	\overline{ACK} Low to Data Valid	t_{IALDV}	0		140	ns
24	\overline{DS} High to Data Invalid	t_{ISHDI}	10		50	ns
25	\overline{DACK} Low to \overline{DONE} /Data Valid	t_{DLDV}	0		50	ns
26	\overline{DTACK} High to \overline{DONE} Invalid/Data	t_{DHDV}	0		40	ns
27	\overline{DS} Low to \overline{DACK} High	t_{DLDH}	0		50	ns
28	\overline{DS} High to Data Invalid	t_{SHDI}	0		40	ns
29	Data Invalid to \overline{DS} High	t_{DVSH}	65		—	ns
30	Clock Low to \overline{DONE} (to LNET) Low	t_{CLDL}	0		100	ns
31	External \overline{DONE} Pulse Width	t_{EDPW}	70		250	ns
32	\overline{DACK} Low to Internal \overline{DONE} Low Delay	t_{DLID}			80	ns
33	\overline{DACK} High to Internal \overline{DONE} High Delay	t_{DHID}			80	ns
34	\overline{DONE} Low to \overline{RXREQ} High	t_{DLRXH}		2		RXCLK
35	\overline{DS} High to IRQ High	t_{DSHIH}		2		RXCLK

Note:

*IRQ assertion on collision dependent on bit 3 of mode register (MR).

MAXIMUM RATINGS

Characteristics	Symbol	Value
Supply Voltage	V_{CC}	-0.3 to +7.0V
Input Voltage	V_{IN}	-0.3 to +7.0V
Operating Temperatures	T_A	0 to 70°C
Storage Temperatures	T_{STG}	-55 to +150°C

Note:

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, normal precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

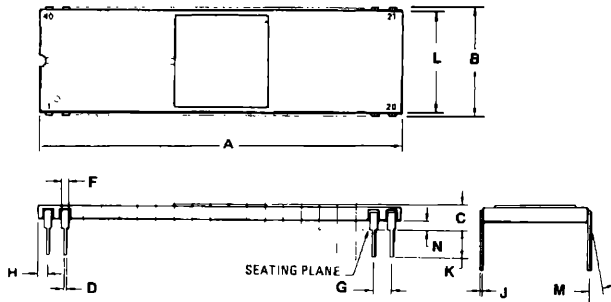
Characteristics	Symbol	Value	Rating
Thermal Resistance	θ_{JA}	50	°C/W
Ceramic		68	°C/W
Plastic			

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{Vdc} \pm 5\%$, $V_{SS} = 0\text{Vdc}$, $T_A = 0$ to 70°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	+2.0	V_{CC}	V	
Input Low Voltage	V_{IL}	-0.3	+0.8	V	
Input Leakage Current R/W, RESET, CS	I_{IN}	—	10	μA	$V_{IN} = 0$ to 5.25V $V_{CC} = 0\text{V}$
Input Leakage Current for Three-State (Off) DTACK, D0-D15	I_{TSI}	—	10	μA	$V_{IN} = 0.4$ to 2.4V $V_{CC} = 0\text{V}$
Output High Voltage RXREQ, TXREQ, DTACK, D0-D15, MILOOP, MAUREQ, ISOLATE TXEN, TXDATA	V_{OH}	+2.4 +2.4 +2.4	— — —	V V V	$V_{CC} = 4.75\text{V}$ $I_{LOAD} = -400\text{ }\mu\text{A}$, $C_{LOAD} = 130\text{ pF}$ $I_{LOAD} = -400\text{ }\mu\text{A}$, $C_{LOAD} = 32\text{ pF}$ $I_{LOAD} = 0$, $C_{LOAD} = 30\text{ pF}$
Output Low Voltage RXREQ, TXREQ, TXEN, TXDATA, DTACK, D0-D15 MILOOP, MAUREQ, ISOLATE IRQ, DONE	V_{OL}	— —	0.5 0.5	V V	$V_{CC} = 4.75\text{V}$ $I_{LOAD} = 3.2\text{ mA}$ $I_{LOAD} = 8.8\text{ mA}$
Power Dissipation	P_{INT}	—	1.0	W	$T_A = 25^\circ\text{C}$
Input Capacitance	C_{IN}	—	13	pF	$V_{CC} = 5.0\text{V}$ $V_{IN} = 0\text{V}$ $f = 1\text{ MHz}$ $T_A = 25^\circ\text{C}$

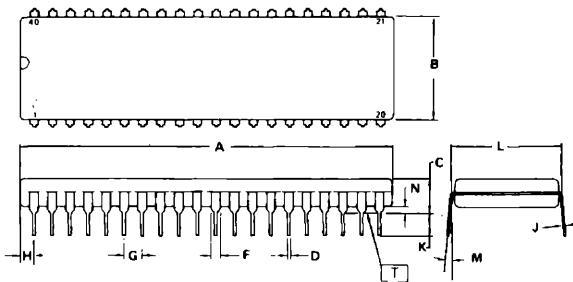
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040



R68C552 DUAL ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (DACIA)

1

PRELIMINARY

DESCRIPTION

The Rockwell CMOS R68C552 Dual Asynchronous Communications Interface Adapter (DACIA) provides an easily implemented, program controlled interface between 16-bit microprocessor-based systems and serial communication data sets and modems.

The DACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 38,400 baud, or at 1/16 times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at 1/16 times the external clock rate. The DACIA is programmable for word lengths of 5, 6, 7 or 8 bits; even, odd, or no parity; and 1 or 2 stop bits.

The DACIA is designed for maximum programmed control from the microprocessor (MPU) to simplify hardware implementation. Dual sets of registers allow independent control and monitoring of each channel. The DACIA also provides a unique, programmable Automatic Address Recognition mode for use in a multi-drop environment.

The Control Register and Status Register permit the MPU to easily select the R68C552's operating modes and determine operational status.

The Interrupt Enable Registers (IER) and Interrupt Status Registers (ISR) allow the MPU to control and monitor the interrupt capabilities of the DACIA.

The Control and Format Register (CFR) permits selection of baud rates, word lengths, parity and stop bits as well as control of DTR and RTS output signals.

The Status Register (SR) gives the MPU access to the state of the modem control lines, framing error, transmitter underrun and break conditions.

The Compare Data Registers (CDR) hold the data value to be used in the compare mode.

The IRQ Vector Register (IVR) holds the interrupt vector for use in the interrupt acknowledge state, or commands a Transmit Break and provides for parity/address recognition during Automatic Address Recognition mode.

ORDERING INFORMATION

Part Number:
R68C552

Package:
C = Ceramic
P = Plastic

FEATURES

- Low power CMOS N-well silicon gate technology
- Two independent full duplex channels with buffered receivers and transmitters.
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 38,400)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Programmable control of edge detect for DCD, DSR, DTR, RTS, and CTS
- Program-selectable serial echo mode for each channel
- Automatic Address Recognition mode for multi-drop operations
- 5.0 Vdc \pm 5% supply requirements
- 40-pin plastic or ceramic DIP
- Full TTL or CMOS input/output compatibility
- Compatible with R68000 microprocessor family

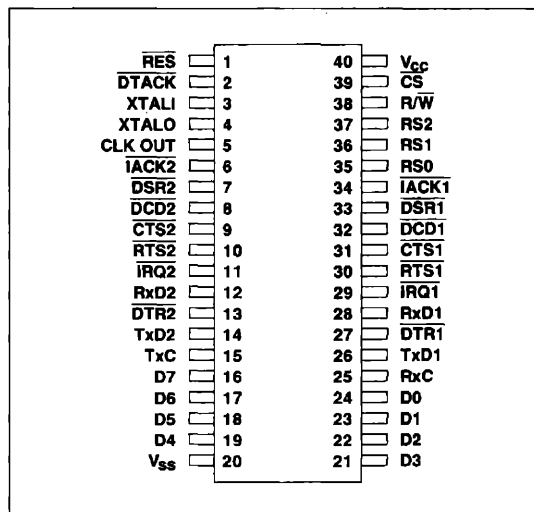


Figure 1. R68C552 Pin Configuration

INTERFACE SIGNALS

Figure 2 shows the DACIA interface signals associated with the microprocessor and the modem.

DATA BUS (D0-D7)

The D0-D7 pins are eight data lines that transfer data between the microprocessor (MPU) and the DACIA. These lines are bidirectional and are normally high-impedance except during READ cycle when the DACIA is selected.

REGISTER SELECTS (RS0, RS1, RS2)

The three register select lines are normally connected to the processor address lines to allow the MPU to select the various internal registers. Table 1 shows the internal register select coding and identifies the abbreviations (ABBR) used throughout the text for each register. Table 2 summarizes the control and status registers and shows each bit allocation.

READ/WRITE (R/W)

The R/W input, generated by the microprocessor, controls the direction of data transfer. A high on the R/W line indicates a read cycle, while a low indicates a write cycle.

CHIP SELECT (CS)

The chip select input is normally connected to the processor address lines either directly or through decoders. The DACIA latches address and R/W inputs on the falling edge of CS and latches the data bus inputs on the rising edge of CS.

RESET (RES)

During system initialization a low level on the RES input causes a RESET to occur. At this time the IER's are set to \$80, the DTR and RTS lines go to the high state, the RDR register is cleared, the IVR is set to \$0F, the compare mode is disabled, and the CTS, DCD, DSR flags are cleared. No other bits are affected.

TRANSMIT DATA (TXD1, TXD2)

The Tx outputs transfer serial non-return to zero (NRZ) data to the data communications equipment (DCE). The data is transferred, LSB first, at a rate determined by the baud rate generator.

RECEIVE DATA (RXD1, RXD2)

The Rx inputs transfer serial NRZ data into the DACIA from the DCE, LSB first. The receiver baud rate is determined by the baud rate generator.

CLEAR TO SEND (CTS1, CTS2)

The CTS control line inputs allow handshaking by the transmitter. When CTS is low, the data is transmitted continuously. When CTS is high, the Transmit Data Register empty bit in the ISR is not set. The word presently in the Transmit Shift Register is sent normally. Any active transition on the CTS lines sets the CTS bit in the appropriate ISR. The CTS status bit in the SR reflects the current high or low state of CTS.

DATA CARRIER DETECT (DCD1, DCD2)

These two lines may be used as general purpose inputs. An active transition sets the DCD bit in the ISR. The DCD bit in the SR reflects the current state of the DCD line.

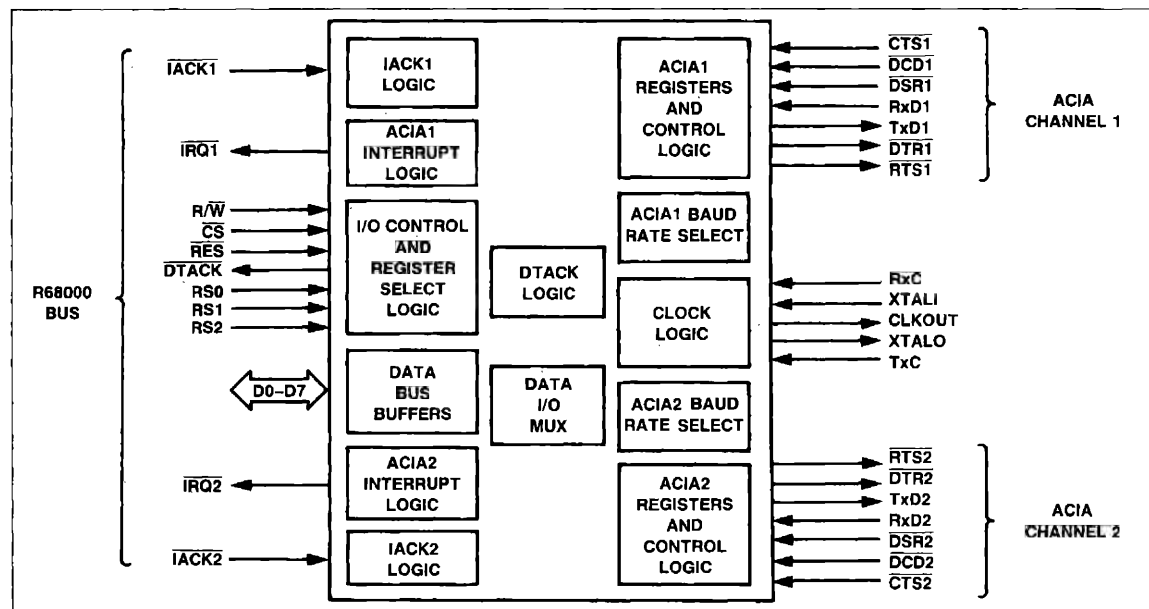


Figure 2. DACIA Interface Signals

DATA SET READY ($\overline{\text{DSR1}}$, $\overline{\text{DSR2}}$)

These two lines may be used as general purpose inputs. An active transition sets the DSR bit in the ISR. The DSR bit in the SR reflects the current state of the DSR line.

REQUEST TO SEND ($\overline{\text{RTS1}}$, $\overline{\text{RTS2}}$)

These two lines may be used as general purpose outputs. They are set high upon reset. Their state may be programmed by setting the appropriate bits in the CFR high or low. The state of the RTS line is reflected by the RTS bit in the SR.

DATA TERMINAL READY ($\overline{\text{DTR1}}$, $\overline{\text{DTR2}}$)

These two lines may be used as general purpose outputs. They are set high upon reset. Their state may be programmed by setting the appropriate bits in the CFR high or low. The state of the DTR line is reflected by the DTR bit in the SR.

INTERRUPT REQUEST ($\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$)

The $\overline{\text{IRQ}}$ lines are open-drain outputs from the interrupt control logic. $\overline{\text{IRQ1}}$ is associated with ACIA1 and $\overline{\text{IRQ2}}$ is associated with ACIA2. These lines are normally high but go low when one of the flags in the ISR is set, provided that its corresponding enable bit is set in the IER.

CLOCK CIRCUIT

The internal clock oscillator supplies the time base for the baud rate generator. The oscillator can be driven by a crystal or an external clock, or it can be disabled, in which case the time base for the baud rate is generated by the Receiver External Clock (RxC) and Transmitter External Clock (TxC) input pins. Figure 3 shows the three possible clock configurations.

CRYSTAL (XTALI, XTALO)

These pins are normally connected to an external 3.6864 MHz crystal used as the time base for the baud rate generator. As an alternative, the XTALI pin may be driven with an externally generated clock in which case the XTALO pin must float.

RECEIVER CLOCK (RxC)

This pin is the Receiver 16x clock input when the baud rate generator is programmed for External Clock. Figure 15 shows timing considerations for RxC.

TRANSMITTER CLOCK (TxC)

This pin is the transmitter 16x clock input when the baud rate generator is programmed for External Clock. Figure 16 shows timing considerations for TxC.

Note

When RxC and TxC are used for external clock input, XTALI must be tied to ground (Vss) and XTALO must be left open (floating).

CLOCK OUT (CLK OUT)

This output is a buffered output from the 3.6864 MHz crystal oscillator. It may be used to drive the XTALI input of another DACIA. This allows multiple DACIA chips to be used in a system with only one crystal needed. CLK OUT is in phase with XTALI.

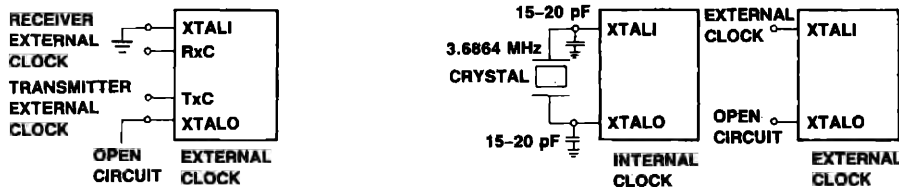


Figure 3. DACIA Clock Generation

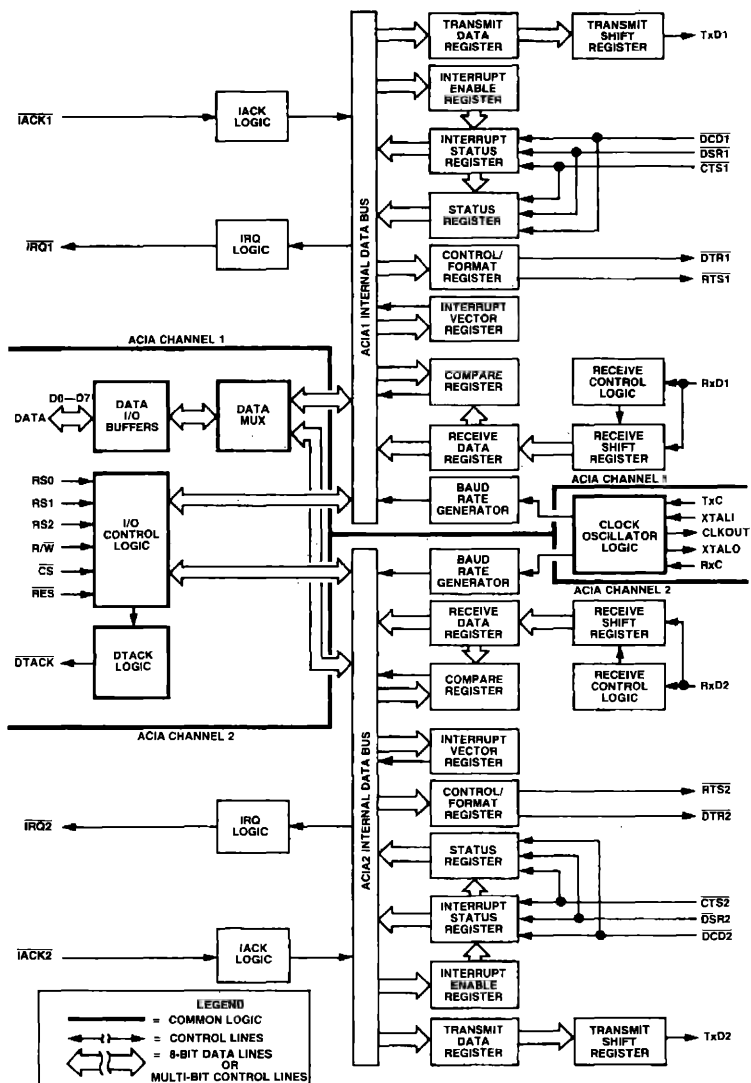


Figure 4. DACIA Block Diagram

FUNCTIONAL DESCRIPTION

Figure 4 is a block diagram of the DACIA which consists of two asynchronous communications interface adapters with common microprocessor interface control logic and data bus buffers. The individual functional elements of the DACIA are described in the following paragraphs.

DATA BUS BUFFER

The Data Bus Buffer is a bidirectional interface between the system data lines and the internal data bus. When R/W is high and CS is low, the Data Bus Buffer passes data from the internal data bus to the system data lines. When R/W is high, CS is high, and either IACK line is low, the IRQ vector is passed to the system data bus. When R/W is low and CS is low, data is brought into the DACIA from the system data bus. The following table summarizes the Data Bus Buffer states.

Data Bus Buffer Summary

R/W	Control Signals			Data Bus Buffer State
	CS	IACK1	IACK2	
L	L	L	L	ILLEGAL MODE — TRI STATE
L	L	L	H	ILLEGAL MODE — TRI STATE
L	L	H	L	ILLEGAL MODE — TRI STATE
L	L	H	H	WRITE MODE — TRI STATE
L	H	L	L	ILLEGAL MODE — TRI STATE
L	H	L	H	ILLEGAL MODE — TRI STATE
L	H	H	L	ILLEGAL MODE — TRI STATE
L	H	H	H	TRI STATE
H	L	L	L	ILLEGAL MODE — OUTPUT \$0F
H	L	L	H	ILLEGAL MODE — OUTPUT \$0F
H	L	H	L	ILLEGAL MODE — OUTPUT \$0F
H	L	H	H	READ MODE — OUTPUT DATA
H	H	L	L	ILLEGAL MODE — OUTPUT \$0F
H	H	L	H	OUTPUT IRQ VECTOR 1
H	H	H	L	OUTPUT IRQ VECTOR 2
H	H	H	H	TRI STATE

TRANSMIT AND RECEIVE DATA REGISTERS

These registers are used as temporary data storage for the DACIA Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.
- Write-Only Register.

The Receive Data Register is characterized in a similar fashion as follows:

- Bit 0 is the leading bit received.
- Unused data bits are the high order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped off after being used for external parity checking. Parity and all unused high-order bits are "0".
- Read-Only Register

Figure 5 shows an example of a single transmitted or received data word. In this example, the data word is formatted with 8 data bits, parity, and two stop bits. Figure 5 also shows a single character transmitted or received in Address Recognition mode. In this example, the address or data word is 8 bits, there is no parity bit, and there are two stop bits. The 10th bit, (normal parity bit) is an address/data indicator bit. A 1 means the 8 bits are an address that will be compared with the address stored in the Compare Data Register. A 0 means the 8 bits are data.

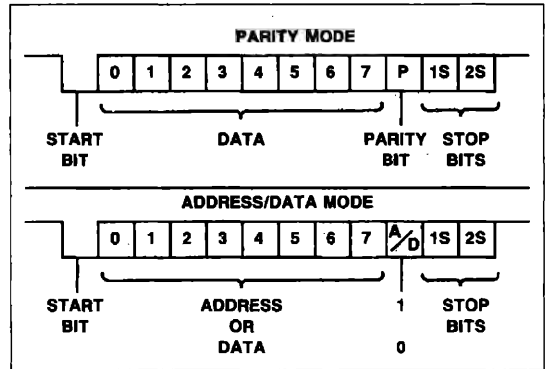


Figure 5. Typical Data Word

INTERRUPT LOGIC

The interrupt logic causes the IRQ lines (IRQ1 or IRQ2) to go low when conditions are met that require the attention of the MPU. There are two registers (the Interrupt Enable Register and the Interrupt Status Register) involved in the control of interrupts in the DACIA. Corresponding bits in both registers must be set to cause an IRQ.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) is a write-only register that allows each of the possible IRQ sources to be enabled, or disabled, individually without affecting any of the other interrupt enable bits in the register. IRQ sources are enabled by writing to the IER with bit 7 set to a 1 and every bit set to a 1 that corresponds to the IRQ source to be enabled. IRQ sources are disabled by writing to the IER with bit 7 set to a 0 and every bit set to a 1 that corresponds to the IRQ source to be disabled. Any bit (except bit 7) to which a 0 is written is unaffected and remains in its original state. As an example, writing \$7F to the IER will disable all IRQ source bits, but writing \$FF to the IER will enable all IRQ source bits. A hardware reset (RES) clears all IRQ source bits to the 0 state. Bit assignments for the IER are as follows:

7	6	5	4	3	2	1	0
CLEAR/ SET BITS	TDR EMPTY IE	CTS IE	DCD IE	DSR IE	PARITY ERROR IE	FRM OVR BRK IE	RDR FULL IE

Table 1. DACIA Register Selection

HEX	REGISTER SELECT LINES			CONTROL & FORMAT REGISTER BITS		REG	REGISTER ACCESS	
00	L	L	L	—	—	IER1 ISR1	INTERRUPT ENABLE REGISTER 1	INTERRUPT STATUS REGISTER 1
01	L	L	H	0	—	CFR1 SR1	CONTROL REGISTER 1	STATUS REGISTER 1
				1	—	CFR1	FORMAT REGISTER 1	INVALID
02	L	H	L	—	0	CDR1	COMPARE DATA REGISTER 1	INVALID
				—	1	IVR1	IRQ VECTOR 1	INVALID
03	L	H	H	—	—	TDR1 RDR1	TRANSMIT DATA REGISTER 1	RECEIVE DATA REGISTER 1
04	H	L	L	—	—	IER2 ISR2	INTERRUPT ENABLE REGISTER 2	INTERRUPT STATUS REGISTER 2
05	H	L	H	0	—	CFR2 SR2	CONTROL REGISTER 2	STATUS REGISTER 2
				1	—	CFR2	FORMAT REGISTER 2	INVALID
06	H	H	L	—	0	CDR2	COMPARE DATA REGISTER 2	INVALID
				—	1	IVR2	IRQ VECTOR 2	INVALID
07	H	H	H	—	—	TDR2 RDR2	TRANSMIT DATA REGISTER 2	RECEIVE DATA REGISTER 2

Table 2. Control and Status Registers Format Summary

REGISTER BIT NUMBERS								REGISTER	RES
7	6	5	4	3	2	1	0	INTERRUPT ENABLE REGISTERS	\$80
CLEAR/SET BITS	TDR EMPTY IE	CTS IE	DCD IE	DSR IE	PARITY ERROR IE	FRM OVR BRK IE	RDR FULL IE	INTERRUPT STATUS REGISTERS	—
ANY BIT SET	TDR EMPTY	CTS TRANS	DCD TRANS	DSR TRANS	PARITY ERROR	FRM OVR BRK	RDR FULL	STATUS REGISTERS	—
FRAMING ERROR	TRANS UNDR	CTS STATUS	DCD STATUS	DSR STATUS	REC BREAK	DTR STATUS	RTS STATUS	CONTROL REGISTERS AND FORMAT REGISTERS	—
0	IVR/CDR REG	NO. STOP BITS	ECHO	BAUD RATE SELECTION				COMPARE DATA REGISTER	—
1	NUMBER OF DATA BITS		PARITY SELECTION		PARITY ENABLE	DTR CONTROL	RTS CONTROL	IA MODE	\$0F
COMPARE BITS (ADDRESS RECOGNITION)								INTERRUPT VECTOR REGISTER	
IRQ VECTOR ADDRESS						IRQ SOURCE		T/R MODE	
NOT USED						TRANS BRK	PAR/ ADDR		

INTERRUPT STATUS REGISTER (ISR)

The Interrupt Status Register (ISR) is a read-only register that identifies the current status condition for each DACIA internal IRQ source. Bits 6 through 0 of the ISR are set to a 1 whenever the corresponding IRQ source condition has occurred in the DACIA. Bit 7 identifies if any of the IRQ source status bits have been set in the ISR.

7	6	5	4	3	2	1	0
ANY BIT SET	TDR EMPTY	CTS TRANS	DCD TRANS	DSR TRANS	PARITY ERROR	FRM OVR BRK	RDR FULL

- Bit 7 Any Bit Set**
 1 Any bit (6 through 0) has been set to a 1
 0 No bits have been set to a 1
- Bit 6 Transmit Data Register Empty (TDR EMPTY)**
 1 Transmit Data Register has been transferred to the shift register
 0 New data has been written to the Transmit Data Register
- Bit 5 Transition On CTS Line (CTS TRANS)**
 1 A positive or negative transition has occurred on CTS
 0 No transition has occurred on CTS, or ISR has been read
- Bit 4 Transition On DCD Line (DCD TRANS)**
 1 A positive or negative transition has occurred on DCD
 0 No transition has occurred on DCD, or ISR has been read
- Bit 3 Transition On DSR Line (DSR TRANS)**
 1 A positive or negative transition has occurred on DSR
 0 No transition has occurred on DSR, or ISR has been read
- Bit 2 Parity Error**
 1 A parity error has occurred in received data
 0 No parity error has occurred, or the Receive Data Register (RDR) has been read
- Bit 1 Frame Error, Overrun or Break (FRM, OVR, BRK)**
 1 A framing error, receive overrun, or receive break has occurred
 0 No error, overrun, break has occurred or RDR has been read
- Bit 0 Receive Data Register Full (RDR FULL)**
 1 Shift register data has been transferred to Receive Data Register
 0 Receive Data Register has been read

INTERRUPT VECTOR REGISTER (IVR)

The DACIA has two Interrupt Vector Registers which are write-only registers. By storing the appropriate vector address number in bits 7 through 2 of the IVR, the DACIA will place the vector on the data bus when requested by the IACK signal. In this mode, bits 1 and 0 identify the source of the IRQ.

Note: In order for the IVR Vector Address to be recognized, bit 6 of the CFR must be a 1.

During the Transmit Receive mode, bits 7 through 2 are not used and are treated as "don't care" bits. In this mode, bits 1 and 0 are used for Transmit Break and Parity/Address recognition.

Writing a 1 to bit 1 of the IVR causes a continuous Break to be transmitted by the ACIA associated with the register. Writing a 0 to this bit allows normal transmission to resume. Writing a 1 to bit 0 of the IVR commands the value of the Parity bit to be sent to the Parity Error bit (bit 2 of the ISR). Writing a 0 to this bit allows normal Parity Error recognition to be in force. When an RES is received by the DACIA, both of these bits are reset to 0. The bits format for the IVR are as follows:

7	6	5	4	3	2	1	0
IRQ VECTOR ADDRESS						IRQ SOURCE	
NOT USED						TRANS BRK	PAR/ ADDR

Interrupt Acknowledge Mode (IA Mode)

Bits 7-2 IRQ Vector Address

- Bit 1 IRQ Source Channel**
 1 ACIA1 selected
 0 ACIA2 selected

- Bit 0 IRQ Source**
 1 Other IRQ (CTS, DCD, DSR, Parity, Break, OV)
 0 Transmit or Receive IRQ

Transmit/Receive Mode (T/R Mode)

Bits 7-2 Not used (don't care)

- Bit 1 Transmit Break (TRANS BRK)**
 1 Transmit continuous Break until disabled
 0 Resume normal transmission

- Bit 0 Parity/Address Recognition (PAR/ADDR)**
 1 Send value of parity to ISR bit 2 (Address Recognition mode)
 0 Return to normal Parity Error recognition mode

COMPARE DATA REGISTER

The Compare Data Register (CDR) is a write-only register which can be accessed when CFR bit 6 = 0. By writing a value into the CDR, the DACIA is put in the compare mode. In this mode, setting of the RDRF bit is inhibited until a character is received which matches the value in the CDR. The next character is then received and the RDRF bit is set. The receiver will now operate normally until the CDR is again loaded.

STATUS REGISTER (SR)

The Status Register (SR) is a read-only register that provides I/O status and error condition information. The SR is normally read after an IRQ has occurred to determine the exact cause of the interrupt condition.

7	6	5	4	3	2	1	0
FRAMING ERROR	TRANS UNDR	CTS STATUS	DCD STATUS	DSR STATUS	REC BREAK	DTR STATUS	RTS STATUS

Bit 7 Framing Error

- 1 A framing error occurred in receive data
0 No framing error occurred, or the RDR was read

Bit 6 Transmitter Underrun (TRANS UNDR)

- 1 Transmit shift register is empty and TDRE bits in IER and ISR are set
0 A write to the TDR has occurred

Bit 5 CTS Status

- 1 CTS line high
0 CTS line low

Bit 4 DCD Status

- 1 DCD line high
0 DCD line low

Bit 3 DSR Status

- 1 DSR line high
0 DSR line low

Bit 2 REC Break

- 1 A Receive Break has occurred
0 No Receive Break occurred, or RDR, was read

Bit 1 DTR Status

- 1 DTR line high
0 DTR line low

Bit 0 RTS Status

- 1 RTS line high
0 RTS line low

CONTROL AND FORMAT REGISTER (CFR)

The Control and Format Register (CFR) is a dual-function, write-only register which allows control of word length, baud rate, control line outputs, parity, echo mode, and compare/IVR access. When the CFR is written to with bit 7 = 0, the CFR functions as a Control Register. When the CFR is written to with bit 7 = 1, the CFR operates as a Format Register.

Control Register (CFR Addressed with Bit 7 = 0)

7	6	5	4	3	2	1	0
0	IVR/CDR	NO. STOP BITS	ECHO	BAUD RATE SELECTION			

Bit 6 IVR/CDR

- 1 Access the IRQ Vector Register (IVR)
0 Access the Compare Data Register (CDR)

Bit 5**Number of Stop Bits**

- 1 Two stop bits
0 One stop bit

Bit 4**Echo Selection (ECHO)**

- 1 Echo activated
0 Echo deactivated

Bits 3-0**Baud Rate Selection****Baud Rate**

3	2	1	0	Baud Rate
0	0	0	0	50
0	0	0	1	109.2
0	0	1	0	134.58
0	0	1	1	150
0	1	0	0	300
0	1	0	1	600
0	1	1	0	1200
0	1	1	1	1800
1	0	0	0	2400
1	0	0	1	3600
1	0	1	0	4800
1	0	1	1	7200
1	1	0	0	9600
1	1	0	1	19200
1	1	1	0	38400
1	1	1	1	External Tx/C and Rx/C Clocks

Format Register (CFR Addressed with Bit 7 = 1)

7	6	5	4	3	2	1	0
1	NUMBER OF DATA BITS	PARITY SELECTION	PARITY ENABLE	DTR CONTROL	RTS CONTROL		

Bits 6-5**Number of Data Bits Per Channel****No. Bits**

6	5	No. Bits
0	0	5
0	1	6
1	0	7
1	1	8

Bits 4-3**Parity Mode Selection****Selects**

4	3	Selects
0	0	Odd Parity
0	1	Even Parity
1	0	Mark Parity
1	1	Space Parity

Bit 2**Parity Enable**

- 1 Parity as specified by bits 4-3
0 No Parity

Bit 1**DTR Control**

- 1 DTR high
0 DTR low

Bit 0**RTS Control**

- 1 RTS high
0 RTS low

OPERATION

The ten modes (or conditions) of operation of the DACIA are:

- Continuous Data Transmit
- Continuous Data Receive
- Transmit Underrun Condition
- Effects of CTS on Transmitter
- Effects of Overrun on Receive
- Echo Mode Timing
- Framing Error
- Transmit Break Character
- Receive Break Character
- Automatic Address Mode

CONTINUOUS DATA TRANSMIT

In the normal operating mode, the TDRE bit in the ISR signals the MPU that the DACIA is ready to accept the next data word. An IRQ occurs if the corresponding TDRE IRQ enable bit is set in the IER. The TDRE bit is set at the beginning of the start bit. When the MPU writes a word to the TDR the TDRE bit is cleared. In order to maintain continuous transmission the TDR must be loaded before the stop bit(s) are ended. Figure 6 shows the relationship between IRQ and TxD for the Continuous Data Transmit mode.

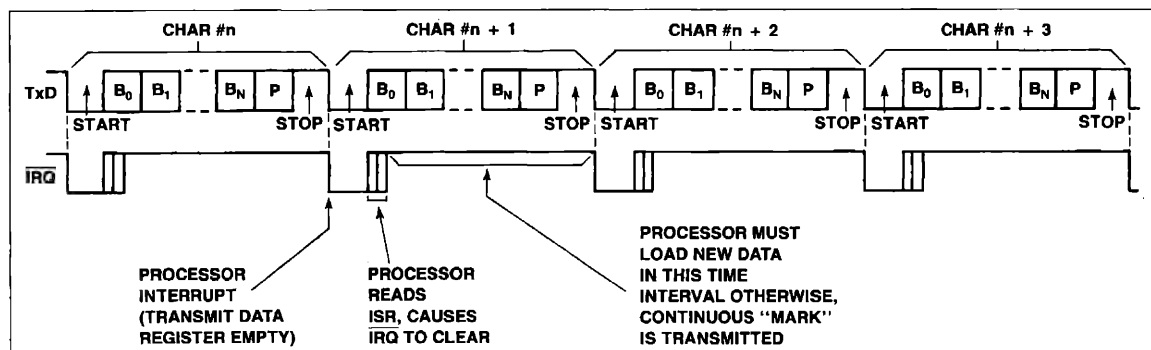


Figure 6. Continuous Data Transmit

CONTINUOUS DATA RECEIVE

Similar to the continuous data transmit mode, the normal receive mode sets the RDRF bit in the ISR when the DACIA has received

a full data word. This occurs at about the 9/16 point through the stop bit. The processor must read the RDR before the next stop bit, or an overrun error occurs. Figure 7 shows the relationship between IRQ and RxD for the continuous Data Receive mode.

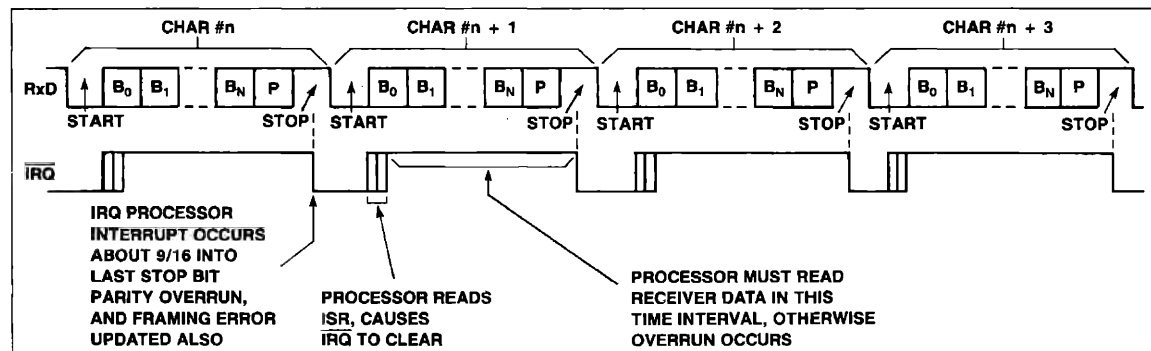


Figure 7. Continuous Data Receive

TRANSMIT UNDERRUN CONDITION

If the MPU is unable to load the TDR before the last stop bit is sent, the Tx_D line goes to the MARK condition and the underrun

flag is set. This condition persists until the TDR is loaded with a new word. Figure 8 shows the relation between IR_Q and Tx_D for the Transmit Underrun Condition.

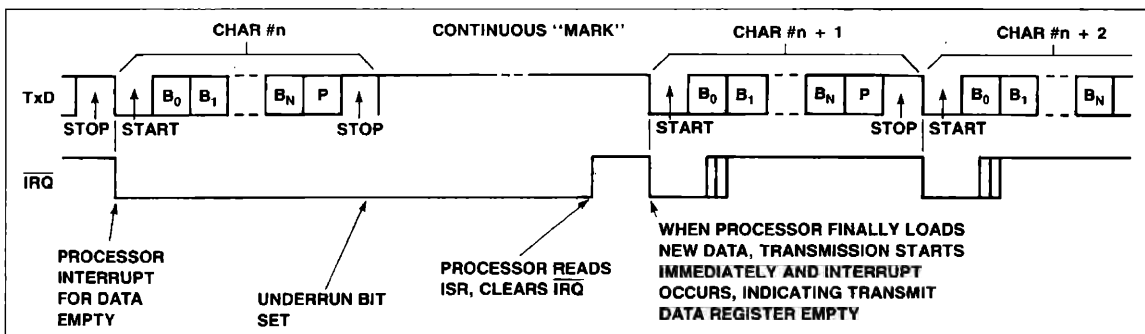


Figure 8. Transmit Underrun Condition Relationship

EFFECTS OF CTS ON TRANSMITTER

The CTS control line controls the transmission of data or the handshaking of data to a "busy" device (such as a printer). When the CTS line is low, the transmitter operates normally. Any transition on this line sets the CTS bit in the ISR. A high condition inhibits

the TDRE bit in the ISR from becoming set. The word currently in the shift register continues to be sent but any word in the TDR is held until CTS goes low. At the high-to-low transition the CTS bit in the ISR is again set. Figure 9 shows the relationship of IR_Q, Tx_D, and CTS for the effects of CTS on the transmitter.

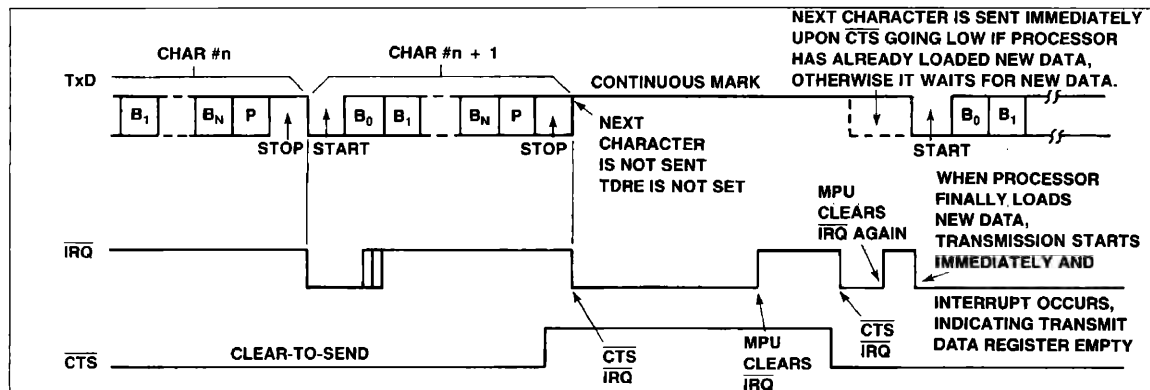


Figure 9. Effects of CTS on Transmitter

EFFECTS OF OVERRUN ON RECEIVER

If the processor does not read the RDR before the stop bit of the next word, an overrun error occurs, the overrun bit is set in the ISR, and the new data word is not transferred to the RDR. The

RDR contains the last word not read by the MPU and all following data is lost. The receiver will return to normal operation when the RDR is read. Figure 10 shows the relation of IRQ and RxD for the effects of overrun on the receiver.

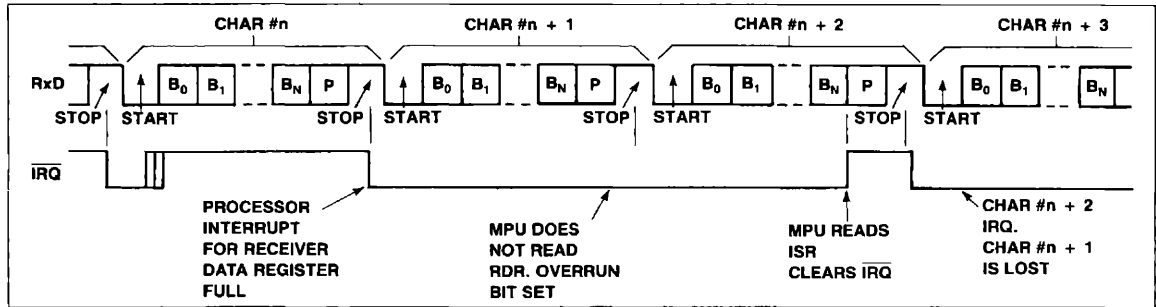


Figure 10. Effects of Overrun on Receiver

ECHO MODE TIMING

In the Echo Mode, the Tx/D line re-transmits the data received on the RxD line, delayed by 1/2 of a bit time. An internal underrun mode must occur before Echo Mode will start transmitting. In nor-

mal transmit mode if TDRE occurs (indicating end of data) an underflow flag would be set and continuous Mark transmitted. If Echo is initiated, the underflow flag will not be set at end of data and continuous Mark will not be transmitted. Figure 11 shows the relationship of RxD and Tx/D for Echo Mode.

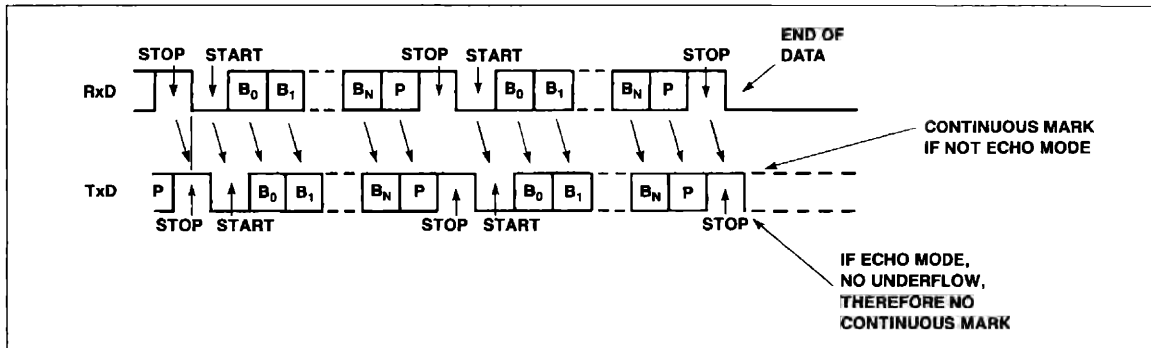


Figure 11. Echo Mode Timing

quent data words are tested separately, so the status bit always reflects the last data word received. Figure 12 shows the relationship of $\overline{\text{IRQ}}$ and RxD when a framing error occurs.

Figure 12. Framing Error

\$00 is stored in the IER at which time a stop bit is sent and transmission may resume. At least one full word time of Break will be sent regardless of the length of time between starting and stopping the Break character. Figure 13 shows the relationship of IRQ and Tx/D for a Transmit Break character.

Figure 13. Transmit Break Character

RECEIVE BREAK CHARACTER

In the event that a Break character is received by the receiver, the Break bit is set. The receiver does not set the RDRF bit and

remains in this state until a stop bit is received. At this time the next character is to be received normally. Figure 14 shows the relationship of $\overline{\text{IRQ}}$ and RxD for a Receive Break Character.

1

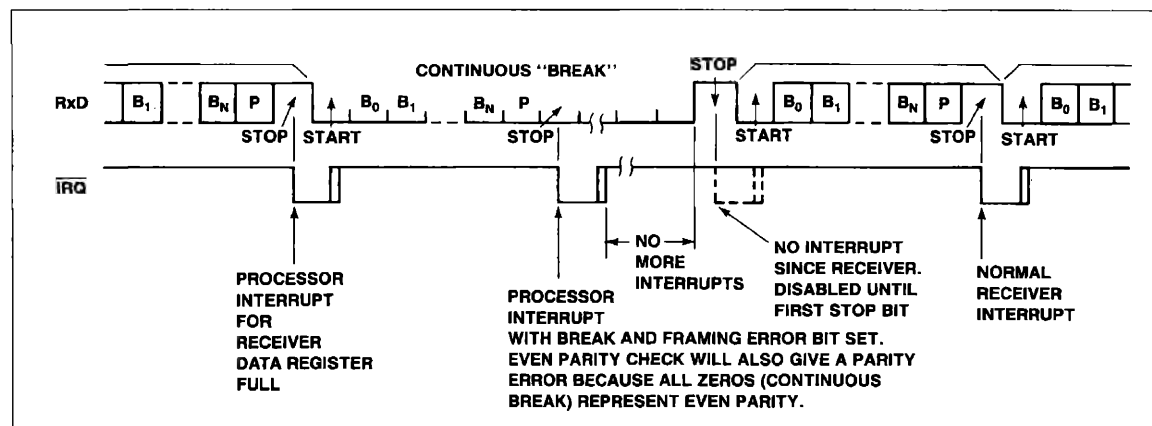


Figure 14. Receive Break Character

AUTOMATIC ADDRESS RECOGNITION

The DACIA offers a unique solution to the standard problem associated with multi-drop environment UARTs and communication interface controllers. In the standard configuration used by other devices, the slave CPU must be constantly interrupted to analyze incoming characters on the communications net to determine if an address word is present and if so, does that address match the address assigned to the slave UART. This CPU interrupt scheme can become intolerable in very large multi-drop networks because every slave on the communications net must "wake-up" its CPU for every character sent down the network by the master. The end results is that the CPUs on the communications net are constantly being interrupted for the mundane task of address recognition.

To avoid this constant CPU interrupt problem, the DACIA has been designed to do address comparison and recognition internally without the need for CPU intervention. Therefore, the slave CPU is not interrupted until the DACIA has determined that the character sent over the communications net by the master was an address and the address matched the address stored in the DACIA Compare Register. At this point the DACIA interrupts the CPU, goes out of Compare Mode, and receives the string of characters being transmitted by the master, (i.e., the data

characters). When all data has been received by the slave, it's CPU must again write the slave address into the DACIA Compare Register which automatically puts it back into the Compare Mode, waiting for another address character.

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the CFR Control Register, as shown in Table 4.

Generating Other Baud Rates

By using a different crystal, other baud rates may be generated.

These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the DACIA with an off-chip oscillator to achieve other baud rates. In this case, XTAL1 (pin 3) must be the clock input and XTAL0 (pin 4) must be a nonconnect.

Table 4. Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 3.6864 MHz Crystal	Baud Rate Generated With a Crystal of Frequency (f)
3	2	1	0			
0	0	0	0	73,728	$(3.6864 \times 10^6)/73,728 = 50$	$f/73,728$
0	0	0	1	33,538	$(3.6864 \times 10^6)/33,538 = 109.92$	$f/33,538$
0	0	1	0	27,408	$(3.6864 \times 10^6)/27,408 = 134.58$	$f/27,408$
0	0	1	1	24,576	$(3.6864 \times 10^6)/24,576 = 150$	$f/24,576$
0	1	0	0	12,288	$(3.6864 \times 10^6)/12,288 = 300$	$f/12,288$
0	1	0	1	6,144	$(3.6864 \times 10^6)/6,144 = 600$	$f/6,144$
0	1	1	0	3,072	$(3.6864 \times 10^6)/3,072 = 1,200$	$f/3,072$
0	1	1	1	2,048	$(3.6864 \times 10^6)/2,048 = 1,800$	$f/2,048$
1	0	0	0	1,536	$(3.6864 \times 10^6)/1,536 = 2,400$	$f/1,536$
1	0	0	1	1,024	$(3.6864 \times 10^6)/1,024 = 3,600$	$f/1,024$
1	0	1	0	768	$(3.6864 \times 10^6)/768 = 4,800$	$f/768$
1	0	1	1	512	$(3.6864 \times 10^6)/512 = 7,200$	$f/512$
1	1	0	0	384	$(3.6864 \times 10^6)/384 = 9,600$	$f/384$
1	1	0	1	192	$(3.6864 \times 10^6)/192 = 19,200$	$f/192$
1	1	1	0	96	$(3.6864 \times 10^6)/96 = 38,400$	$f/96$
1	1	1	1	16	$TxC/16 = \text{Baud Rate or } RxC/16 = \text{Baud Rate}$	

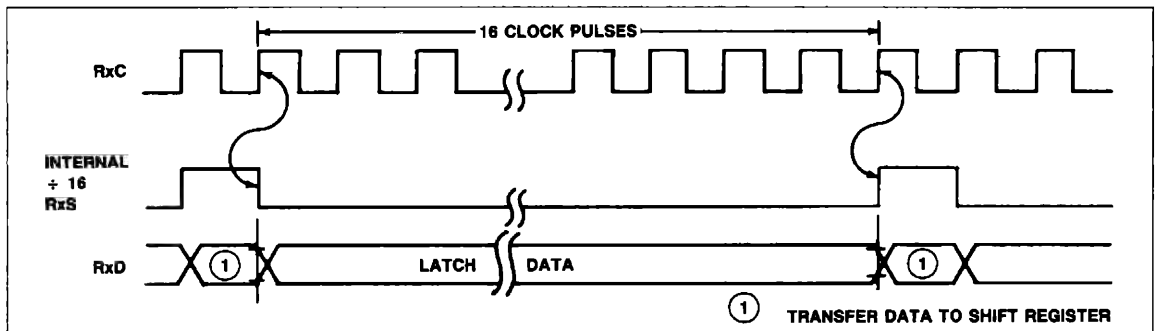


Figure 15. DACIA External Clock Timing — Receive Data

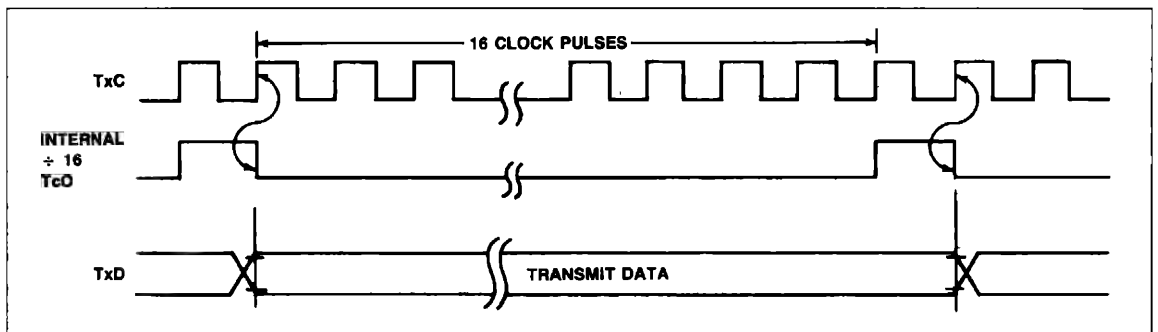
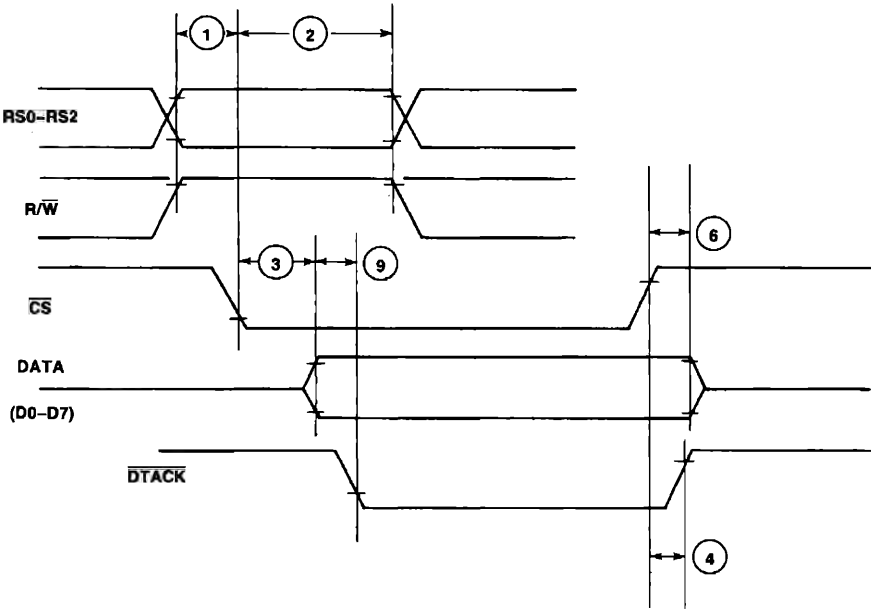
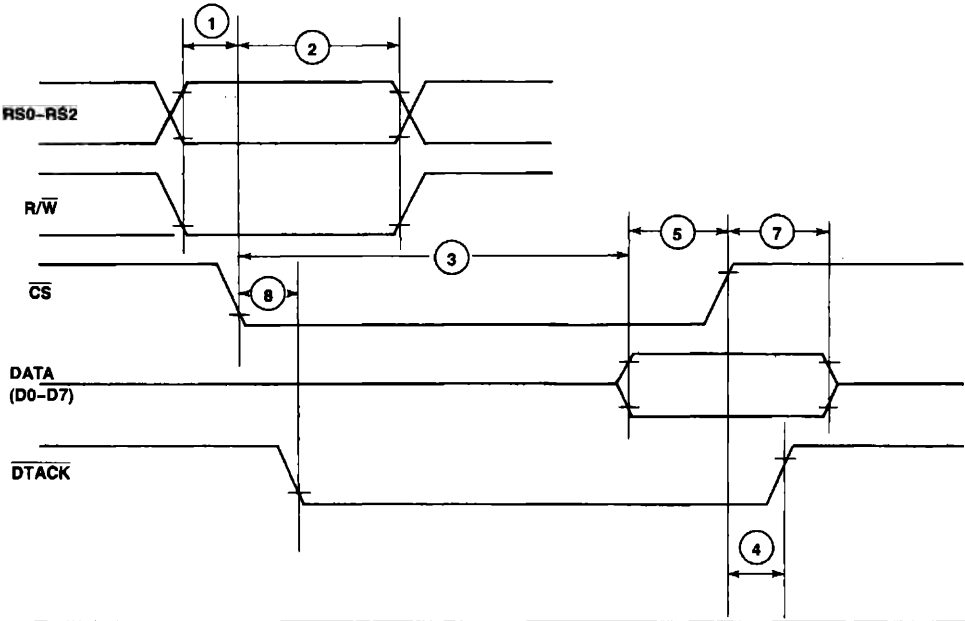


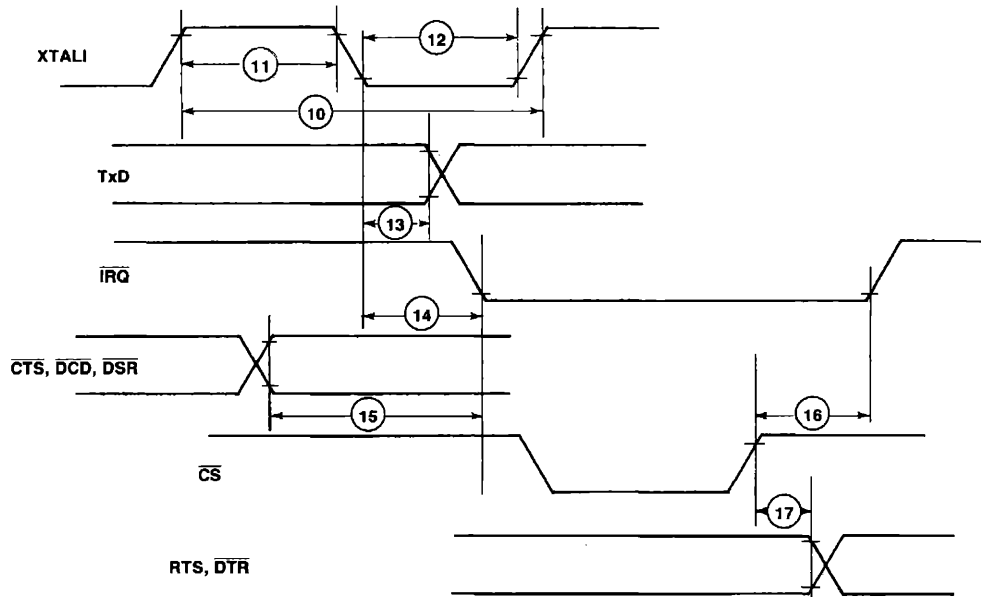
Figure 16. DACIA External Clock Timing — Transmit Data



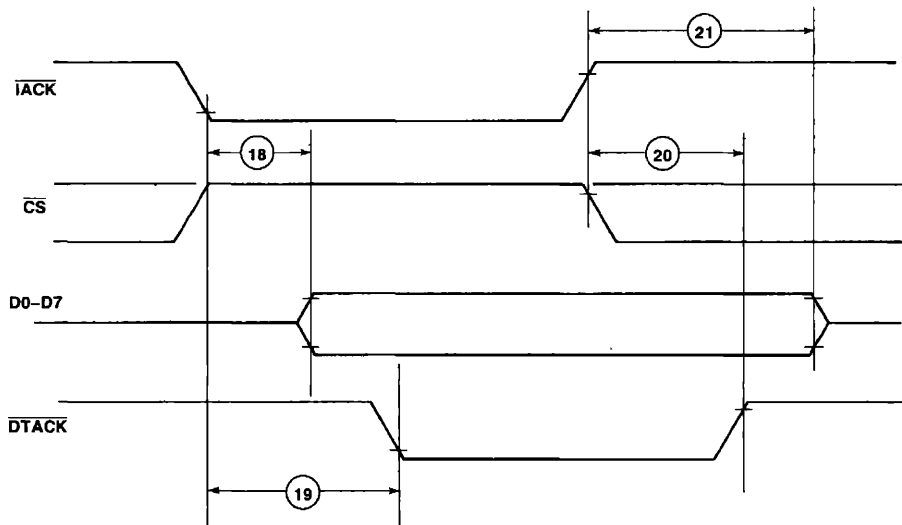
DACIA Read Cycle Timing



DACIA Write Cycle Timing



DACIA Transmit/Receiver Timing



DACIA Interrupt Acknowledge Timing

SPECIFICATIONS

AC CHARACTERISTICS

($V_{CC} = 5 \text{ Vdc} \pm 5\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = T_L$ to T_H , unless otherwise noted)

Number	Characteristic	Symbol	Min.	Max.	Unit
--------	----------------	--------	------	------	------

READ/WRITE TIMING

1	R/W, RS0–RS2 Valid to \overline{CS} Low (Setup)	t_{RVCL}	0	—	ns
2	\overline{CS} Low to R/W, RS0–RS2 Read (Hold Time)	t_{CLRv}	65	—	ns
3	\overline{CS} Low to Data Valid	t_{CLDV}	—	100	ns
4	\overline{CS} High to \overline{DTACK} High	t_{CHTH}	—	10	ns
5	Data Valid to \overline{CS} High	t_{DVCH}	20	—	ns
6	\overline{CS} High to Data Invalid (Read)	t_{CHDZ}	10	30	ns
7	\overline{CS} High to Data Invalid (Write)	t_{CHDZ}	—	40	ns
8	\overline{CS} Low to \overline{DTACK} Low (Write)	t_{CLTL}	0	—	ns
9	Data Valid to \overline{DTACK} Low (Read)	t_{DVTL}	0	—	ns

TRANSMIT/RECEIVE TIMING

10	Transmit/Receive Clock Rate	t_{CY}	250	—	ns
11	Transmit/Receive Clock High	t_{CH}	100	—	ns
12	Transmit/Receive Clock Low	t_{LL}	100	—	ns
13	XTALI to TxD Propagation Delay	t_{CLTD}	—	250	ns
14	XTALI to \overline{IRQ} Propagation Delay	t_{CLID}	—	250	ns
15	\overline{CTS} , \overline{DCD} , \overline{DSR} Valid to \overline{IRQ} Low	t_{SVIL}	—	150	ns
16	\overline{IRQ} Propagation Delay (Clear)	t_{IRQC}	—	150	ns
17	\overline{RTS} , \overline{DTR} Propagation Delay	t_{RDPD}	—	150	ns

INTERRUPT ACKNOWLEDGE TIMING

18	\overline{IACK} Low to Data Valid	t_{ILDV}	—	100	ns
19	\overline{IACK} Low to \overline{DTACK} Low	t_{ILTL}	0	—	ns
20	\overline{IACK} High to \overline{DTACK} High	t_{IHTH}	0	—	ns
21	\overline{IACK} High to Data Invalid	t_{IHDZ}	10	30	ns

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	Vdc
Output Voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	Vdc
Operating Temperature Commercial Industrial	T_A	0 to +70 -40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V \pm 5%
Temperature Range Commercial Industrial	T_A	0 to 70°C -40°C to +85°C

DC CHARACTERISTICS

($V_{CC} = 5.0\text{ V} \pm 5\%$, $V_{SS} = 0$, $T_A = T_L$ to T_H , unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTALI and XTALO XTALI and XTALO	V_{IH}	+2.0 +2.4	— —	$V_{CC} + 0.3$ $V_{CC} + 0.3$	V	
Input Low Voltage Except XTALI and XTALO XTALI and XTALO	V_{IL}	-0.3 -0.3	— —	+0.8 +0.4	V	
Input Leakage Current R/W, RES, RS0, RS1, RS2, RxD, \overline{CTS} , \overline{DCD} , \overline{DSR} , \overline{RxC} , \overline{TxC} , CS, IACK	I_{IN}	—	10	50	μA	$V_{IN} = 0\text{V to } 5.0\text{V}$ $V_{CC} = 5.25\text{V}$
Input Leakage Current for Three-State Off D0-D7	I_{TSI}	—	± 2	10	μA	$V_{IN} = 0.4\text{V to } 2.4\text{V}$ $V_{CC} = 5.25\text{V}$
Output High Voltage D0-D7, TxD, CLK OUT, RTS, DTR	V_{OH}	+2.4 1.5	— —	— —	V	$V_{CC} = 4.75\text{V}$ $I_{LOAD} = -100\text{ }\mu\text{A}$
Output Low Voltage D0-D7, TxD, CLK OUT, RTS', DTR	V_{OL}	—	—	+0.4	V	$V_{CC} = 4.75\text{V}$ $I_{LOAD} = 1.6\text{ mA}$
Output Leakage Current (Off State) IRQ, DTACK	I_{OFF}	—	± 2	± 10	μA	$V_{CC} = 5.25\text{V}$ $V_{OUT} = 0\text{ to } 2.4\text{V}$
Power Dissipation	P_D	—	—	10	mW/MHz	
Input Capacitance Except XTALI and XTALO XTALI and XTALO	C_{IN}	— —	— —	5 10	pF pF	$V_{CC} = 5.0\text{V}$ $V_{IN} = 0\text{V}$ $f = 2\text{ MHz}$ $T_A = 25^\circ\text{C}$
Output Capacitance	C_{OUT}	—	—	10	pF	

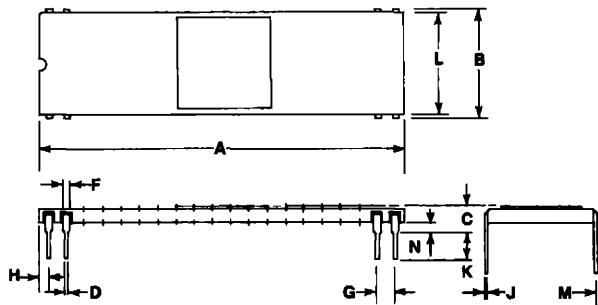
Notes:

1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.

PACKAGE DIMENSIONS

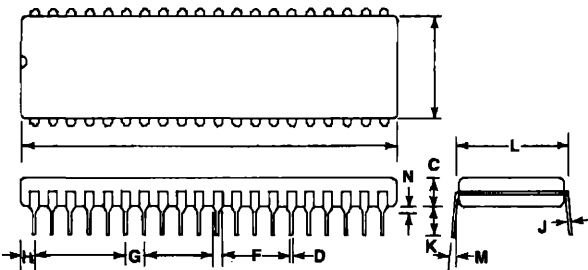
1

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.88	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
V	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

SECTION 2

8-BIT MICROPROCESSORS AND PERIPHERALS

2

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R6500 MICROPROCESSOR AND PERIPHERAL FAMILY

Fastest Executing, Largest Selling 8-Bit Family Now Also In CMOS

There is no microprocessor family easier to implement than the R6500. It's the fastest instruction executing 8-bit family. It's software compatible with a family of single-chip microcomputers. It's available in NMOS and CMOS versions. It has a wide variety of CPUs and peripheral controllers and versatile memory-I/O-timer combinations.

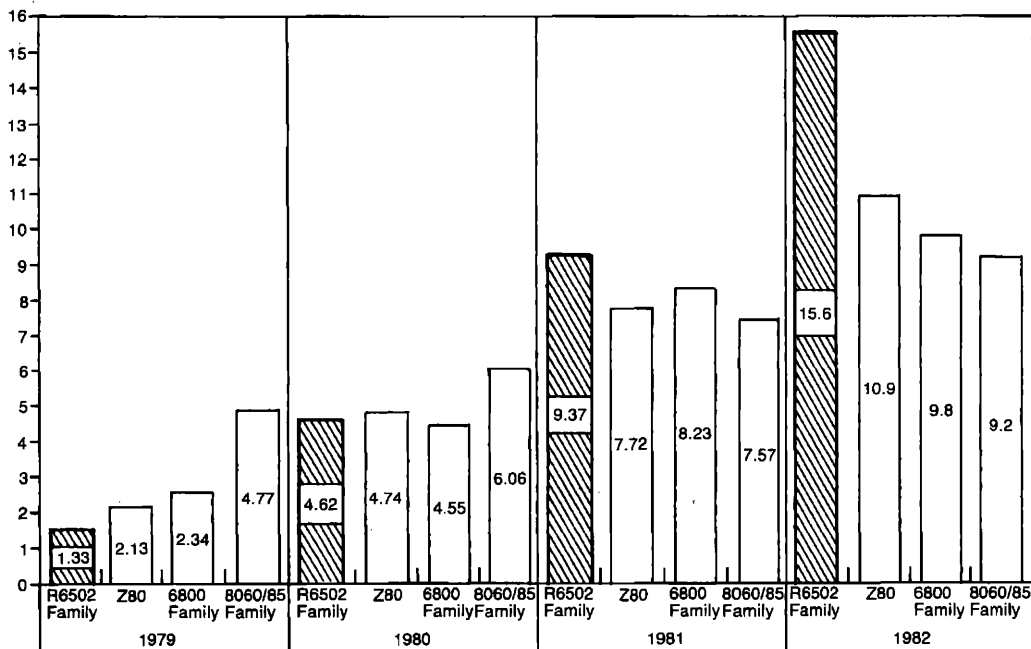
In the 8-bit range, nothing gives higher performance than this third generation microprocessor family. Pipeline architecture provides much faster instruction execution (1 μ sec). Thirteen address modes provide the most efficient ways of addressing memory. R6500 peripherals are system oriented, designed to implement systems with minimum chips.

And now, it's available in CMOS, for even higher speed, low power applications—the R65C00 family. It's now possible to move complete product and system designs directly into CMOS, being downward software compatible with the NMOS R6500 family.

Because of its inherent characteristics, the advanced Rockwell CMOS provides low power consumption, high noise immunity and high speed operation. Its 2 MHz CPU dissipates only 40 mW (compared to 700-800 mW in NMOS) and requires only 10 μ A standby current. Instructions can be executed in only 500 nanoseconds. Instruction memory requirements are 20% less due to added bit manipulation features. And, there are even more advantages.

The entire 8-bit R6500 family is upward compatible with the 16-bit R68000 bus, software compatible to the R6500/-single-chip microcomputers and are the building blocks for the RM 65 module family and AIM 65 board microcomputer families, for a wide range of system applications. There's no wonder it's one of the world's largest selling families of microprocessors, as documented by Dataquest. (See below)

Millions of Units



Source: Dataquest—April 1983

Estimated Worldwide Shipments of Multisourced 8-Bit Microprocessors



R650X and R651X MICROPROCESSORS (CPU)

2

DESCRIPTION

The 8-bit R6500 microprocessor devices are produced with N-channel, silicon gate technology. Its performance speeds are enhanced by advanced system architecture. This innovative architecture results in smaller chips—the semiconductor threshold is cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, described in this document. Rockwell also provides single chip microcomputers, memory and peripheral devices—as well as low-cost design aids and documentation.

Ten CPU devices are available. All are software-compatible. They provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. All are bus-compatible with earlier generation microprocessors like the M6800 devices.

The R650X and R651X family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory. All R6500 microprocessors are also available in a variety of packaging (ceramic and plastic), operating frequency (1 MHz, 2 MHz and 3 MHz) and temperature (commercial and industrial) versions.

ORDERING INFORMATION

Part Number: R65XX_ _ _

Temperature Range (T_L to T_H):

No letter = 0°C to $+70^{\circ}\text{C}$

E = -40°C to $+85^{\circ}\text{C}$

Package:

C = Ceramic

P = Plastic

Frequency Range:

No letter = 1 MHz

A = 2 MHz

B = 3 MHz

Model Designator:

XX = 02, 03, 04, ... 15

FEATURES

- N-channel, silicon gate, depletion load technology
- 8-bit parallel processing
- 56 instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt request
- Non-maskable interrupt
- Use with any type of speed memory
- 8-bit bidirectional data bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct Memory Access capability
- Bus compatible with M6800
- 1 MHz, 2 MHz, and 3 MHz versions
- Choice of external or on-chip clocks
- On-chip clock options
 - External single clock input
 - Crystal time base input
- Commercial and industrial temperature versions
- Pipeline architecture
- Single +5V supply

R6500 CPU FAMILY MEMBERS

Microprocessors with Internal Two Phase Clock Generator

Model	No. Pins	Addressable Memory
R6502	40	64K Bytes
R6503	28	4K Bytes
R6504	28	8K Bytes
R6505	28	4K Bytes
R6506	28	4K Bytes
R6507	28	8K Bytes

Microprocessors with External Two Phase Clock Input

Model	No. Pins	Addressable Memory
R6512	40	64K Bytes
R6513	28	4K Bytes
R6514	28	8K Bytes
R6515	28	4K Bytes

INTERFACE SIGNAL DESCRIPTIONS

CLOCKS ($\phi 1$, $\phi 2$)

The R651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level. The R650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

ADDRESS BUS (A0-A15, R6502)

The address line outputs access data in memory device locations or cells, access data in I/O device registers and/or effect logical operations in I/O or controller devices depending on system design. The addressing range is determined by the number of address lines available on the particular CPU device. The R6502 and R6512 can address 64K bytes with a 16-bit address bus (A0-A15); the R6504, R6507, and the R6514 can address 8K bytes with a 13-bit address bus (A0-A12); and the R6503, R6505, R6506, R6513, and R6515 can address 4K bytes with a 12-bit address bus (A0-A11). These outputs are TTL-compatible and are capable of driving one standard TTL load and 130 pF.

DATA BUS (D0-D7)

The data lines (D0-D7) form an 8-bit bidirectional data bus which transfers data between the CPU and memory or peripheral devices. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

DATA BUS ENABLE (DBE, R6512 ONLY)

The TTL-compatible DBE input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE is driven by the phase two ($\phi 2$) clock, thus allowing data output from microprocessor only during $\phi 2$. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

READY (RDY)

The Ready input signal allows the user to halt or single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one ($\phi 1$) will halt the microprocessor with the output address lines reflecting the current address being fetched. If Ready is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent phase two ($\phi 2$) in which the Ready signal is low. This feature allows microprocessor interfacing with the low speed PROMs as well as Direct Memory Access (DMA).

INTERRUPT REQUEST (\overline{IRQ})

The TTL level active-low \overline{IRQ} input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Processor Status Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register

are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts can occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K Ω external resistor should be used for proper wire-OR operation.

NON-MASKABLE INTERRUPT (\overline{NMI})

A negative going edge on the \overline{NMI} input requests that a non-maskable interrupt sequence be generated within the microprocessor.

\overline{NMI} is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for \overline{IRQ} will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

\overline{NMI} also requires an external 3K Ω resistor to V_{CC} for proper wire-OR operations.

Inputs \overline{IRQ} and \overline{NMI} are hardware interrupts lines that are sampled during $\phi 2$ (phase 2) and will begin the appropriate interrupt routine on the $\phi 1$ (phase 1) following the completion of the current instruction.

SET OVERFLOW FLAG (\overline{SO})

A negative going edge on the \overline{SO} input sets the overflow bit in the Processor Status Register. This signal is sampled on the trailing edge of $\phi 1$ and must be externally synchronized.

SYNC

The SYNC output line identifies those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\phi 1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\phi 1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

RESET (\overline{RES})

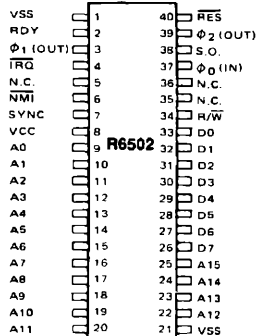
The active low \overline{RES} resets, or starts, the microprocessor from a power down or restart condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag is set and the microprocessor loads the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

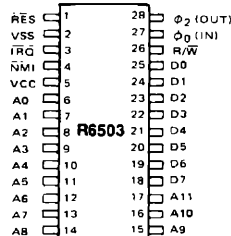
After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and SYNC signals become valid.

R6502 FEATURES

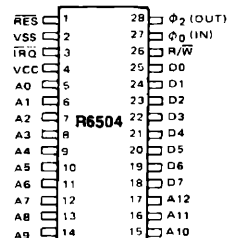
- 64K addressable bytes of memory (A0-A15)
- $\overline{\text{IRQ}}$ interrupt
- On-chip clock
 - TTL-level single phase input
 - RC time base input
 - crystal time base input
- SYNC signal
 - (can be used for single instruction execution)
- RDY signal
 - (can be used to halt or single cycle execution)
- Two phase output clock for timing of support chips
- $\overline{\text{NMI}}$ interrupt
- 40-pin DIP

**R6503 FEATURES**

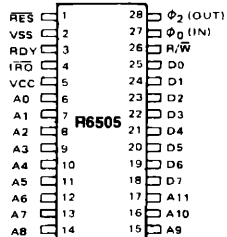
- 4K addressable bytes of memory (A0-A11)
- On-chip clock
- $\overline{\text{IRQ}}$ interrupt
- $\overline{\text{NMI}}$ interrupt
- 8-bit bidirectional data bus
- 28-pin DIP

**R6504 FEATURES**

- 8K addressable bytes of memory (A0-A12)
- On-chip clock
- $\overline{\text{IRQ}}$ interrupt
- 8-bit bidirectional data bus
- 28-pin DIP

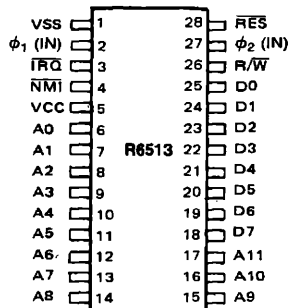
**R6505 FEATURES**

- 4K addressable bytes of memory (A0-A11)
- On-chip clock
- $\overline{\text{IRQ}}$ interrupt
- RDY signal
- 8-bit bidirectional data bus
- 28-pin DIP

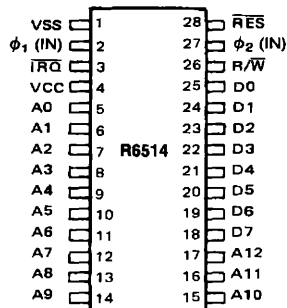


R6513 FEATURES

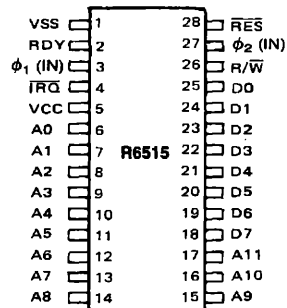
- 4K addressable bytes of memory (A0-A11)
- Two phase clock input
- $\overline{\text{IRQ}}$ interrupt
- $\overline{\text{NMI}}$ interrupt
- 8-bit bidirectional data bus
- 28-pin DIP

**R6514 FEATURES**

- 8K addressable bytes of memory (A0-A12)
- Two phase clock input
- $\overline{\text{IRQ}}$ interrupt
- 8-bit bidirectional data bus

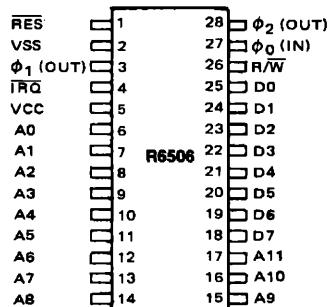
**R6515 FEATURES**

- 4K addressable bytes of memory (A0-A11)
- Two phase clock input
- $\overline{\text{IRQ}}$ interrupt
- RDY signal
- 8-bit bidirectional data bus

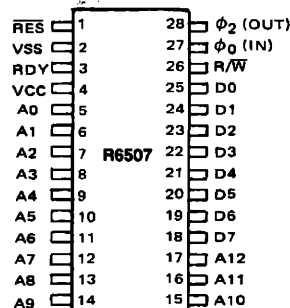


R6506 FEATURES

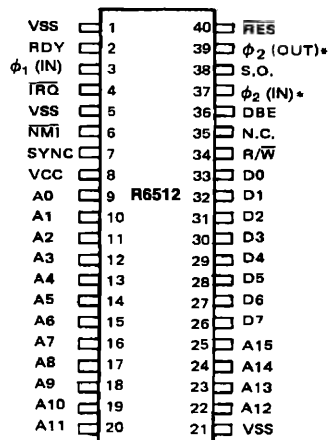
- 4K addressable bytes of memory (A0-A11)
- On-chip clock
- $\overline{\text{IRQ}}$ Interrupt
- Two phase output clock for timing of support chips
- 8-bit bidirectional data bus
- 28-pin DIP

**R6507 FEATURES**

- 8K addressable bytes of memory (A0-A12)
- On-chip clock
- RDY signal
- 8-bit bidirectional data bus
- 28-pin DIP

**R6512 FEATURES**

- 64K addressable bytes of memory (A0-A15)
- $\overline{\text{IRQ}}$ interrupt
- $\overline{\text{NMI}}$ interrupt
- RDY signal
- 8-bit bidirectional data bus
- SYNC signal
- Two phase clock input
- Data Bus Enable
- 40-pin DIP



*Pins 37 and 39 are connected internally

FUNCTIONAL DESCRIPTION

The internal organization of all R6500 CPUs is identical except for some variations in clock interface, the number of address output lines, and some unique input/output lines between versions.

CLOCK GENERATOR

The clock generator develops all internal clock signals, and (where applicable) external clock signals, associated with the device. It is the clock generator that drives the timing control unit and the external timing for slave mode operations.

TIMING CONTROL

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

PROGRAM COUNTER

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

INSTRUCTION REGISTER AND DECODE

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

ACCUMULATOR

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations, and in addition, the accumulator usually contains one of the two data words used in these operations.

INDEX REGISTERS

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

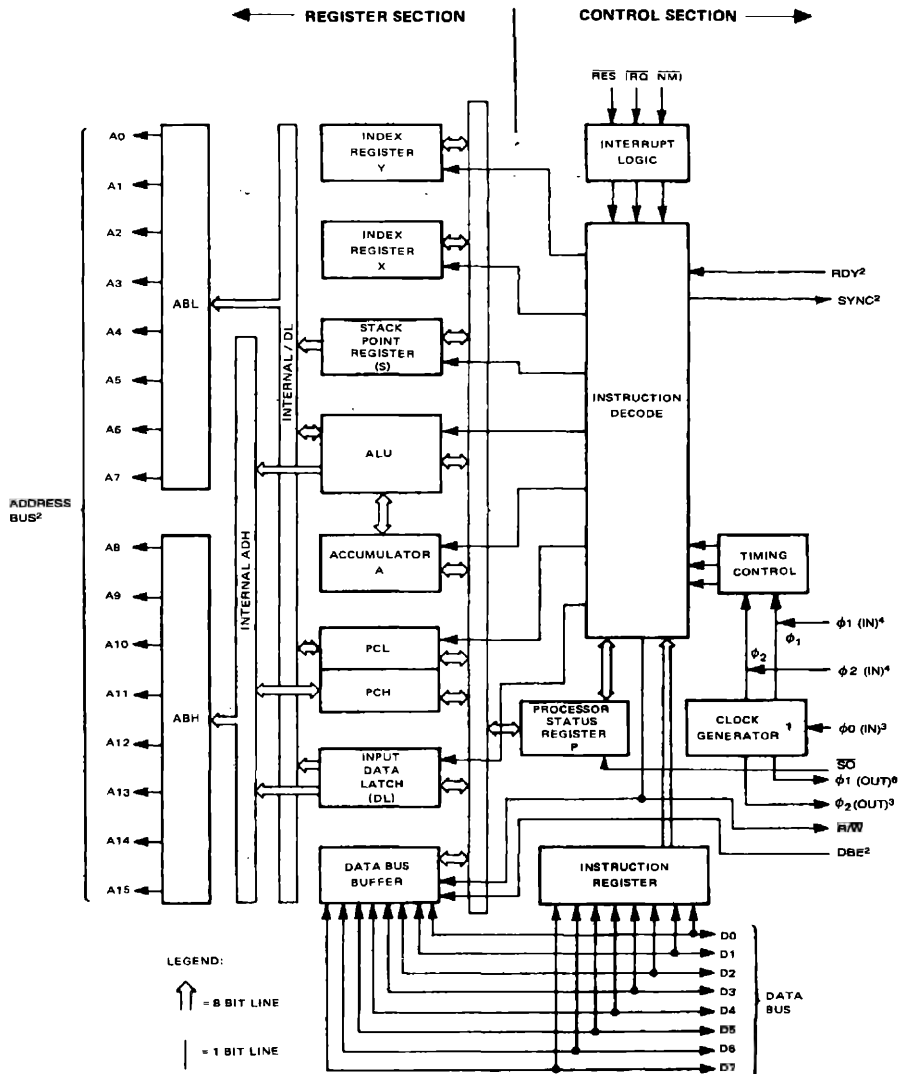
When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

STACK POINTER

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{\text{NMI}}$ and $\overline{\text{IRQ}}$). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

PROCESSOR STATUS REGISTER

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU.



R650X and R651X Internal Architecture

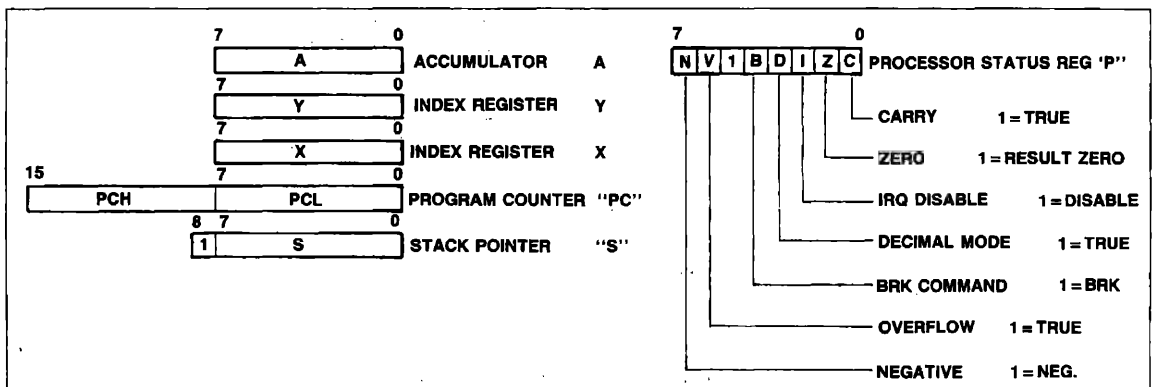
INSTRUCTION SET

The R6500 CPU has 56 instruction types which are enhanced by up to 13 addressing modes for each instruction. The accu-

mulator, index registers, Program Counter, Stack Pointer and Processor Status Register are illustrated below.

Alphabetic Listing of Instruction Set

Mnemonic	Function	Mnemonic	Function
ADC	Add Memory to Accumulator with Carry	JMP	Jump to New Location
AND	"AND" Memory with Accumulator	JSR	Jump to New Location Saving Return Address
ASL	Shift Left One Bit (Memory or Accumulator)		
BCC	Branch on Carry Clear	LDA	Load Accumulator with Memory
BCS	Branch on Carry Set	LDX	Load Index X with Memory
BEQ	Branch on Result Zero	LDY	Load Index Y with Memory
BIT	Test Bits in Memory with Accumulator	LSR	Shift One Bit Right (Memory or Accumulator)
BMI	Branch on Result Minus	NOP	No Operation
BNE	Branch on Result not Zero	ORA	"OR" Memory with Accumulator
BPL	Branch on Result Plus	PHA	Push Accumulator on Stack
BRK	Force Break	PHP	Push Processor Status on Stack
BVC	Branch on Overflow Clear	PLA	Pull Accumulator from Stack
BVS	Branch on Overflow Set	PLP	Pull Processor Status from Stack
CLC	Clear Carry Flag	ROL	Rotate One Bit Left (Memory or Accumulator)
CLD	Clear Decimal Mode	ROR	Rotate One Bit Right (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit	RTI	Return from Interrupt
CLV	Clear Overflow Flag	RTS	Return from Subroutine
CMP	Compare Memory and Accumulator		
CPX	Compare Memory and Index X	SBC	Subtract Memory from Accumulator with Borrow
CPY	Compare Memory and Index Y	SEC	Set Carry Flag
DEC	Decrement Memory by One	SED	Set Decimal Mode
DEX	Decrement Index X by One	SEI	Set Interrupt Disable Status
DEY	Decrement Index Y by One	STA	Store Accumulator in Memory
EOR	"Exclusive-OR" Memory with Accumulator	STX	Store Index X in Memory
INC	Increment Memory by One	STY	Store index Y in Memory
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index Y by One	TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
		TXA	Transfer Index X to Accumulator
		TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator



Programming Model

ADDRESSING MODES

The R6500 CPU family has 13 addressing modes. In the following discussion of these addressing modes, a bracketed expression follows the title of the mode. This expression is the term used in the Instruction Set Op Code Matrix table (later in this product description) to make it easier to identify the actual addressing mode used by the instruction.

ACCUMULATOR ADDRESSING [Accum]—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING [IMM]—In immediate addressing, the second byte of the instruction contains the operand, with no further memory addressing required.

ABSOLUTE ADDRESSING [Absolute]—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING [ZP]—The zero page instructions allow for shorter code and execution times by fetching only the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING [ZP, X or Y]—(X, Y indexing)—This form of addressing is used with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING [ABS, X or Y]—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X" and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain

the base address. This type of indexing allows any location referencing and the index to modify multiple fields, resulting in reduced coding and execution time.

IMPLIED ADDRESSING [Implied]—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING [Relative]—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING [(IND, X)]—In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents are the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING [(IND), Y]—In indirect indexed addressing (referred to as (Indirect, Y)), the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT [Indirect]—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter. (JMP (IND) only)

INSTRUCTION SET OP CODE MATRIX

The following matrix shows the Op Codes associated with the R6500 family of CPU devices. The matrix identifies the hexadecimal code, the mnemonic code, the addressing mode, the

number of instruction bytes, and the number of machine cycles associated with each Op Code. Also, refer to the instruction set summary for additional information on these Op Codes.

MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5		PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	
1	BPL Relative 2 2**	ORA (IND, Y) 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6		CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5		PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6		SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5		PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	
5	BVC Relative 2 2**	EOR (IND, Y) 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6		CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5		PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6		SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3		DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4		TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3		TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	
B	BCS Relative 2 2**	LDA (IND, Y) 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4		CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5		INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	
D	BNE Relative 2 2**	CMP (IND, Y) 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6		CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5		INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	
F	BEQ Relative 2 2**	SBC (IND, Y) 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6		SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

0	BRK Implied 1 7	—OP Code
		—Addressing Mode
		—Instruction Bytes; Machine Cycles

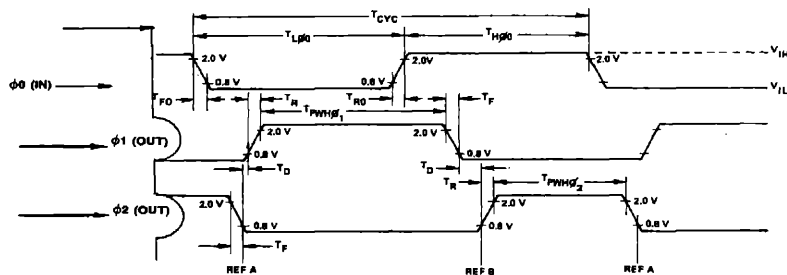
*Add 1 to N if page boundary is crossed.

**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

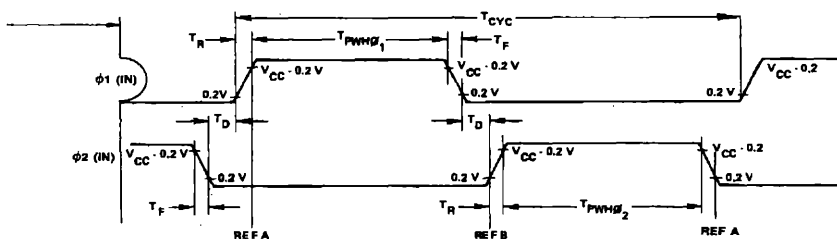
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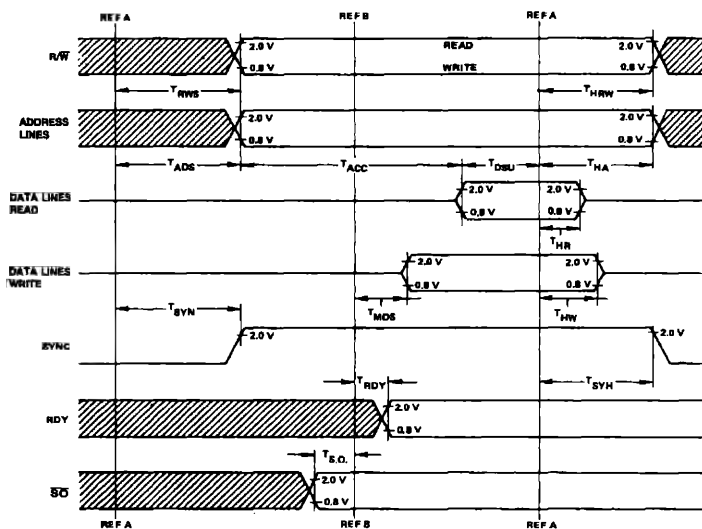
R650X CLOCK TIMING



R651X CLOCK TIMING



R65XX READ WRITE TIMING



AC CHARACTERISTICS

Characteristic	Symbol	R65XX (1 MHz)		R65XXA (2 MHz)		R65XXB (3 MHz)		Unit
		Min	Max	Min	Max	Min	Max	

R650X CLOCK TIMING

Clock Cycle Time	T_{CYC}	1.0	10	0.5	10	0.33	10	μs
$\phi 0$ (IN) Low Pulse Width	$T_{L\phi 0}$	480	—	240	—	160	—	ns
$\phi 0$ (IN) High Pulse Width	$T_{H\phi 0}$	460	—	240	—	160	—	ns
$\phi 0$ (IN) Rise and Fall Time ^{1, 2}	$T_{R\phi 0}, T_{F\phi 0}$	—	10	—	10	—	10	ns
$\phi 1$ (OUT) High Pulse Width	$T_{PWH\phi 1}$	460	—	235	—	155	—	ns
$\phi 2$ (OUT) High Pulse Width	$T_{PWH\phi 2}$	460	—	240	—	160	—	ns
Delay Between $\phi 1$ (OUT) and $\phi 2$ (OUT)	T_D	0	—	0	—	0	—	ns
$\phi 1$ (OUT), $\phi 2$ (OUT) Rise and Fall Time ^{1, 2}	$T_{R\phi 1}, T_{F\phi 1}$	—	25	—	25	—	15	ns

R651X CLOCK TIMING

Clock Cycle Time	T_{CYC}	1.0	10	0.5	10	0.33	10	μs
$\phi 1$ (IN) High Pulse Width	$T_{PWH\phi 1}$	430	—	215	—	150	—	ns
$\phi 2$ (IN) High Pulse Width	$T_{PWH\phi 2}$	470	—	235	—	160	—	ns
Delay Between $\phi 1$ and $\phi 2$	T_D	0	—	0	—	0	—	ns
$\phi 1$ (IN), $\phi 2$ (IN) Rise and Fall Time ^{1, 3}	$T_{R\phi 1}, T_{F\phi 1}$	—	25	—	20	—	15	ns

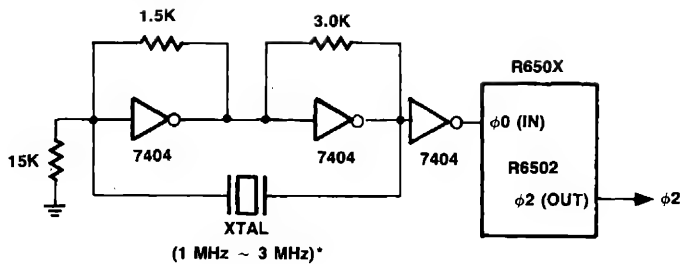
R65XX READ/WRITE TIMING

R/W Setup Time	T_{RWS}	—	225	—	140	—	110	ns
R/W Hold Time	T_{HRW}	30	—	30	—	15	—	ns
Address Setup Time	T_{ADS}	—	225	—	140	—	110	ns
Address Hold Time	T_{HA}	30	—	30	—	15	—	ns
Read Access Time	T_{ACC}	—	650	—	310	—	170	ns
Read Data Setup Time	T_{DSU}	100	—	50	—	50	—	ns
Read Data Hold Time	T_{HR}	10	—	10	—	10	—	ns
Write Data Setup Time	T_{MDS}	—	175	—	100	—	85	ns
Write Data Hold Time	T_{HW}	30	—	30	—	15	—	ns
SYNC Hold Time	T_{SYH}	30	—	30	—	15	—	ns
RDY Setup Time	T_{RDY}	100	—	50	—	35	—	ns
\overline{SO} Setup Time	T_{SO}	100	—	50	—	35	—	ns
SYNC Setup Time	T_{SYN}	—	225	—	140	—	110	ns

Notes:

1. Loads: All output except clocks = 1 TTL + 130 pF. Clock outputs = 1 TTL + 30 pF.
2. Measured between 0.8 and 2.0 points on waveform load.
3. Measured between 10% and 90% points on waveforms.
4. *RDY must never switch states within T_{RDY} to end of $\phi 2$.

RECOMMENDED TIME BASE GENERATION FOR R6502



*CRYSTAL: CTS KNIGHTS MP SERIES, OR EQUIVALENT

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Range Commercial Industrial	T_A		°C
		-40 to +85	
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V \pm 5%
Temperature Range Commercial Industrial	T_A	0°C to 70°C -40°C to +85°C

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0$, $T_A = T_L$ to T_H , unless otherwise noted)

Parameter	Symbol	Min.	Typ. ⁵	Max.	Unit ¹	Test Conditions
Input High Voltage Logic, $\emptyset 0$ (IN) $\emptyset 1$ (IN), $\emptyset 2$ (IN)	V_{IH}	2.0 $V_{CC} - 0.3$	— —	V_{CC} $V_{CC} + 0.25$	V	
Input Low Voltage Logic, $\emptyset 0$ (IN) $\emptyset 1$ (IN), $\emptyset 2$ (IN)	V_{IL}	-0.3 -0.3	— —	0.8 0.4	V	
Input Leakage Current Logic (Excl. RDY, S.O.) $\emptyset 1$ (IN), $\emptyset 2$ (IN) $\emptyset 0$ (IN)	I_{IN}	— — —	— — —	2.5 100 10	μA	$V_{IN} = 0V$ to 5.25V $V_{CC} = 0V$
Input Leakage Current for Three State Off D0-D7	I_{TSI}	—	—	10	μA	$V_{IN} = 0.4V$ to 2.4V $V_{CC} = 5.25V$
Output High Voltage SYNC, D0-D7, A0-A15, R/\overline{W} , $\emptyset 1$ (OUT), $\emptyset 2$ (OUT)	V_{OH}	+2.4	—	—	V	$I_{LOAD} = -100 \mu A$ $V_{CC} = 4.75V$
Output Low Voltage SYNC, D0-D7, A0-A15, R/\overline{W} , $\emptyset 1$ (OUT), $\emptyset 2$ (OUT)	V_{OL}	—	—	+0.4	V	$I_{LOAD} = 1.6 mA$ $V_{CC} = 4.75V$
Power Dissipation 1 and 2 MHz 3 MHz	P_D	— —	450 500	700 800	mW	
Capacitance Logic D0-D7 A0-A15, R/\overline{W} , SYNC $\emptyset 0$ (IN) $\emptyset 1$ (IN) $\emptyset 2$ (IN)	C C_{IN} — — C_{OUT} $C_{\emptyset 0(IN)}$ $C_{\emptyset 1}$ $C_{\emptyset 2}$	— — — — — — — —	— — — — — 30 50	10 15 12 15 50 80	pF	$V_{CC} = 5.0V$ $V_{IN} = 0V$ $f = 1 MHz$ $T_A = 25^\circ C$

Notes:

- All units are direct current (dc) except for capacitance.
- Negative sign indicates outward current flow, positive indicates inward flow.
- IRQ and NMI require 3K pull-up resistor.
- $\emptyset 1$ (IN) and $\emptyset 2$ (IN) apply to R6512, 13, 14, and 15; $\emptyset 0$ (IN) applies to R6502, 03, 04, 05, 06 and 07.
- Typical values shown for $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.



R6501Q AND R6511 Q **ONE-CHIP MICROPROCESSOR**

INTRODUCTION

The Rockwell R6501Q and R6511Q are extended, high performance 8-bit NMOS-3, single chip microprocessors, and are compatible with all members of the R6500 family.

The devices contain an enhanced R6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory, and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability. A full 16-bit address bus and 8-bit data bus provide accessing to 65K bytes of external memory.

The devices come in a 64-pin Quad Inline package (QUIP).

The devices may be used as a CPU-RAM-I/O counter device in multichip systems or as an emulator for the R6500/11 family of microcomputers. They provide all R6500/11 interface lines, plus the address bus, data bus and control lines to interface with external memory.

SYSTEMS DEVELOPMENT

Rockwell supports development of the devices with the Rockwell Design Center System and the R6500/* Personality Set: Complete in-circuit emulation with the Personality Set allows total systems test and evaluation.

This data sheet is for the reader familiar with the R6502 CPU hardware and programming capabilities. For additional information see the R6501Q Product Description, (Document Order Number 2145) or the R6511Q Product Description, (Document Order Number 2133).

ORDERING INFORMATION

Part Number	Package Type	Frequency Option	Temp. Range
R6501Q	Plastic (QUIP)	1 MHz	0°C to 70°C
R6501AQ	Plastic (QUIP)	2 MHz	0°C to 70°C
R6511Q	Plastic (QUIP)	1 MHz	0°C to 70°C
R6511AQ	Plastic (QUIP)	2 MHz	0°C to 70°C

FEATURES

- Enhanced R6502 CPU
 - Four new bit manipulation instructions
 - Set Memory Bit (SMB)
 - Reset Memory Bit (RMB)
 - Branch on Bit Set (BBS)
 - Branch on Bit Reset (BBR)
 - Decimal and binary arithmetic modes
 - 13 Addressing modes
 - True indexing

- 192-byte static RAM
- 32 bidirectional, TTL-compatible I/O lines (four ports)
- One 8-bit port may be tri-stated under software control
- One 8-bit port may have latched inputs under software control
- Two 16-bit programmable counter/timers, with 3 latches
 - Pulse width measurement
 - Pulse generation (1 symmetrical, 1 asymmetrical)
 - Interval timer
 - Event counter
 - Retriggerable interval timer
- Serial Port — Full Duplex, Buffered UART
 - Receiver Wake Up and Transmitter End of Transmission Features
 - Programmable Standard Asynchronous Baud Rates from 50 to 125K bits/sec at 2 MHz
 - Satisfies SMPTE 422 Broadcast Standard (8 Data, Parity, 1 Stop) at 38.4K bits/sec
 - Programmable 5-8 bit Character Lengths, with or without parity
 - Receiver Error Detection for Framing, Parity, and Overrun
 - Synchronous Shift Register alternate mode (250KC at 2 MHz)
- Ten interrupts
 - Four edge-sensitive lines; two positive, two negative
 - Two counter underflows
 - Serial data receiver buffer full
 - Serial data transmitter buffer empty
 - Non-maskable
 - Reset
- Full data and address pins for 65K bytes of external memory
- Flexible clock circuitry
 - 2 MHz or 1 MHz internal operation
 - Internal clock with external XTAL at four times internal frequency (R6501Q) or two times internal frequency (R6511Q)
 - External clock input divided by one or four (R6501Q) or one or two (R6511Q)
- 68% of the instructions have execution times less than 2 μ s at 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- 65-pin QUIP
- R6501Q has pullup resistors on PA, PB, and PC
- R6511Q has no pullup resistors

FUNCTIONAL DESCRIPTION

CENTRAL PROCESSING UNIT (CPU)

The internal CPU of the device is a standard R6502 configuration with the standard R6502 instructions plus 4 new bit manipulation instructions. These new bit manipulator instructions form an enhanced R6502 instruction set and improve memory utilization efficiency and performance.

Set Memory Bit (SMB #,ADDR.)

This instruction sets to "1" one bit of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and which one of 8 bits to be set. The second byte of the instruction designates the address (0-225) of the byte or I/O port to be operated upon.

Reset Memory Bit (RMB #,ADDR.)

This instruction is the same operation and format as the SMB instruction except a reset to "0" of the bit results.

Branch on Bit Set Relative (BBS #,ADDR.,DEST)

This instruction tests one of 8 bits designated by a 3-bit immediate field within the first byte of the instruction. The second byte is used to designate the location of the byte or I/O port to be tested within the zero page address range. The third byte of the instruction is used to specify the 8-bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

Branch on Bit Reset Relative (BBR #,ADDR.,DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

Random Access Memory (RAM)

The RAM consists of 192 by 8 bits of read/write memory with an assigned page zero address of 0040 through 00FF. The devices provide a separate power pin (V_{RR}) which may be used for standby power. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin.

Clock Oscillator

The clock oscillator provides the basic timing signals. A reference frequency can be generated with the on board oscillator (with external crystal) or an external reference source can be driven into the XTLI pin. If the XTLO pin is left floating, the reference frequency is internally divided by four (R6501Q) or two (R6511Q) to obtain the internal clock. The internal clock is then available as an output at the $\phi 2$ pin. The XTLI pin may be used as an undivided clock input by connecting XTLO to V_{SS} , in which case the internal division circuitry is bypassed and the device operates at the reference frequency.

Parallel Input/Output Ports

The devices have 32 I/O lines grouped into four 8-bit ports (PA, PB, PC, PD). Ports A through C may be used either for input or output individually, or in groups of any combination. The

R6501Q has pullup resistors on PA, PB and PC. The R6511Q has no pullup resistors. Port D may be used as all inputs or all outputs. It has active pull-ups.

Port A (PA) can be programmed as a standard parallel 8-bit I/O port or under software control as serial I/O lines, counter I/O lines, positive (2) and negative (2) edge detects, or an input data strobe for the Port B (PB) input latch.

Port B (PB) can be programmed as an I/O port with latched input enabled or disabled.

Port C (PC) can be programmed as an I/O port, as an abbreviated bus, as a multiplexed bus, or as part of the full address mode. In the full address mode pins PC6 and PC7 serve as addresses A13 and A14, respectively; PC0-PC5 are I/O pins.

Port D (PD) functions as an I/O port, an 8-bit tri-state data bus, or as a multiplexed address/data bus.

Serial Input/Output Channel — UART

The devices provide a full duplex serial I/O channel with programmable bit rates covering all standard baud rates from 50 to 125K bits/sec including the SMPTE 422 standard at 38.4K bits/sec. Character lengths of 5 to 8 bits, with or without parity are programmable. A full complement of flags provides for Receiver Wake Up; Receiver Buffer Full; Receiver Error Conditions detecting Framing, Parity, and Overrun errors; Transmitter End of Transmission and Transmitter Buffer Empty. In addition, a synchronous shift register mode to 250 KC at 2 MHz is available.

Wake-Up Feature

In a multi-distributed microcomputer application, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPUs to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit.

Counter/Latch Logic

The devices contain two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A

- Pulse width measurement
- Pulse Generation
- Interval Timer
- Event Counter

Counter B

- Retriggerable Interval Counter
- Asymmetrical Pulse Generation
- Interval Timer
- Event Counter

Mode Control Register (MCR)

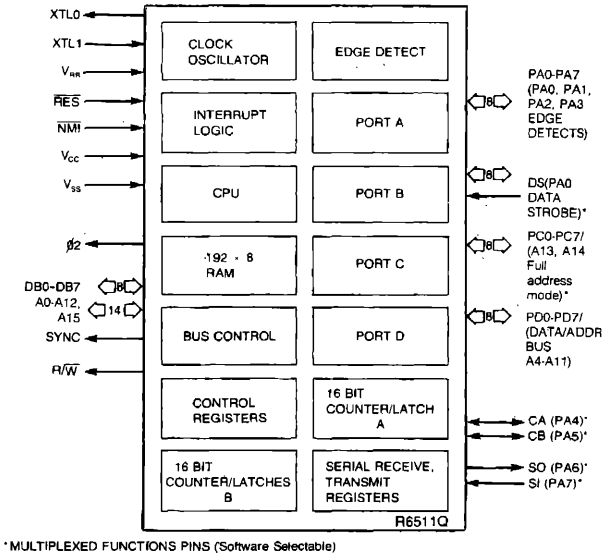
The Mode Control Register contains control bits for the multi-function I/O ports and mode select bits for Counter A and Counter B.

Ports C and D Operation Modes

There are four operating modes available in ports C and D, software programmable via the Mode Control Register. The full address mode allows access to a full 65K bytes of external storage. In this mode PC6 and PC7 are automatically used for A13 and A14. In the Input/Output mode the four ports are all used for I/O. In the abbreviated and multiplexed modes some port pins set up for addressing 64 or 16,384 bytes of external memory.

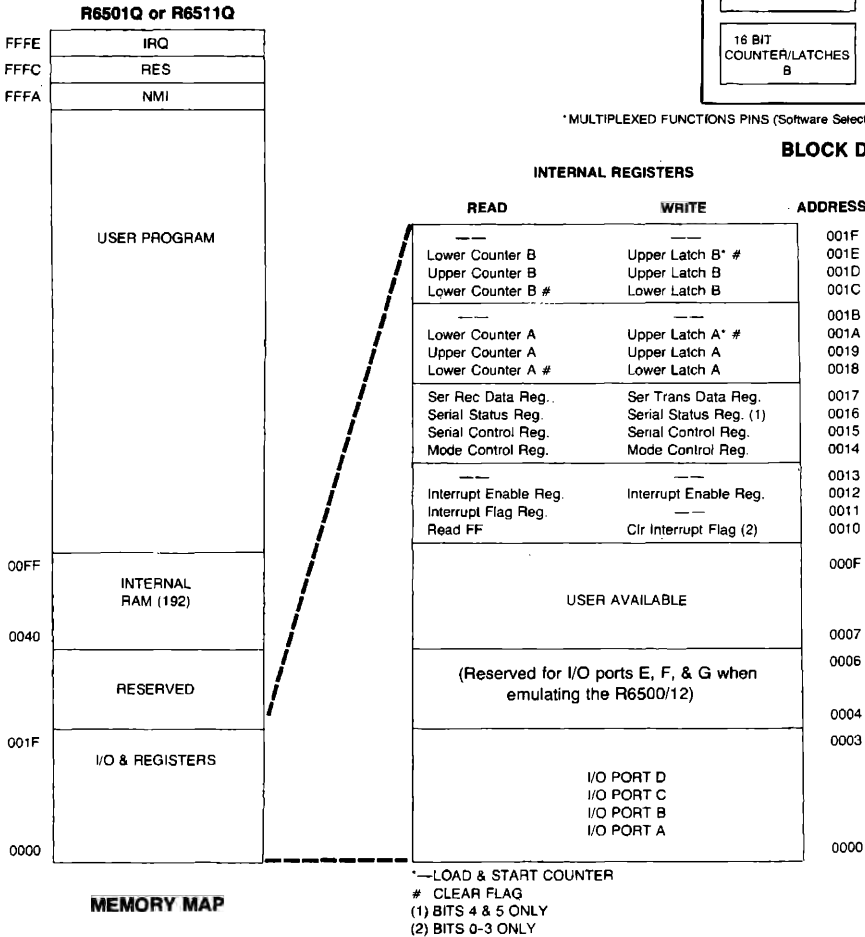
Interrupt Flag Register (IFR) and Interrupt Enable Register (IER)

The devices include an Interrupt Flag Register and an Interrupt Enable Register which flags and controls I/O and counter status.

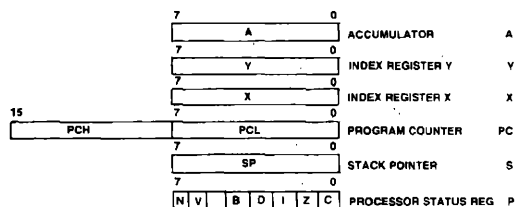


* MULTIPLEXED FUNCTIONS PINS (Software Selectable)

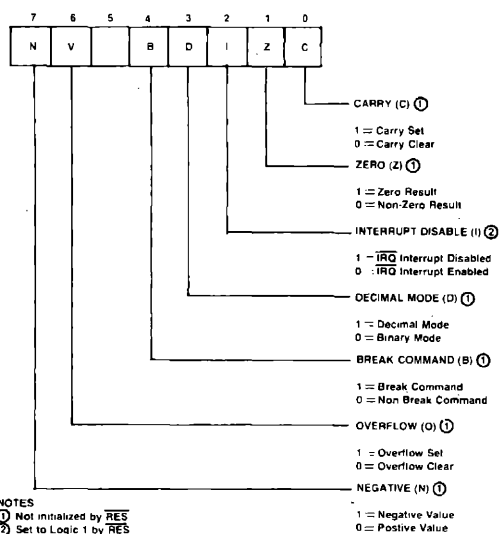
BLOCK DIAGRAM



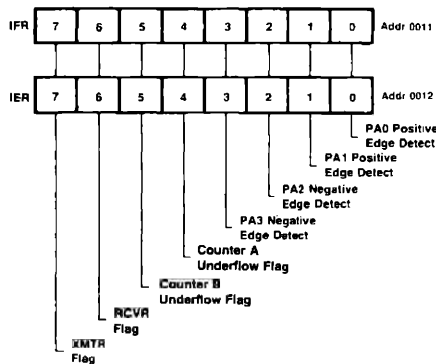
KEY REGISTER SUMMARY



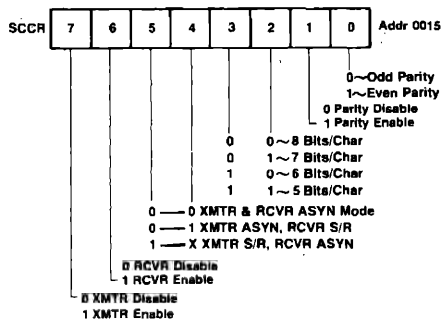
CPU Registers



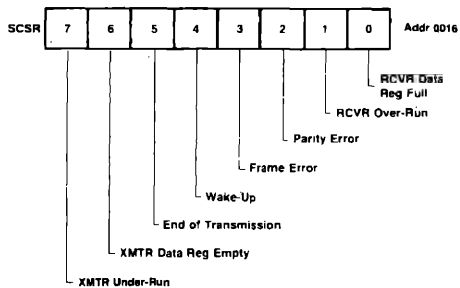
Processor Status Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



Serial Communications Status Register

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Commercial	T	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

($V_{CC} = 5V \pm 5\% V_{SS} = 0$)

Parameter	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High) Commercial at 25°C	P_D	—	—	1200	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial at 25°C	I_{RR}	—	4	—	mAdc
Input High Voltage Except XTLI	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	—	+0.8	Vdc
Input Leakage Current (RES, NMI) $V_{IN} = 0$ to 5.0 Vdc	I_{IN}	—	—	± 10	μ Adc
Input Low Current ($V_{IL} = 0.4$ Vdc)	I_{IL}	—	-1.0	-1.6	mAdc
Output High Voltage Except XTLO ($I_{LOAD} = -100 \mu$ Adc)	V_{OH}	+2.4	—	V_{CC}	Vdc
Output Low Voltage ($I_{LOAD} = 1.5$ mAdc)	V_{OL}	—	—	+0.4	Vdc
Input Capacitance ($V_{IN} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz) XTL1, XTLO All Others	C_{IN}	— —	— —	50 10	pF
I/O Port Pull-Up Resistance PA0-PA7, PB0-PB7, PC0-PC7 R6501Q only	R_L	3.0	6.0	11.5	K Ω

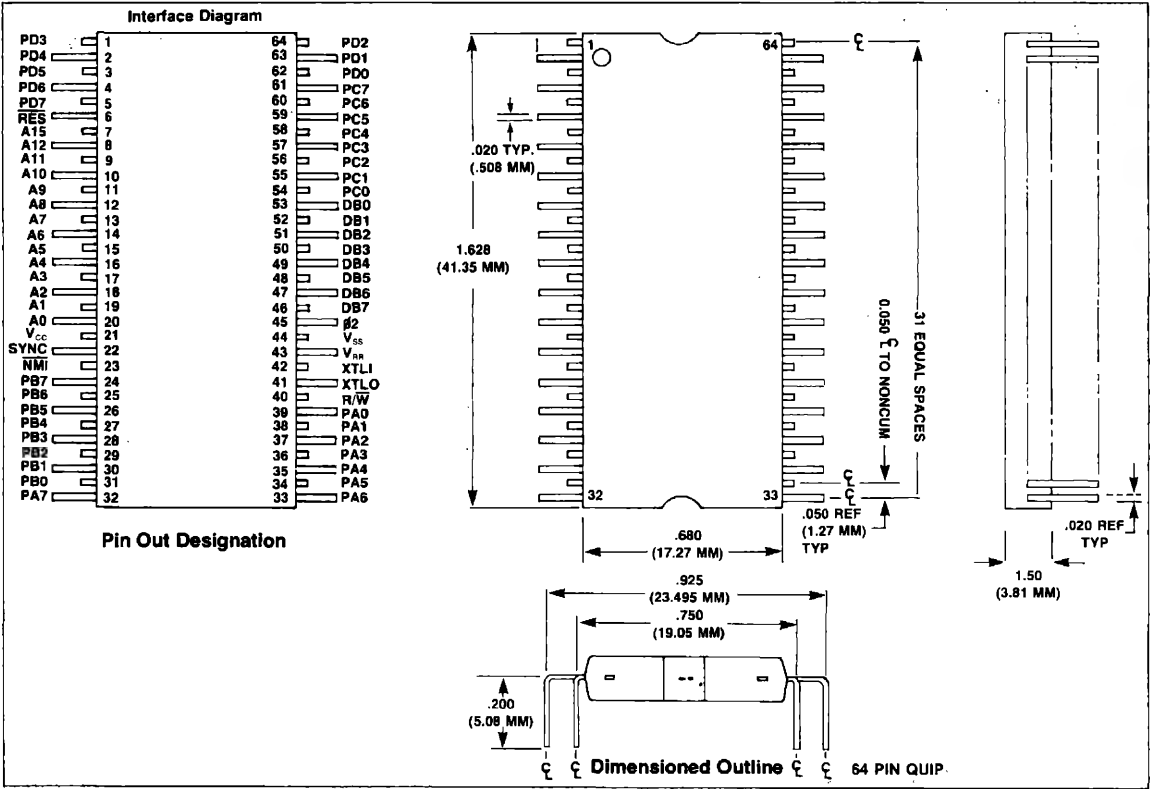
Note: Negative sign indicates outward current flow, positive indicates inward flow.

AC CHARACTERISTICS

($V_{CC} = 5V \pm 6\% V_{SS} = 0$)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{CYC}	1.0	10.0	0.500	10.0	μ sec
Internal Write to Peripheral Data Valid (TTL)	T_{POW}	1.0	—	0.5	—	μ sec
Peripheral Data Setup Time	T_{PDSU}	500	—	500	—	nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0	—	0.5	—	μ sec

PACKAGE DIMENSIONS





R6520 PERIPHERAL INTERFACE ADAPTER (PIA)

DESCRIPTION

The R6520 Peripheral Interface Adapter (PIA) is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the R6500, R6500* or R65C00 family of microprocessors, the R6520 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or to "handshake" data between the processor and a peripheral device.

FEATURES

- Direct replacement for MC6820 PIA
- Two 8-bit bidirectional I/O ports with individual data direction control
- Automatic "Handshake" control of data transfers
- Two interrupts (one for each port) with program control
- Commercial and industrial temperature range versions
- 40-pin plastic and ceramic versions
- 5 volt $\pm 5\%$ supply requirements
- Compatible with the R6500, R6500/* and R65C00 family of microprocessors
- 1 and 2 MHz versions

ORDERING INFORMATION

Part Number R6520

Temperature Range (T_L to T_H):

Blank = 0°C to $+70^\circ\text{C}$

E = -40°C to $+85^\circ\text{C}$

Package:

C = Ceramic

P = Plastic

Frequency Range:

No letter = 1 MHz

A = 2 MHz

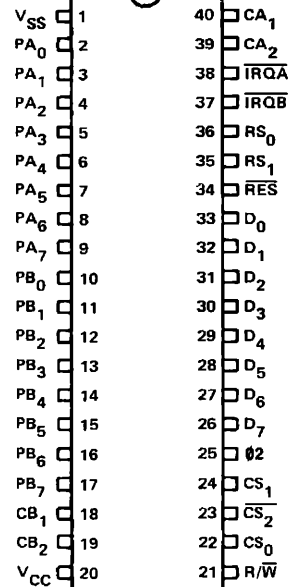


Figure 1. R6520 Pin Configuration

FUNCTIONAL DESCRIPTION

The R6520 PIA is organized into two independent sections referred to as the A Side and the B Side. Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, OBR), Interrupt Status Control (ISCA, ISCB), and the buffers necessary to drive the

Peripheral Interface buses. Data Bus Buffers (DBB) interface data from the two sections to the data bus, while the Data Input Register (DIR) interfaces data from the DBB to the PIA registers. Chip Select and R/W control circuitry interface to the processor bus control lines. Figure 2 is a block diagram of the R6520 PIA.

2

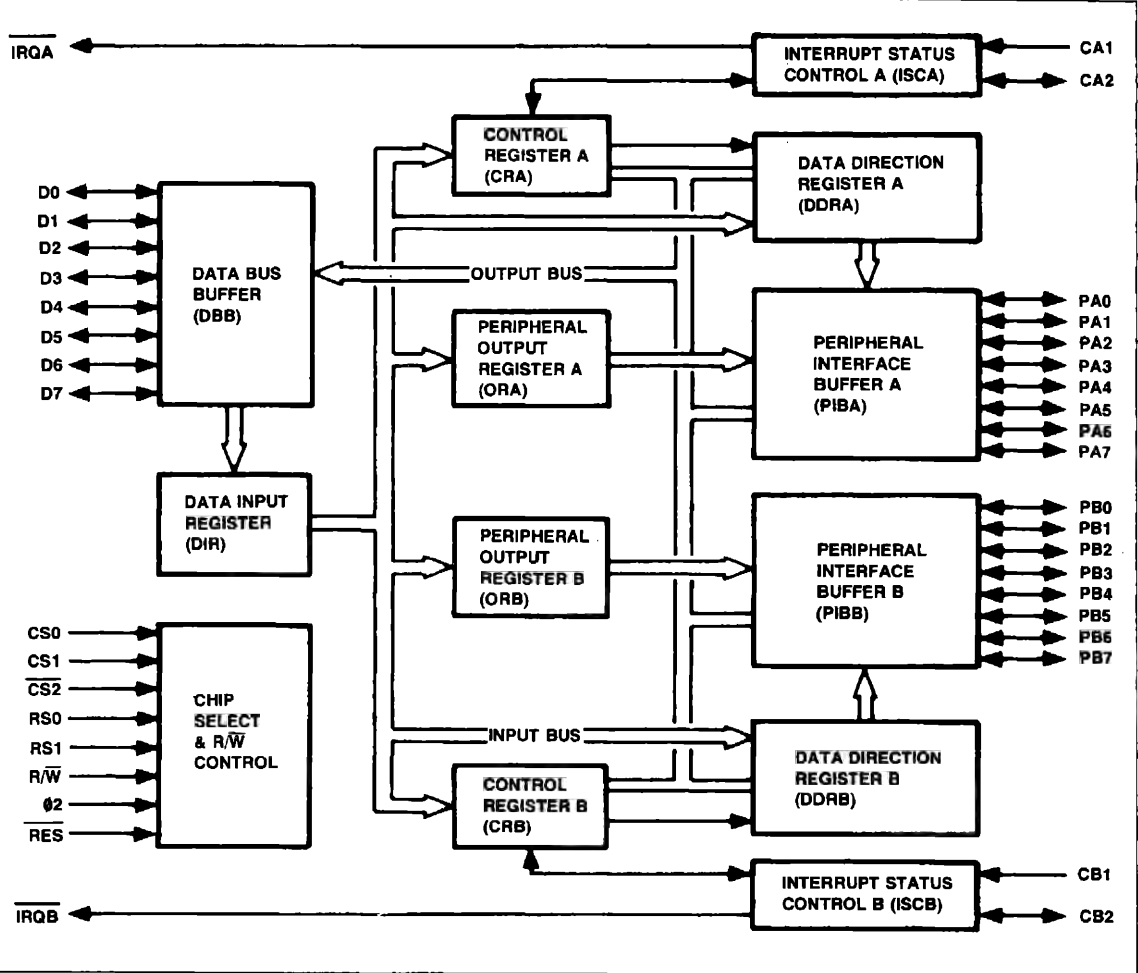


Figure 2. R6520 PIA Block Diagram

DATA INPUT REGISTER (DIR)

When the microprocessor writes data into the PIA, the data which appears on the data bus during the $\phi 2$ clock pulse is latched into the Data Input Register (DIR). The data is then transferred into one of six internal registers of the PIA after the trailing edge of the $\phi 2$ clock. This assures that the data on the peripheral output lines will make smooth transitions from high to low (or from low to high) and the voltage will remain stable except when it is going to the opposite polarity.

CONTROL REGISTERS (CRA and CRB)

Table 1 illustrates the bit designation and functions in the two control registers. The control registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) in each control register indicate the status of the Interrupt Input lines (CA1, CA2, CB1, CB2). These Interrupt Status bits (IRQA1, IRQA2 or IRQB1, IRQB2) are normally interrogated by the microprocessor during the IRQ interrupt service routine to determine the source of the interrupt.

DATA DIRECTION REGISTERS (DDRA, DDRB)

The Data Direction Registers (DDRA, DDRB) allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Writing a "0" in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

Bit 2 (DDRA, DDRB) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a "1," a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a "0," a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1) selects the various internal registers as shown in Table 2.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

PERIPHERAL OUTPUT REGISTERS (ORA, ORB)

The Peripheral Output Registers (ORA, ORB) store the output data from the Data Bus Buffers (DBB) which appears on the Peripheral I/O port. If a line on the Peripheral A Port is programmed as an output by the DDRA, writing a 0 into the corresponding bit in the ORA causes that line to go low (<0.4 V); writing a 1 causes the line to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

INTERRUPT STATUS CONTROL (ISCA, ISCB)

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register and detects active transitions on the interrupt inputs.

PERIPHERAL I/O PORTS (PA0-PA7, PB0-PB7)

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by writing data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a 1 in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A 0 in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-up devices. These pull-up devices are resistive in nature and therefore allow the output voltage to go to VCC for a logic 1. The switches can sink a full 3.2 mA, making these buffers capable of driving two standard TTL loads.

In the input mode, the pull-up devices are still connected to the I/O pin and still supply current to this pin. For this reason, these lines also represent two standard TTL loads in the input mode.

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output is similar to the Peripheral A port, as is the effect of reading or writing this port. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

Table 1. Control Registers Bit Designations

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
	7	6	5	4	3	2	1	0
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

The Peripheral B I/O port buffers are push-pull devices i.e., the pull-up devices are switched OFF in the 0 state and ON for a logic 1. Since these pull-ups are active devices, the logic 1 voltage will not go higher than +2.4V.

Another difference between the PA0-PA7 lines and the PB0 through PB7 lines is that they have three-state capability which allows them to enter a high impedance state when programmed to be used as input lines. In addition, data on these lines will be read properly, when programmed as output lines, even if the data signals fall below 2.0 volts for a "high" state or are above 0.8 volts for a "low" state. When programmed as output, each line can drive at least a two TTL load and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch, such as a Darlington pair.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic is the high-impedance input state which is a function of the Peripheral B push-pull buffers. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

DATA BUS BUFFERS (DBB)

The Data Bus Buffers are 8-bit bidirectional buffers used for data exchange, on the D0-D7 Data Bus, between the microprocessor and the PIA. These buffers are tri-state and are capable of driving a two TTL load (when operating in an output mode) and represent a one TTL load to the microprocessor (when operating in an input mode).

INTERFACE SIGNALS

The PIA interfaces to the R6500, R6500/* or the R65C00 microprocessor family with a reset line, a $\phi 2$ clock line, a read/write line, two interrupt request lines, two register select lines, three chip select lines, and an 8-bit bidirectional data bus.

The PIA interfaces to the peripheral devices with four interrupt/control lines and two 8-bit bidirectional data buses.

Figure 1 (on the front page) shows the pin assignments for these interface signals and Figure 3 shows the interface relationship of these signals as they pertain to the CPU and the peripheral devices.

CHIP SELECT ($\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$)

The PIA is selected when $\overline{CS0}$ and $\overline{CS1}$ are high and $\overline{CS2}$ is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits. When the PIA is selected, data will be transferred between the data lines and PIA registers, and/or peripheral interface lines as determined by the $\overline{R/\overline{W}}$, $\overline{RS0}$, and $\overline{RS1}$ lines and the contents of Control Registers A and B.

RESET SIGNAL (\overline{RES})

The Reset (\overline{RES}) input initializes the R65C21 PIA. A low signal on the \overline{RES} input causes all internal registers to be cleared.

CLOCK SIGNAL ($\phi 2$)

The Phase 2 Clock Signal ($\phi 2$) is the system clock that triggers all data transfers between the CPU and the PIA. $\phi 2$ is generated by the CPU and is therefore the synchronizing signal between the CPU and the PIA.

READ/WRITE SIGNAL ($\overline{R/\overline{W}}$)

Read/Write ($\overline{R/\overline{W}}$) controls the direction of data transfers between the PIA and the data lines associated with the CPU and the peripheral devices. A high on the $\overline{R/\overline{W}}$ line permits the peripheral devices to transfer data to the CPU from the PIA. A low on the $\overline{R/\overline{W}}$ line allows data to be transferred from the CPU to the peripheral devices from the PIA.

REGISTER SELECT ($\overline{RS0}$, $\overline{RS1}$)

The two Register Select lines ($\overline{RS0}$, $\overline{RS1}$), in conjunction with the Control Registers (CRA, CRB) Data Direction Register access bits (see Table 1, bit 2) select the various R65C21 registers to be accessed by the CPU. $\overline{RS0}$ and $\overline{RS1}$ are normally connected to the microprocessor (CPU) address output lines. Through control of these lines, the CPU can write directly into the Control

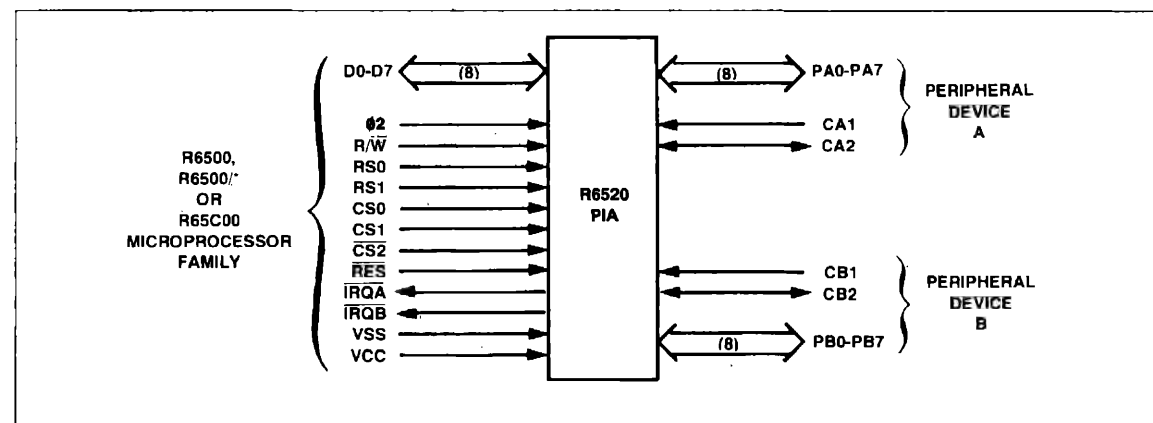


Figure 3. Interface Signals Relationship

Registers (CRA, CRB) the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore are shown separately in Table 2.

Table 2. ORA and ORB Register Addressing

Register Address (Hex)	Register Select Lines		Data Direction Control		Register Operation	
	RS1	RS0	CRA (Bit 2)	CRB (Bit 2)	R/W=H	R/W=L
0	L	L	1	—	Read PIBA	Write ORA
0	L	L	0	—	Read DDRA	Write DDRA
1	L	H	—	—	Read CRA	Write CRA
2	H	L	—	1	Read PIBB	Write ORB
2	H	L	—	0	Read DDRB	Write DDRB
3	H	H	—	—	Read CRB	Write CRB

INTERRUPT REQUEST LINES (IRQA, IRQB)

The active low Interrupt Request lines (IRQA and IRQB) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are open drain and are capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a wired-OR configuration. The A and B in the titles of these lines correspond to the peripheral port A and the peripheral port B so that each interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers (CRA, CRB). These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2). The four interrupt flags are set (enabled) by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

CRA bit 7 (IRQA1) is always set by an active transition of the CA1 interrupt input signal. However, IRQA can be disabled by setting bit 0 in CRA to a 0. Likewise, CRA bit 6 (IRQA2) can be set by an active transition of the CA2 interrupt input signal and IRQA can be disabled by setting bit 3 in CRA to a 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the read/write, proper data direction register and register select signals are provided to allow the processor to read the Peripheral A I/O port. A summary of IRQA control is shown in Table 3.

Control of IRQB is performed in exactly the same manner as that described above for IRQA. Bit 7 in CRB (IRQB1) is set by an active transition on CB1 and IRQB from this flag is controlled

by CRB bit 0. Likewise, bit 6 (IRQB2) in CRB is set by an active transition on CB2, and IRQB from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 of CRB are reset by a "Read Peripheral B Output Register" operation. A summary of IRQB control is shown in Table 3.

Table 3. IRQA and IRQB Control Summary

Control Register Bits	Action
CRA-7=1 and CRA-0=1	IRQA goes low (Active)
CRA-6=1 and CRA-3=1	IRQA goes low (Active)
CRB-7=1 and CRB-0=1	IRQB goes low (Active)
CRB-6=1 and CRB-3=1	IRQB goes low (Active)
Note:	
The flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.	

INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 4 summarizes the operation of these control lines.

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

Note:

A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

CA2 can act as a totally independent interrupt or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupt.

In the output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a 0 and CRA, bit 3 to a 1. This pulse output can be used to control the counters, shift registers, etc., which make sequential data available on the Peripheral input lines.

CONTROL REGISTER A (CRA)

CA2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQA1 FLAG	IRQA2 FLAG	CA2 INPUT MODE SELECT (=0)	IRQA2 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA2	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			IRQA/IRQA2 CONTROL			$\overline{\text{IRQA}}/\text{IRQA1}$ CONTROL	

2

CA2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQA1 FLAG	0	CA2 OUTPUT MODE SELECT (=1)	CA2 OUTPUT CONTROL	CA2 RESTORE CONTROL	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			CA2 CONTROL			$\overline{\text{IRQA}}/\text{IRQA1}$ CONTROL	

CA2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7	IRQA1 FLAG
1	A transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria. This bit is cleared by a read of Output Register A or by RES.
0	No transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria.
Bit 2	OUTPUT REGISTER A SELECT
1	Select Output Register A.
0	Select Data Direction Register A.
Bit 1	IRQA1 POSITIVE TRANSITION
1	Set IRQA1 Flag (bit 7) on a positive (low-to-high) transition of CA1.
0	Set IRQA1 Flag (bit 7) on a negative (high-to-low) transition of CA1.
Bit 0	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
1	Enable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.
0	Disable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.

CA2 INPUT MODE (BIT 5 = 0)

Bit 6	IRQA2 FLAG
1	A transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria. This flag is cleared by a read of Output Register A or by RES.
0	No transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria.
Bit 5	CA2 MODE SELECT
0	Select CA2 Input Mode.
Bit 4	IRQA2 POSITIVE TRANSITION
1	Set IRQA2 Flag (bit 6) on a positive (low-to-high) transition of CA2.
0	Set IRQA2 Flag (bit 6) on a negative (high-to-low) transition of CA2.
Bit 3	$\overline{\text{IRQA}}$ ENABLE FOR IRQA2
1	Enable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.
0	Disable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.

CA2 OUTPUT MODE (BIT 5 = 1)

Bit 6	NOT USED
0	Always zero.
Bit 5	CA2 MODE SELECT
1	Select CA2 Output Mode.
Bit 4	CA2 OUTPUT CONTROL
1	CA2 goes low when a zero is written into CRA bit 3.
	CA2 goes high when a one is written into CRA bit 3.
0	CA2 goes low on the first negative (high-to-low) $\emptyset 2$ clock transition following a read of Output Register A. CA2 returns high as specified by bit 3.
Bit 3	CA2 READ STROBE RESTORE CONTROL (4 = 0)
1	CA2 returns high on the next $\emptyset 2$ clock negative transition following a read of Output Register A.
0	CA2 returns high on the next active CA1 transition following a read of Output Register A as specified by bit 1.

Figure 4. Control Line Operations Summary (1 of 2)

CONTROL REGISTER B (CRB)

CB2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQB1 FLAG	IRQB2 FLAG	CB2 INPUT MODE SELECT (=0)	IRQB2 POSITIVE TRANSITION	IRQB ENABLE FOR IRQB2	ORB SELECT	IRQB1 POSITIVE TRANSITION	IRQB ENABLE FOR IRQB1
			IRQB/IRQB2 CONTROL			IRQB/IRQB1 CONTROL	

CB2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQB1 FLAG	0	CB2 OUTPUT MODE SELECT (=1)	CB2 OUTPUT CONTROL	CB2 RESTORE CONTROL	ORB SELECT	IRQB1 POSITIVE TRANSITION	IRQB ENABLE FOR IRQB1
			CB2 CONTROL			IRQB/IRQB1 CONTROL	

CB2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7	IRQB1 FLAG
1	A transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria. This bit is cleared by a read of Output Register B or by RES.
0	No transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria.
Bit 2	OUTPUT REGISTER B SELECT
1	Select Output Register B.
0	Select Data Direction Register B.
Bit 1	IRQB1 POSITIVE TRANSITION
1	Set IRQB1 Flag (bit 7) on a positive (low-to-high) transition of CB1.
0	Set IRQB1 Flag (bit 7) on a negative (high-to-low) transition of CB1.
Bit 0	IRQB ENABLE FOR IRQB1
1	Enable assertion of IRQB when IRQB1 Flag (bit 7) is set.
0	Disable assertion of IRQB when IRQB1 Flag (bit 7) is set.

CB2 INPUT MODE (BIT 5 = 0)

Bit 6	IRQB2 FLAG
1	A transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria. This flag is cleared by a read of Output Register B or by RES.
0	No transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria.
Bit 5	CB2 MODE SELECT
0	Select CB2 Input Mode.
Bit 4	IRQB2 POSITIVE TRANSITION
1	Set IRQB2 Flag (bit 6) on a positive (low-to-high) transition of CB2.
0	Set IRQB2 Flag (bit 6) on a negative (high-to-low) transition of CB2.
Bit 3	IRQB ENABLE FOR IRQB2
1	Enable assertion of IRQB when IRQB2 Flag (bit 6) is set.
0	Disable assertion of IRQB when IRQB2 Flag (bit 6) is set.

CB2 OUTPUT MODE (BIT 5 = 1)

Bit 6	NOT USED
0	Always zero.
Bit 5	CB2 MODE SELECT
1	Select CB2 Output Mode.
Bit 4	CB2 OUTPUT CONTROL
1	CB2 goes low when a zero is written into CRB bit 3. CB2 goes high when a one is written into CRB bit 3.
0	CB2 goes low on the first negative (high-to-low) \emptyset 2 clock transition following a write to Output Register B. CB2 returns high as specified by bit 3.
Bit 3	CB2 WRITE STROBE RESTORE CONTROL (BIT 4 = 0)
1	CB2 returns high on the next \emptyset 2 clock negative transition following a write to Output Register B.
0	CB2 returns high on the next active CB1 transition following a write to Output Register B as specified by bit 1.

Figure 4. Control Line Operations Summary (2 of 2)

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 or CRA to a 1 or a 0 respectively.

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

READING THE PERIPHERAL A I/O PORT

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly

transfers the data on the Peripheral A I/O lines to the data bus. In this situation, the data bus will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read by the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

READING THE PERIPHERAL B I/O PORT

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back to the processor on a Read operation.

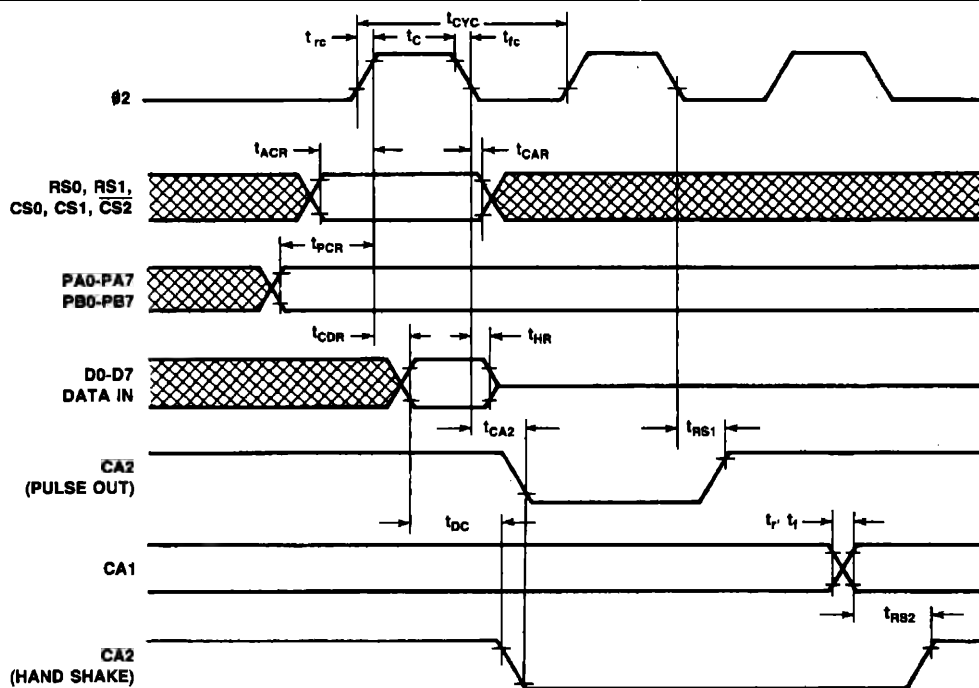


Figure 5. Read Timing Waveforms

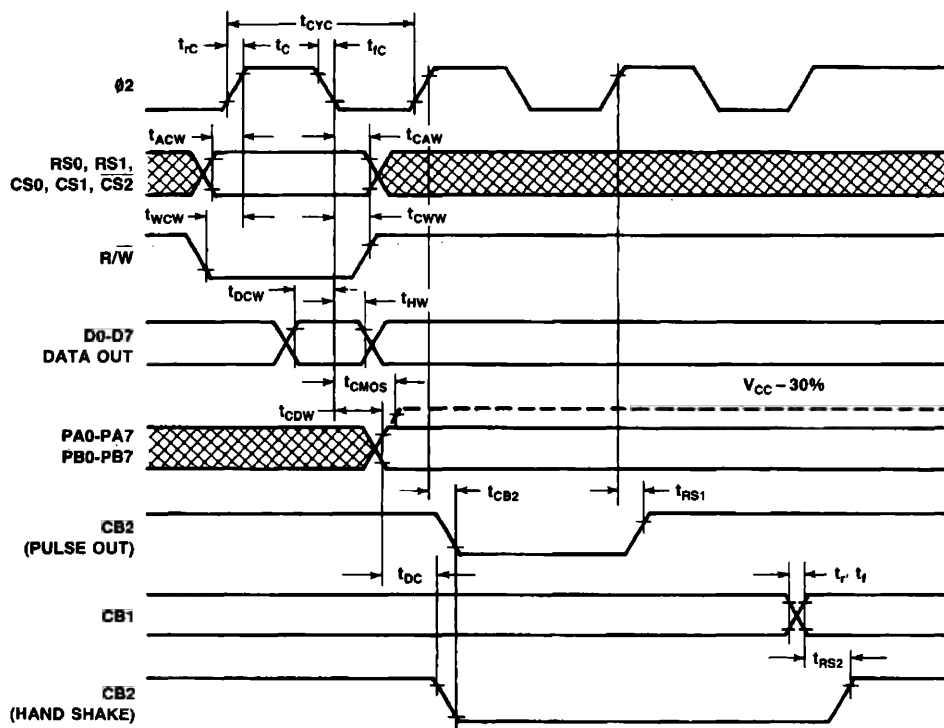


Figure 6. Write Timing Waveforms

BUS TIMING CHARACTERISTICS

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
Ø2 Cycle	t_{CYC}	1.0	—	0.5	—	μs
Ø2 Pulse Width	t_C	470	25	235	25	ns
Ø2 Rise and Fall Time	$t_{r\bar{r}}, t_f$	—	25	—	15	ns

READ TIMING

Address Set-Up Time	t_{ACR}	150	—	90	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	ns
Peripheral Data Set-Up Time	t_{PCR}	300	—	150	—	ns
Data Bus Delay Time	t_{CDR}	—	395	—	190	ns
Data Bus Hold Time	t_{HR}	10	—	10	—	ns

WRITE TIMING

Address Set-Up Time	t_{ACW}	180	—	90	—	ns
Address Hold Time	t_{CAW}	0	—	0	—	ns
R/W Set-Up Time	t_{WCW}	130	—	65	—	ns
R/W Hold Time	t_{CWW}	50	—	25	—	ns
Data Bus Set-Up Time	t_{DCW}	300	—	150	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	ns
Peripheral Data Delay Time	t_{CPW}	—	1.0	—	0.5	μs
Peripheral Data Delay Time to CMOS Level	t_{CMOS}	—	2.0	—	1.0	μs

PERIPHERAL INTERFACE TIMING

Peripheral Data Set-Up	t_{PCR}	300	—	150	—	ns
Ø2 Low to CA2 Low Delay	t_{CA2}	—	1.0	—	0.5	μs
Ø2 Low to CA2 High Delay	t_{RS1}	—	1.0	—	0.5	μs
CA1 Active to CA2 High Delay	t_{RS2}	—	2.0	—	1.0	μs
Ø2 High to CB2 Low Delay	t_{CB2}	—	1.0	—	0.5	μs
Peripheral Data Valid to CB2 Low Delay	t_{DC}	0	1.5	0	0.75	μs
Ø2 High to CB2 High Delay	t_{RS1}	—	1.0	—	0.5	μs
CB1 Active to CB2 High Delay	t_{RS2}	—	2.0	—	1.0	μs
CA1, CA2, CB1 and CB2 Input Rise and Fall Time	t_r, t_f	—	1.0	—	1.0	μs

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to V_{CC}	Vdc
Operating Temperature Range Commercial Industrial	T_A	T_L T_H 0 to +70 -40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V \pm 5%
Temperature Range Commercial Industrial	T_A	0°C to 70°C -40°C to +85°C

DC CHARACTERISTICS

(V_{CC} = 5.0V \pm 5%, V_{SS} = 0, T_A = T_L to T_H , unless otherwise noted)

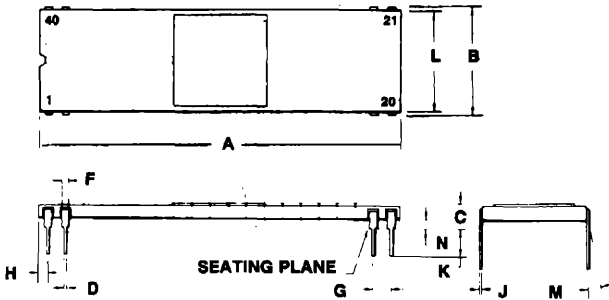
Parameter	Symbol	Min.	Typ. ³	Max.	Unit ¹	Test Conditions
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	V	
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V	
Input Leakage Current R/W, \overline{RES} , RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, $\emptyset 2$	I_{IN}	—	± 1	± 2.5	μA	V_{IN} = 0V to 5.25V V_{CC} = 0V
Output Leakage Current for Three-State Off D0-D7, PB0-PB7, CB2	I_{TSI}	—	± 2	± 10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0-PA7, CA2	I_{IH}	-100	-250	—	μA	V_{IH} = 2.4V
Input Low Current PA0-PA7, CA2	I_{IL}	—	-1	-1.6	mA	V_{IL} = 0.4V
Output High Voltage All outputs PB0-PB7, CB2 (Darlington Drive)	V_{OH}	2.4 1.5	— —	— —	V V	V_{CC} = 4.75V I_{LOAD} = -100 μA I_{LOAD} = -1.0 mA
Output Low Voltage	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0-PB7, CB2 (Darlington Drive)	I_{OH}	-100 -1.0	-1000 -2.5	— -10	μA mA	V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking)	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Output Leakage Current (Off State) IRQA, IRQB	I_{OFF}	—	1	± 10	μA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D		200	500	mW	
Input Capacitance D0-D7, PA0-PA7, PB0-PB7, CA2, CB2 R/W, \overline{RES} , RS0, RS1, CS0, CS1, $\overline{CS2}$ CA1, CB1, $\emptyset 2$	C_{IN}	— — —	— — —	10 7.0 20	pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:

1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

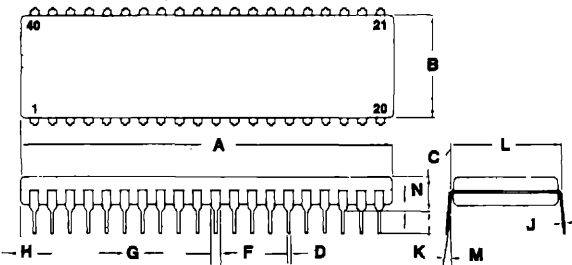
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.82	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0	10	0	10
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.15	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7	10	7	10
N	0.51	1.02	0.020	0.040



R6522 VERSATILE INTERFACE ADAPTER (VIA)

DESCRIPTION

The R6522 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bidirectional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each line can be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register and a pair of function control registers are provided.

FEATURES

- Two 8-bit bidirectional I/O ports
- Two 16-bit programmable timer/counters
- Serial data port
- TTL compatible
- CMOS compatible peripheral control lines
- Expanded "handshake" capability allows positive control of data transfers between processor and peripheral devices.
- Latched output and input registers
- 1 MHz and 2 MHz operation
- Single +5V power supply

ORDERING INFORMATION

Part Number:
R6522

Temperature Range
Blank = 40°C to +70°C
E = 40°C to +85°C

Package
C = Ceramic
P = Plastic

Frequency
No Letter = 1 MHz
A = 2 MHz

VSS	1	40	CA1
PA0	2	39	CA2
PA1	3	38	RS0
PA2	4	37	RS1
PA3	5	36	RS2
PA4	6	35	RS3
PA5	7	34	RES
PA6	8	33	D0
PA7	9	32	D1
PB0	10	31	D2
PB1	11	30	D3
PB2	12	29	D4
PB3	13	28	D5
PB4	14	27	D6
PB5	15	26	D7
PB6	16	25	φ2
PB7	17	24	CS1
CB1	18	23	CS2
CB2	19	22	R/W
VCC	20	21	IRQ

R6522 Pin Configuration

INTERFACE SIGNALS

RESET (\overline{RES})

A low reset (\overline{RES}) input clears all R6522 internal registers to logic 0 (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupting from the chip.

INPUT CLOCK (PHASE 2)

The input clock is the system $\phi 2$ clock and triggers all data transfers between processor bus and the R6522.

READ/WRITE (R/\overline{W})

The direction of the data transfers between the R6522 and the system processor is controlled by the R/\overline{W} line in conjunction with the $CS1$ and $\overline{CS2}$ inputs. When R/\overline{W} is low, (write operation) and the R6522 is selected, data is transferred from the processor bus into the selected R6522 register. When R/\overline{W} is high, (read operation) and the R6522 is selected, data is transferred from the selected R6522 register to the processor bus.

DATA BUS (D0-D7)

The eight bidirectional data bus lines transfer data between the R6522 and the system processor bus. During read cycles, the contents of the selected R6522 register are placed on the data bus lines. During write cycles, these lines are high-impedance inputs and data is transferred from the processor bus into the selected register. When the R6522 is not selected, the data bus lines are high-impedance.

CHIP SELECTS ($CS1$, $\overline{CS2}$)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected R6522 register is accessed when $CS1$ is high and $\overline{CS2}$ is low.

REGISTER SELECTS ($RS0$ - $RS3$)

The coding of the four Register Select inputs select one of the 16 internal registers of the R6522, as shown in Table 1.

INTERRUPT REQUEST (\overline{IRQ})

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is open-drain to allow the interrupt request signal to be wire-OR'ed with other equivalent signals in the system.

PERIPHERAL PORT A ($PA0$ - $PA7$)

Port A consists of eight lines which can be individually programmed to act as inputs or outputs under control of Data Direction Register A. The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of the $CA1$ line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Figure 2 illustrates the output circuit.

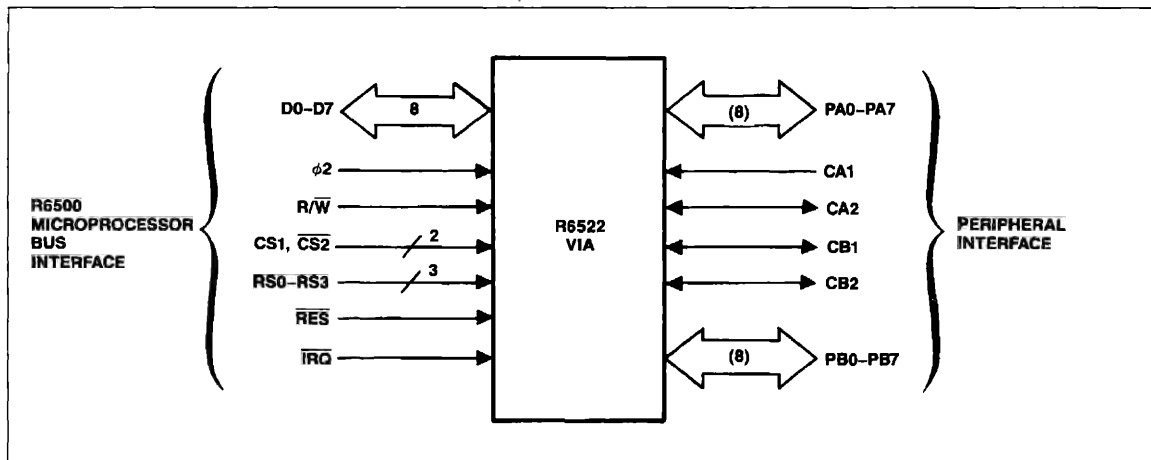


Figure 1. R6522 VIA Interface Signals

PORT A CONTROL LINES (CA1, CA2)

The two Port A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Port A input lines. CA1 is a high-impedance input only while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

PORT B (PB0-PB7)

Peripheral Port B consists of eight bidirectional lines which are controlled by an output register and a data direction register in much the same manner as the Port A. In addition, the polarity of the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. Port B lines represent one standard TTL load in

the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0 mA at 1.5 Vdc in the output mode to allow the outputs to directly drive Darlington transistor circuits. Figure 3 is the circuit schematic.

PORT B CONTROL LINES (CB1, CB2)

The Port B control lines act as interrupt inputs or as handshake outputs. As with CA1 and CA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. CB2 can also drive a Darlington transistor circuit; however, CB1 cannot.

Table 1. R6522 Register Addressing

Register Number	RS Coding				Register Desig.	Register/Description	
	RS3	RS2	RS1	RS0		Write (R/W = L)	Read (R/W = H)
0	0	0	0	0	ORB/IRB	Output Register B	Input Register B
1	0	0	0	1	ORA/IRA	Output Register A	Input Register A
2	0	0	1	0	DDRB	Data Direction Register B	
3	0	0	1	1	DDRA	Data Direction Register A	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	T2 Low-Order Counter
8	1	0	0	0	T2C-L	T2 Low-Order Latches	
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Output Register B*	Input Register B*

NOTE: *Same as Register 1 except no handshake.

NOTE: *Same as Register 1 except no handshake.

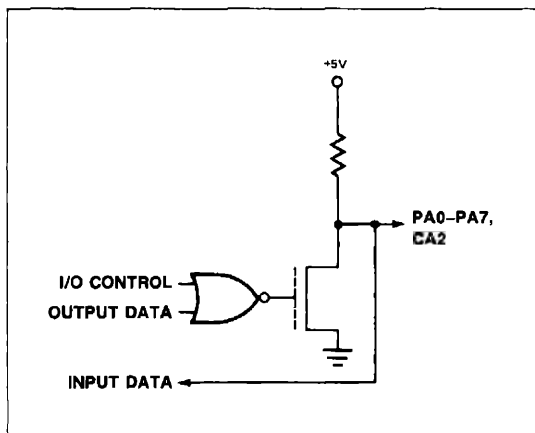


Figure 2. Port A Output Circuit

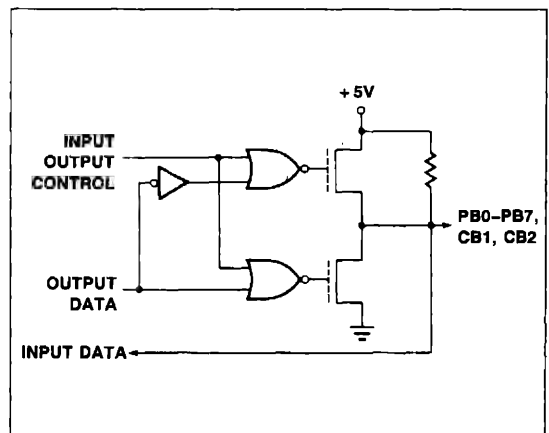


Figure 3. Port B Output Circuit

FUNCTIONAL DESCRIPTION

The internal organization of the R6522 VIA is illustrated in Figure 4.

PORT A AND PORT B OPERATION

The R6522 VIA has two 8-bit bidirectional I/O ports (Port A and Port B) and each port has two associated control lines.

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A 0 in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A 1 causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register (ORA, ORB) and the Input Register (IRA, IRB). When the pin is programmed as an output, the voltage on the pin is controlled by the corresponding bit of the Output Register. A 1 in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled, IRA will reflect the levels on the PA pins at the time the latching occurred (via CA1).

The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the *level on the pin* determines whether a 0 or a 1 is sensed. When reading IRB, however, the bit stored in the *output register*, ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 5 through 8 illustrate the formats of the port registers. In addition, the input latching modes are selected by the Auxiliary Control Register (Figure 14).

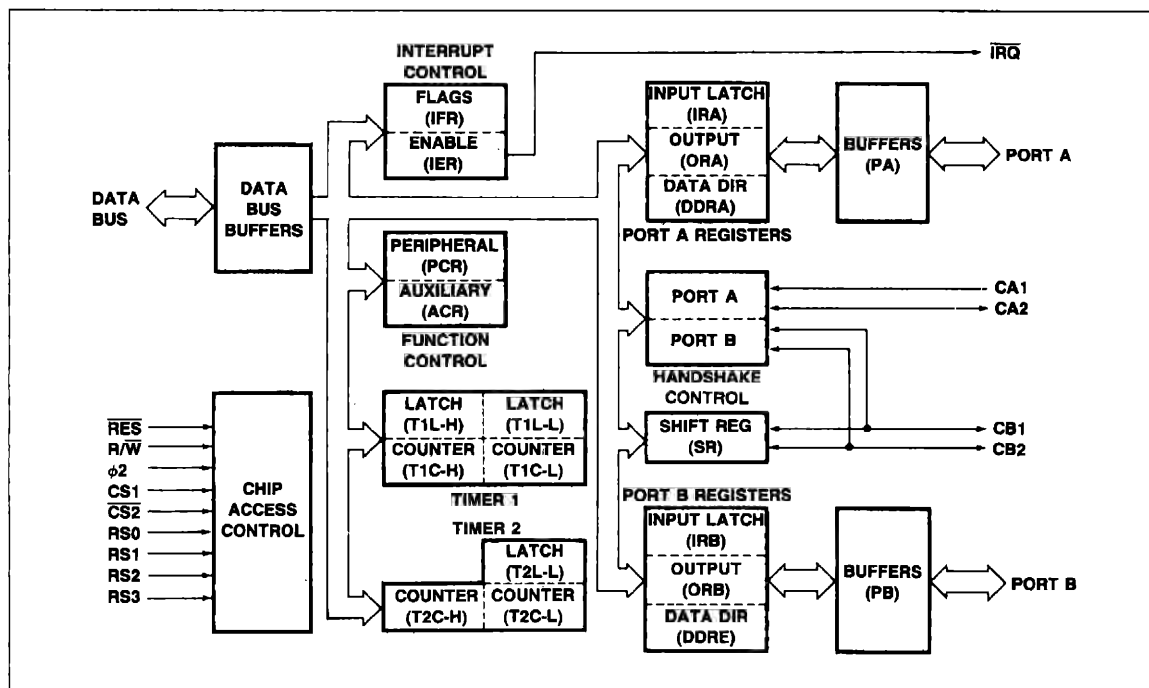


Figure 4. R6522 VIA Block Diagram

HANDSHAKE CONTROL OF DATA TRANSFERS

The R6522 allows positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the

data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the R6522, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 9 which illustrates the normal Read Handshake sequence.

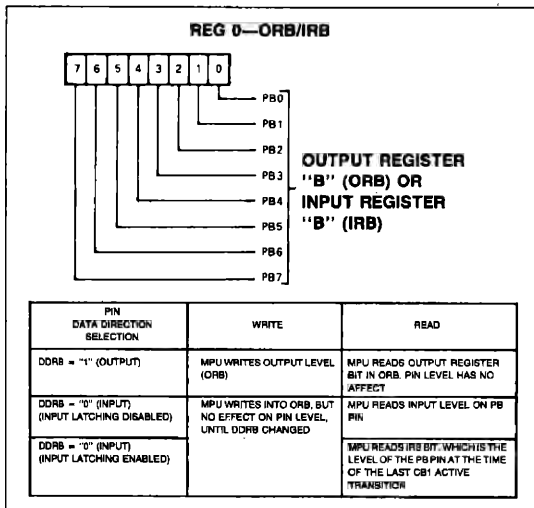


Figure 5. Output Register B (ORB), Input Register B (IRB)

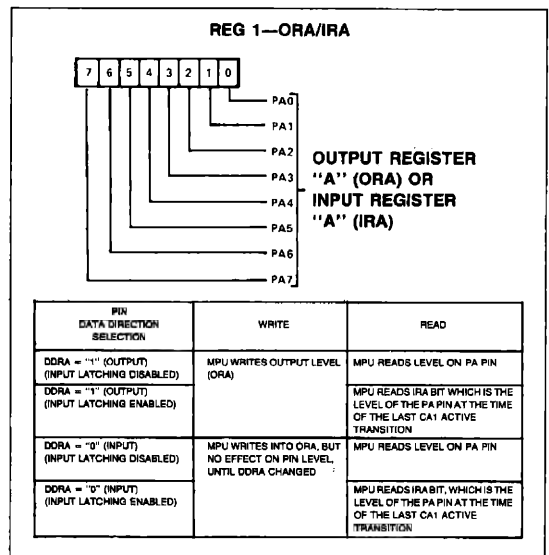


Figure 6. Output Register A (ORA), Input Register A (IRA)

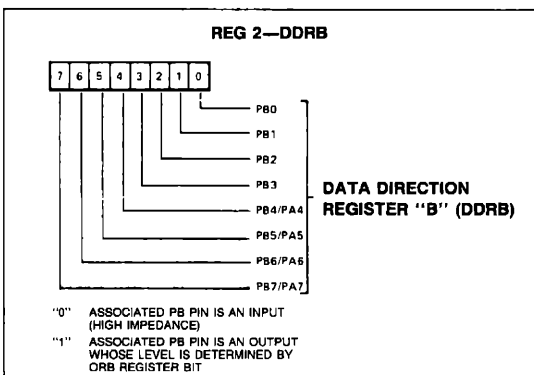


Figure 7. Data Direction Register B (DDRB)

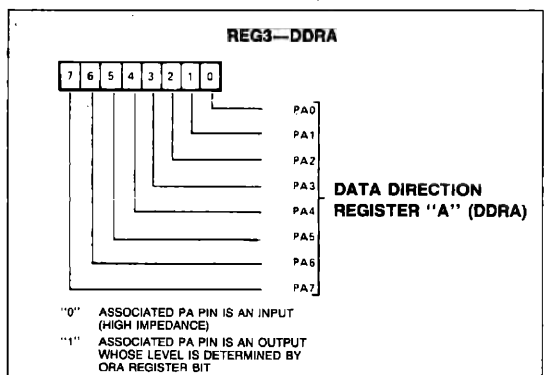


Figure 8. Data Direction Register A (DDRA)

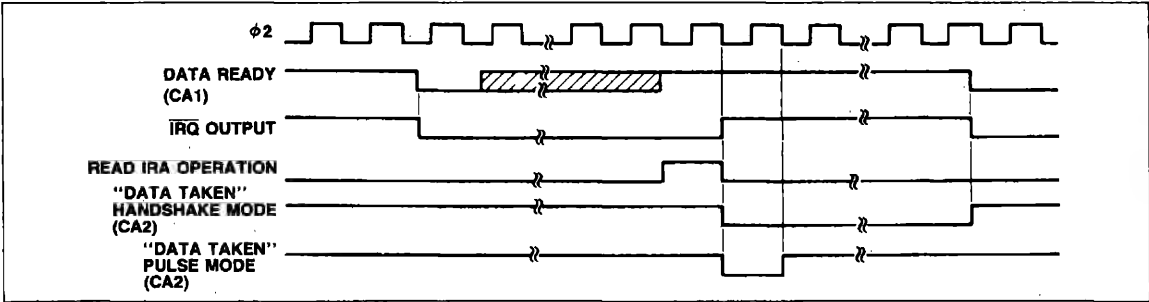


Figure 9. Read Handshake Timing (Port A, Only)

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the R6522 generates the "Data Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the R6522. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and clearing the "Data Ready" output. This sequence is shown in Figure 10.

Selection of operating modes for CA1, CA2, CB1, and CB2 is accomplished by the Peripheral Control Register (Figure 11).

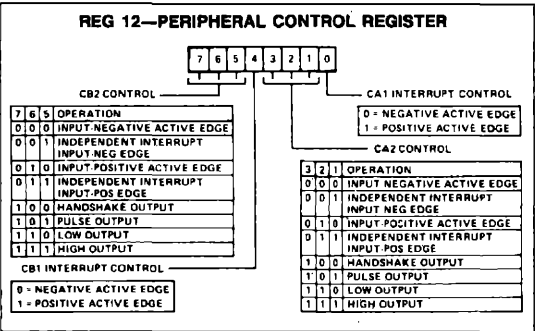


Figure 11. Peripheral Control Register (PCR)

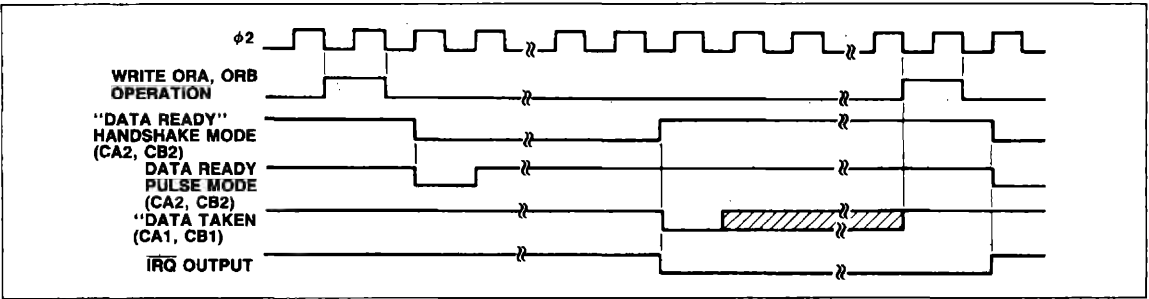


Figure 10. Write Handshake Timing

COUNTER/TIMERS

There are two independent 16-bit counter/timers (called Timer 1 and Timer 2) in the R6522. Each timer is controlled by writing bits into the Auxiliary Control Register (ACR) to select the mode of operation (Figure 14).

Timer 1 Operation

Interval Timer T1 consists of two 8-bit latches (Figure 12) and a 16-bit counter (Figure 13). The latches store data which is to be loaded into the counter. After loading, the counter decrements at $\phi 2$ clock rate. Upon reaching zero, an interrupt flag is set, and IRQ goes low if the T1 interrupt is enabled. Timer 1 then disables any further interrupts, or automatically transfers the contents of

the latches into the counter and continues to decrement. In addition, the timer may be programmed to invert the output signal on a peripheral pin (PB7) each time it "times-out". Each of these modes is discussed separately below.

Note that the processor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch (T1L-L) when the processor writes into the high order counter (T1C-H). In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order latch.

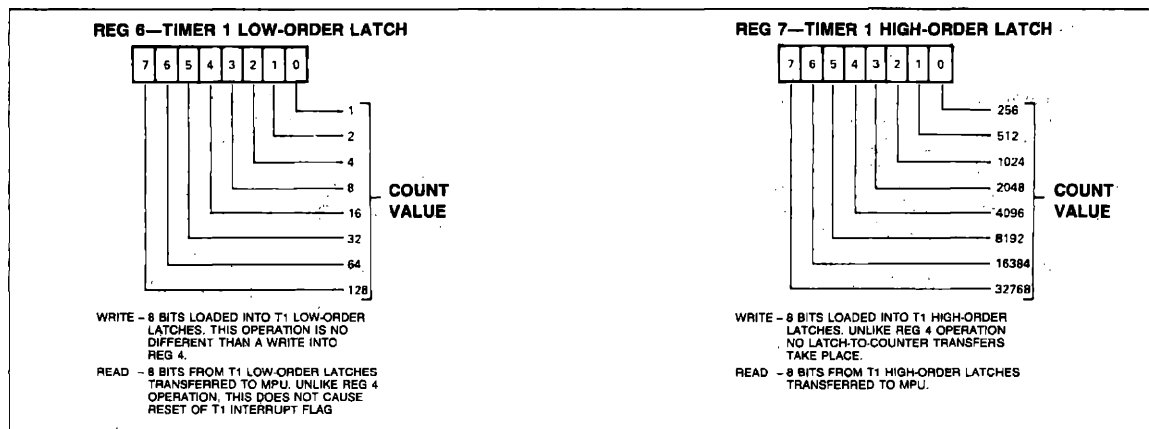


Figure 12. Timer 1 (T1) Latch Registers

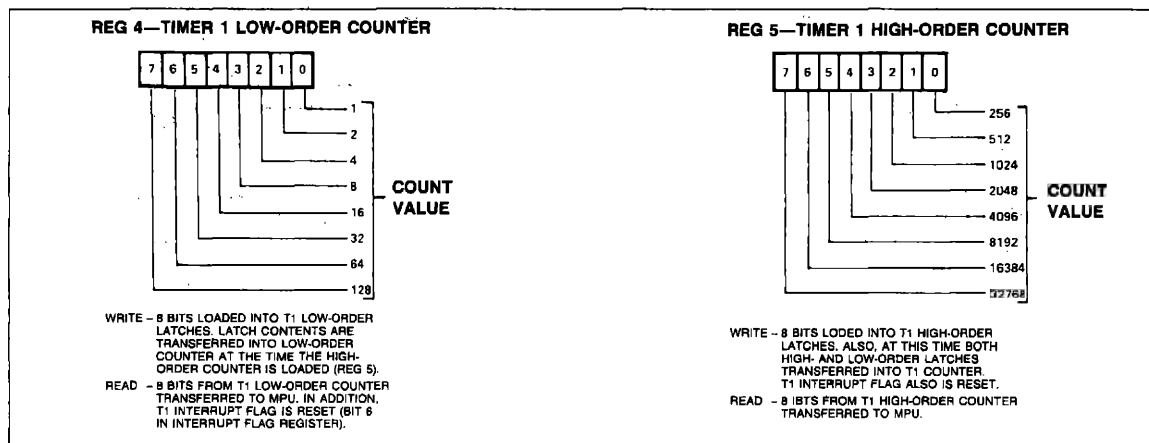


Figure 13. Timer 1 (T1) Counter Registers

REG 11—AUXILIARY CONTROL REGISTER

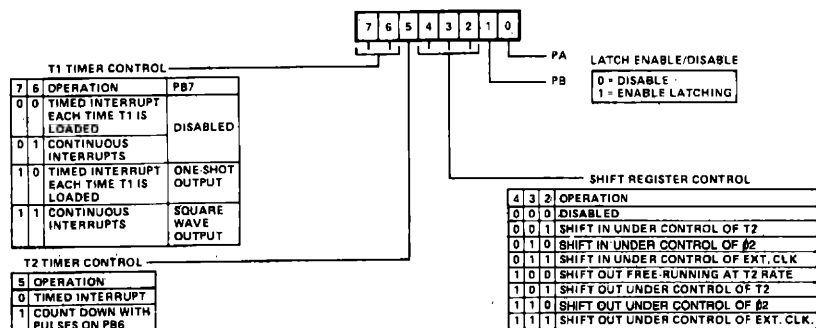


Figure 14. Auxiliary Control Register (ACR)

Timer 1 One-Shot Mode

The Timer 1 one-shot mode generates a single interrupt for each timer load operation. As with any interval timer, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR7=1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

T1 interrupt flag will be set, the $\overline{\text{IRQ}}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared as described in this specification.

Timing for the R6522 interval timer one-shot modes is shown in Figure 15.

In the one-shot mode, writing into the T1L-H has no effect on the operation of Timer 1. However, it will be necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation. When the processor writes into the high order counter (T1C-H), the T1 interrupt flag will be cleared, the contents of the low order latch will be transferred into the low order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the $\phi 2$ following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{\text{IRQ}}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared as described in this specification.

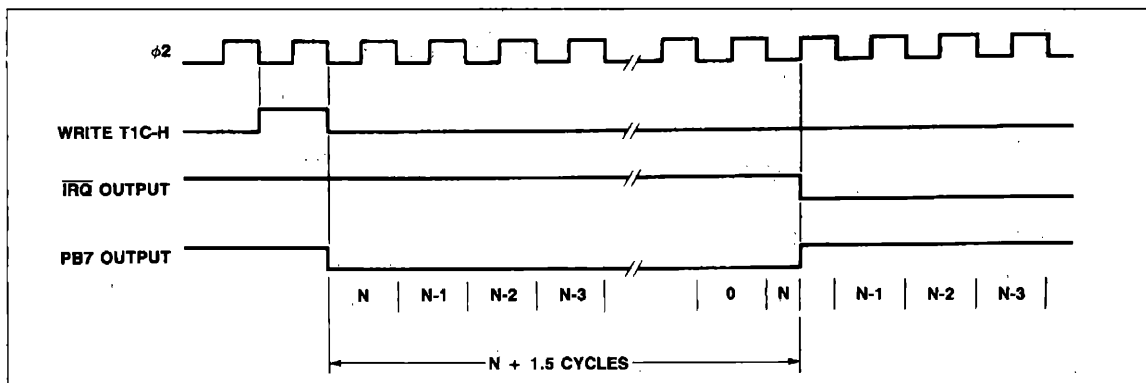


Figure 15. Timer 1 One-Shot Mode Timing

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero. However, instead of continuing to decrement from zero after a time-out, the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H, by reading T1C-L, or by writing directly into the flag as described later. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out.

All interval timers in the R6522 are "re-triggerable". Rewriting the

counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated.

A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If one is 1 and the other is 0, then PB7 functions as a normal output pin, controlled by ORB bit 7.

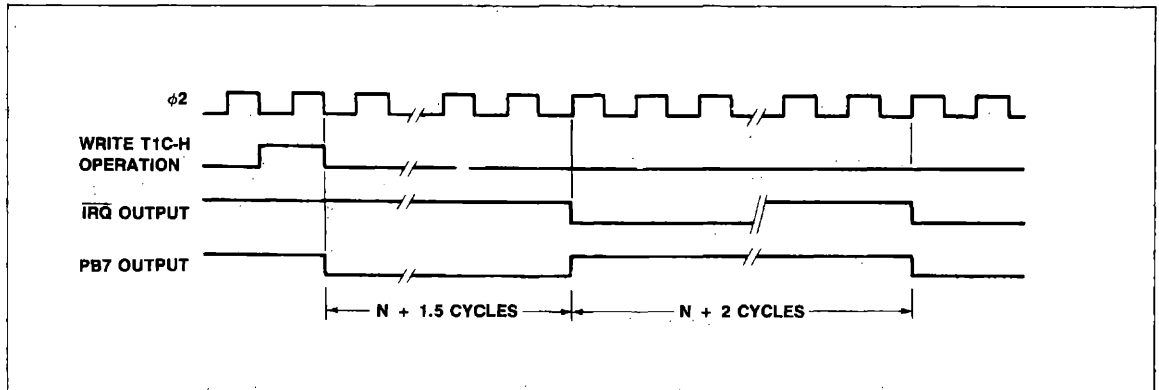


Figure 16. Timer 1 Free-Run Mode Timing

Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-slot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit in the Auxiliary Control Register selects between these two modes. This timer is comprised of a "write-only" lower-order latch (T2L-L), a "read-only" low-order counter (T2C-L) and a read/write high order counter (T2C-H). The counter registers act as a 16-bit counter which decrements at $\phi 2$ rate. Figure 17 illustrates the T2 Latch/Counter Registers.

Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag is disabled after initial time-out so that it will not be set by the counter

decrementing again through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 counts a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag is set when T2 counts down past zero. The counter will then continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on a subsequent time-out. Timing for this mode is shown in Figure 19. The pulse must be low on the leading edge of $\phi 2$.

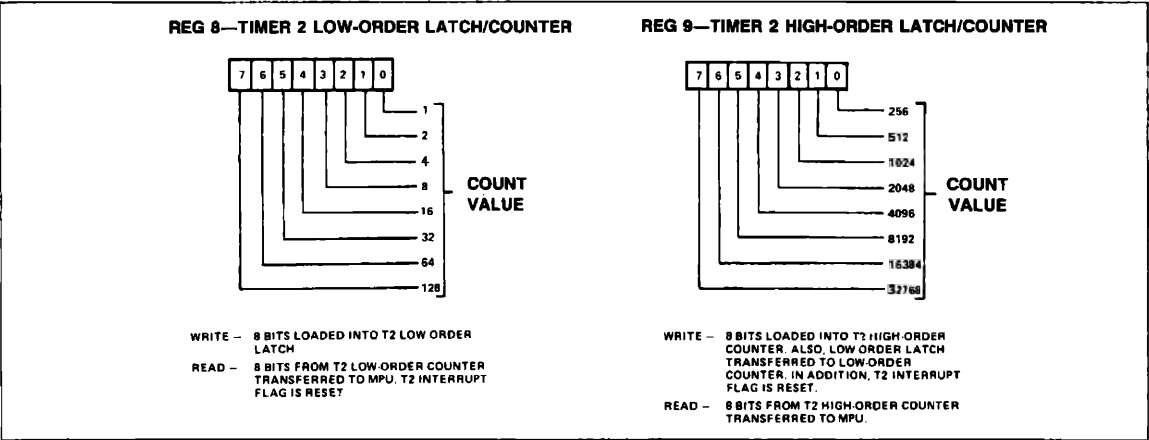


Figure 17. Timer 2 (T2) Latch/Counter Registers

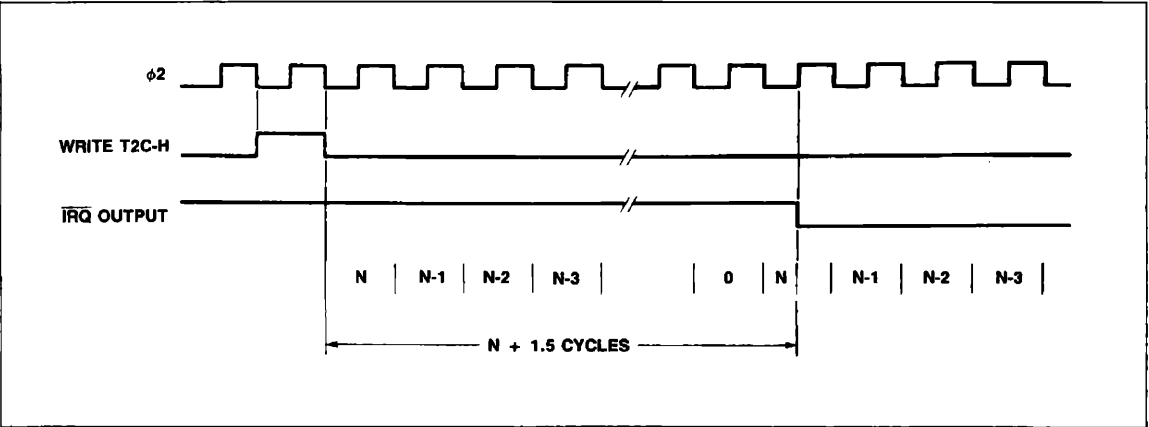


Figure 18. Timer 2 One-Shot Mode Timing

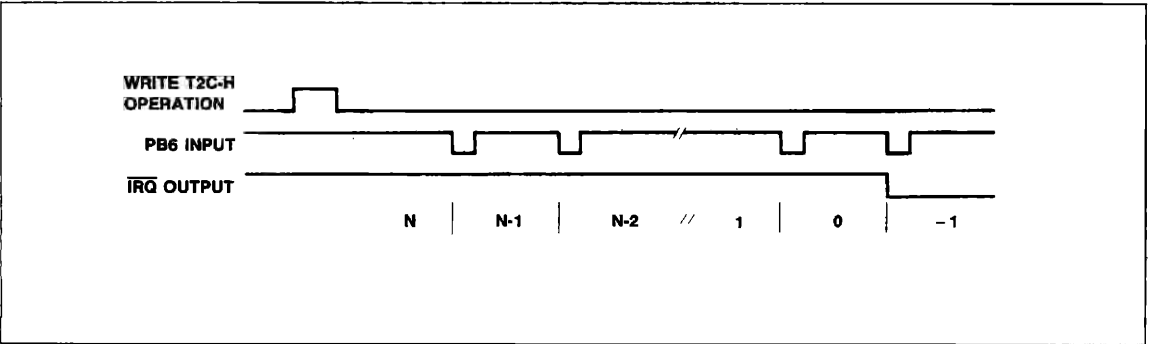


Figure 19. Timer 2 Pulse Counting Mode

SHIFT REGISTER OPERATION

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 20 illustrates the configuration of the SR data bits and Figure 21 shows the SR control bits of the ACR.

SR Mode 0 — Disabled

Mode 0 disables the Shift Register. In this mode the microprocessor can write or read the SR and the SR will shift on each CB1 positive edge shifting in the value on CB2. In this mode the SR interrupt flag is disabled (held to a logic 0).

SR Mode 1 — Shift In Under Control of T2

In mode 1, the shifting rate is controlled by the low order 8 bits of T2 (Figure 22). Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by the read or write of the SR if the SR flag is set in the IFR. Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit of the shift register on the negative-going edge of each clock pulse. The input data should change before the positive-going edge of the CB1 clock pulse. This data is shifted into the shift register during the $\phi 2$ clock cycle following the positive-going edge of the CB1 clock pulse. After 8 CB1 clock pulses, the shift register interrupt flag will set and IRQ will go low.

SR Mode 2 — Shift In Under $\phi 2$ Control

In mode 2, the shift rate is a direct function of the system clock frequency (Figure 23). CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted, first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each $\phi 2$ clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.

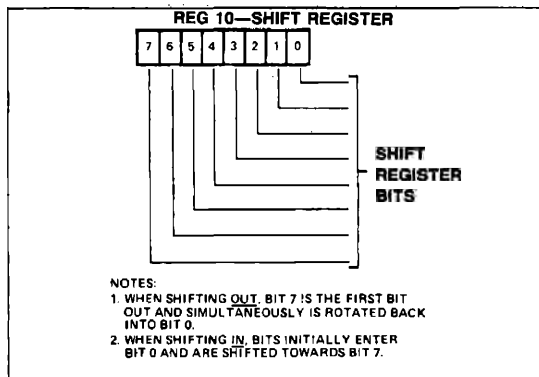


Figure 20. Shift Registers

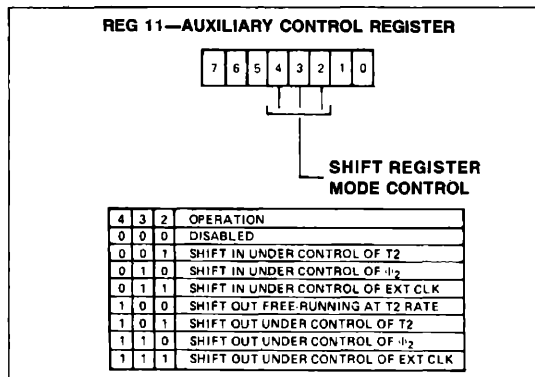


Figure 21. Shift Register Modes

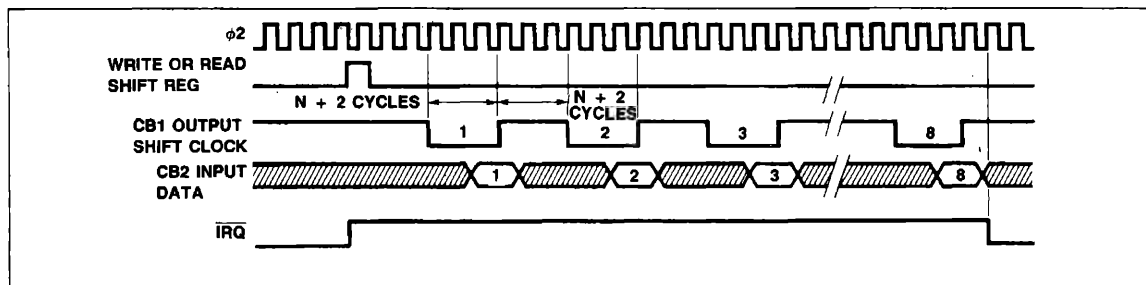


Figure 22. SR Mode 1 — Shift In Under T2 Control

SR Mode 3 — Shift in Under CB1 Control

In mode 3, external pin CB1 becomes an Input (Figure 24). This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. However, the shift register counter does not stop the shifting operation; it acts simply as a pulse counter. Reading or writing the Shift Register resets the Interrupt Flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

SR Mode 4 — Shift Out Under T2 Control (Free-Run)
Mode 4 is very similar to mode 5 in which the shifting rate is set by

T2. However, in mode 4 the SR Counter does not stop the shifting operation (Figure 25). Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CB2 repetitively. In this mode the shift register counter is disabled.

SR Mode 5 — Shift Out Under T2 Control

In mode 5, the shift rate is controlled by T2 (as in mode 4). The shifting operation is triggered by the read or write of the SR if the SR flag is set in the IFR (Figure 26). Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.

2

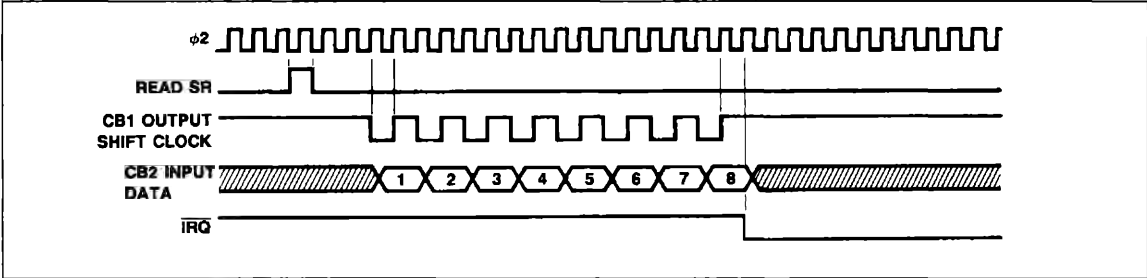


Figure 23. SR Mode 2 — Shift In Center φ2 Control

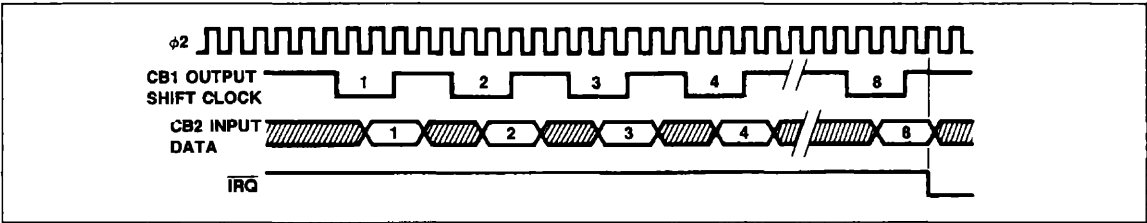


Figure 24. SR Mode 3 — Shift In Under CB1 Control

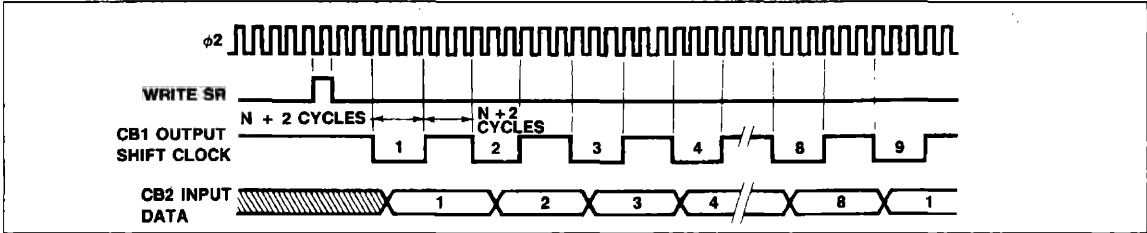


Figure 25. SR Mode 4 — Shift Out Under T2 Control (Free-Run)

SR Mode 6 — Shift Out Under $\phi 2$ Control

In mode 6, the shift rate is controlled by the $\phi 2$ system clock (Figure 27).

SR Mode 7 — Shift Out Under CB1 Control

In mode 7, shifting is controlled by pulses applied to the CB1 pin by an external device (Figure 28). The SR counter sets the SR

Interrupt Flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor, writes or reads the shift register, the SR Interrupt Flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the Interrupt Flag is set. The microprocessor can then load the shift register with the next byte of data.

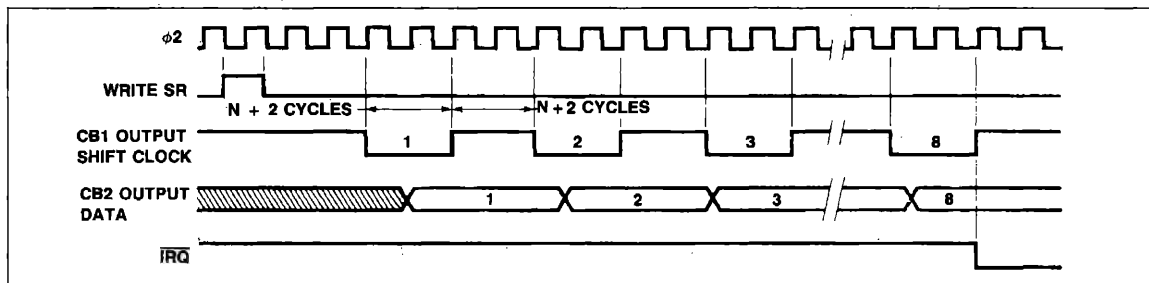


Figure 26. SR Mode 5 — Shift Out Under T2 Control

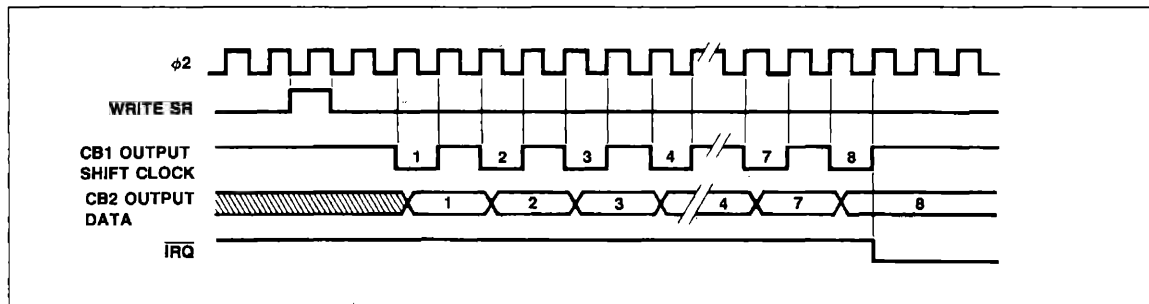


Figure 27. SR Mode 6 — Shift Out Under $\phi 2$ Control

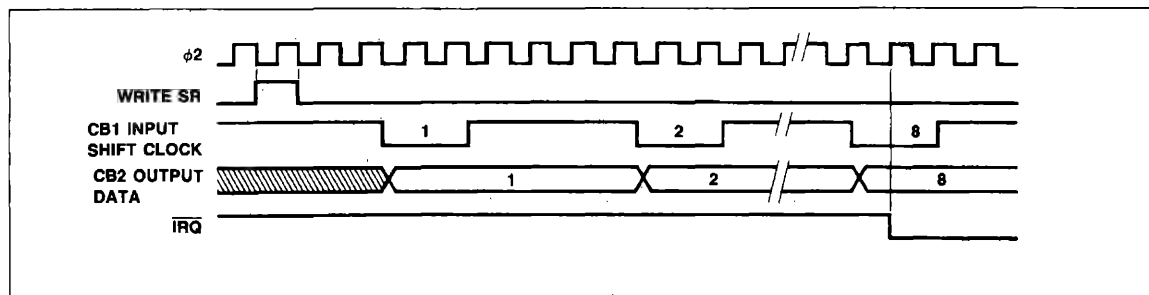


Figure 28. SR Mode 7 — Shift Out Under CB1 Control

Interrupt Operation

Controlling interrupts within the R6522 involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupt exists within the chip. Interrupt flags are set in the Interrupt Flag Register (IFR) by conditions detected within the R6522 or on inputs to the R6522. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order, from highest to lowest priority.

Associated with each Interrupt flag is an interrupt enable bit in the Interrupt Enable Register (IER). This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output (IRQ) will go low. IRQ is an "open-collector" output which can be "wire-OR'ed" with other devices in the system to interrupt the processor.

Interrupt Flag Register (IFR)

In the R6522, all the interrupt flags are contained in one register, i.e., the IFR (Figure 29). In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

The Interrupt Flag Register (IFR) may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the

status of the $\overline{\text{IRQ}}$ output. This bit corresponds to the logic function: $\text{IRQ} = \text{IFR6} \times \text{IER6} + \text{IFR5} \times \text{IER5} + \text{IFR4} \times \text{IER4} + \text{IFR3} \times \text{IER3} + \text{IFR2} \times \text{IER2} + \text{IFR1} \times \text{IER1} + \text{IFR0} \times \text{IER0}$.

Note:

\times = logic AND, $+$ = Logic OR.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

Interrupt Enable Register (IER)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register (IER) (Figure 30). Individual bits in the IER can be set or cleared to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to the (IER) after bit 7 set or cleared to, in turn, set or clear selected enable bits. If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Selected bits in the IER can be set by writing to the IER with bit 7 in the data word set to a 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the contents of this register can be read at any time. Bit 7 will be read as a logic 1, however.

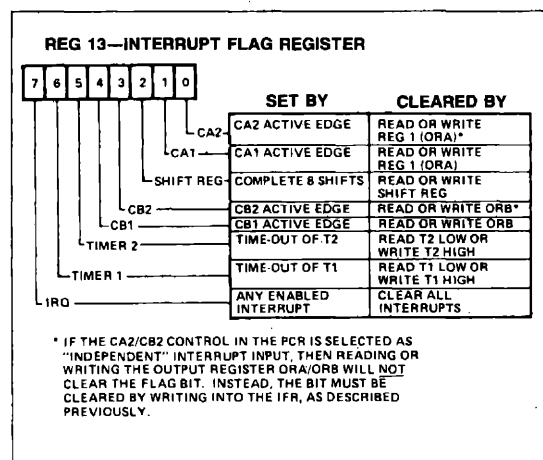


Figure 29. Interrupt Flag Register (IFR)

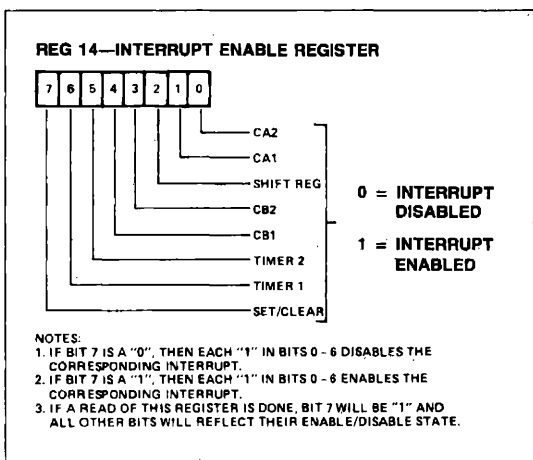


Figure 30. Interrupt Enable Register (IER)

PERIPHERAL INTERFACE CHARACTERISTICS

Symbol	Characteristic	Min.	Max.	Unit	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals	—	1.0	μs	—
t_{CA2}	Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	—	1.0	μs	31a, 31b
t_{RS1}	Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	—	1.0	μs	31a
t_{RS2}	Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	—	2.0	μs	31b
t_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	0.05	1.0	μs	31c, 31d
t_{DS}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0.20	1.5	μs	31c, 31d
t_{RS3}	Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (pulse mode)	—	1.0	μs	31c
t_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	—	2.0	μs	31d
t_{21}	Delay Time Required from CA2 Output to CA1 Active Transition (handshake mode)	400	—	ns	31d
t_{IL}	Setup Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	300	—	ns	31e
t_{AL}	CA1, CB1 Setup Prior to Transition to Arm Latch	300	—	ns	31e
t_{PDH}	Peripheral Data Hold After CA1, CB1 Transition	150	—	ns	31e
t_{SR1}	Shift-Out Delay Time — Time from ϕ_2 Falling Edge to CB2 Data Out	—	300	ns	31f
t_{SR2}	Shift-In Setup Time — Time from CB2 Data In to ϕ_2 Rising Edge	300	—	ns	31g
t_{SR3}	External Shift Clock (CB1) Setup Time Relative to ϕ_2 Trailing Edge	100	T_{CY}	ns	31g
t_{IPW}	Pulse Width — PB6 Input Pulse	$2 \times T_{CY}$	—		31i
t_{ICW}	Pulse Width — CB1 Input Clock	$2 \times T_{CY}$	—		31h
t_{IPS}	Pulse Spacing — PB6 Input Pulse	$2 \times T_{CY}$	—		31i
t_{ICS}	Pulse Spacing — CB1 Input Pulse	$2 \times T_{CY}$	—		31h

PERIPHERAL INTERFACE WAVEFORMS

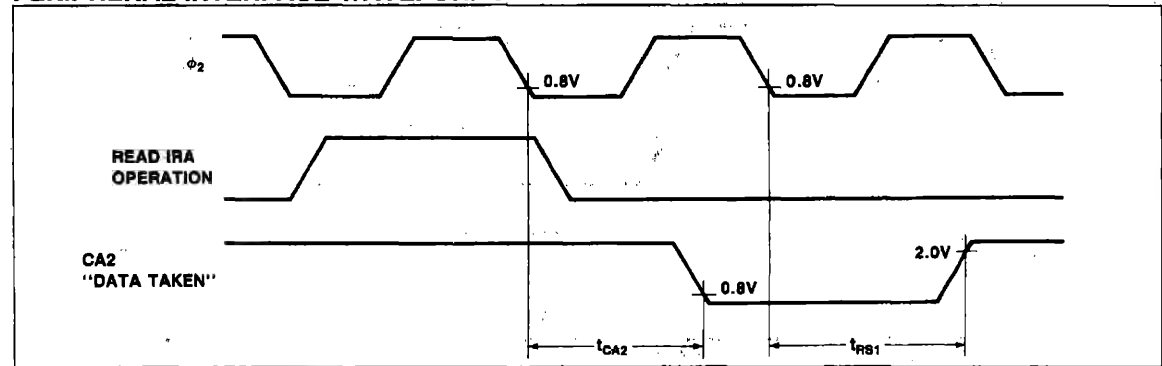


Figure 31a. CA2 Timing for Read Handshake, Pulse Mode

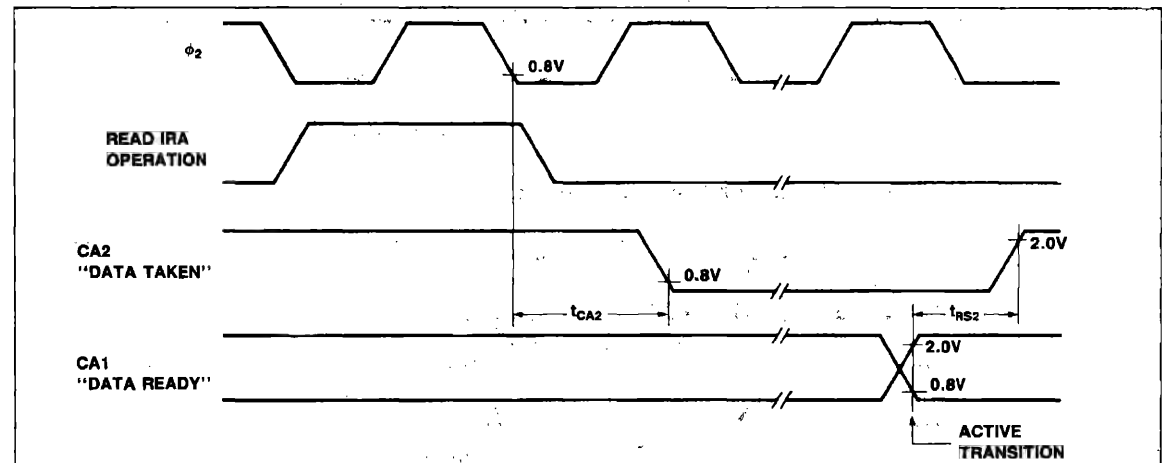


Figure 31b. CA2 Timing for Read Handshake, Handshake Mode

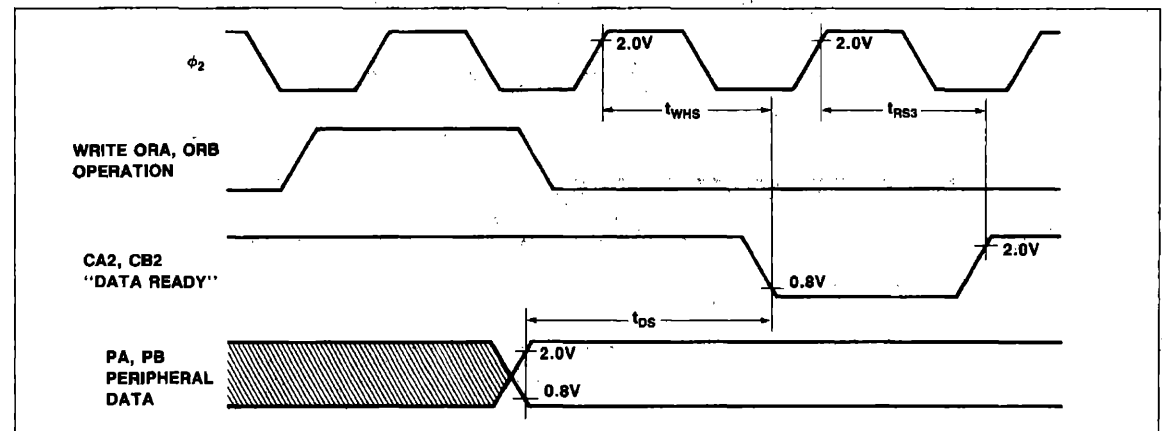


Figure 31c. CA2, CB2 Timing for Write Handshake, Pulse Mode

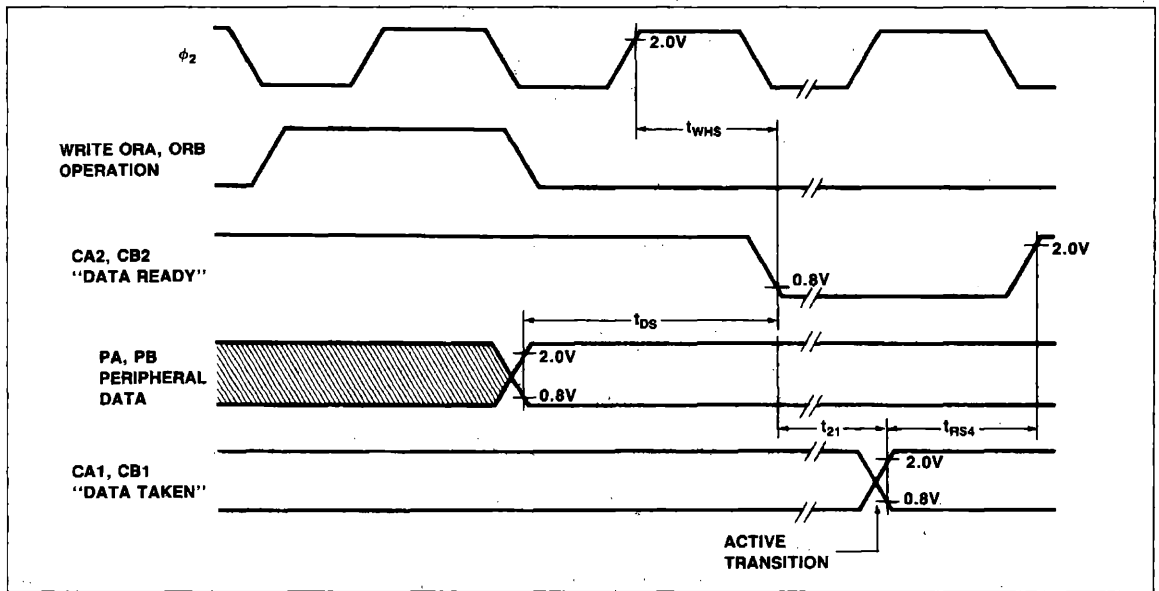


Figure 31d. CA2, CB2 Timing for Write Handshake, Handshake Mode

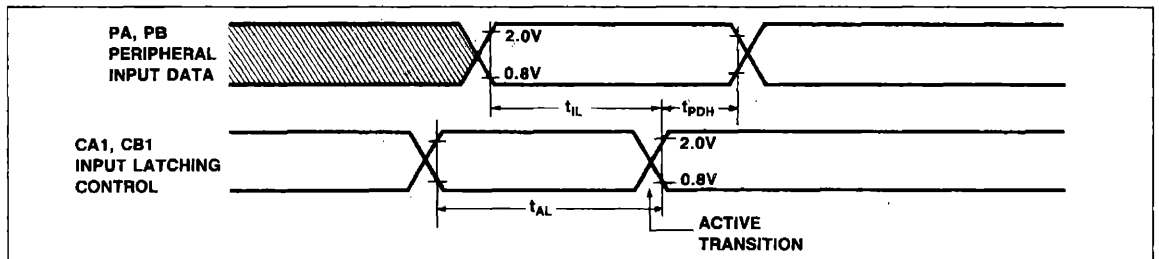


Figure 31e. Peripheral Data Input Latching Timing

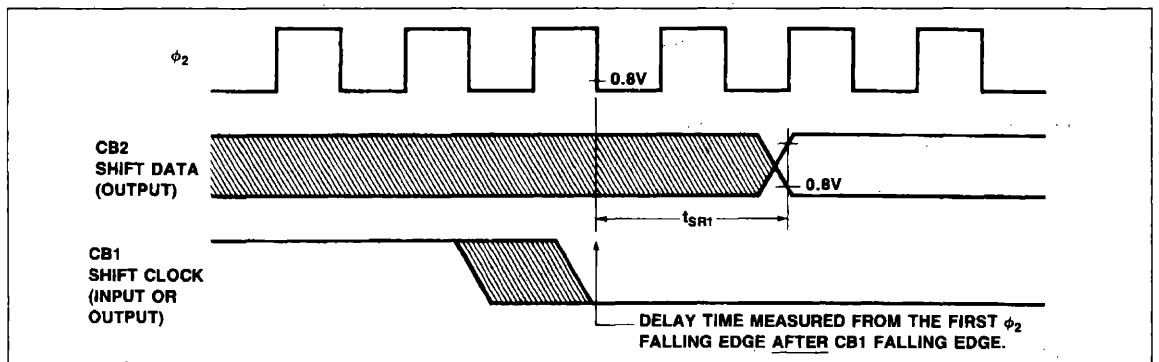


Figure 31f. Timing for Shift Out with Internal or External Shift Clocking

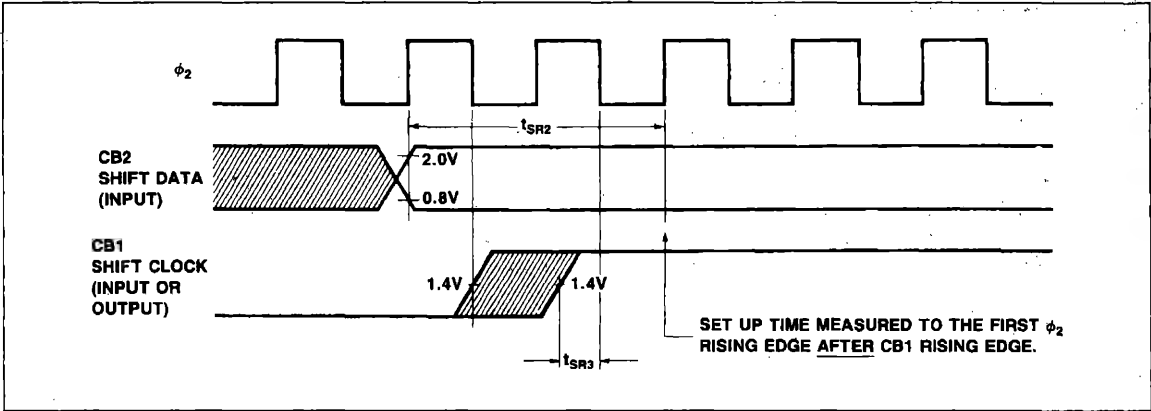


Figure 31g. Timing for Shift In with Internal or External Shift Clocking

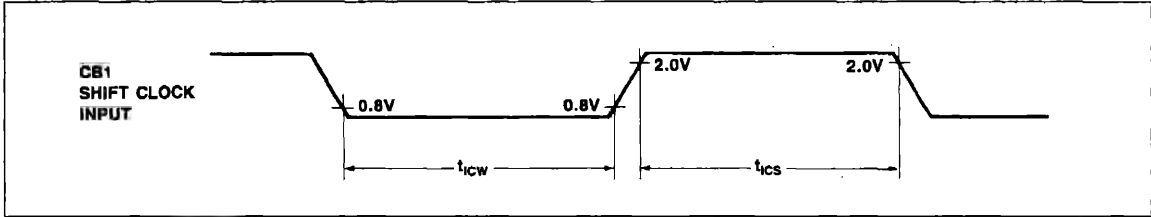


Figure 31h. External Shift Clock Timing

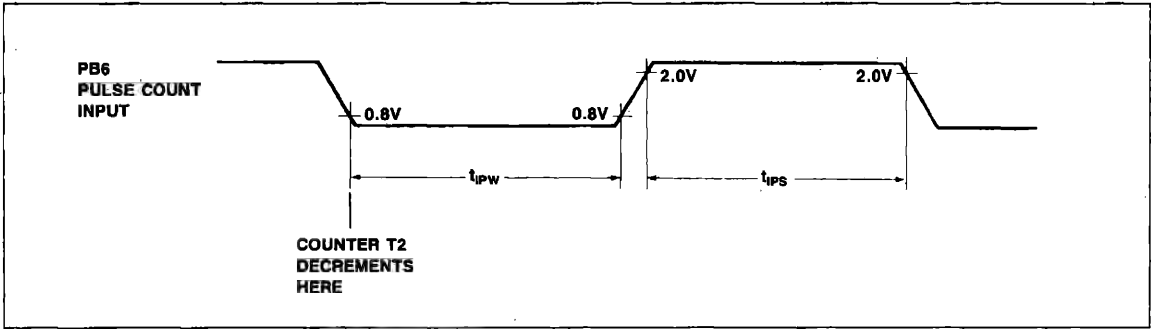


Figure 31i. Pulse Count Input Timing

BUS TIMING CHARACTERISTICS

Parameter	Symbol	R6522 (1 MHz)		R6522A (2 MHz)		Unit
		Min.	Max.	Min.	Max.	

READ TIMING

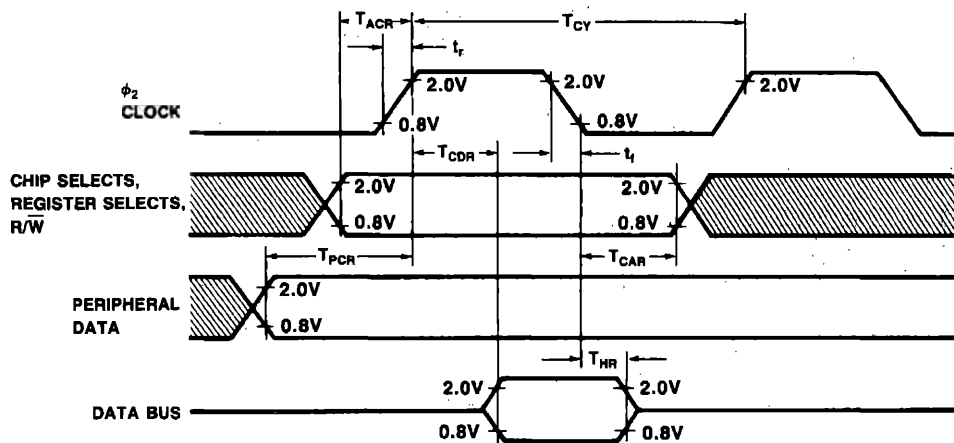
Cycle Time	T_{CY}	1	10	0.5	10	μs
Address Set-Up Time	T_{ACR}	180	—	90	—	ns
Address Hold Time	T_{CAR}	0	—	0	—	ns
Peripheral Data Set-Up Time	T_{PCR}	300	—	150	—	ns
Data Bus Delay Time	T_{CDR}	—	365	—	190	ns
Data Bus Hold Time	T_{HR}	10	—	10	—	ns

WRITE TIMING

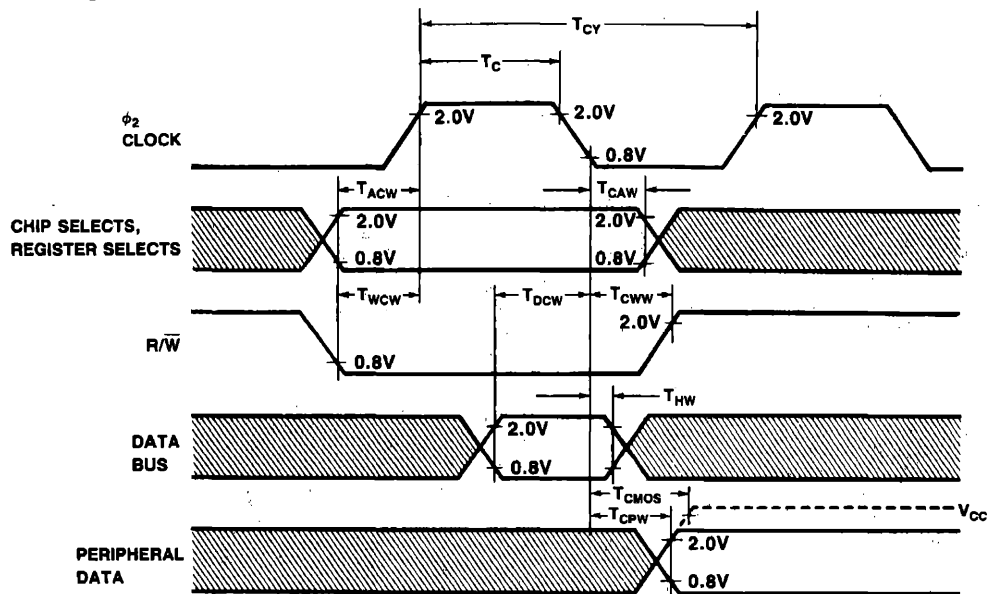
Cycle Time	T_{CY}	1	10	0.50	10	μs
$\phi 2$ Pulse width	T_C	470	—	235	—	ns
Address Set-Up Time	T_{ACW}	180	—	90	—	ns
Address Hold Time	T_{CAW}	0	—	0	—	ns
R/W Set-Up Time	T_{WCW}	180	—	90	—	ns
R/W Hold Time	T_{CWW}	0	—	0	—	ns
Data Bus Set-Up Time	T_{DCW}	200	—	90	—	ns
Data Bus Hold Time	T_{HW}	10	—	10	—	ns
Peripheral Data Delay Time	T_{CPW}	—	1.0	—	0.5	μs
Peripheral Data Delay Time to CMOS Levels	T_{CMOS}	—	2.0	—	1.0	μs
Note: t_R and t_F = 10 to 30 ns.						

BUS TIMING WAVEFORMS

Read Timing Waveforms



Write Timing Waveforms



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to -7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	0 to +70 -40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V \pm 5%
Temperature Range Commercial	T_A	0°C to 70°C

DC CHARACTERISTICS

($V_{CC} = 5.0$ Vdc \pm 5%, $V_{SS} = 0$, $T_A = T_L$ to T_H , unless otherwise noted)

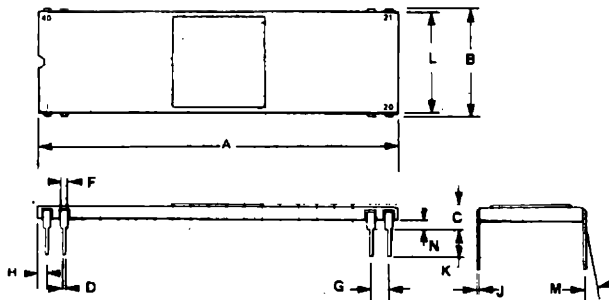
Parameter	Symbol	Min.	Typ. ³	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	2.4	—	V_{CC}	V	
Input Low Voltage	V_{IL}	-0.3	—	0.4	V	
Input Leakage Current R/W, RES, RS0, RS1, RS2, RS3, CS1, CS2, CA1, \emptyset 2	I_{IN}	—	± 1	± 2.5	μ A	$V_{IN} = 0$ V to 5.25V $V_{CC} = 0$ V
Input Leakage Current for Three-State Off D0-D07	I_{TSI}	—	± 2	± 10	μ A	$V_{IN} = 0.4$ V to 2.4V $V_{CC} = 5.25$ V
Input High Current PA0-PA7, CA2, PB0-PB7, CB1, CBS	I_{IH}	-100	-200	—	μ A	$V_{IN} = 2.4$ V $V_{CC} = 5.25$ V
Input Low Current PA0-PA7, CA2, PB0-PB7, CB1, CB2	I_{IL}	—	-0.9	-1.8	mA	$V_{IL} = 0.4$ V $V_{CC} = 5.25$ V
Output High Voltage All outputs PB0-PB7, CB2 (Darlington Drive)	V_{OH}	2.4 1.5	— —	— —	V V	$V_{CC} = 4.75$ V $I_{LOAD} = -100$ μ A $I_{LOAD} = -1.0$ mA
Output Low Voltage	V_{OL}	—	—	0.4	V	$V_{CC} = 4.75$ V $I_{LOAD} = 1.6$ mA
Output High Current (Sourcing) Logic PB0-PB7, CB2 (Darlington Drive)	I_{OH}	-100 -1.0	-1000 -2.5	— -10	μ A mA	$V_{OH} = 2.4$ V $V_{OH} = 1.5$ V
Output Low Current (Sinking)	I_{OL}	1.6	—	—	mA	$V_{OL} = 0.4$ V
Output Leakage Current (Off State) IRQ	I_{OFF}	—	4	± 10	μ A	$V_{OH} = 2.4$ V $V_{CC} = 5.25$ V
Power Dissipation	P_D	—	450	700	mW	
Input Capacitance R/W, RES, RS0, RS1, RS2, RS3, CS1, CS2, D0-D7, PA0-PA7, CA1, CA2, PB0-PB7 CB1, CB2 \emptyset 2 Input	C_{IN}	— — —	— — —	7 10 20	pF pF pF	$V_{CC} = 5.0$ V $V_{IN} = 0$ V $f = 1$ MHz $T_A = 25^\circ$ C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:

1. All units are direct current (DC) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values shown for $V_{CC} = 5.0$ V and $T_A = 25^\circ$ C.

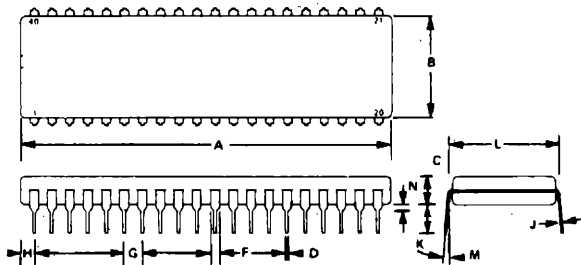
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.85	15.82	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54	BSC	0.100	BSC
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0"	10"	0"	10"
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24	BSC	0.600	BSC
M	7"	10"	7"	10"
N	0.51	1.02	0.020	0.040



R6530 ROM-RAM-I/O-TIMER (RRIOT)

DESCRIPTION

The R6530 ROM-RAM-I/O-Timer (RRIOT) combines read only memory, random access memory, parallel I/O data ports, and timer functions into a single peripheral device which operates in conjunction with any CPU in the R6500 microprocessor family. The R6530 allows two chip solutions in a variety of production applications. It is comprised of a mask programmable 1024 × 8 ROM, a 64 × 8 static RAM, two software controlled 8-bit bidirectional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, and a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods.

FEATURES

- 1024 × 8 mask programmable ROM
- 64 × 8 static RAM
- Two 8-bit bidirectional data ports for interface to peripherals
- Two programmable data direction registers
- Programmable interval timer
- Programmable interval timer interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with direct transistor drive capability
- 8-bit directional data bus for direct communication with the microprocessor
- High impedance three-state data bus
- Allows up to 7K contiguous bytes of ROM with no external decoding

ORDERING INFORMATION

Part Number: R6530

Package:

C = Ceramic DIP

P = Plastic DIP

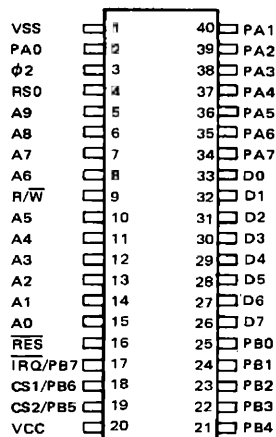
Temperature Range:

0°C to 70°C

Frequency:

1 MHz

Note: A custom part number will be assigned by Rockwell. ROM codes should be submitted using ROM Code Order Form, Order No. 2137.



R6530 Pin Configuration

INTERFACE SIGNALS

RESET (\overline{RES})

During system initialization, a \overline{RES} input causes zeroing of all four I/O registers. This in turn causes all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an off state during Reset. Interrupt capability is disabled with the \overline{RES} signal. The \overline{RES} signal must be held low for at least one clock period when reset is required.

READ/WRITE (R/\overline{W})

The R/\overline{W} input is supplied by the microprocessor and controls the transfer of data between the R6530 and the microprocessor via the data bus. A high on the R/\overline{W} pin reads (with proper addressing) data from the R6530 onto the data bus. A low on the R/\overline{W} pin writes (with proper addressing) data from the data bus into R6530.

PHASE 2 CLOCK ($\emptyset 2$)

The Phase 2 clock ($\emptyset 2$) input is the system clock generated by the CPU that triggers all data transfers between the data bus and the R6530.

INTERRUPT REQUEST (\overline{IRQ})

The \overline{IRQ} pin is an interrupt pin from the interval timer. This same pin, if not used as an interrupt, can be used as a peripheral I/O pin (PB7). When used as an interrupt, the pin should be set up as an input by the Data Direction Register. The pin will be normally high with a low indicating an interrupt from the R6530. An external pull-up device is not required; however, if collector-OR'd with other devices, the internal pullup may be omitted with a mask option.

DATA BUS (D0–D7)

The R6530 has eight bidirectional data pins (D0–D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor. The output buffers remain in the off state except when selected for a Read operation.

ADDRESS LINES (A0–A9)

There are 10 address pins (A0–A9). In addition, there is the ROM Select pin (RS0). Further, pins PB5 and PB6 are mask programmable, and can be used either individually or together as chip selects. When used as peripheral data pins they cannot be used as chip selects.

ROM SELECT (RS0)

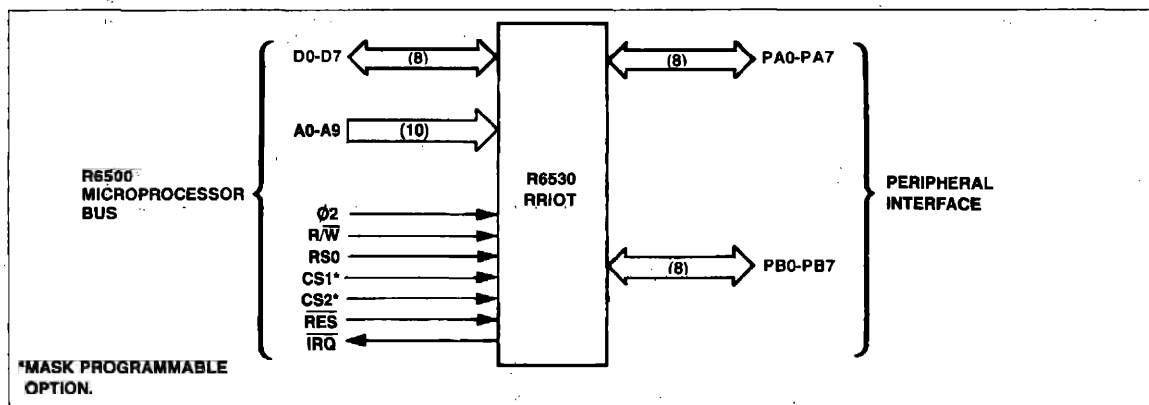
RS0 serves as an additional address input line. When RS0 is high, internal ROM is selected; when RS0 is low, internal ROM is not selected.

PERIPHERAL DATA PORTS

The R6530 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0–PA7 and PB0–PB7. PB5, PB6 and PB7 also have other uses which are discussed in later sections. The pins are set up as an input by writing a "0" into the corresponding bit of the Data Direction Register. A "1" into the Data Direction Register causes its corresponding bit to be an output. When in the input mode, the Peripheral Data Buffers are in the "1" state and the internal pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the R6530 it receives data stored in the Output Register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts (for a "1") or less than 0.8 volts (for a "0") as the peripheral pins are all TTL compatible.

CHIP SELECT (CS0, CS1)

Pins 18 and 19 are individually selectable at mask time as either chip selects CS1 and CS2, respectively, or port B functions PB6 and PB5, respectively.



Interface Signals

INTERNAL ORGANIZATION

The R6530 is divided into four basic sections: RAM, ROM, I/O and Timer. The RAM and ROM interface directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an Output Register.

ROM—1K BYTE (8K BITS)

The 1K byte ROM is in a 1024×8 configuration. Address lines A0–A9, as well as RS0 are needed to address the entire ROM. With the addition of CS1 and CS2, seven R6530's may be addressed, giving 7168×8 bits of contiguous ROM.

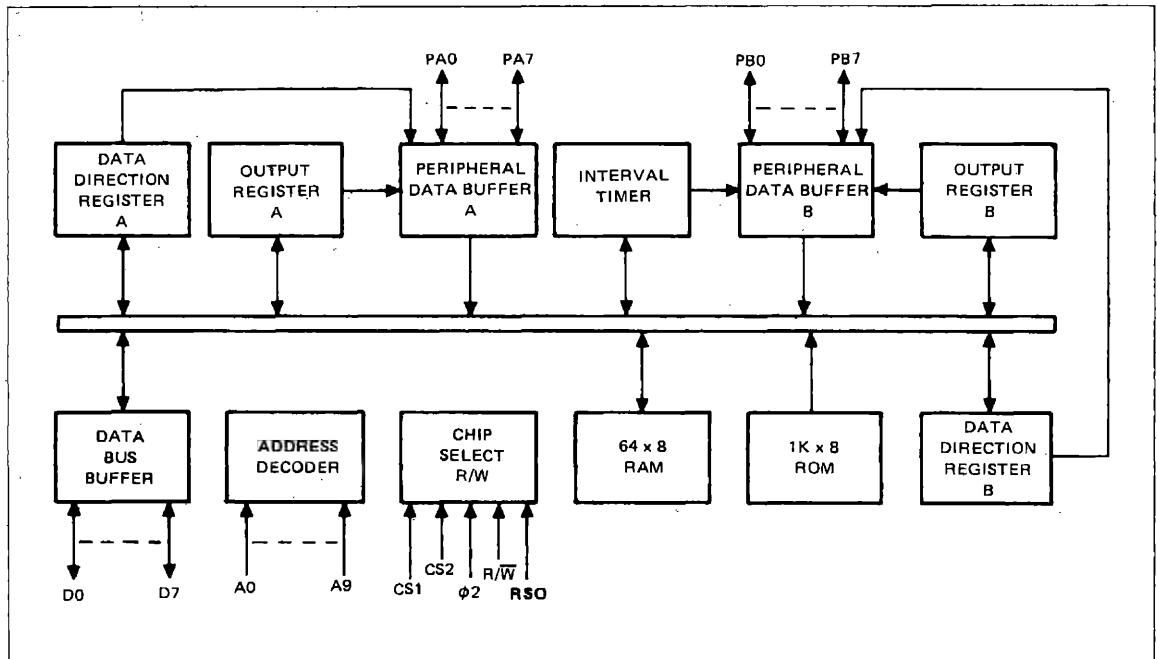
RAM—64 BYTES (512 BITS)

A 64×8 static RAM is contained on the R6530. It is addressed by A0–A5 (Byte Select), RS0, A6, A7, A8, A9 and, depending on the number of chips in the system, CS1 and CS2.

INTERNAL PERIPHERAL REGISTERS

There are four internal registers, two data direction registers and two output registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral buffer pin as an output. Therefore, anything then written into the Output Register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data from the Output Register. For example, a "1" loaded into Data Direction Register A, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and remain in the high state. The two Data Output Registers are used to latch data from the Data Bus during a Write operation until the peripheral device can read the data supplied by the microprocessor.

During a Read operation the microprocessor is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the Output Register. The only way the Output Register data can be changed is by a microprocessor Write operation. The Output Register is not affected by a Read of the data on the peripheral pins.



R6530 Block Diagram

INTERVAL TIMER

The Timer section of the R6530 contains three basic parts: pre-scale divide down register, programmable 8-bit register and interrupt logic.

The interval timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock begins counting down to a maximum of -225T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

The 8 bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Timer Register.

At the same time that data is being written to the Interval Timer, the counting interval (1, 8, 64, or 1024T) is decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., A3 = 1 enables \overline{IRQ} on PB7, A3 = 0 disables \overline{IRQ} on PB7. When PB7 is to be used as an interrupt flag with the interval timer it should be programmed as an input. If PB7 is enabled by A3 and an interrupt occurs PB7 will go low. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

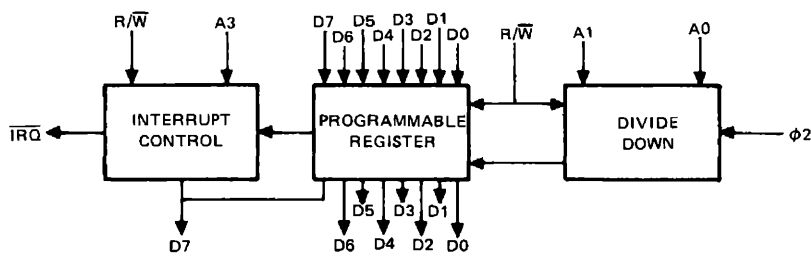
When the timer has counted down to 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the Timer Register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is in one's complement.

Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1 = 27

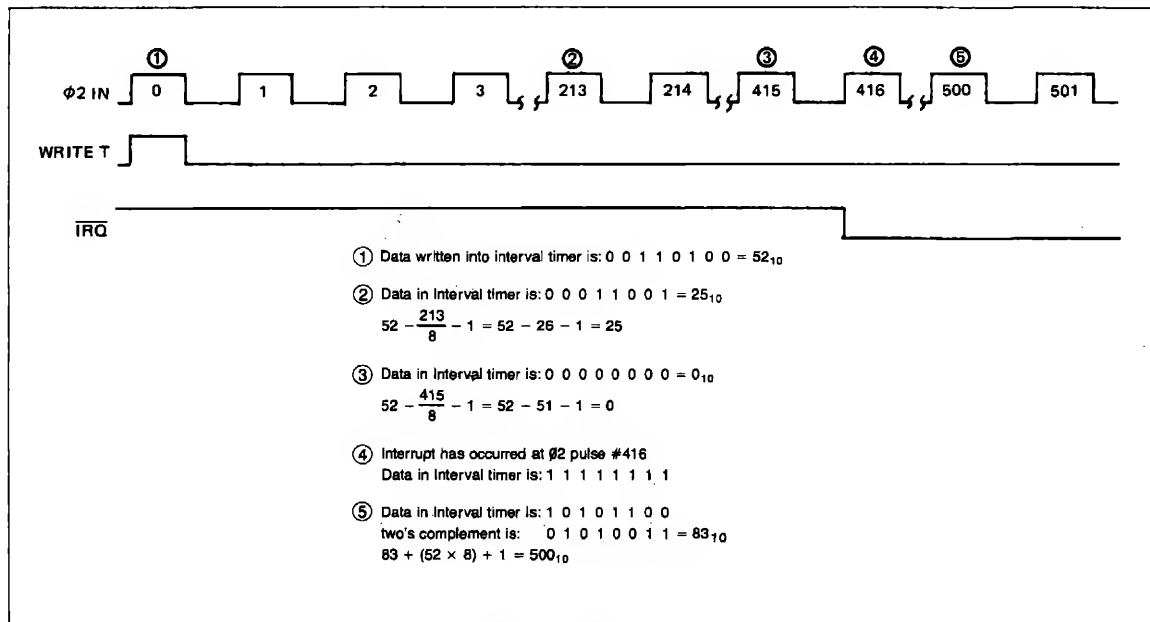
Thus, to arrive at the total elapsed time, merely do a one's complement and add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is $(52 \times 8) + 1 = 417T$. Total elapsed time would be $417T + 27T = 444T$, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After the interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flag is read on D7 all other D outputs (D0 through D6) go to "0".

When reading the timer after an interrupt, A3 should be low so as to disable the \overline{IRQ} pin. This is done so as to avoid future interrupts until after another Write timer operation.



Basic Elements of Interval Timer



R6530 Timer Example

ADDRESSING

Addressing of the R6530 offers many variations to the user for greater flexibility. The user may configure his system with RAM in lower memory, ROM in higher memory, and I/O registers with interval timers between the extremes. There are 10 address lines (A0–A9). In addition, there is the possibility of 3 additional address lines to be used as chip-selects and to distinguish between ROM, RAM, I/O and interval timer. Two of the additional lines are chip-selects 1 and 2 (CS1 and CS2). The chip-select pins can also be PB5 and PB6. Whether the pins are used as chip-selects or peripheral I/O pins is a mask option and must be specified when ordering the part. Both pins act independently of each other in that either or both pins may be designated as a chip-select. The third additional address line is RS0. The R6502 and R6530 in a 2-chip system would use RS0 to distinguish between ROM and non-ROM sections of the R6530. With the addressing pins available, a total of 7K contiguous ROM may be addressed with no external decode. Following is an example of a 1-chip and a 7-chip R6530 Addressing Scheme.

ONE-CHIP ADDRESSING

A 1-chip system decode is illustrated in the R6530 One-Chip Address Encoding Diagram.

SEVEN-CHIP ADDRESSING

In the seven-chip system, the objective would be to have 7K bytes of contiguous ROM, with RAM in low order memory. The 7K of ROM could be placed between addresses 65,535 and 1024. For this case, assume A13, A14 and A15 are all 1 when addressing ROM, and 0 when addressing RAM or I/O. This would place the 7K ROM between addresses 65,535 and 58,367. The two pins designated as chip-select, or I/O, would be masked programmed as chip-select pins. Pin RS0 would be connected to address line A10. Pins CS1 and CS2 would be connected to address lines A11 and A12 respectively. See table 1.

The two examples shown would allow addressing of the ROM and RAM; however, once the I/O or timer has been addressed, further decoding is necessary to select which of the I/O registers are desired, as well as the coding of the interval timer.

I/O REGISTER—TIMER ADDRESSING

Table 2, Addressing Decode for I/O Register and Timer, illustrates the address decoding for the internal elements and timer programming. Address lines A2 distinguishes I/O registers from the timer. When A2 is high and I/O timer select is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the divide by matrix. In addition, Address A3 is used to enable the interrupt flag to PB7.

Table 1. R6530 Seven-Chip Addressing Scheme

Device	Function	Address, Chip Select and Register Select Lines						
		CS2 A12	CS1 A11	RS0 A10	A9	A8	A7	A6
R6530 #1	ROM Select	0	0	1	X	X	X	X
	RAM Select	0	0	0	0	0	0	0
	I/O Timer	0	0	0	1	0	0	0
R6530 #2	ROM Select	0	1	0	X	X	X	X
	RAM Select	0	0	0	0	0	0	1
	I/O Timer	0	0	0	1	0	0	1
R6530 #3	ROM Select	0	1	1	X	X	X	X
	RAM Select	0	0	0	0	0	1	0
	I/O Timer	0	0	0	1	0	1	0
R6530 #4	ROM Select	1	0	0	X	X	X	X
	RAM Select	0	0	0	0	0	1	1
	I/O Timer	0	0	0	1	0	1	1
R6530 #5*	ROM Select	1	0	1	X	X	X	X
	RAM Select	0	0	0	0	1	0	0
	I/O Timer	0	0	0	1	1	0	0
R6530 #6	ROM Select	1	1	0	X	X	X	X
	RAM Select	0	0	0	0	1	0	1
	I/O Timer	0	0	0	1	1	0	1
R6530 #7	ROM Select	1	1	1	X	X	X	X
	RAM Select	0	0	0	0	1	1	0
	I/O Timer	0	0	0	1	1	1	0

Note: * RAM select for R6530 #5 would read = A12•A11•A10•A9•A8•A7•A6

A. X indicates mask programming, i.e.:

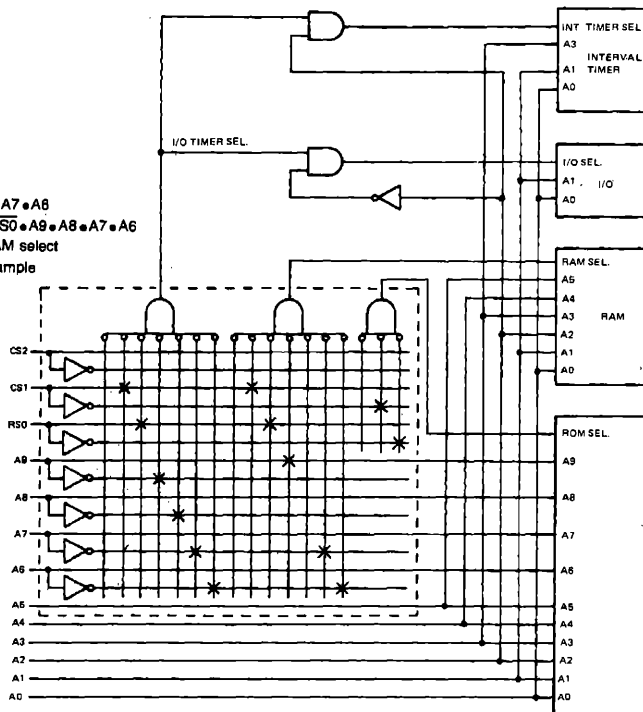
ROM select = $CS1 \cdot RS0$

RAM select = $CS1 \cdot RS0 \cdot A9 \cdot A7 \cdot A8$

I/O TIMER SELECT = $CS1 \cdot RS0 \cdot A9 \cdot A8 \cdot A7 \cdot A6$

B. Notice that A8 is a don't care for RAM select

C. CS2 can be used as PB5 in this example



R6530 One-Chip Address Encoding Diagram

Table 2. Addressing Decode for I/O Register and Timer

Function	Addressing Decode							
	ROM Select	RAM Select	I/O Timer Select	R/W	A3	A2	A1	A0
Read ROM	1	0	0	1	X	X	X	X
Write RAM	0	1	0	0	X	X	X	X
Read RAM	0	1	0	1	X	X	X	X
Write DDRA	0	0	1	0	X	0	0	1
Read DDRA	0	0	1	1	X	0	0	1
Write DDRB	0	0	1	0	X	0	1	1
Read DDRB	0	0	1	1	X	0	1	1
Write Per. Reg. A	0	0	1	0	X	0	0	0
Read Per. Reg. A	0	0	1	1	X	0	0	0
Write Per. Reg. B	0	0	1	0	X	0	1	0
Read Per. Reg. B	0	0	1	1	X	0	1	0
Write Timer								
÷IT	0	0	1	0	*	1	0	0
÷8T	0	0	1	0	*	1	0	1
÷64T	0	0	1	0	*	1	1	0
÷1024T	0	0	1	0	*	1	1	1
Read Timer	0	0	1	1	*	1	X	0
Read Interrupt Flag	0	0	1	1	X	1	X	1

Notes: *A3 = 1 Enables \overline{IRQ} to PB7

A3 = 0 Disables \overline{IRQ} to PB7

TIMING CHARACTERISTICS

Read Timing

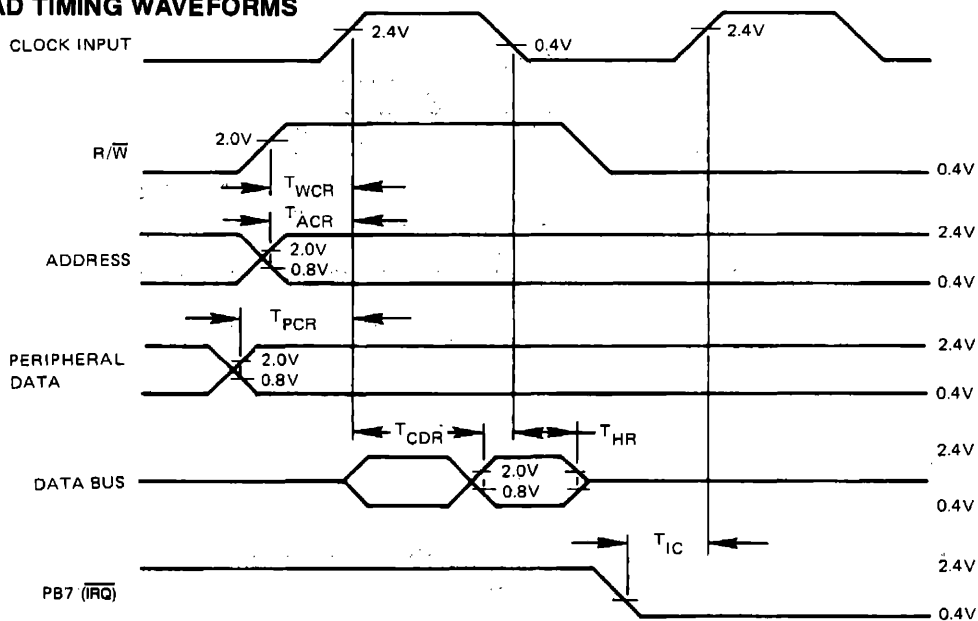
Characteristic	Symbol	Min	Max	Unit
R/W valid before positive transition of clock	T_{WCR}	180	—	ns
Address valid before positive transition of clock	T_{ACR}	180	—	ns
Peripheral data valid before positive transition of clock	T_{PCR}	300	—	ns
Data Bus valid after positive transition of clock	T_{CDR}	—	395	ns
Data Bus Hold Time	T_{HR}	10	—	ns
IRQ (Interval Timer Interrupt) valid before positive transition of clock	T_{IC}	200	—	ns
Note: Loading = 30 pF + 1 TTL load for PA0–PA7, PB0–PB7 = 130 pF + 1 TTL load for D0–D7				

2

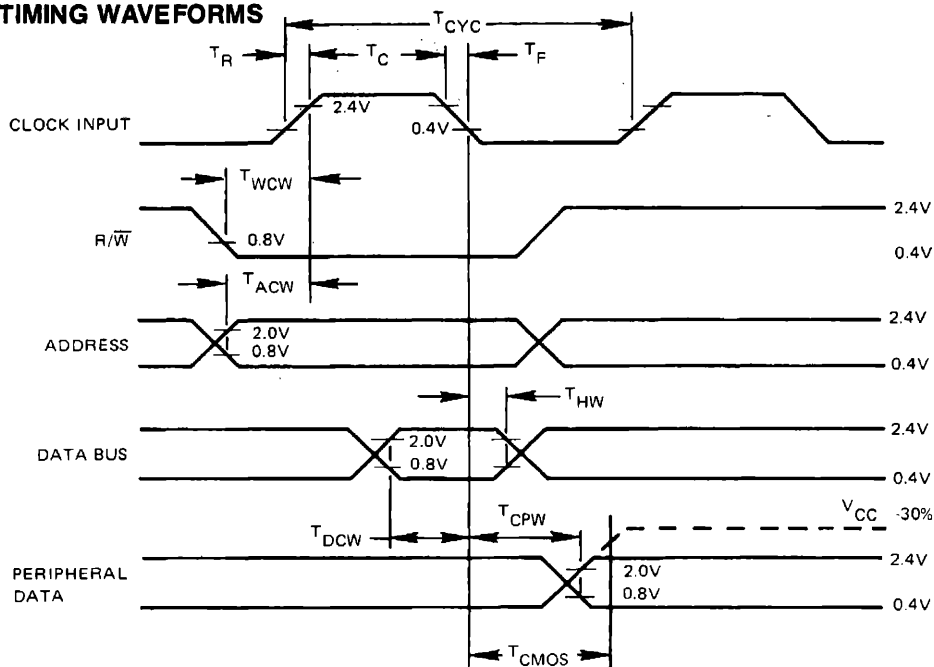
Write Timing

Characteristic	Symbol	Min	Max	Unit
Clock Period	T_{CYC}	1	10	μ S
Rise & Fall Times	T_R, T_F	—	25	ns
Clock Pulse Width	T_C	470	—	ns
R/W valid before positive transition of clock	T_{WCW}	180	—	ns
Address valid before positive transition of clock	T_{ACW}	180	—	ns
Data Bus valid before negative transition of clock	T_{DCW}	300	—	ns
Data Bus Hold Time	T_{HW}	10	—	ns
Peripheral data valid after negative transition of clock	T_{CPW}	—	1	μ S
Peripheral data valid after negative transition of clock driving CMOS (Level = VCC – 30%)	T_{CMOS}	—	2	μ S

READ TIMING WAVEFORMS



WRITE TIMING WAVEFORMS



MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input/Output Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*Note: All inputs contain protection circuitry to prevent damage due to high static charges. Care should be taken to prevent unnecessary application of voltage outside the specification range.

2

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $0^\circ C$ to $70^\circ C$, unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	+2.4		V_{CC}	V	
Input Low Voltage	V_{IL}	-0.3		+0.4	V	
Input Leakage Current A0-A9, RS0, R/W, RES, 02, PB6 ⁽³⁾ , PB5 ⁽³⁾	I_{IN}		1.0	2.5	μA	$V_{IN} = 0$ to +5.0V $V_{CC} = 0$
Input Leakage Current for Three State Off D0-D7	I_{TSI}		± 1.0	± 10	μA	$V_{IN} = 0.4V$ to 2.4V $V_{CC} = 5.25V$
Input High Current PA0-PA7, PB0-PB7	I_{IH}	-100	-300		μA	$V_{IN} = 2.4V$
Input Low Current; PA0-PA7, PB0-PB7	I_{IL}		-1.0	-1.6	mA	$V_{IN} = 0.4V$
Output High Voltage PA0-PA7, PB0-PB7 (TTL drive), D0-D7 PB0-PB7, (other drive, e.g., Darlington)	V_{OH}	+2.4 +1.5			V	$V_{CC} = 4.25V$ $I_{LOAD} = -100 \mu A$ $I_{LOAD} = 3.0 mA$
Output Low Voltage	V_{OL}			+0.4	V	$V_{CC} = 4.25V$ $I_{LOAD} = 1.6 mA$
Output High Current (Sourcing) PA0-PA7, PB0-PB7 (TTL drive), D0-D7 PB0-PB7 (other drive)	I_{OH}	-100 -3.0	-1000 -5.0		μA mA	$V_{OH} = 2.4V$ $V_{OH} = 1.5V$
Output Low Current (Sinking) PA0-PA7, PB0-PB7	I_{OL}	1.6			mA	$V_{OL} = 0.4V$
Power Dissipation	P_D		500	1000	mW	
Input Capacitance #2 Logic	C_{CLK} C_{IN}			30 10	pF pF	$V_{IN} = 0$, $f = 1 MHz$ $T_A = 25^\circ C$
Output Capacitance	C_{OUT}					

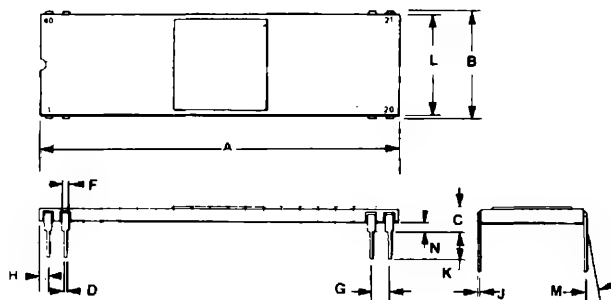
Note: 1. All units are direct current (DC).

2. Negative sign indicates outward current flow, positive indicates inward flow.

3. When programmed as address pins.

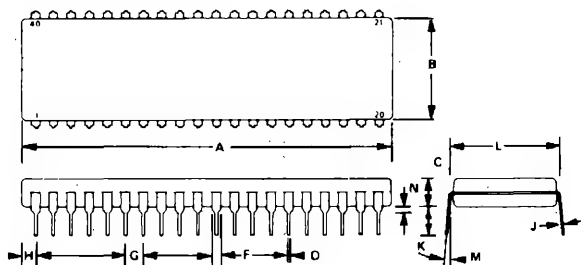
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040



R6531 ROM-RAM-I/O COUNTER (RRIOC)

2

DESCRIPTION

The R6531 ROM-RAM-I/O-Counter (RRIOC) integrates read-only memory, random access memory, various I/O data port configurations and timer functions into a single peripheral device which operates in conjunction with any CPU in the R6500 microprocessor family. The R6531 provides innovative system designers with a two-chip solution to a wide range of applications. It can also be combined in a variety of multi-chip system configurations with other R6531's, ROMs, RAMs and other I/O devices.

There are two R6531 versions: a 40-pin dual-in-line package; another with expanded I/O in a compact 52-pin quad-in-line package. Both versions contain a 2048 \times 8 mask-programmable ROM, a 128 \times 8 static RAM, a software programmable multi-mode counter, an 8-bit serial data channel, and 15 bidirectional data lines (two ports) with a handshake control mode and four interrupt inputs. The 52-pin version has an 8-bit output port and a 4-bit input port for a total of 27 I/O lines. Several mask options are available to provide a RAM standby power pin and chip selects for multi-chip systems.

Prototyping circuits are available in both the 40- and 52-pin packages, and in 1- and 2-MHz versions. They are offered as part numbers R6531-098 and R6531-098A for the 40-pin part, and as part numbers R6531-099 and R6531-099A for the 52-pin part.

ORDERING INFORMATION

Part Number:
R6531

Temperature Range: (T_L - T_H)
Blank = 0° to +70°C
E = -40°C to +85°C

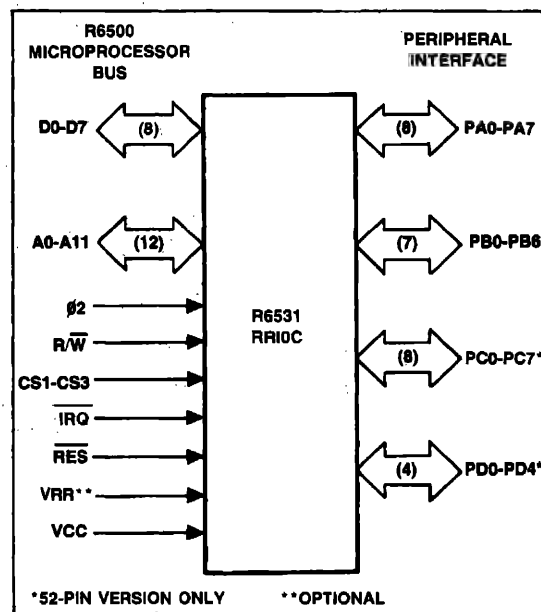
Package:
C = 40-Pin DIP, Ceramic
P = 40-Pin DIP, Plastic
Q = 52-Pin QUIP, Plastic

Frequency Range:
No letters = 1 MHz
A = 2 MHz

NOTE: Contact your local Rockwell representative for availability.

FEATURES

- 2048 \times 8 mask programmable ROM
- 128 \times 8 static RAM
- 16-bit multi-mode counter/latch
 - internal timer (one shot or free-running)
 - pulse generator (one-shot or free-running)
 - event counter
 - external trigger
- 8-bit serial channel
- TTL compatible I/O, drive one TTL load
- 15 bidirectional I/O lines (2 ports — 40-pin package)
- Expansion 8-bit output port and 4-bit input port (52-pin package)
- I/O handshake control
- Four edge sensitive interrupt inputs
- 1 MHz or 2 MHz operation
- ROM-less versions available for prototyping
- Single +5V power supply



Interface Signals

INTERFACE SIGNALS

RESET ($\overline{\text{RES}}$)

This active low signal initializes the R6531. It clears all internal registers (except the counter and serial registers) to logic zero. This action places all bidirectional I/O lines in the input state and the Port C outputs in the high state. The timer, shift register, and interrupts are disabled. The $\overline{\text{RES}}$ signal must be low for at least four clock periods when reset is required.

ADDRESS BUS (A0–A11) AND CHIP SELECTS (CS1–CS3)

Memory and register selection is accomplished using the 12 address lines and, in multiple device systems, also using one or more of the three Chip Select mask options. When PB4, PB5, or PD2 are chosen as chip selects, they cannot be used as peripheral I/O pins.

DATA BUS (D0–D7)

The R6531 has eight data bus lines, which allow data to be transferred to or from the microprocessor. The output buffers remain in the off-state except when the R6531 is selected for a read operation.

READ/WRITE ($\text{R}/\overline{\text{W}}$)

The $\text{R}/\overline{\text{W}}$ input controls the transfer of data to and from the microprocessor and the R6531. A high on the $\text{R}/\overline{\text{W}}$ pin allows the processor to read (with proper addressing) the data supplied by the R6531. A low on the $\text{R}/\overline{\text{W}}$ pin allows a write (with proper addressing) to the R6531.

PHASE 2 CLOCK ($\phi 2$)

The Phase 2 Clock ($\phi 2$) input is the system clock that triggers all data transfers between the data bus and the R6531.

PERIPHERAL DATA PORTS (PA0–PA7, PB0–PB6, PC0–PC7, PD0–PD3)

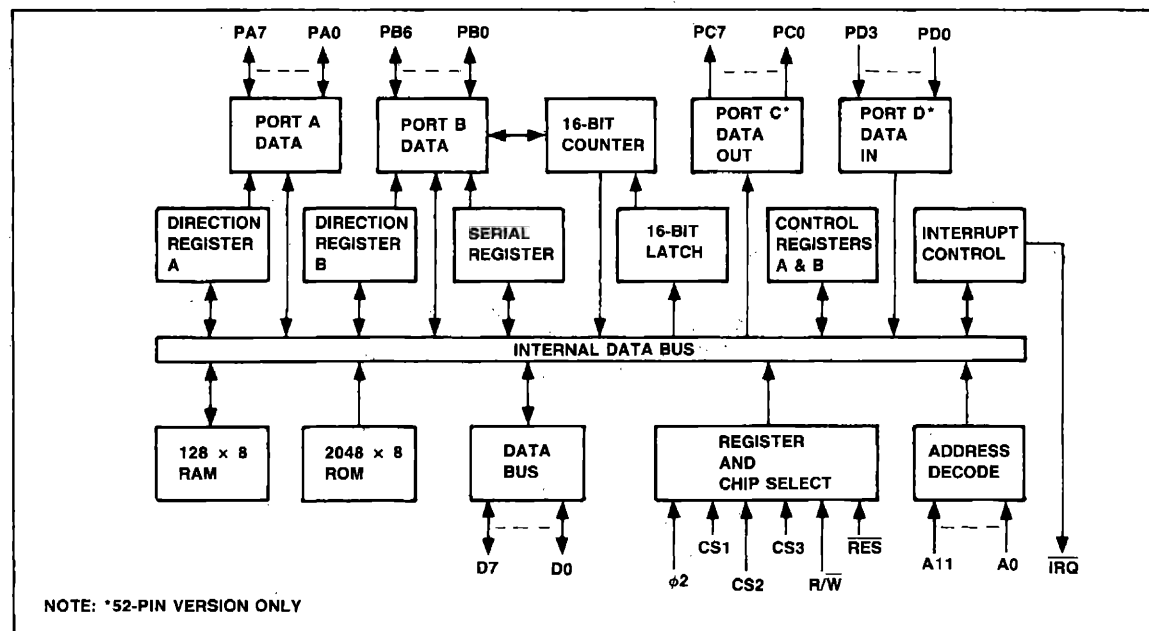
Both versions of the R6531 have 15 pins available for peripheral I/O operations. Each pin is software programmable to act as an input or an output. The pins are grouped into an 8-bit port, PA0–PA7, and a 7-bit port, PB0–PB6. The lines of the PB port may serve other functions. Ports PA and PB have associated data direction registers.

The expanded I/O of the 52-pin version provides an 8-bit output only port, PC0–PC7, and a 4-bit input only port PD0–PD3. PD2 and PD3 may be assigned other functions as described later.

The outputs are push/pull type drivers capable of driving a single TTL load. When inputs are selected the drivers float. If PB6 is programmed as the $\overline{\text{IRQ}}$ request output, the line is driven low and requires an external pull-up, thus allowing the wire OR-ing of $\overline{\text{IRQ}}$ from other devices.

RAM RETENTION VOLTAGE (VRR)

A separate pin for a power supply for the read/write memory is available as a mask option. This allows the retention of RAM data by using a battery back-up for the RAM only. Pin PB6 in the 40-pin version or PD3 in the 52-pin version is mask programmable as the VRR pin. Address line A10 must be held in the logic state which deselected RAM (user-defined) in order to protect the RAM data when VCC falls below the specified level or is turned off.



R6531 Block Diagram

VSS	1	40	PB3/SDIO
(CS2) PB4/CNT0	2	39	R/W
(CS1) PB5/CNT1	3	38	PB2/SCLK
PB6/IRQ	4	37	PB1/CA2
RES	5	36	PB0/CA1
D7	6	35	PA7
D6	7	34	PA6
D5	8	33	PA5
A8	9	32	PA4
A7	10	31	A5
$\phi 2$	11	30	A6
D4	12	29	PA3
D3	13	28	PA2
D2	14	27	PA1
D1	15	26	PA0
D0	16	25	A2
A0	17	24	A4
A11	18	23	A1
A9	19	22	A3
A10	20	21	VCC

PB6 OPTION

VSS	1	40	PB3/SDIO
(CS2) PB4/CNT0	2	39	R/W
(CS1) PB5/CNT1	3	38	PB2/SCLK
RES	4	37	PB1/CA2
D7	5	36	PB0/CA1
D6	6	35	PA7
D5	7	34	PA6
A8	8	33	PA5
A7	9	32	PA4
$\phi 2$	10	31	A5
D4	11	30	A6
D3	12	29	PA3
D2	13	28	PA2
D1	14	27	PA1
D0	15	26	PA0
A0	16	25	A2
A11	17	24	A4
A9	18	23	A1
A10	19	22	A3
VRR	20	21	VCC

VRR OPTION

R6531 40-Pin DIP Configurations

VSS	1	52	PB3/SDIO
(CS2) PB4/CNT0	2	51	R/W
(CS1) PB5/CNT1	3	50	PC6
PB6/IRQ	4	49	PB2/SCLK
PC7	5	48	PB1/CA2
RES	6	47	PB0/CA1
D7	7	46	PC5
D6	8	45	PA7
D5	9	44	PA6
PD3	10	43	PA5
(CS3) PD2	11	42	PA4
A8	12	41	PC4
A7	13	40	A5
$\phi 2$	14	39	A6
PD1	15	38	PC3
D4	16	37	PA3
D3	17	36	PA2
PD0	18	35	PA1
D2	19	34	PA0
D1	20	33	A2
D0	21	32	A4
A0	22	31	PC2
A11	23	30	PC1
PC0	24	29	A1
A9	25	28	A3
A10	26	27	VCC

PD3 OPTION

VSS	1	52	PB3/SDIO
(CS2) PB4/CNT0	2	51	R/W
(CS1) PB5/CNT1	3	50	PC6
PB6/IRQ	4	49	PB2/SCLK
PC7	5	48	PB1/CA2
RES	6	47	PB0/CA1
D7	7	46	PC5
D6	8	45	PA7
D5	9	44	PA6
(CS3) PD2	10	43	PA5
A8	11	42	PA4
A7	12	41	PC4
$\phi 2$	13	40	A5
PD1	14	39	A6
D4	15	38	PC3
D3	16	37	PA3
PD0	17	36	PA2
D2	18	35	PA1
D1	19	34	PA0
D0	20	33	A2
A0	21	32	A4
A11	22	31	PC2
PC0	23	30	PC1
A9	24	29	A1
A10	25	28	A3
VRR	26	27	VCC

VRR OPTION

R6531Q 52-Pin QUIP Configurations

INTERNAL ORGANIZATION

The R6531 is divided into three basic functions: ROM, RAM, and I/O. The selection of any one of these three is accomplished by issuing the appropriate address information on the address bus when the chip is selected.

ROM—2K BYTES (16K BITS)

The 16K ROM is a 2048×8 bit configuration. An address on lines A0-A10 uniquely selects one byte of ROM. Additionally, address line A11 and the chip selects are required to select the ROM function on a given chip. In a system with multiple R6531's, the CS1, CS2, and CS3 mask options allow up to seven devices with 14K bytes of ROM without the need for external decoding.

RAM—128 BYTES (1024 BITS)

The 128×8 static RAM of a given R6531 is addressed by lines A0-A6. Additionally, address lines A7-A11 and chip selects CS1, CS2, and CS3 provide selection of the RAM section of the device as well as the device itself when additional RAM devices or R6531's are in the system.

INPUT/OUTPUT

The input/output section is comprised of the data ports, direction registers, counter and associated latches, control registers, and interrupt registers. These I/O functions are all accessible by the R6502 CPU's instruction set using address bits A0-A3 for the specific function of the device. Address bits A4-A11 and CS1, CS2, and CS3 additionally may be decoded to select a given R6531 device in a multichip system.

Control Registers

Two control registers allow software selection of various I/O functions. The Peripheral Control Register (PCR) is primarily associated with Port B functions and the Auxiliary Control Register (ACR) is associated with the counter and serial data functions which also affect Port B.

ADDRESSING

Addressing of the R6531 offers many variations to the user for system configuration flexibility. Combination with other R6531 ROMs, RAMs or I/O devices is possible without need for external address decoding. Each of the three basic functions on the device has its own decode mask for unique selection.

The specific address ranges and chip selects are defined by the user and are dependent on the number of chips in the system. The programmed options to be fixed by masking are shown in Table 1.

Table 1. R6531 Addressing

R6531 Function	Chip Selects			Address Inputs (A0-A11)											
	CS3	CS2	CS1	11	10	9	8	7	6	5	4	3	2	1	0
ROM	X	X	X	X	2K ROM Decode										
RAM	Y	Y	Y	Y	Y	Y	Y	Y	128 RAM Decode						
I/O	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	I/O Decode			

The X, Y, and Z bits may be selected as high, low or no effect.

The chip select pins are also discrete I/O pins PB5, PB4, and PD2. The pins are independent of each other in that any one may be used as a chip select. The user specifies as mask options which pins are to be used as I/O and which as chip selects.

40-PIN PROTOTYPING CIRCUIT

Prototyping circuits R6531-098 (1 MHz) and R6531-098A (2 MHz) are packaged in a 40-pin dual in-line package that has the same pinouts as the 40-pin R6531 with PB6 option. In this prototyping circuit, the ROM is disabled and there is no VRR option. Access codes for this prototyping circuit are shown in Table 2.

Table 2. R6531-098 Addressing

R6531-098 Function	Chip Selects		Address Inputs (A0 - A11)											
	CS2	CS1	11	10	9	8	7	6	5	4	3	2	1	0
RAM	N	N	L	L	L	N	L	128 RAM Decode						
I/O	N	N	L	H	H	H	L	L	L	L	I/O Decode			

N means No Effect, H means High and L means Low.

52-PIN PROTOTYPING CIRCUIT

Prototyping circuits R6531-099 (1 MHz) and R6531-099A (2 MHz) are packaged in the 52-pin quad in-line package, with VRR option. PD2 is used as a chip select (CS3), and PB4 and PB5 are available as I/O lines. Access codes for the prototyping circuit are shown in Table 3.

Table 3. R6531-099 Addressing

R6531-099 Function	Chip Selects			Address Inputs (A0-A11)											
	CS3	CS2	CS1	11	10	9	8	7	6	5	4	3	2	1	0
ROM	H	N	N	H	2K ROM Decode										
RAM	L	N	N	L	L	L	N	L	128 RAM Decode						
I/O	L	N	N	L	H	H	H	L	L	L	L	I/O Decode			

The 128 words of RAM have been mapped into the first half of both Page 0 and Page 1, to accommodate zero page addressing and stack operations. The full I/O capabilities described for the R6531 are available in the prototyping circuit, except that I/O lines PD2 and PD3 are dedicated to the VRR and CS3 mask options.

REGISTERS

REGISTER SELECTION

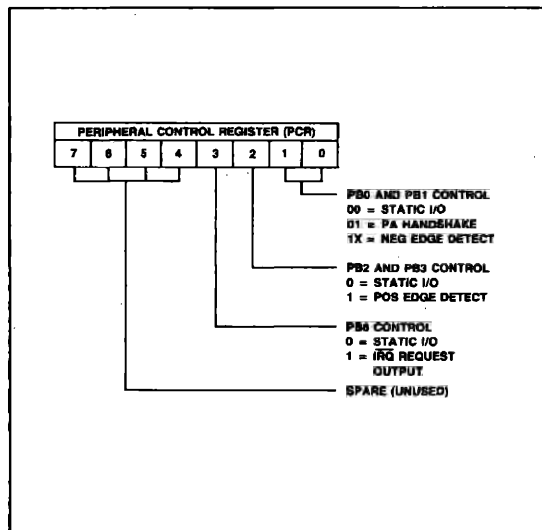
The register selection and/or general operation performed by the 15 R6531 addresses in conjunction with the R/W state is shown in Table 4.

Table 4. Register Selection

Hex Addr	Address Line				Operation	
	A3	A2	A1	A0	R/W = High	R/W = Low
0	L	L	L	L	Read Port A Data	Write Port A Data
1	L	L	L	H	Read Port B Data	Write Port B Data
2	L	L	H	L	—	Write Port C Data
3	L	L	H	H	—	Write Port D Data
4	L	H	L	L	Read Lower Counter	Write Lower Latch
5	L	H	L	H	Read Upper Counter	Write Upper Latch and Download
6	L	H	H	L	—	Write Lower Latch
7	L	H	H	H	—	Write Upper Latch
8	H	L	L	L	Read Serial Data Register	Write Serial Data Register
9	H	L	L	H	Read Interrupt Flag Register	Write Interrupt Flag Register
A	H	L	H	L	Read Interrupt Enable Register	Write Interrupt Enable Register
B	H	L	H	H	Read Auxiliary Control Register	Write Auxiliary Control Register
C	H	H	L	L	Read Peripheral Control Register	Write Peripheral Control Register
D	H	H	L	H	—	Write Port A Data Direction Register
E	H	H	H	L	—	Write Port B Data Direction Register

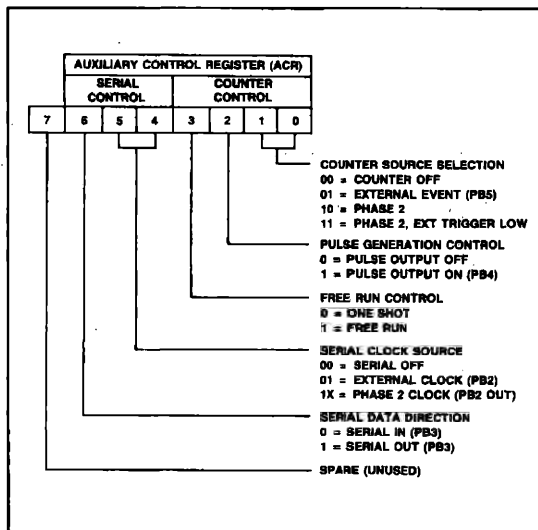
Peripheral Control Register (PCR)

Some Port B operating options are software selectable by writing control bits to the Peripheral Control Register (PCR).



Auxiliary Control Register (ACR)

Operating Modes for the Timer/Counter, PB2/PB3 Serial input/output and PB4 pulse output are selected by writing bits to the Auxiliary Control Register (ACR).



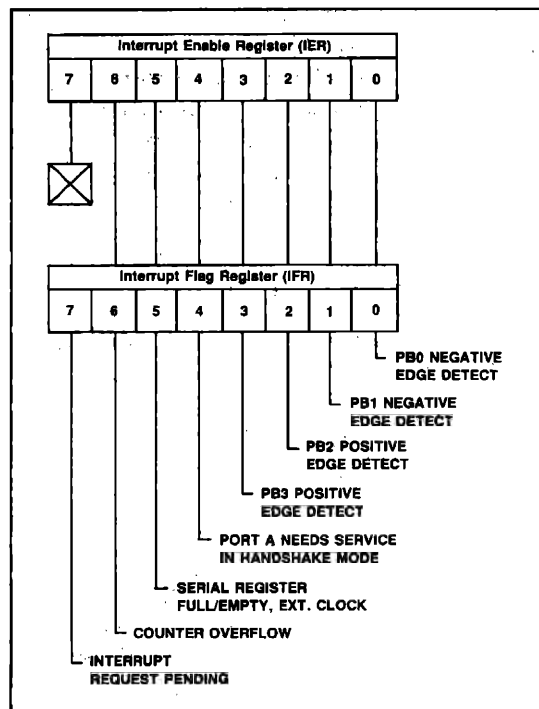
Interrupt Enable and Flag Registers

Two registers are provided for interrupt control. Corresponding bits in the enable and flag registers are logically ANDed to set the Interrupt Request Pending flag. If the pending flag is set and PB6 is selected as an IRQ Request Output, then PB6 will be set low to request the R6502 CPU to service IRQ.

The interrupt enable bits are set or reset by writing into the Interrupt Enable Register. The interrupt flag bits IFR0-IFR6 can be cleared directly by writing a byte to the flag register which has 1's in those bit positions to be cleared.

IFR4 and IFR5 may also be cleared by reading or writing the Port A or Serial Data Registers respectively. IFR6 may also be cleared by reading the lower counter with I/O address hex 4 writing the upper latch with I/O addresses hex 5 or 7.

These registers and their bit assignments are illustrated.



PERIPHERAL DATA PORTS

Each line of the 8-bit data Port A may be individually selected as an input or output. Associated with the port is Data Direction Register — Port A (DDRA). Each line of the 7-bit data Port B may be individually selected as an input or an output. This port also has a Data Direction Register (DDRB). The two data direction registers (A and B) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral pin as an output. Therefore, anything written into the data register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data from the data register. For example, a "1" loaded into DDRA, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and would be in a float state.

Note that when lines in the PB port are used alternately as control lines for other on-chip functions, Direction Register B must also be loaded to set up the proper direction — the Control Registers have no effect on data direction.

The 8-bit Port C is an output only port. The 4-bit data Port D is an input only port.

For those lines being used as outputs, the data registers are used to latch data from the Data Bus during a Write operation so the peripheral device can read the data supplied by the microprocessor.

For the lines being used as inputs, the microprocessor is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the Output data.

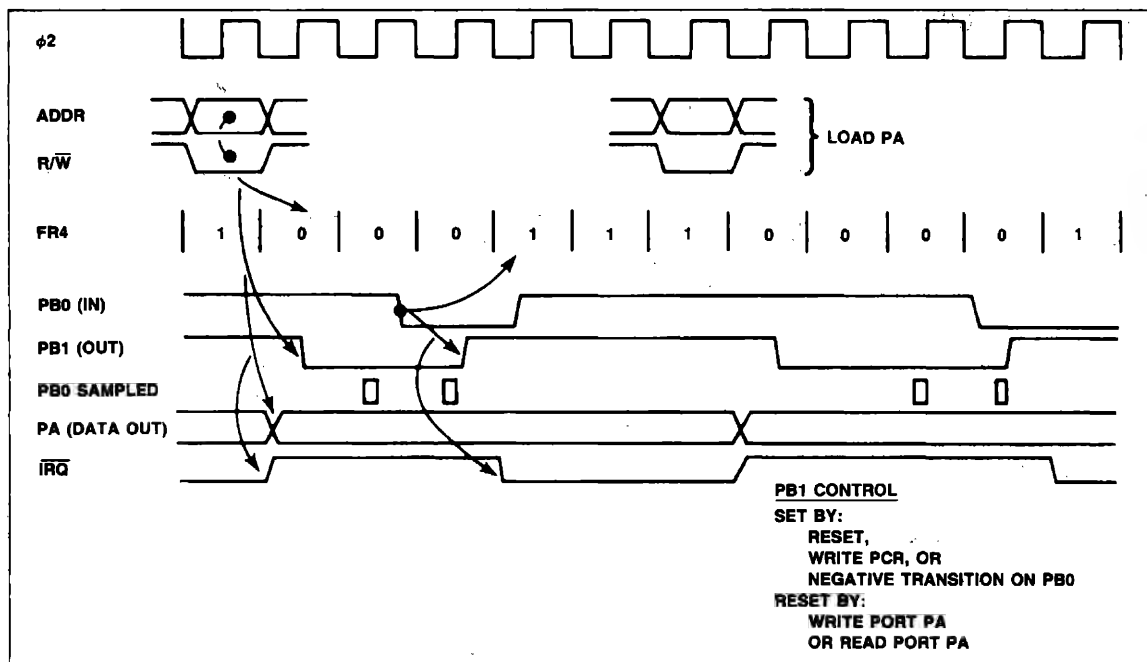
EDGE DETECT LOGIC

Operating in parallel with the I/O operation of PB0-PB3 is edge detect logic that is enabled by Peripheral Control Register bits 1 and 2. PCR1 enables logic that upon detection of a negative edge on PB0 or PB1 will set a corresponding flag in the Interrupt Flag Register. PCR2 enables logic that upon detection of a positive edge on PB2 or PB3 will set corresponding flags in the Interrupt Flag Register. If corresponding bits are set in the Interrupt Enable Register, then the Interrupt Request Pending flag will be set.

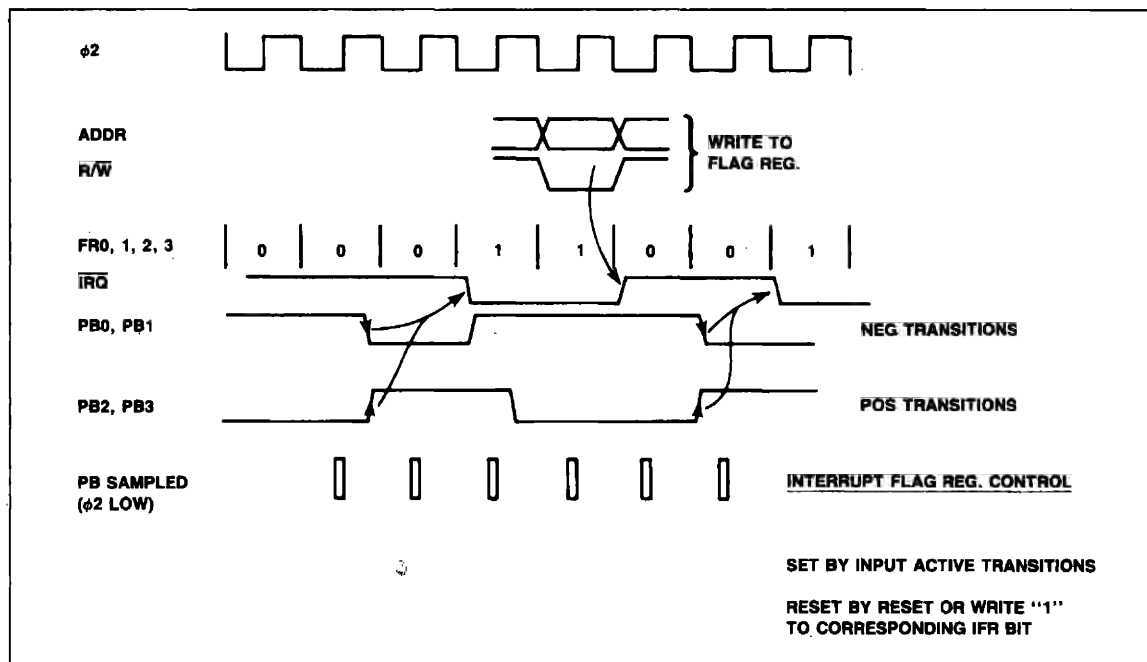
HANDSHAKE OPERATIONS

PB0 and PB1 may be used as handshake control lines for data transmissions over Port PA; see PCR definition. PB0 is a control input, PB1 is a control output. PB1 switches low on a read or write to Port PA, and switches high in response to a negative transition on PB0.

IFR4 in the Flag Register is set by a negative transition on PB0, and cleared by a Read or Write to Port PA; see Handshake Timing Diagram for timing details.



R6531 Timing for Handshake Mode



R6531 Timing for Interrupt Mode

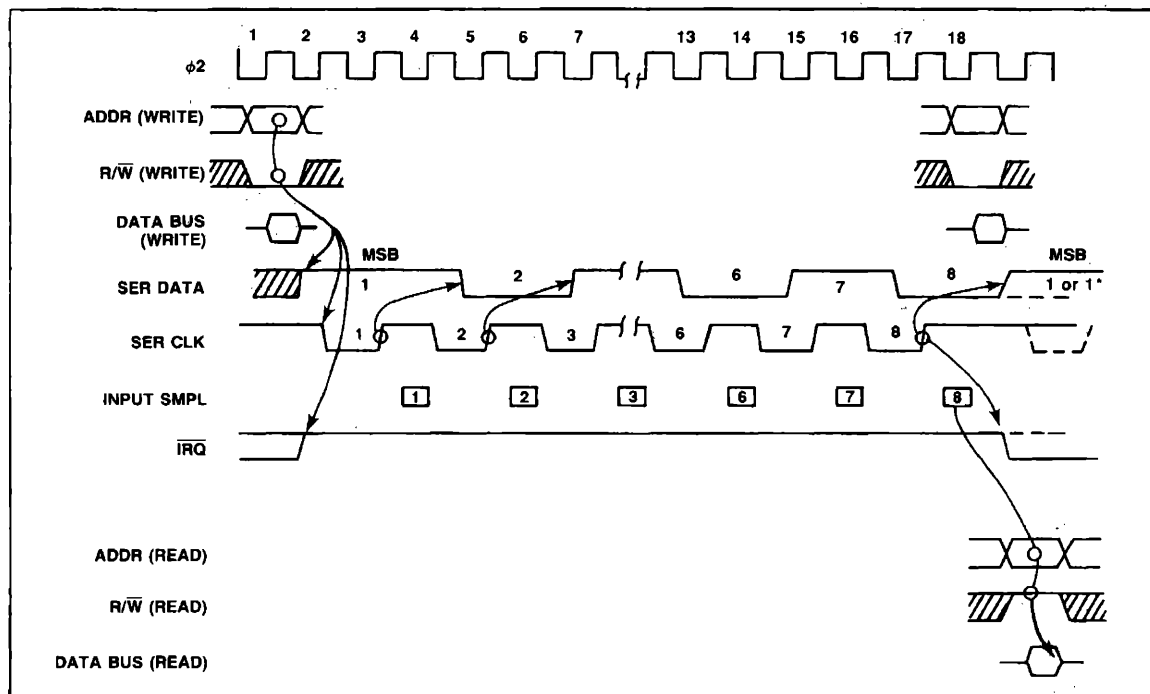
SERIAL DATA CHANNEL

The R6531 has an 8-bit serial channel. PB2 and PB3 are software selectable as the serial clock (SCLK) and serial data (SDIO) lines respectively.

The software sets Auxiliary Control Register bits 4 and 5 to enable the serial channel and to specify the source of the shift clock. Selection of the internal clock will shift data at one half the system $\phi 2$ clock rate. If the external clock is used, data may be shifted at any rate up to one half the system $\phi 2$ clock rate. In the external clock mode, the counter may be operated in the free run pulse generation mode using the CNT0 line externally connected to the SCLK line to provide the desired shift rate.

Auxiliary Control Register bit 6 sets the serial data direction. Data are shifted in or out, most significant bit first, under control of the shift clock.

In the external clock mode, the completion of eight shifts of the serial register will set bit 5 of the interrupt flag register. If the corresponding bit of the Interrupt Enable Register is also set an Interrupt Request Pending flag will be set.



R6531 Serial I/O Timing

COUNTER/TIMER

The R6531 contains a multi-mode 16-bit counter/timer with an associated 16-bit latch whose modes are software selectable by setting appropriate bits in the Auxiliary Control Register. The latch holds the counter preset value and all 16 bits download to the counter simultaneously upon command (I/O address hex 5) of the software or automatically in free run modes upon overflow of the counter. The counter is a decrementing counter and causes the setting of a flag in the Interrupt Flag Register when it overflows. This interrupt flag, bit 6, is logically ANDed with a corresponding counter overflow interrupt enabled bit to set the Interrupt Request Pending flag. The Auxiliary Control Register is used to set four basic modes which specify the source of the count information, and to select two mode modifiers that apply equally to the three active modes.

- Mode 0 — Counter Off
- Mode 1 — Event Counter — counts external event inputs (negative transitions) at PB5
- Mode 2 — Interval Timer — counts $\phi 2$ system clock pulses.

Mode 3

— External Trigger — counts $\phi 2$ system clock pulses starting with a negative transition on PB5.

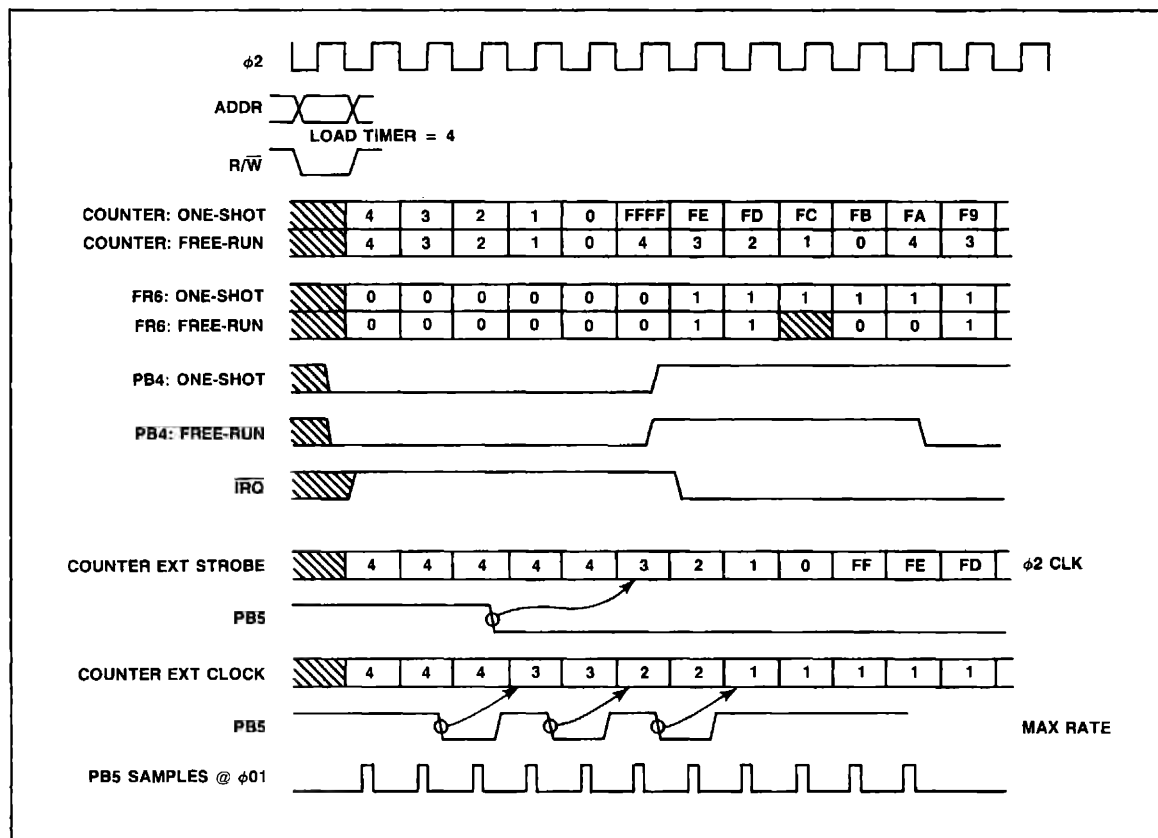
Mode Modifier A

— Pulse Generation Control — causes the output level on PB4 to switch low each time the counter is loaded using I/O address hex. 5. At counter overflow, PB4 switches high. If in the free run mode, PB4 continues to toggle at each subsequent counter overflow; otherwise there are no further transitions until the counter is reactivated by the software.

Mode Modifier B

— Free-Run Control — causes the full 16-bit latch to be downloaded to the counter, continues to count, and sets the counter overflow flag bit every time the counter overflows. Otherwise the counter is a one shot mode in which the counter overflow flag is set one time only until the counter is reactivated by the software.

2



R6531 Counter/Timer Timing

BUS TIMING CHARACTERISTICS

Characteristic	Symbol	R6531 (1 MHz)		R6531A (2 MHz)		Unit
		Min	Max	Min	Max	
Clock Period	T_{CYC}	1.0	10	0.5	10	μs
Clock Pulse Width	T_C	470	—	235	—	ns
Rise & Fall Times	T_{R1}, T_F	—	25	—	15	ns

READ TIMING

R/W valid before positive transition of clock	T_{WCR}	180	—	120	—	ns
Address valid before positive transition of clock	T_{ACR}	180	—	120	—	ns
Peripheral data valid before positive transition of clock	T_{PCR}	270	—	135	—	ns
Data Bus valid after positive transition of clock	T_{CDR}	—	350	—	180	ns
Data Bus Hold Time	T_{HR}	10	—	10	—	ns
IRQ valid after negative transition of clock	T_{IC}	—	900	—	450	ns

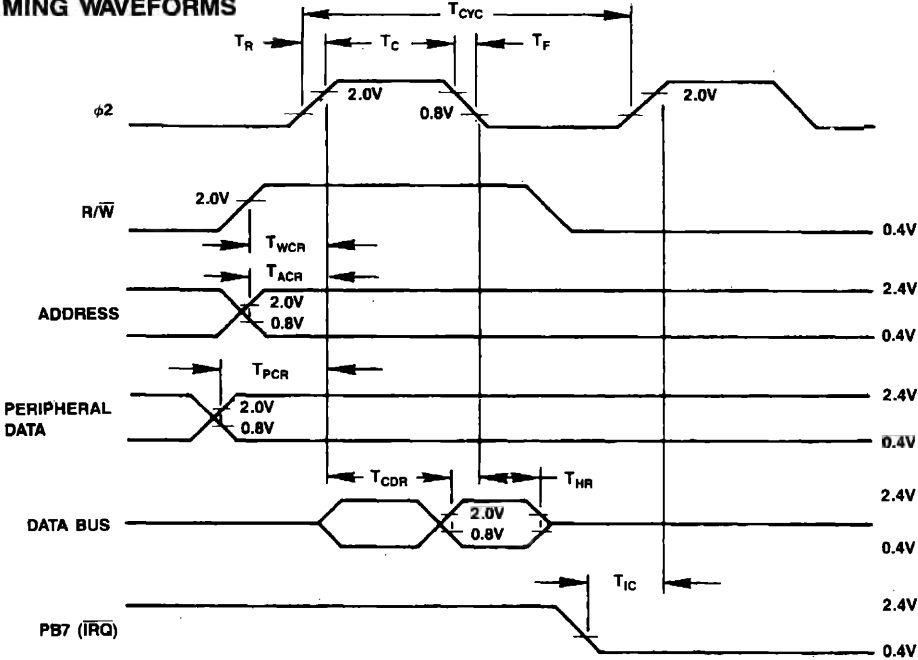
WRITE TIMING

R/W valid before positive transition of clock	T_{WCW}	180	—	120	—	ns
Address valid before positive transition of clock	T_{ACW}	180	—	120	—	ns
Data Bus valid before negative transition of clock	T_{DCW}	270	—	135	—	ns
Data Bus Hold Time	T_{HW}	10	—	10	—	ns
Peripheral data valid after negative transition of clock	T_{CPW}	—	900	—	450	ns

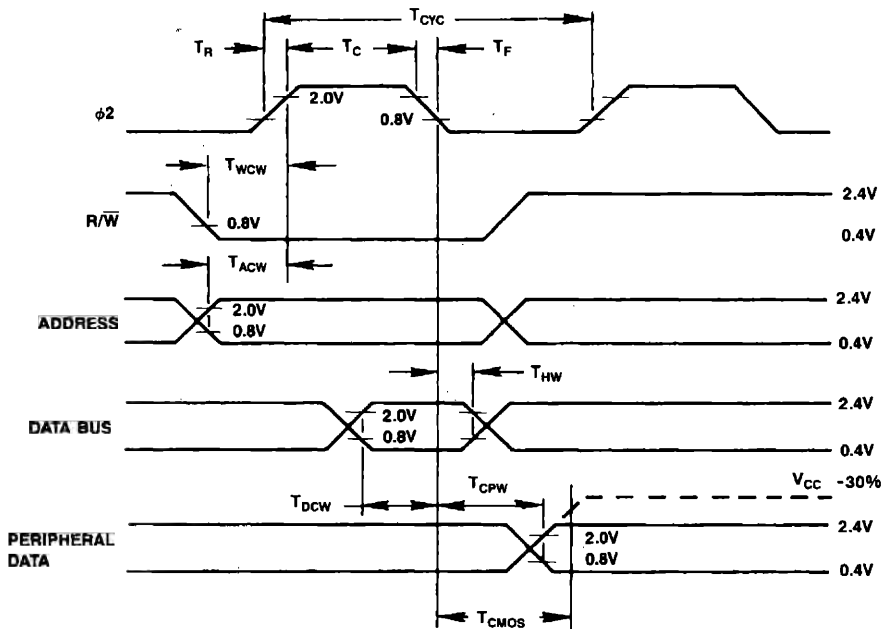
NOTES:

Load = 100 pF + 1 TTL for PA0-PA7, PB0-PB6, and PC0-PC7.
 = 100 pF + 1 TTL for D0-D7 (R6531A).
 = 130 pF + 1 TTL for D0-D7 (R6531).

READ TIMING WAVEFORMS



WRITE TIMING WAVEFORMS



MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to 7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Range Commercial Industrial	T_A	0 to +70 -40 to +85	°C °C
Storage Temperature Range	T_{stg}	-55 to +150	°C

*Note: This device contains circuitry to protect the inputs against damage due to high static voltages, however, normal precautions should be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

DC CHARACTERISTICS

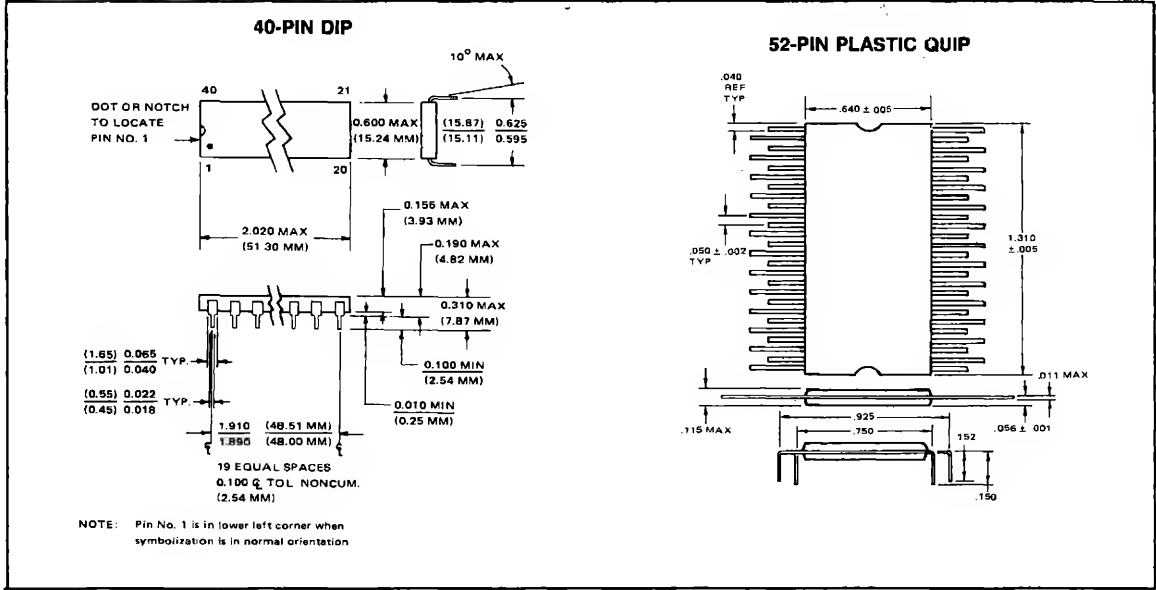
(V_{CC} 5.0V \pm 10%, V_{CC} = 5.0V \pm 5% A, V_{SS} = 0, T_A = T_L to T_H , unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit ⁽¹⁾	Test Conditions
Input High Voltage	V_{IH}	2.0	V_{CC}	V	
Input Low Voltage	V_{IL}	-0.3	+0.8	V	
Input Leakage Current A0-A11, CS1-CS3, $\overline{R}/\overline{W}$, \overline{RES} , $\phi 2$, PD0-PD3	I_{IN}	—	2.5	μ A	V_{IN} = 0V to 5.0V V_{CC} = 0V
Leakage Current for Three-State Off (Three State) D0-D7, PA0-PA7, PB0-PB6	I_{TSI}	—	± 10	μ A	V_{IN} = 0.4V to 2.4V V_{CC} = 5.0V
Input High Current PA0-PA7, PB0-PB6, PD0-PD3	I_{IH}	-100	—	μ A	V_{IN} = 2.4V
Input Low Current PA0-PA7, PB0-PB6, PD0-PD3	I_{IL}	1.6	—	mA	V_{IN} = 0.4V
Output High Voltage D0-D7, PA0-PA7, PB0-PB6, PC0-PC7	V_{OH}	+2.4	—	V	V_{CC} = 4.75V I_{LOAD} = -200 μ A
Output Low Voltage D0-D7, PA0-PA7, PB0-PB6, PC0-PC7	V_{OL}	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 2.5 mA
Output High Current (Sourcing); PA0-PA7, PB0-PB6, PC0-PC7	I_{OH}	-200	—	μ A	V_{OH} = 2.4V
Output Low Current (Sinking) PA0-PA7, PB0-PB7, PC0-PC7	I_{OL}	2.1	—	mA	V_{OL} = 0.4V
Input Capacitance $\phi 2$ Logic	C_{CLK} C_{IN}	—	20 10	pF pF	V_{CC} = 5.0V, V_{IN} = 0V, f = 1 MHz, T_A = 25°C
Output Capacitance	C_{OUT}	—	10	pF	
Power Dissipation	P_D	—	1.0	W	

NOTES:

1. All units are direct current (DC).
2. Negative sign indicates current flow, positive indicates inward flow.

PACKAGE DIMENSIONS





R6532 RAM-I/O-TIMER (RIOT)

DESCRIPTION

The R6532 RAM-I/O-Timer (RIOT) integrates random access memory (RAM), parallel I/O data ports and timer functions into a single peripheral device which operates in conjunction with any CPU in the R6500 microprocessor family. It is comprised of a 128 × 8 static RAM, two software-controlled, 8-bit bidirectional data ports allowing direct interfacing between the micro-computer and peripheral devices, a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge-detect circuit.

FEATURES

- 128 × 8 static RAM
- Two 8 bit bidirectional data ports
- Programmable interval timer with interrupt capability
- TTL & CMOS compatible peripheral lines
- One port has direct transistor drive capability
- Programmable edge-sensitive interrupt input
- 8 bit bidirectional data bus
- 6500/6800 bus compatible
- 1 MHz and 2 MHz parts available
- Single +5V power supply

ORDERING INFORMATION

Part Number: R6532

Temperature Range:
Blank = 0°C to +70°C
E = -40°C to +85°C

Package:
C = Ceramic DIP
P = Plastic DIP

Frequency:
No Letter = 1 MHz
A = 2 MHz

VSS	1	40	A6
A5	2	39	φ2
A4	3	38	CS1
A3	4	37	CS2
A2	5	36	RS
A1	6	35	R/W
A0	7	34	RES
PA0	8	33	D0
PA1	9	32	D1
PA2	10	31	D2
PA3	11	30	D3
PA4	12	29	D4
PA5	13	28	D5
PA6	14	27	D6
PA7	15	26	D7
PB7	16	25	IRQ
PB6	17	24	PB0
PB5	18	23	PB1
PB4	19	22	PB2
VCC	20	21	PB3

R6532 Pin Configuration

INTERFACE SIGNALS

RESET (\overline{RES})

During system initialization, a low \overline{RES} input causes a zeroing of all four I/O registers. This in turn causes all I/O buses to act as inputs thus protecting external components from possible damage, and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the \overline{RES} signal. The \overline{RES} signal must be held low for at least two clock periods when reset is required.

READ/WRITE (R/\overline{W})

The R/\overline{W} signal is supplied by the microprocessor and controls the transfer of data to and from the R6532. A high on the R/\overline{W} pin allows the processor to read (with proper addressing) the data supplied by the R6532. A low on the R/\overline{W} pin allows a write (with proper addressing) to the R6532.

INTERRUPT REQUEST (\overline{IRQ})

The \overline{IRQ} pin is an interrupt pin from the interrupt control logic. The pin will be normally high with a low indicating an interrupt from the R6532. An external 3K pull-up resistor is required. The \overline{IRQ} pin may be activated by a transition on PA7 or timeout of the interval timer.

DATA BUS (D0–D7)

The R6532 has eight bidirectional data pins (D0–D7). These pins connect to the system's data lines and transfer data between the R6532 and the microprocessor data bus. The output buffers remain off, or tri-stated, except when the R6532 is selected for a Read operation.

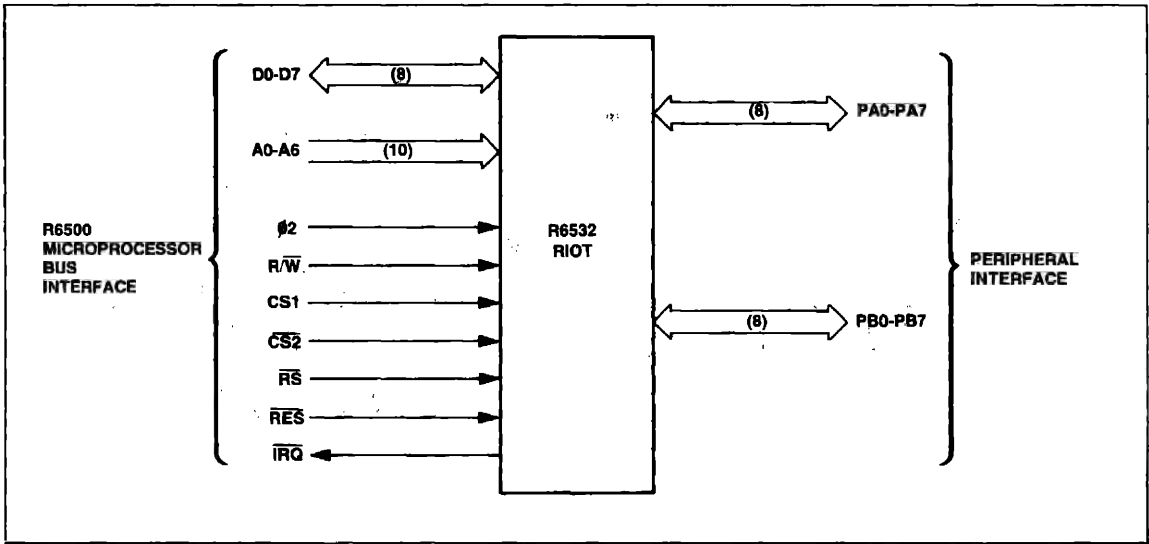
ADDRESS LINES (A0–A6)

There are seven address pins (A0–A6). In addition, there is the RAM SELECT (\overline{RS}) pin. The pins A0–A6 and \overline{RS} are always used as addressing pins. There are two additional pins which are used as CHIP SELECTS. They are pins CS1 and CS2. Tables 1 and 2 identify the functions selected and registers addressed depending upon the address line and \overline{RS} inputs in conjunction with the R/\overline{W} level.

2

I/O PORTS (PA0–PA7, PB0–PB7)

The R6532 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0–PA7 and PB0–PB7. (PA7 also has another use which is discussed later.) Each is set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" written into the data direction register causes its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state, and the internal pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor reads the peripheral pin. When the peripheral device gets information from the R6532 it receives data stored in the data register. The microprocessor reads valid pin information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volt for a "0" as the peripheral pins are all TTL compatible. Pins PB0–PB7 are also capable of sourcing 3 ma at 1.5V, thus making them capable of Darlington drive.



RIOT Interface Signals

Table 1. Address Decoding

Operation	RS	R/W	A4	A3	A2	A1	A0
Write RAM	0	0	—	—	—	—	—
Read RAM	0	1	—	—	—	—	—
Write Output Reg A	1	0	—	—	0	0	0
Read Output Reg A	1	1	—	—	0	0	0
Write DDRA	1	0	—	—	0	0	1
Read DDRA	1	1	—	—	0	0	1
Write Output Reg B	1	0	—	—	0	1	0
Read Output Reg B	1	1	—	—	0	1	0
Write DDRB	1	0	—	—	0	1	1
Read DDRB	1	1	—	—	0	1	1
Write Timer							
÷ 1T	1	0	1	(a)	1	0	0
÷ 8T	1	0	1	(a)	1	0	1
÷ 64T	1	0	1	(a)	1	1	0
÷ 1024T	1	0	1	(a)	1	1	1
Read Timer	1	1	—	(a)	1	—	0
Read Interrupt Flag	1	1	—	—	1	—	1
Write Edge Detect Control	1	0	0	—	1	(b)	(c)

Notes:

— = Don't Care, "1" = High level ($\geq 2.4V$), "0" = Low level ($\leq 0.4V$)(a) A3 = 0 to disable interrupt from timer to \overline{IRQ}
A3 = 1 to enable interrupt from timer to \overline{IRQ} (c) A0 = 0 for negative edge-detect
A0 = 1 for positive edge-detect(b) A1 = 0 to disable interrupt from PA7 to \overline{IRQ}
A1 = 1 to enable interrupt from PA7 to \overline{IRQ}

Table 2. Register Addressing

Start Address +	Register/Function	Start Address +	Register/Function
\$0	DRA ('A' side data register)	\$7	Write edge-detect control (positive edge-detect, enable interrupt)
\$1	DDRA ('A' side data direction register)		Read timer (enable interrupt)
\$2	DRB ('B' side data register)	\$C	Write timer (divide by 1, disable interrupt)
\$3	DDRB ('B' side data direction register)	\$14	Write timer (divide by 8, disable interrupt)
\$4	Read timer (disable interrupt)	\$15	Write timer (divide by 64, disable interrupt)
\$4	Write edge-detect control (negative edge-detect, disable interrupt)	\$16	Write timer (divide by 1024, disable interrupt)
\$5	Read interrupt flag register (bit 7 = timer, bit 6 = PA7 edge-detect) Clear PA7 flag	\$17	Write timer (divide by 1, enable interrupt)
\$5	Write edge-detect control (positive edge-detect, disable interrupt)	\$1D	Write timer (divide by 8, enable interrupt)
\$6	Write edge-detect control (negative edge-detect, enable interrupt)	\$1E	Write timer (divide by 64, enable interrupt)
		\$1F	Write timer (divide by 1024, enable interrupt)

INTERNAL ORGANIZATION

The R6532 is divided into four basic sections, RAM, I/O, Timer, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and a Data Register (DR).

RAM—128 BYTES (1024 BITS)

The 128 × 8 Read/Write Memory acts as a conventional static RAM and can be accessed from the microprocessor by selecting the chip (CS1 = high, CS2 = low) and by setting RS low. Address lines A0 through A6 then select the desired byte of storage.

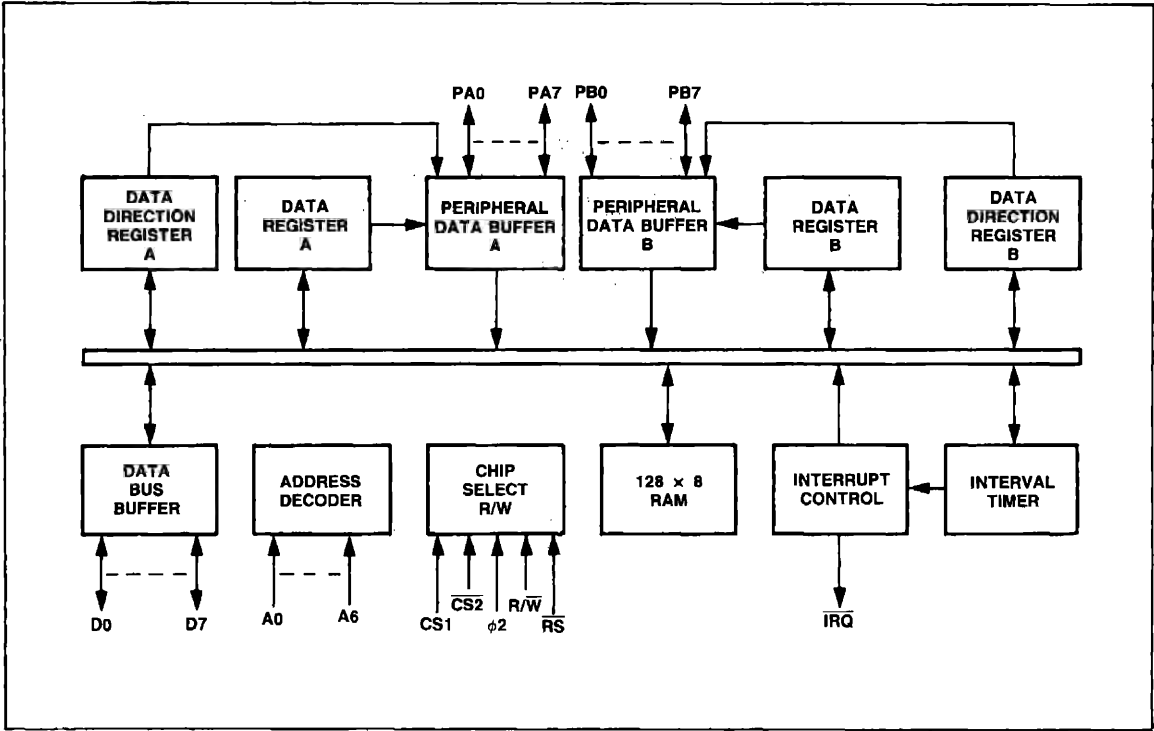
I/O PORTS AND REGISTERS

The I/O Ports consist of eight lines which can be individually programmed to act as either an input or an output. A logic zero in a bit of the Port A Data Direction Register (DDRA) causes the corresponding line of Port A to act as an input. A logic one causes the corresponding Port A line to act as an output. The voltage on any line programmed to be an output is determined by the corresponding bit in the Port A Data Register (DRA).

Data is read directly from the data pins during any read operation. For any output pin, the data transferred into the processor will be the same as that contained in the Data Register if the voltage on the pin is allowed to go to 2.4V for a logic one. Note that for input lines, the processor can write into the corresponding bit of the Data Register. This will not affect the polarity on the pin until the corresponding bit of DDRA is set to a logic one to allow the I/O line to act as an output.

The operation of the Port B is exactly the same as the normal I/O operation of the Port A. Each of the eight lines can each be programmed to act as either an input or as an output by placing a 0 or a 1 into the Port B Data Direction register (DDRB). In the output mode, the voltage on a peripheral pin is controlled by the Port B Data Register (DRB).

The primary difference between Port A and the Port B is in the operation of the output buffers which drive these pins. The Port B output buffers are push-pull devices which are capable of sourcing 3 ma at 1.5V. This allows these pins to directly drive transistor switches. To assure that the microprocessor will read proper data on a "Read Port B" operation, logic in the R6532 allows the microprocessor to read the Output Register instead of reading the peripheral pin as on Port A.



R6532 Block Diagram

EDGE DETECTING WITH PA7

In addition to acting as a peripheral I/O line, the PA7 line can be used as an edge-detecting input. In this mode, an active transition sets the internal interrupt flag (bit 6 of the Interrupt Flag register). Setting the interrupt flag causes $\overline{\text{IRQ}}$ output to go low if the PA7 interrupt has been enabled.

Control of the PA7 edge detecting mode is accomplished by writing to one of four addresses. In this operation, A0 controls the polarity of the active transition and A1 acts to enable or disable interrupting of the processor. The data which is placed on the Data Bus during this operation is discarded and has no effect on the control of PA7.

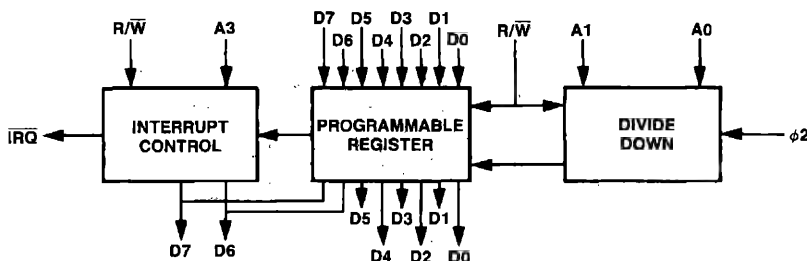
The PA7 interrupt flag is set on an active transition, even if the pin is being used as a normal input or as a peripheral control output. The flag is also set by an active transition if the PA7 interrupt is disabled. The reset signal ($\overline{\text{RES}}$) disables the PA7 interrupt and enables negative (high-to-low) edge detection on PA7. The PA7 edge detect logic can be set to detect either a positive or negative transition and to either enable or disable interrupt ($\overline{\text{IRQ}}$) generation upon detection.

During system initialization, the interrupt flag may inadvertently be set by an unexpected transition on the PA7. It is therefore recommended that the interrupt flag be cleared *before* enabling interrupting from PA7. To clear PA7 interrupt flag, simply read the interrupt Flag Register.

INTERVAL TIMER

The Timer section of the R6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic.

The Timer can be programmed to count up to 255 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to logic "1". After the interrupt flag is set the internal clock begins counting down at the system clock rate to a maximum of $-255T$. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.



Basic Elements of Interval Timer

INTERVAL TIMER EXAMPLE

The 8-bit microprocessor data bus transfers data to and from the Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the data bus and written into the divide by 1 Timer register.

At the same time that data is being written to the Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., A3 = 1 enables $\overline{\text{IRQ}}$, A3 = 0 disables $\overline{\text{IRQ}}$. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

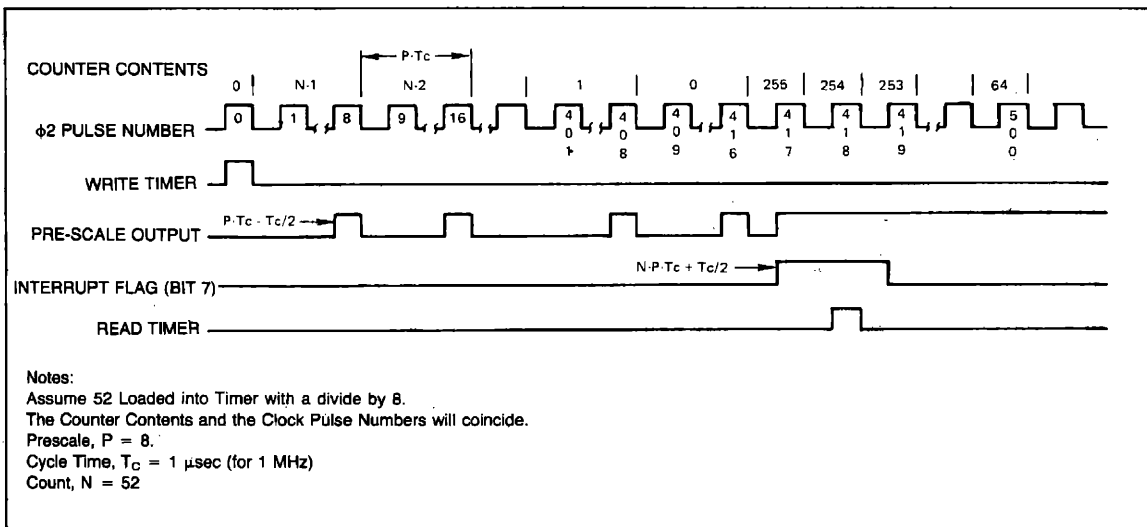
When the Timer has counted through 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After the interrupt flag is set, the timer register decrements at a divide by "1" rate of the system clock. If the timer is read after the interrupt flag is set and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is in two's complement, but remember that interrupt occurred on count number one. Therefore, we must subtract 1.

Value read = 1 1 1 0 0 1 0 0
 Complement = 0 0 0 1 1 0 1 1
 ADD 1 = 0 0 0 1 1 1 0 0 = 28 Equals two's complement of register
 SUB 1 = 0 0 0 1 1 0 1 1 = 27

Thus, to arrive at the *total* elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is $(52 \times 8) + 1 = 417T$. Total elapsed time would be $416T + 27T = 443T$, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

The interrupt flag will be reset whenever the Timer is accessed by a read or a write. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flags are read (D7 for the timer, D6 for the edge detect) data bus lines D0–D5 go to 0.

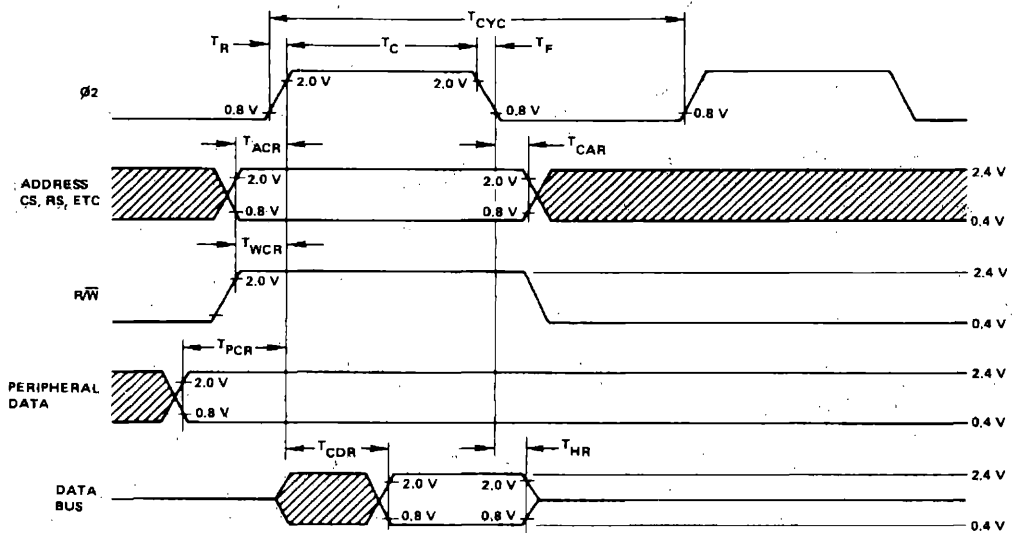
When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{\text{IRQ}}$ pin. This is done so as to avoid future interrupts until after another Write timer operation.



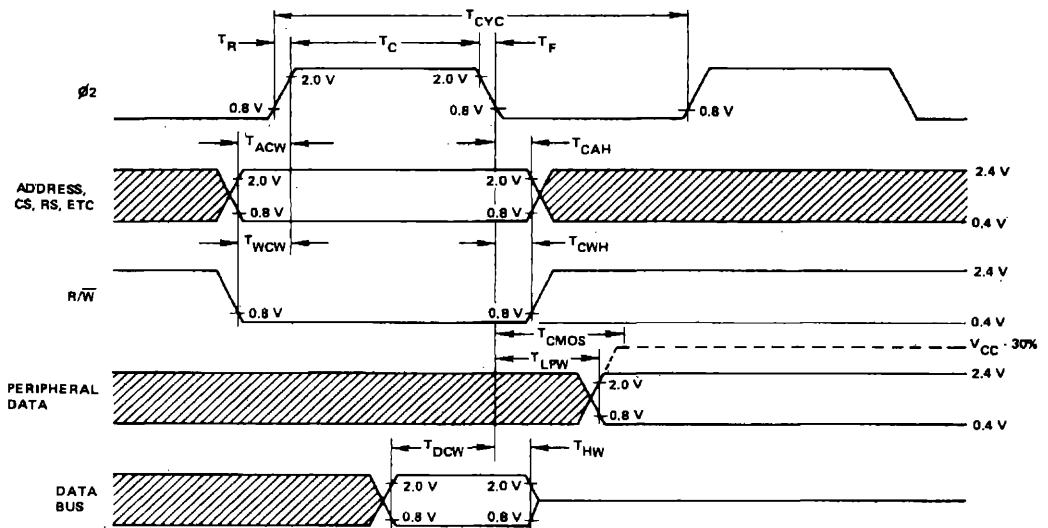
Interval Time Example Waveforms

BUS AND PERIPHERAL TIMING WAVEFORMS

READ TIMING



WRITE TIMING



AC CHARACTERISTICS

Characteristic	Symbol	R6532 (1 MHz)		R6532A (2 MHz)		Unit
		Min	Max	Min	Max	
Clock Cycle Time	T_{CYC}	1	10	0.5	10	μs
Clock Pulse Width	T_C	470	—	240	—	ns
Rise & Fall Times	T_R, T_F	—	25	—	15	ns

READ TIMING

Address Set Up Time	T_{ACR}	180	—	90	—	ns
Address Hold Time	T_{CAR}	0	—	0	—	ns
R/W Set Up Time	T_{WCR}	180	—	90	—	ns
Data Bus Delay Time	T_{CDR}	—	395	—	190	ns
Data Bus Hold Time	T_{HR}	10	—	10	—	ns
Peripheral Data Set Up Time	T_{PCR}	300	—	150	—	ns

WRITE TIMING

$\phi 2$ Cycle Time	T_{CYC}	1	10	0.5	10	μs
$\phi 2$ Pulse Width	T_C	470	—	240	—	ns
Address Set Up Time	T_{ACW}	180	—	90	—	ns
Address Hold Time	T_{CAH}	0	—	0	—	ns
R/W Set Up Time	T_{WCW}	180	—	90	—	ns
R/W Hold Time	T_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	T_{DCW}	200	—	90	—	ns
Data Bus Hold Time	T_{HW}	10	—	10	—	ns
Peripheral Data Delay Time	T_{CPW}	—	1	—	0.5	μs
Peripheral Data Delay Time CMOS	T_{CMOS}	—	2	—	1	μs

MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	0 to +70 -40 to +85	°C °C
Storage Temperature	T_{STG}	-55 to +150	°C

*Note: This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

DC CHARACTERISTICS

($V_{CC} = 5.0 \pm 5\%$, $T_A = T_L$ to T_H unless otherwise noted)

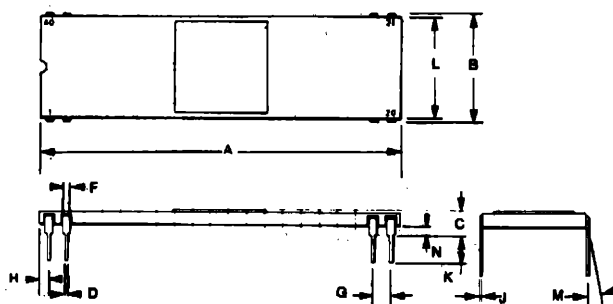
Characteristic	Symbol	Min	Max	Unit ⁽¹⁾	Test Conditions
Input High Voltage	V_{IH}	2.4	V_{CC}	V	
Input Low Voltage	V_{IL}	0	0.4	V	
Input Leakage Current: A0-A6, RS, R/W, RES, Ø2, CS1, CS2	I_{IN}	—	2.5	µA	$V_{IN} = 0V$ to 5.0V $V_{CC} = 0V$
Input Leakage Current for Three-State Off D0-D7	I_{TSI}	—	±10	µA	$V_{IN} = 0.4V$ to 2.4V
Input High Current PA0-PA7, PB0-PB7	I_{IH}	-100	—	µA	$V_{IH} = 2.4V$
Input Low Current PA0-PA7, PB0-PB7	I_{IL}	—	-1.6	mA	$V_{IN} = 0.4V$
Output High Voltage PA0-PA7, PB0-PB7 (TTL drive), D0-D7 PB0-PB7 (other than TTL drive, e.g., Darlington)	V_{OH}	2.4 1.5	— —	V	$V_{CC} = 4.75V$ $I_{LOAD} = -100 \mu A$ $I_{LOAD} = 3 mA$
Output Low Voltage D0-D7	V_{OL}	—	0.4	V	$V_{CC} = 4.75V$ $I_{LOAD} = 1.6 mA$
Output High Current (Sourcing) PA0-PA7, PB0-PB7 (TTL drive), D0-D7 PB0-PB7 (other drive, e.g., Darlington)	I_{OH}	-100 -3.0	—	µA mA	$V_{OH} = 2.4V$ $V_{OH} = 1.5V$
Output Low Current (Sinking) PA0-PA7, PB0-PB7	I_{OL}	1.6	—	mA	$V_{OL} = 0.4V$
Input Capacitance Ø2 Other	C_{CLK} C_{IN}	— —	30 10	pF pF	$V_{CC} = 5.0V$ $V_{IN} = 0V$ $f = 1 MHz$ $T_A = 25^\circ C$
Other Capacitance	C_{OUT}	—	10	pF	
Power Dissipation	P_D	—	1000	mW	$T_A = 0^\circ C$

Notes:

1. All units are direct current (DC).
2. Negative sign indicates outward current flow, positive indicates inward flow.

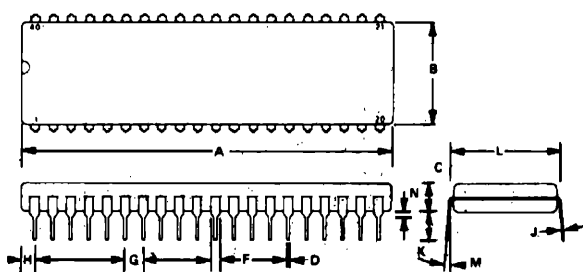
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.26	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040



R6541Q, R6500/41, R6500/42 & R6500/43 ONE-CHIP INTELLIGENT PERIPHERAL CONTROLLER

INTRODUCTION

The Rockwell R6541Q, R6500/41, R6500/42 and R6500/43 One-Chip Intelligent Peripheral Controllers (IPC) are general purpose, programmable interface I/O devices designed for use with a variety of 8-bit and 16-bit microprocessor systems.

NOTE

This document describes four Intelligent Peripheral Controller devices. In the text, the terms IPC or device will be used when describing all parts. The few differences will be described in the text using the terms R6541Q, R6500/41, R6500/42, or R6500/43.

The one-chip R6500/41 IPC has an enhanced R6502 CPU, 1.5K by 8-bit ROM, 64 by 8-bit RAM, three I/O ports with multiplexed special functions, and a multi-function timer all contained within a 40 pin package.

For systems requiring additional I/O ports, the device is also available in a 64-pin QUIP version, R6500/42, that provides three additional 8-bit ports.

Another 64 pin QUIP version, R6500/43, is functionally equivalent to the R6500/41 except 4K addresses and a data bus are provided on pins, and the ROM size is optionally 256 or 0 bytes.

The R6541Q, also a 64 pin QUIP version, is functionally identical to the R6500/43 except it has no options. The part has no ROM and no port pull-up resistors. It can be used as an IPC microprocessor or as an emulator for the family.

In all versions, special interface registers allow these IPC devices to function as peripheral controllers for the 6500, 6800, Z80, 8080, and other 8-bit or 16-bit host microcomputer systems. The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as the instruction simplicity results in system cost-effectiveness and a wide range of computational power. These features make the device a leading candidate for IPC computer applications.

FEATURES

- Directly compatible with 6500, 6800, 8080, and Z80 bus families
- Asynchronous Host interface that allows independent clock operation
- Input, Output and Status Registers for CPU/Host data transfers
- Interrupt or polled data interchange with Host
- Enhanced 6502 CPU
 - Four new bit manipulation instructions:
 - Set Memory Bit (SMB)
 - Reset Memory Bit (RMB)
 - Branch on Bit Set (BBS)
 - Branch on Bit Reset (BBR)
 - Decimal and binary arithmetic modes
 - 13 addressing modes
 - True indexing
- 1.5K, 256 or zero bytes mask-programmable ROM
- 64-byte static RAM
- 47 TTL-compatible I/O lines (R6500/42)
- 23 TTL-compatible I/O lines (all others)
- A 16-bit programmable counter/timer, with latch
 - Pulse width measurement
 - Pulse generation
 - Interval timer
 - Event counter
- Seven interrupts
 - Two edge-sensitive lines: one positive, one negative
 - Reset
 - Counter
 - Host data received
 - Output Data Register full
 - Input Data Register empty
- Multiplexed bus expandable to 4K bytes of external memory
- Unmultiplexed bus for Peripheral I/O expansion
- 68% of the instructions are executed in less than 2 μ s at 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 40-pin DIP (R6500/41)
- 64-pin QUIP (all others)

Rockwell supports development of the R6500/41, R6500/42, and R6500/43 with the System 65 Microcomputer development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This document is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Order Number 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order Number 202).

Additional information on the devices can be obtained from the R6500/41 and R6500/42 Product Description (Order Number 2135) and the R6500/43 and R6541Q Product Description (Order Number 2136).

FUNCTIONAL DESCRIPTION

The internal CPU or the device is a standard R6502 configuration with the standard R6502 instructions, plus four new bit manipulation instructions. These new bit manipulator instructions form an enhanced R6502 instruction set and improve memory utilization efficiency and performance.

Set Memory Bit (SMB #,ADDR.)

This instruction sets to "1" one bit of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and which one of the eight bits to set. The second byte of the instruction designates the address (0-255) of the byte or the I/O port to be operated on.

Reset Memory Bit (RMB #,ADDR.)

This instruction has the same operation and format as the SMB instruction except that a reset to "0" results.

Branch on Bit Set Relative (BBS #,ADDR.,DEST)

This instruction tests one of the eight bits designated by a 3-bit immediate field within the first byte of the instruction. The second byte designates the location of the byte or I/O port to be tested within the zero page address range. The third byte of the instruction specifies the 8-bit relative address that the instruction will branch to if the tested bit is a "1". If the bit tested is not set, the next sequential instruction is executed.

Branch on Bit Reset Relative (BBR #,ADDR.,DEST)

This instruction has the same operation and format as the BBS instruction except that a branch occurs if the bit tested is a "0".

Read Only Memory (ROM)

The ROM consists of 1536 bytes of mask programmable memory with an address space from FA00 to FFFF for the

MASK OPTIONS

The R6500/41 provides for internal pull-up resistors on PA and PC ports as a mask option. This option is available for port groups only, not for individual port lines.

The R6500/42 has provision for pull-up resistors on PA, PC, PF, and PG ports as a mask option. This option is available for port groups only, not for individual port lines.

The R6500/43 allows for 256 Bytes of ROM or no ROM, the Reset vector at FFFC or 0FFC, and pull-up resistors on PA and PC ports as independent mask options. The port resistor options are available for port groups only, not for individual port lines.

The R6541Q has no options. It is configured with no ROM, Reset vector at FFFC, and no pull-up resistors.

R6500/41 and R6500/42. The R6500/43 has an optional 256 bytes of ROM at address space 0F00 to 0FFF. The R6541Q has no ROM.

Random Access Memory (RAM)

The RAM consists of 64 bytes of read/write memory with an assigned page zero address of 0040 through 007F.

System Clock

The device functions with an external clock. It is fully asynchronous in reference to the Host computer timing. The device clock frequency equals the external clock frequency. It is also made available for any external device synchronization at pin $\phi 2$.

Parallel Input/Output Ports

All of the devices except the R6500/42 have 23 I/O lines grouped into three ports (PA, PB, PC). Ports A and C may be used either for input or output individually or in groups of any combination. Port B may be used as all inputs or all outputs.

Port A (PA)

Port A can be programmed as a standard parallel 8-bit I/O port or, under software control, as a counter I/O line or positive and negative edge detects.

Port B (PB)

Port B can be programmed as an I/O port.

Port C (PC)

Port C has seven pins and can be programmed as an I/O port.

Ports E, F, and G (PE, PF, & PG) R6500/42 only

The R6500/42 has all of the above ports A, B, and C, plus three extra ports (PE, PF, PG). Port E is outputs only. Ports F and G are bidirectional in any combination.

Host Computer Interface

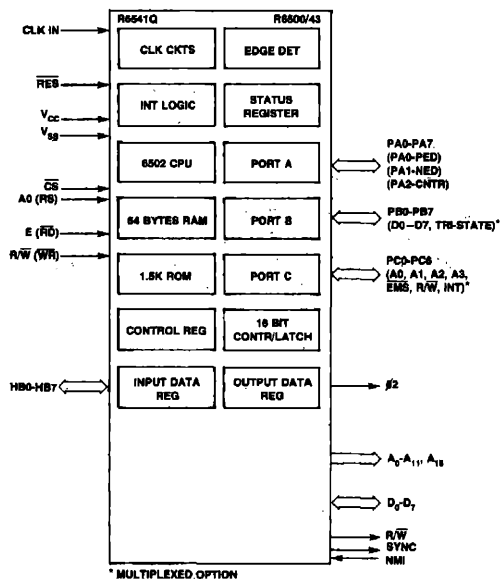
The device will work with a variety of Host Computers. The HOST interface consists of a chip select, one address line, two control lines, and an 8-bit 3-state data bus. Internal logic (controlled by MCR4) configures the address and two control lines to either a 6500 or 8080 operational methodology. The interface is completely asynchronous and will work with a Host Computer up to a 5 MHz bus transfer rate. The device clock input frequency need not be the same as the Host's. A mode control register is set to match the interface to that of the Host device as follows:

The device has an 8-bit Input Data Register (IDR) and an 8-bit Output Data Register (ODR). The IDR serves as a temporary storage for commands and data from the Host to the device.

The ODR serves as a temporary storage for data from the device to the Host.

A Host Status Flag Register facilitates a software protocol that permits independent and uninterrupted flow of data asynchronously between the Host Computer and the device.

The Host Status Flag Register contains eight flag bits that can be read at any time by either the Host or the device.



Counter/Latch Logic

The device contains a 16-bit counter and a 16-bit latch associated with it. The counter can be independently programmed to operate in one of four modes:

Counter

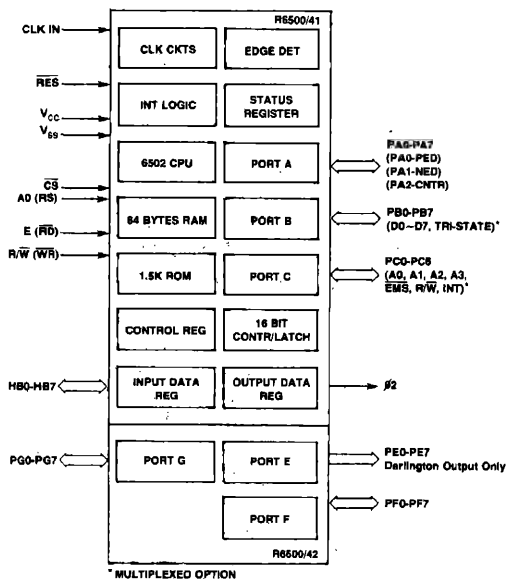
- Pulse width measurement
- Pulse Generation
- Interval Timer
- Event Counter

Mode Control Register (MCR)

The Mode Control Register contains control bits for the multi-function I/O ports, mode select bits for the Counter, and a selection bit for the type of Host interface.

Interrupt Flag Register (IFR) and Interrupt Enable Register (IER)

The device includes an Interrupt Flag Register and an Interrupt Enable Register which flags and controls I/O and counter status.



MEMORY MAP

R6500/41 AND R6500/42

NORMAL BUS MODE

FFFF	IRQ VECTOR
FFFC	RES VECTOR
FFFA	ROM (1.5K)
FA00	RESERVED
00FF	INTERNAL RAM (64)
0040	RESERVED
001F	I/O & REGISTERS
0000	

ABBREVIATED BUS MODE

FFFF	IRQ VECTOR
FFFC	RES VECTOR
FFFA	ROM (1.5K)
FA00	RESERVED
00FF	PERIPHERAL ADDRESSES (16)
0040	INTERNAL RAM (64)
001F	RESERVED
0000	I/O & REGISTERS

MULTIPLEXED BUS MODE

FFFF	IRQ VECTOR
FFFC	RES VECTOR
FFFA	ROM (1.5K)
FA00	RESERVED
00FF	EXTERNAL MEMORY 4096-128
0040	INTERNAL RAM (64)
001F	RESERVED
0000	I/O & REGISTERS

R6500/43

(W/BOOT STRAP ROM)

FFFF	IRQ VECTOR
FFFC	(OP RESET VECTOR)
FFFA	NMI VECTOR
FA00	4K USER PROGRAM
1000	RESET VECTOR
0FFC	BOOT STRAP ROM (256)
0F00	NOT AVAILABLE
0100	INTERNAL RAM (64)
007F	RESERVED
0040	I/O & REGISTERS
001F	
0000	

R6541 & R6500/43

(W/O BOOT STRAP ROM)

FFFF	IRQ
FFFC	RES
FFFA	NMI
FA00	4K USER PROGRAM
00FF	NOT AVAILABLE
0080	EXTERNAL MEMORY 4096-128
007F	INTERNAL RAM (64)
0040	RESERVED
001F	I/O & REGISTERS
0000	

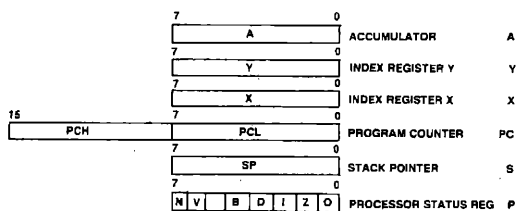
INTERNAL REGISTERS

READ	WRITE	ADDRESS
HBB Status Register	HBB Status Register	000F
Input Host Bus Buffer	Output Host Bus Buffer	001E
Lower Counter A	Lower Latch A	001D
Upper Counter A	Upper Latch A	001C
Lower Counter A	Lower Latch A	001A
Upper Counter A	Upper Latch A	0019
Mode Control Reg.	Mode Control Reg.	0018
Interrupt Enable Reg.	Interrupt Enable Reg.	0017
Interrupt Flag Reg.	Interrupt Flag Reg.	0016
Read FF	Cir Interrupt Flag Reg	0015
		0014
		0013
		0012
		0011
		0010
		000F
	NOT AVAILABLE	0007
	I/O PORTS E, F, G (R6500/42 ONLY)	0006
	NOT AVAILABLE	0004
	NOT AVAILABLE	0003
	I/O PORT C	0002
	I/O PORT B	0001
	I/O PORT A	0000

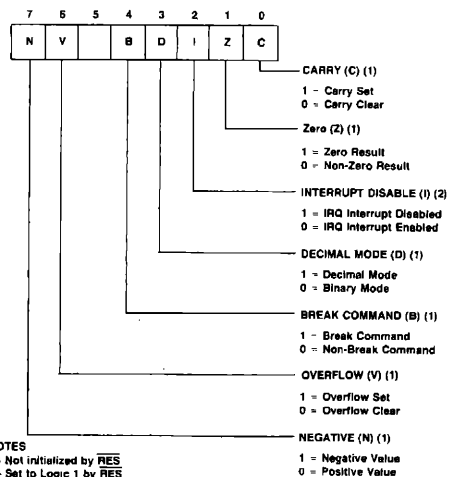
* AND START COUNTER
* CLEAR FLAG

KEY REGISTER SUMMARY

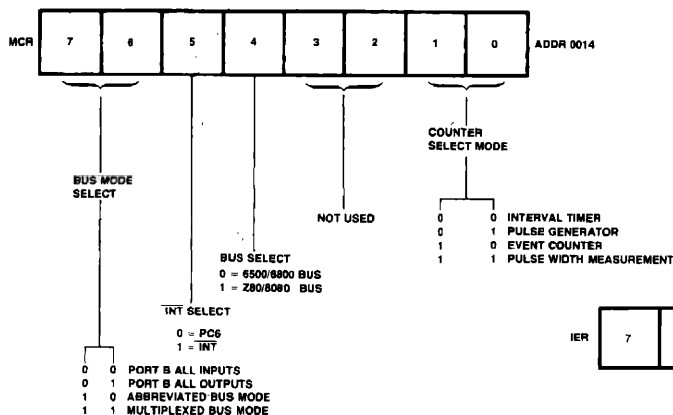
CPU Registers



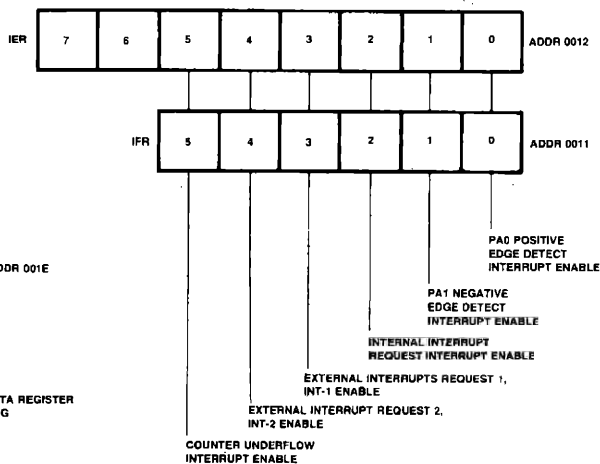
Processor Status Register



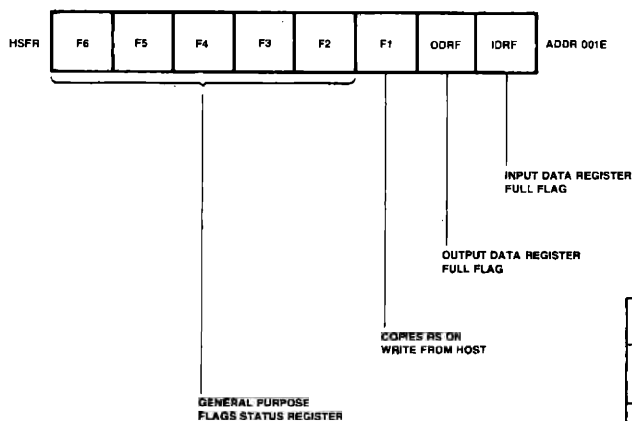
Mode Control Register



Interrupt Enable and Flag Registers



Host Status Flag Register



Host Addressing Matrix

RS (A ₀)	READ	WRITE
1	HOST STATUS FLAG	COMMAND INPUT
0	DATA REG INPUT	DATA REG OUTPUT

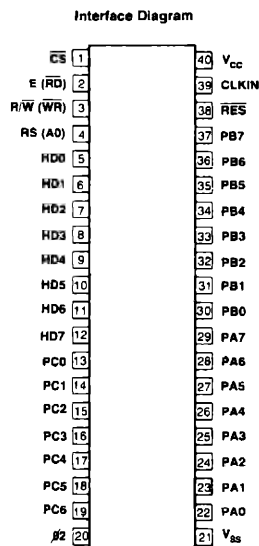


FIGURE 2-2. R6500/41 Pin Out Designation (40 PIN DIP)

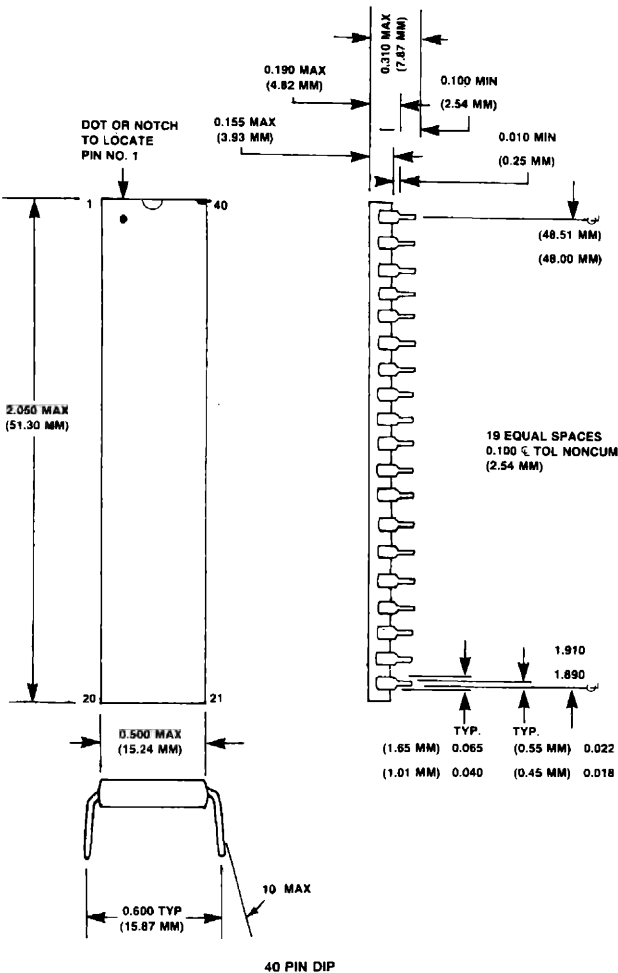


FIGURE 2-3. R6500/41 Dimensional Outline

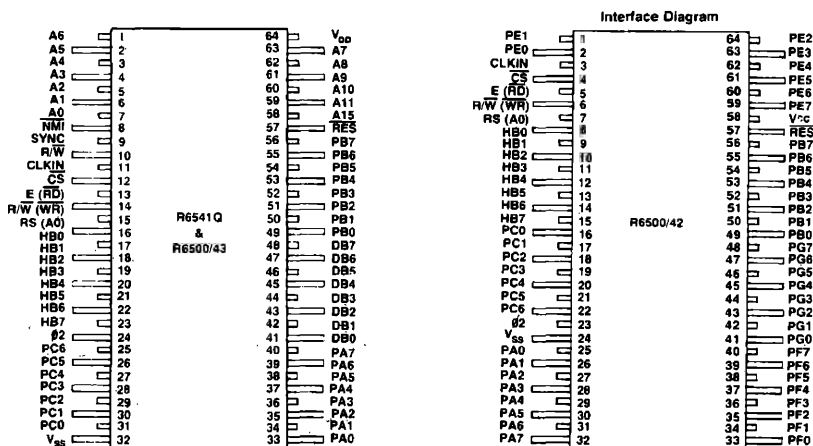


FIGURE 2-4. R6541Q, R6500/42 & R6500/43 Pin Out Designations (64 PIN QUIP)

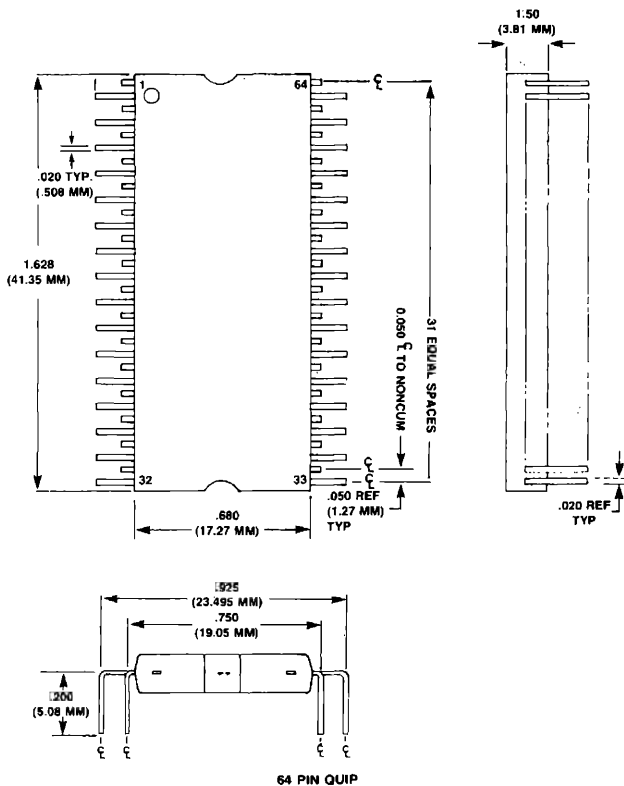


FIGURE 2-5. 64 PIN QUIP Dimensional Outline

ELECTRICAL SPECIFICATIONS

Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range, Commercial	T	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. Characteristics ($V_{CC} = 5V \pm 5\%$; $V_{SS} = 0$)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS
Power Dissipation (Outputs High) Commercial 0°C to +70°C	P_D	—	500	—	mW
Input High Voltage (Normal Operating Levels)	V_{IH}	-2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	—	-0.8	Vdc
Input Leakage Current $V_{in} = 0$ to 5.25 Vdc	I_{IN}	-10.0	—	+10.0	μ Adc
Input Low Current ($V_{in} = 0.4$ Vdc)	I_{IL}	—	-1.0	-1.6	mAdc
Output High Voltage ($V_{CC} = \min$, $I_{OAH} = -100$ μ Adc)	V_{OH}	-2.4	—	V_{CC}	Vdc
Output High Voltage ($V_{CC} = \min$)	V_{Cmos}	$V_{CC} - 30\%$	—	V_{CC}	Vdc
Output Low Voltage ($V_{CC} = \min$, $I_{OL} = 1.6$ mAdc)	V_{OL}	—	—	-0.4	Vdc
Output High Current (Sourcing) ($V_{OH} = 2.4$ Vdc)	I_{OH}	-100	—	—	μ Adc
Output Low Current (Sinking) ($V_{OL} = 0.4$ Vdc)	I_{OL}	1.6	—	—	mAdc
Darlington Current Drive, PE* ($V_{OL} = 1.5$ Vdc)	I_{OL}	-1.0	—	—	mAdc
Output Low Current, PE* ($V_{OL} = 0.4$ Vdc)	I_{OL}	1.6	—	—	mAdc
Input Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz) PA, PB, PC, PF*, PG*	C_{in}	—	—	10	pF
Output Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz)	C_{out}	—	—	10	pF
I/O Port Resistance PA0-PA7, PC0-PC6 PF0-PF7, PG0-PG7	R_L	3.0	6.0	11.5	K Ω

NOTE: Negative sign indicates outward current flow, positive indicates inward flow. $V_{CC} = 5V \pm 5\%$. *R6500/42 only.



R6545-1 CRT CONTROLLER (CRTC)

DESCRIPTION

The R6545-1 CRT Controller (CRTC) interfaces an 8-bit microprocessor to CRT raster scan video displays, and adds an advanced CRT controller to the established and expanding line of R6500, R6500/* and R65C00 microprocessor, microcomputer and peripheral device products.

The R6545-1 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545-1 is that the refresh memory may be addressed in either straight binary or by row/column.

Other functions in the R6545-1 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register. The refresh address lines are configured to provide direct dynamic memory refresh.

All timing for the video refresh memory signals is derived from the character clock input. Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows noninterlaced video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545-1 operation. The RES input allows the CRTC-generated field rate to be dynamically-synchronized with line frequency jitter.

FEATURES

- Compatible with 8-bit microprocessors
- Up to 2.5 MHz character clock operation
- Refresh RAM may be configured in row/column or straight binary addressing
- Alphanumeric and limited graphics capability
- Up and down scrolling by page, line, or character
- Programmable Vertical Sync Width
- Fully programmable display (rows, columns, character matrix)
- Video Display RAM may be configured as part of microprocessor memory field or independently slaved to R6545-1 (Transparent Addressing)
- Non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 40-Pin ceramic or plastic DIP
- Pin-compatible with MC6845
- Single +5 \pm 5% Volt Power Supply

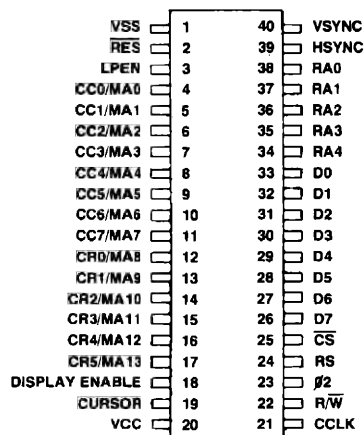
ORDERING INFORMATION

Part Number: R6545-1

— Operating Temperature (T_L to T_H)
No letter = 0°C to 70°C
E = -40°C to 85°C

— Package
P = Plastic
C = Ceramic

— Operating Frequency
No Letter = 1 MHz
A = 2 MHz



R6545-1 Pin Configuration

INTERFACE SIGNAL DESCRIPTION

Figure 1 illustrates the interface between the CPU, the R6545-1, and the video circuitry. Figure 2 shows typical timing waveforms at the video interface.

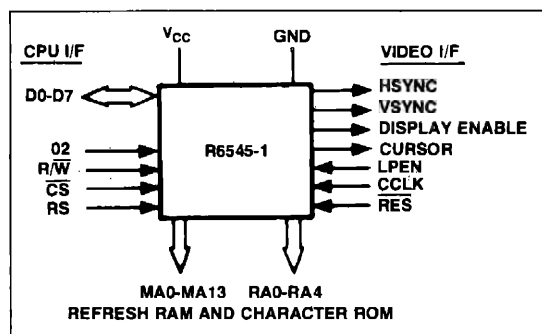


Figure 1. R6545-1 Interface Diagram

CPU INTERFACE

$\phi 2$ (Phase 2 Clock)

The Phase 2 ($\phi 2$) input clock triggers all data transfers between the system processor (CPU) and the R6545-1. Since there is no maximum limit to the allowable $\phi 2$ clock time, it is not necessary for it to be a continuous clock. This capability permits the R6545-1 to be easily interfaced to non-6500 compatible microprocessors.

R/\bar{W} (Read/Write)

The R/\bar{W} input signal generated by the processor controls the direction of data transfers. A high on the R/\bar{W} pin allows the processor to read the data supplied by the R6545-1, a low on the R/\bar{W} pin allows data on data lines D0-D7 to be written into the R6545-1.

\bar{CS} (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The R6545-1 is selected when \bar{CS} is low.

RS (Register Select)

The Register Select input accesses internal registers. A low on this pin permits writes ($R/\bar{W} = \text{low}$) into the Address Register and reads ($R/\bar{W} = \text{high}$) from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

D0-D7 (Data Bus)

The eight data lines (D0-D7) transfer data between the processor and the R6545-1. These lines are bidirectional and are normally high-impedance except during read cycles when the chip is selected ($\bar{CS} = \text{low}$).

VIDEO INTERFACE

HSYNC (Horizontal Sync)

The HSYNC active-high output signal determines the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC active-high output signal determines the vertical position of displayed text. Like HSYNC, VSYNC may drive a CRT monitor or composite video generation circuits. VSYNC time position and width are both programmable.

DISPLAY ENABLE (Display Enable)

The DISPLAY ENABLE active-high output signal indicates when the R6545-1 is generating active display information. The number of horizontal display characters per row and the number of vertical display rows are both fully programmable and together generate the DISPLAY ENABLE signal. DISPLAY ENABLE delays one character time by setting bit 4 of R8 to a 1.

CURSOR (Cursor Coincidence)

The CURSOR active-high output signal indicates when the scan coincides with the programmed cursor position. The cursor position is programmable to any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The cursor position may be delayed by one character time by setting Bit 5 of R8 to a 1.

LPEN (Light Pen Strobe)

The LPEN edge-sensitive input signal loads the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The low-to-high transition activates LPEN.

CCLK (Clock)

The CCLK character timing clock input signal is the time base for all internal count/control functions.

\bar{RES}

The \bar{RES} active-low input signal initializes all internal scan counter circuits. When \bar{RES} is low, all internal counters stop and clear all scan and video outputs go low with no affect on control registers. \bar{RES} must stay low for at least one CCLK period. All scan timing initiates when \bar{RES} goes high. In this way, \bar{RES} can synchronize display frame timing with line frequency. \bar{RES} may also synchronize multiple CRTC's in horizontal and/or vertical split screen operation.

2

REFRESH RAM AND CHARACTER ROM INTERFACE

MA0-MA13 (Refresh RAM Address Lines)

These 14 active-high output signals address the Refresh RAM for character storage and display operations. The fully programmable starting scan address and ending scan address determines the total number of characters displayed, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the straight binary mode (R8, Mode Control, bit 2 = 0), characters are stored in successive memory locations. Thus, the software design must translate row and column character coordinates into sequentially-numbered addresses. In the row/column mode (R8, Mode Control, bit 2 = 1), MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row addresses CR0-CR5. In this case, the software manipulates characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory-efficient binary address scheme.

RA0-RA4 (Raster Address Lines)

These five active-high output signals select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the R6545-1 is programmed to operate in the "Transparent Address Mode." In this case the strobe is an active-high output and is true at the time the Refresh RAM update address gates on to the address lines, MA0-MA13. In this way, updates and readouts of the Video Display RAM can be made under control of the R6545-1 with only a small amount of external circuitry.

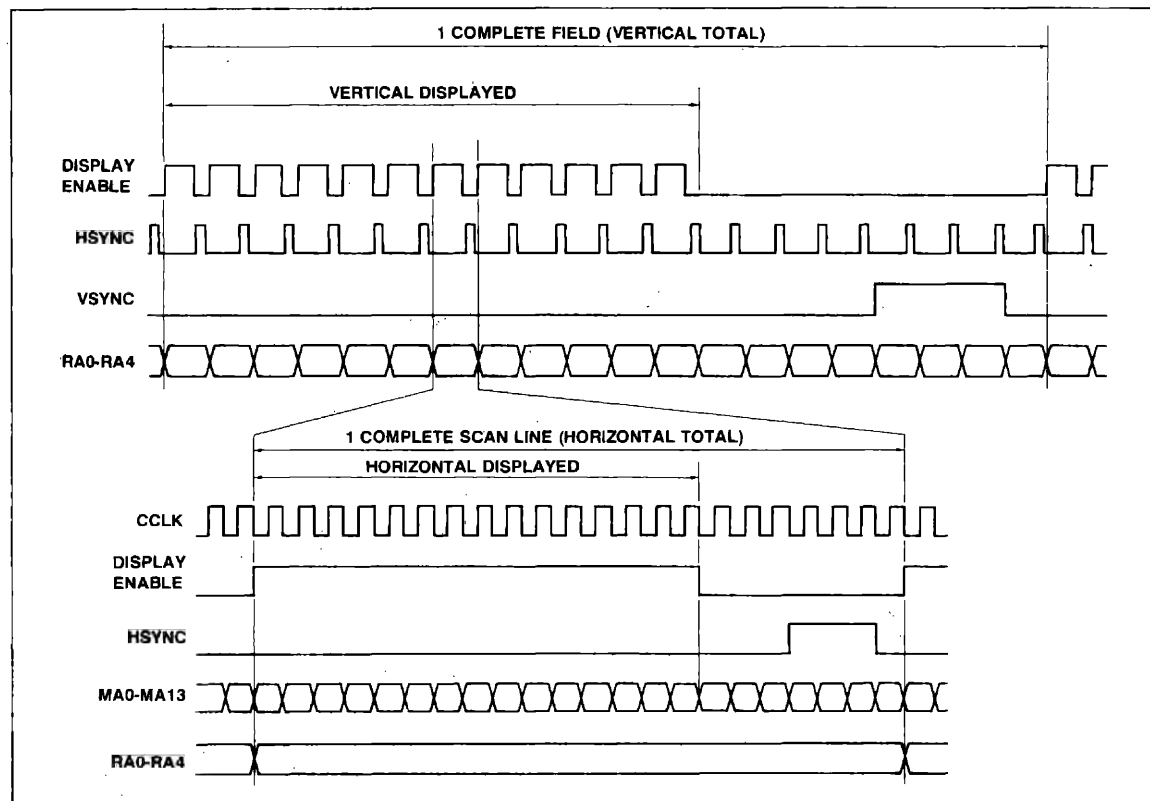


Figure 2. Vertical and Horizontal Timing

INTERNAL REGISTER DESCRIPTION

Table 1 summarizes the internal registers and indicates their address selection and read/write capabilities.

ADDRESS REGISTER

7	6	5	4	3	2	1	0
—	—	—	A ₄	A ₃	A ₂	A ₁	A ₀

This 5-bit write-only register is used as a "pointer" to direct CRTC/CPU data transfers within the CRTC. It contains the number of the desired register (0-31). With \overline{CS} and RS low, this register may be loaded; with \overline{CS} low and RS high, the selected register is the one whose identity is stored in this address register.

STATUS REGISTER (SR)

7	6	5	4	3	2	1	0
UR	LRF	VRT	—	—	—	—	—

This 8-bit register contains the status of the CRTC. Only three bits are assigned, as follows:

SR

7 UR —Update Ready

0 This bit goes to 0 when register R31 has been either read or written by the CPU.

1 This bit goes to 1 when an Update strobe occurs.

SR

6 LRF —LPEN Register Full

0 Register R16 or R17 has been read by the CPU.

1 LPEN strobe has been received.

SR

5 VRF —Vertical Re-Trace

0 Scan is not currently in the vertical re-trace time.

1 Scan currently in its vertical re-trace time. Note that this bit actually goes to a 1 when vertical re-trace starts, but goes to a 0 five character clock times before vertical re-trace ends to ensure that critical timings for refresh RAM operations are avoided.

SR

4-0 —Not used.

Table 1. Internal Register Summary

		Address Reg.					Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit								
CS	RS	4	3	2	1	0						7	6	5	4	3	2	1	0	
1	—	—	—	—	—	—	—													
0	0	—	—	—	—	—	—	Address Reg.	Reg. No.		✓				A ₄	A ₃	A ₂	A ₁	A ₀	
0	0	—	—	—	—	—	—	Status Reg.		✓		U	L	V						
0	1	0	0	0	0	0	R0	Horiz. Total -1	# Charac.		✓	•	•	•						
0	1	0	0	0	0	1	R1	Horiz. Displayed	# Charac.		✓	•	•	•						
0	1	0	0	0	1	0	R2	Horiz. Sync Position	# Charac.		✓	•	•	•						
0	1	0	0	0	1	1	R3	VSING, HSYNC Widths	# Scan Lines and # Char. Times		✓	V ₃	V ₂	V ₁	V ₀	H ₃	H ₂	H ₁	H ₀	
0	1	0	0	1	0	0	R4	Vert. Total -1	# Charac. Row		✓		•	•	•					
0	1	0	0	1	0	1	R5	Vert. Total Adjust	# Scan Lines		✓				•	•	•			
0	1	0	0	1	1	0	R6	Vert. Displayed	# Charac. Rows		✓		•	•	•	•	•	•	•	
0	1	0	0	1	1	1	R7	Vert. Sync Position	# Charac. Rows		✓		•	•	•	•	•	•	•	
0	1	0	1	0	0	0	R8	Mode Control			✓	U ₁	U ₀	C	D	T	RC		0	
0	1	0	1	0	0	1	R9	Scan Lines -1	# Scan Lines		✓				•	•	•	•	•	
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		✓			B ₁	B ₀					
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		✓									
0	1	0	1	1	0	0	R12	Display Start Addr (H)			✓			•						
0	1	0	1	1	0	1	R13	Display Start Addr (L)			✓	•	•	•						
0	1	0	1	1	1	0	R14	Cursor Position (H)			✓	✓			•					
0	1	0	1	1	1	1	R15	Cursor Position (L)			✓	✓	•	•	•	•	•	•	•	
0	1	1	0	0	0	0	R16	Light Pen Reg (H)			✓				•					
0	1	1	0	0	0	1	R17	Light Pen Reg (L)			✓				•					
0	1	1	0	0	1	0	R18	Update Address Reg (H)			✓									
0	1	1	0	0	1	1	R19	Update Address Reg (L)			✓				•	•	•	•	•	
0	1	1	1	1	1	1	R31	Dummy Location												

Notes: Designates used bit in register
 Designates unused bit in register. Reading this bit is always 0, except for R31, which does not drive the data bus at all, and for CS = 1 which operates likewise.

R0—HORIZONTAL TOTAL CHARACTERS

7	6	5	4	3	2	1	0
NUMBER OF CHARACTERS -1							

This 8-bit write-only register contains the total of displayed and non-displayed characters, minus one, per horizontal line. This register determines the frequency of HSYNC.

R1—HORIZONTAL DISPLAYED CHARACTERS

7	6	5	4	3	2	1	0
NUMBER OF CHARACTERS							

This 8-bit write-only register contains the number of displayed characters per horizontal line.

R2—HORIZONTAL SYNC POSITION

7	6	5	4	3	2	1	0
HORIZONTAL SYNC POSITION							

This 8-bit write-only register contains the position of HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left to right location of the displayed text on the video screen. In this way, the side margins are adjusted.

R3—HORIZONTAL AND VERTICAL SYNC WIDTHS

7	6	5	4	3	2	1	0
V ₃	V ₂	V ₁	V ₀	H ₃	H ₂	H ₁	H ₀

This 8-bit write-only register contains the widths of both HSYNC and VSYNC, as follows:

HVSW**7-4 VSYNC Pulse Width**

The width of the vertical sync pulse (VSYNC) in the number of scan lines. When bits 4-7 are all 0, VSYNC is 16 scan lines wide.

HVSW**3-0 HSYNC Pulse Width**

The width of the horizontal sync pulse (HSYNC) in the number of character clock times (CCLK).

Control of these parameters allows the R6545-1 to interface with a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one shot timing.

R4—VERTICAL TOTAL ROWS

7	6	5	4	3	2	1	0
NO. OF CHAR. ROWS -1							

The 7-bit Vertical Total Register contains the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close

to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then RES may provide absolute synchronism.

R5—VERTICAL TOTAL LINE ADJUST

7	6	5	4	3	2	1	0
SCAN LINES							

The 5-bit write-only Vertical Total Line Adjust Register (R5) contains the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

R6—VERTICAL DISPLAYED ROWS

7	6	5	4	3	2	1	0
DISPLAYED CHAR. ROWS							

This 7-bit write-only register contains the number of displayed character rows in each frame. This determines the vertical size of the displayed text.

R7—VERTICAL SYNC POSITION

7	6	5	4	3	2	1	0
VERTICAL POSITION							

This 7-bit write-only register selects the character row time at which the vertical SYNC pulse is desired to occur and, thus, positions the displayed text in the vertical direction.

R8—MODE CONTROL (MC)

7	6	5	4	3	2	1	0
UM(T)	US(T)	CSK	DES	RRA	RAD	—	0

This 8-bit write-only register selects the operating modes of the R6545-1, as follows:

MC

7	UM(T) — Update/Read Mode (Transparent Mode)
0	Update occurs during horizontal and vertical blanking times with update strobe.
1	Update interleaves during Ø2 portion of cycle.

MC

6	US(T) — Update Strobe (Transparent Mode)
0	Pin 34 functions as memory address.
1	Pin 34 functions as update strobe.

MC

5	CSK — Cursor Skew
0	No delay
1	Delays Cursor one character time.

MC

4	DES — Display Enable Skew
0	No delay
1	Display Enable delays one character time.

MC

3 RRA —Refresh RAM Access

- 0 Shared memory access
1 Transparent memory access

MC

2 RAD —Refresh RAM Addressing Mode

- 0 Straight binary addressing
1 Row/column addressing

MC

- 1 —Not Used—don't care

MC

- 0 —Not Used—must be a 0.

R9—ROW SCAN LINES

7	6	5	4	3	2	1	0
—	—	—	SCAN LINES -1				

This 5-bit write-only register contains the number of scan lines, minus one, per character row, including spacing.

R10—CURSOR START LINE

7	6	5	4	3	2	1	0
—	B ₁	B ₀	START SCAN LINE				

R11—CURSOR END LINE

7	6	5	4	3	2	1	0
—	—	—	END SCAN LINE				

These 5-bit write-only registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor blink mode, as follows:

B ₁	B ₀	Cursor Operating Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

A one character wide cursor can be controlled by storing values into the Cursor Start Line (R10) and Cursor End Line (R11) registers and into the Cursor Position Address High (R14) and Cursor Position Low (R15) registers.

R12—DISPLAY START ADDRESS HIGH

7	6	5	4	3	2	1	0
—	—	DISPLAY START ADDRESS HIGH					

R13—DISPLAY START ADDRESS LOW

7	6	5	4	3	2	1	0
DISPLAY START ADDRESS LOW							

These registers form a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the R6545-1 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

R14—CURSOR POSITION HIGH

7	6	5	4	3	2	1	0
—	—	CURSOR POSITION HIGH					

R15—CURSOR POSITION LOW

7	6	5	4	3	2	1	0
CURSOR POSITION LOW							

These registers form a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

A cursor of up to 32 characters in height can be displayed on and between the scan lines as loaded into the Cursor Start Line (R10) and Cursor End Line (R11) Registers.

The cursor is positioned on the screen by loading the Cursor Position Address High (R14) and Cursor Position Address Low (R15) registers with the desired refresh RAM address. The cursor can be positioned in any of the 16K character positions. Hardware paging and data scrolling is thus allowed without loss of cursor position. Figure 3 is an example of the display cursor scan line.

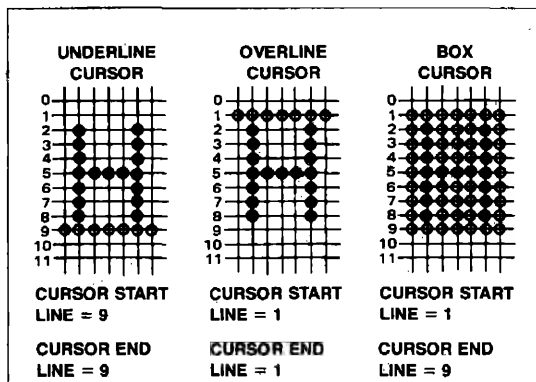


Figure 3. Cursor Display Scan Line Control Examples

R16—LIGHT PEN HIGH

7	6	5	4	3	2	1	0
—	—						

LPEN HIGH

R17—LIGHT PEN LOW

7	6	5	4	3	2	1	0

LPEN LOW

These registers form a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

R18—UPDATE ADDRESS HIGH

7	6	5	4	3	2	1	0
—	—						

UPDATE ADDRESS HIGH

R19—UPDATE ADDRESS LOW

7	6	5	4	3	2	1	0

UPDATE ADDRESS LOW

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent address mode, only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document. The section on REFRESH RAM ADDRESSING describes this more fully.

R31—DUMMY LOCATION

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

REGISTER FORMATS

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

- (1) Straight binary, if register R8, bit 2 = 0
- (2) Row/Column, if register R8, bit 2 = 1. In this case the low byte is the Character Column and the high byte is the Character Row.

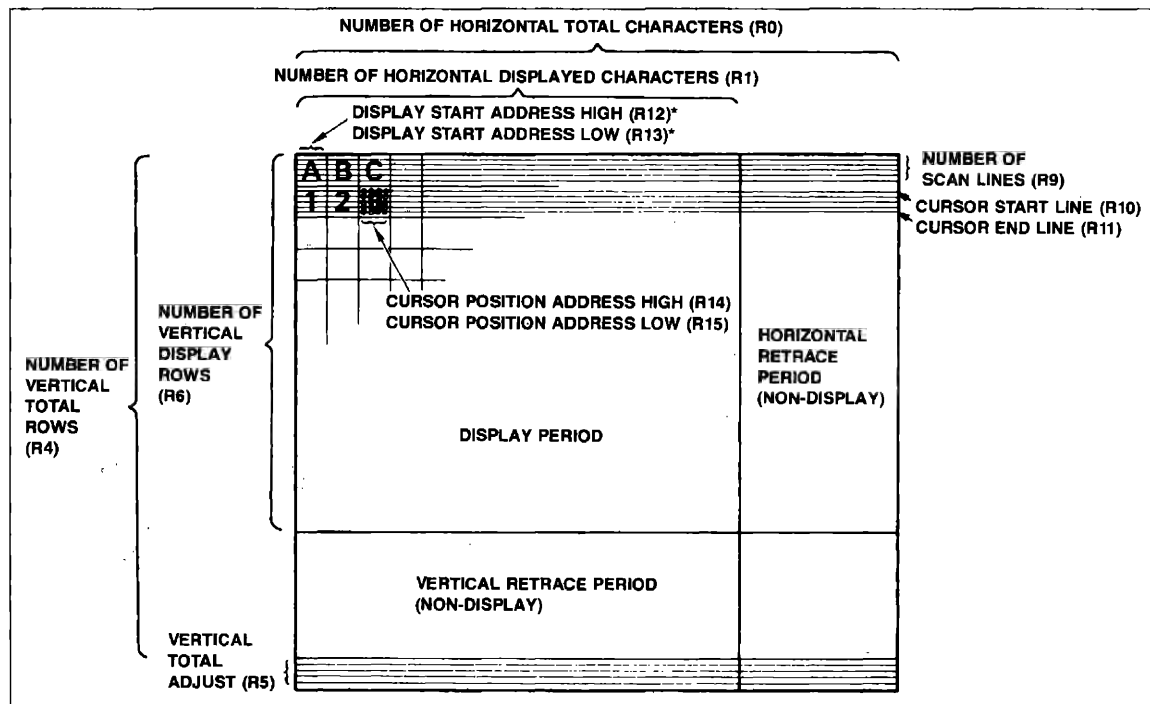


Figure 4. Video Display Format

DESCRIPTION OF OPERATION

VIDEO DISPLAY

Figure 4 indicates the relationship of the various program registers in the R6545-1 and the resultant video display.

Non-displayed areas of the Video Display are for horizontal and vertical retrace functions of the CRT monitor. The horizontal and vertical sync signals, HSYNC and VSYNC, are programmed to occur during these intervals and trigger the retrace in the CRT monitor. The pulse widths are constrained by the monitor requirements. The time position of the pulses may be adjusted to vary the display margins (left, right, top, and bottom).

REFRESH RAM ADDRESSING

There are two modes of addressing for the video display memory:

Shared Memory Mode (R8, BIT 3 = 0)

In this mode, the Refresh RAM address lines (MA0-MA13) directly reflect the contents of the internal refresh scan character counter. Multiplex control, to permit addressing and selection of the RAM by both the CPU and the CRTC, must be provided external to the CRTC. In the Row/Column address mode, lines MA0-MA7 become character column addresses (CC0-CC7) and MA8-MA13 become character row addresses (CR0-CR5). Figure 5 illustrates the system configuration.

2

Transparent Memory Addressing

For this mode, the display RAM is not directly accessible by the CPU, but is controlled entirely by the R6545-1. All CPU accesses are made via the R6545-1 and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

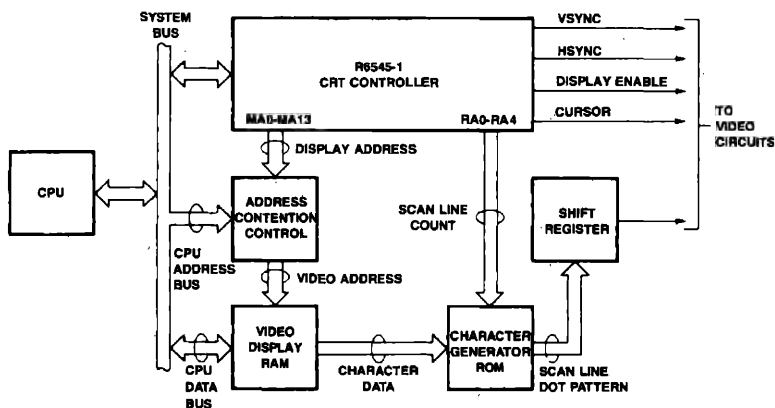


Figure 5. Shared Memory System Configuration

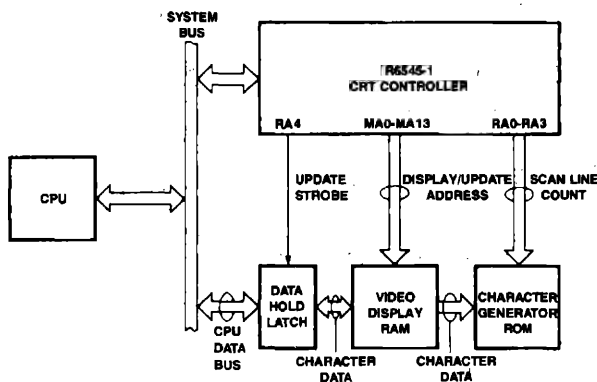


Figure 6. Transparent Memory Addressing System Configuration
(Data Hold Latch Needed for Horizontal/Vertical Blanking Updates, Only).

ADDRESSING MODES

Figure 7 illustrates the address sequence for both modes of the Refresh RAM address.

Row/Column

In this mode, the CRTC address lines (MA0-MA13) generate as 8 column (MA0-MA7) and 6 row (MA8-MA13) addresses. Extra hardware is needed to compress this addressing into a straight binary sequence in order to conserve memory in the refresh RAM (register R8, bit 2 is a 1).

Binary

In this mode, the CRTC address lines are straight binary and no compression circuits are needed. However, software complexity increases since the CRT characters cannot be stored in terms of their row and column locations, but must be sequential (register R8, bit 2 is a 0).

USE OF DYNAMIC RAM FOR REFRESH MEMORY

The R6545-1 permits use of dynamic RAMS as storage devices for the Refresh RAM by continuing to increment memory addresses in the non-display intervals of the scan. This is a

viable technique, since the Display Enable signal controls the actual video display blanking. Figure 7 illustrates Refresh RAM addressing for both row/column and binary addressing for 80 columns and 24 rows with 10 non-displayed columns and 10 non-displayed rows.

Note that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, gaps exist. This requires that the system be equipped with more memory than actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

The user selects whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column minimizes software requirements.

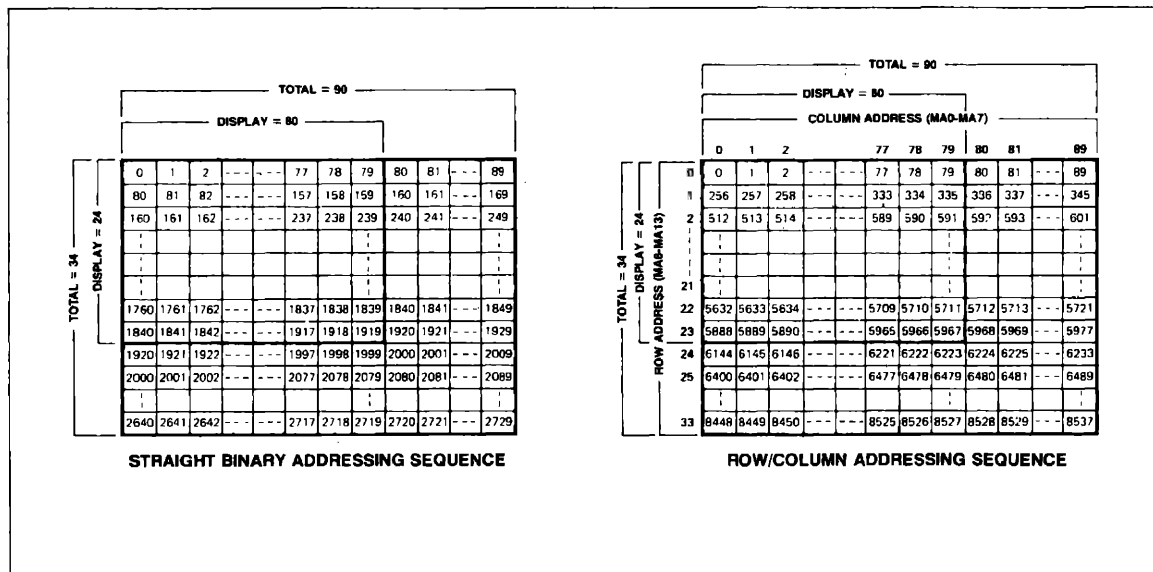


Figure 7. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

MEMORY CONTENTION SCHEMES FOR SHARED MEMORY ADDRESSING

From the diagram of Figure 5, it is clear that both the R6545-1 and the system CPU must address the video display memory. The R6545-1 repetitively fetches character information to generate the video signals in order to keep the screen display active. The CPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

- CPU Priority

In this technique, the address lines to the video display memory are normally driven by the R6545-1 unless the CPU needs access, in which case the CPU addresses immediately override those from the R6545-1 giving the CPU immediate access.

- $\phi 1/\phi 2$ Memory Interleaving

This method permits both the R6545-1 and the CPU access to the video display memory by time-sharing via the system $\phi 1$ and $\phi 2$ clocks. During the $\phi 1$ portion of each cycle (the time when $\phi 2$ is low), the R6545-1 address outputs are gated to the video display memory. In the $\phi 2$ time, the CPU address lines are switched in. In this way, both the R6545-1 and the CPU have unimpeded access to the memory. Figure 8 illustrates the timings.

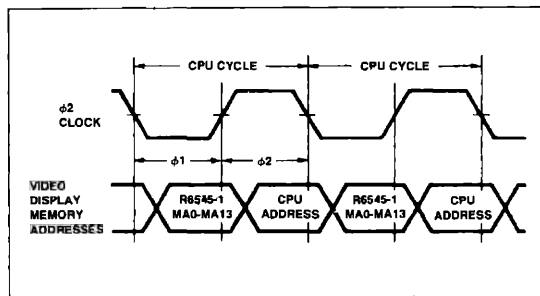


Figure 8. $\phi 1/\phi 2$ Interleaving

- Vertical Blanking

With this approach, the address circuitry is identical to the case for CPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the CPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a 1). In this way, no visible screen perturbations result. See Figure 10 for details.

TRANSPARENT MEMORY ADDRESSING

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the R6545-1. In effect, the contention is handled by the R6545-1. As a result, the schemes for accomplishing CPU memory access are different:

- $\phi 1/\phi 2$ Interleaving

This mode is similar to the Interleave mode used with shared memory. In this case, however, the $\phi 2$ address is generated from the Update Address Register (R18 and R19) in the R6545-1. Thus, the CPU must first load the address to be accessed into R18/R19 and then this address is always gated onto the MA lines during $\phi 2$. Figure 9 shows the timing.

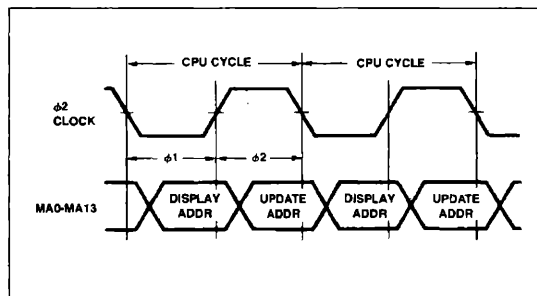


Figure 9. $\phi 1/\phi 2$ Transparent Interleaving

- Horizontal/Vertical Blanking

In this mode, the CPU loads the Update Address, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STB) is provided as an alternate function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system CPU is not halted waiting for the blanking time to arrive. Figure 11 illustrates the address and strobe timing for this mode.

CURSOR AND DISPLAY ENABLE SKEW CONTROL

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 12 illustrates the effect of the delays.

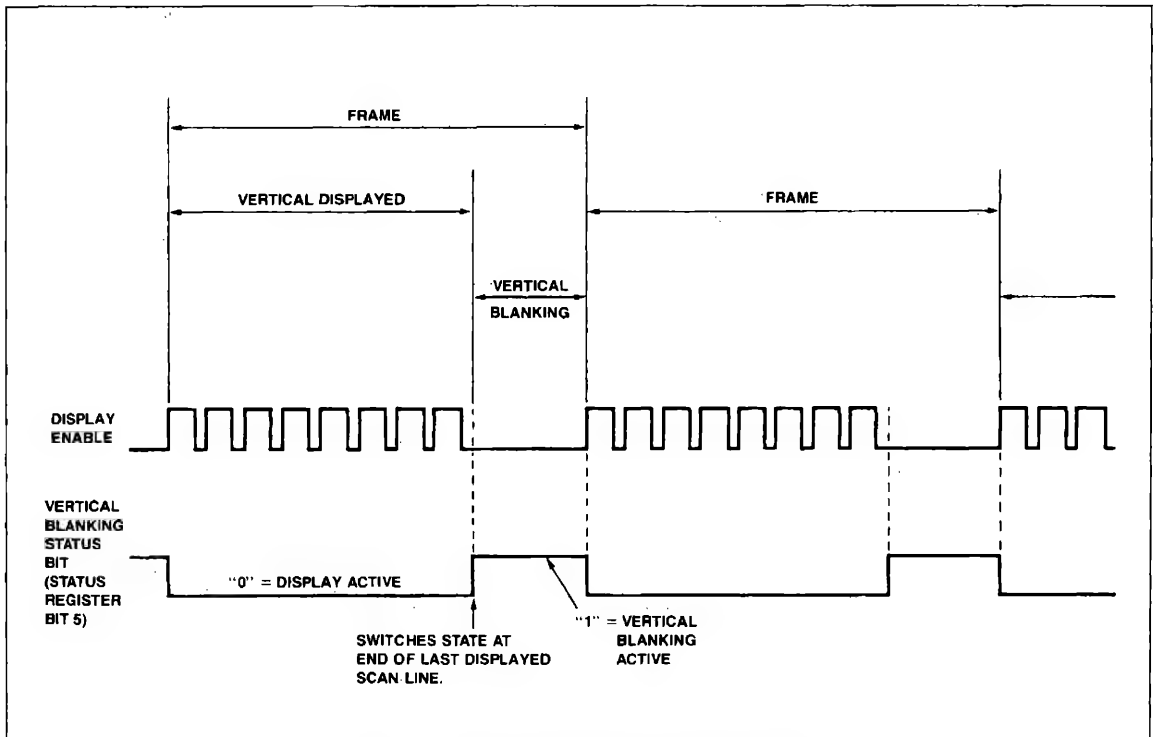


Figure 10. Operation of Vertical Blanking Status Bit

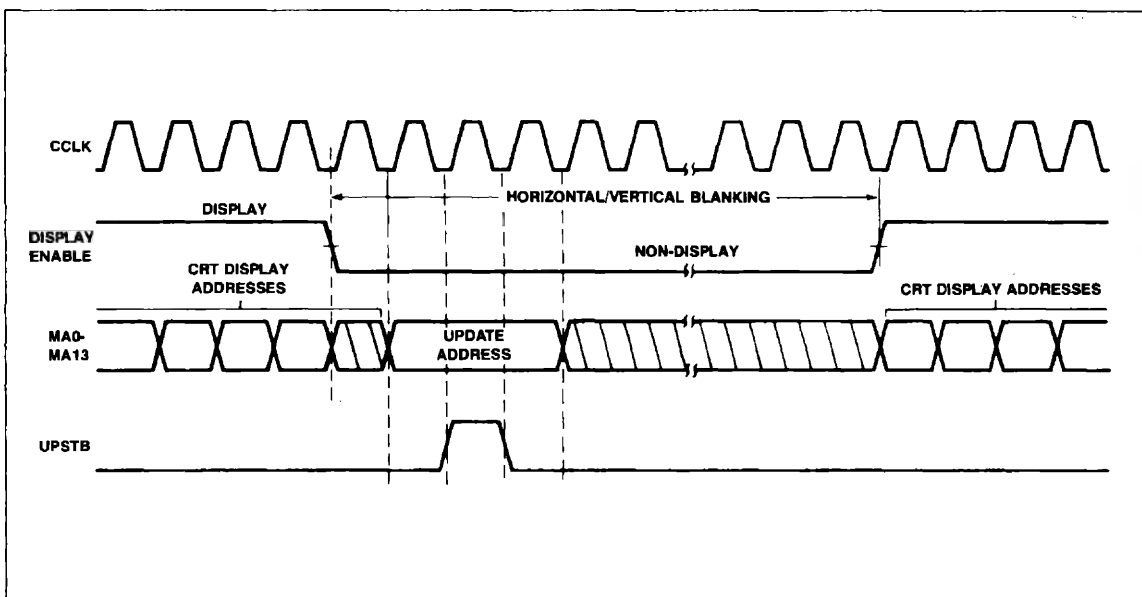


Figure 11. Retrace Update Timing

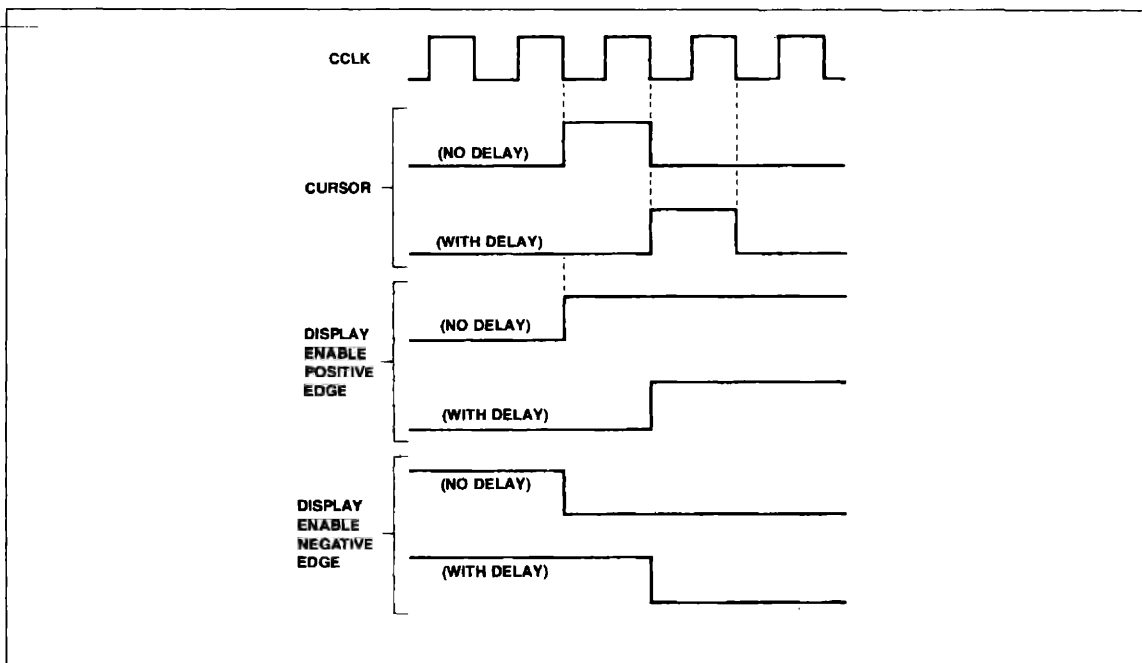


Figure 12. Cursor and Display Enable Skew

WRITE TIMING CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $T_A = T_L$ to T_H , unless otherwise noted)

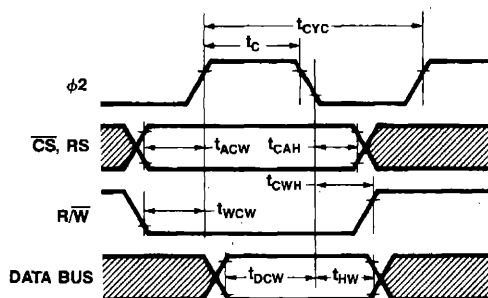
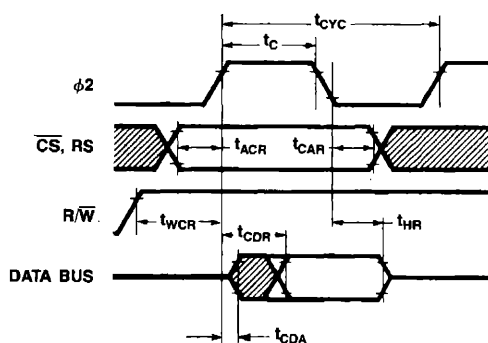
Symbol	Characteristic	R6545-1		R6545A-1		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	$\phi 2$ Pulse Width	440	—	200	—	ns
t_{ACW}	Address Set-Up Time	180	—	90	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/\bar{W} Set-Up Time	180	—	90	—	ns
t_{CWH}	R/\bar{W} Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	265	—	100	—	ns
t_{HW}	Data Bus Hold Time	10	—	10	—	ns

(t_R and $t_F = 10$ to 30 ns)

READ TIMING CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $T_A = T_L$ to T_H , unless otherwise noted)

Symbol	Characteristic	R6545-1		R6545A-1		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	$\phi 2$ Pulse Width	440	—	200	—	ns
t_{ACR}	Address Set-Up Time	180	—	90	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	R/\bar{W} Set-Up Time	180	—	90	—	ns
t_{CDR}	Read Access Time (Valid Data)	—	340	—	150	ns
t_{HR}	Read Hold Time	10	—	10	—	ns
t_{CDA}	Data Bus Active Time (Invalid Data)	40	—	40	—	ns

(t_R and $t_F = 10$ to 30 ns)

WRITE TIMING WAVEFORMS**READ TIMING WAVEFORMS**

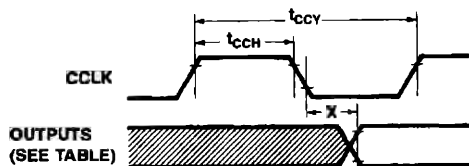
MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = T_L to T_H, unless otherwise noted)

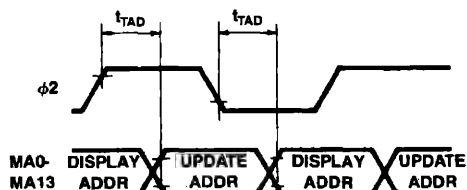
Symbol	Characteristic	R6545-1		R6545A-1		Unit
		Min.	Max.	Min.	Max.	
t _{CCY}	Character Clock Cycle Time	0.40	—	0.40	—	μs
t _{CCH}	Character Clock Pulse Width	200	—	200	—	ns
(X)t _{MAD}	MA0-MA13 Propagation Delay	—	300	—	300	ns
(X)t _{RAD}	RA0-RA4 Propagation Delay	—	300	—	300	ns
(X)t _{DTD}	DISPLAY ENABLE Propagation Delay	—	450	—	450	ns
(X)t _{HSD}	HSYNC Propagation Delay	—	450	—	450	ns
(X)t _{VSD}	VSYSN Propagation Delay	—	450	—	450	ns
(X)t _{CDD}	CURSOR Propagation Delay	—	450	—	450	ns
t _{TAD}	MA0-MA13 Switching Delay	—	200	—	200	ns

Note:
t_R t_F = 20 ns (max).

SYSTEM TIMING WAVEFORMS



TRANSPARENT ADDRESSING WAVEFORMS (φ1/φ2 INTERLEAVING)

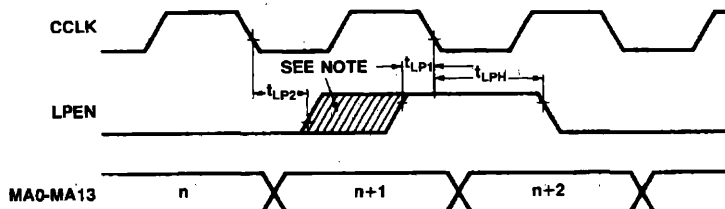


LIGHT PEN STROBE TIMING CHARACTERISTICS

Symbol	Characteristic	R6545-1		R6545A-1		Unit
		Min.	Max.	Min.	Max.	
t _{LPH}	LPEN Hold Time	150	—	150	—	ns
t _{LP1}	LPEN Setup Time	20	—	20	—	ns
t _{LP2}	CCLK to LPEN Delay	0	—	0	—	ns

Note:
t_R t_F = 20 ns (max)

LIGHT PEN STROBE TIMING WAVEFORMS



NOTE: "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register.
t_{LP2} and t_{LP1} are time positions causing uncertain results.

ABSOLUTE MAXIMUM RATINGS*

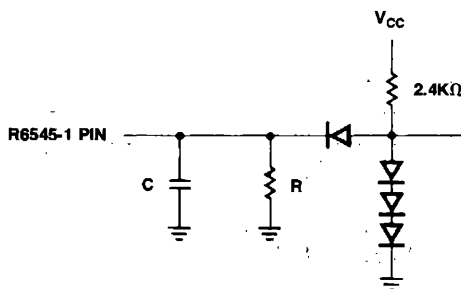
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Range Commercial Industrial	T_A	0 to +70 -40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $T_A = T_L$ to T_H , unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.4	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	0.4	Vdc
Input Leakage ($\overline{\phi 2}$, $\overline{R/W}$, \overline{RES} , \overline{CS} , \overline{RS} , \overline{LPEN} , \overline{CCLK})	I_{IN}	—	2.5	μA_{dc}
Three-State Input Leakage (D0-D7) ($V_{IN} = 0.4$ to $2.4V$)	I_{TSI}	—	± 10.0	μA_{dc}
Output High Voltage $I_{LOAD} = 205 \mu A_{dc}$ (D0-D7) $I_{LOAD} = 100 \mu A_{dc}$ (all others)	V_{OH}	2.4	—	Vdc
Output Low Voltage $I_{LOAD} = 1.6 mA_{dc}$	V_{OL}	—	0.4	Vdc
Power Dissipation	P_D	—	900	mW
Input Capacitance $\overline{\phi 2}$, $\overline{R/W}$, \overline{RES} , \overline{CS} , \overline{RS} , \overline{LPEN} , \overline{CCLK} D0-D7	C_{IN}	—	10.0 12.5	pF pF
Output Capacitance	C_{OUT}	—	10.0	pF

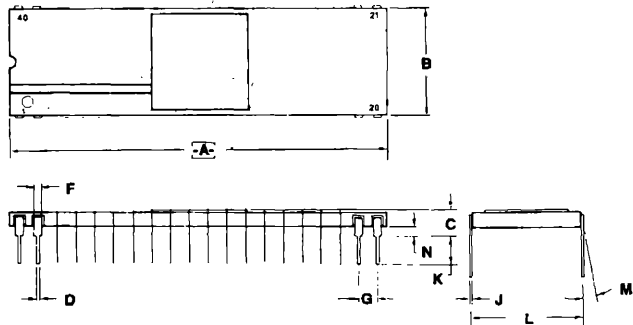
TEST LOAD



$R = 11K\Omega$ FOR D0-D7
 $= 24K\Omega$ FOR ALL OTHER OUTPUTS
 $C = 130$ pF TOTAL FOR D0-D7
 $= 30$ pF ALL OTHER OUTPUTS

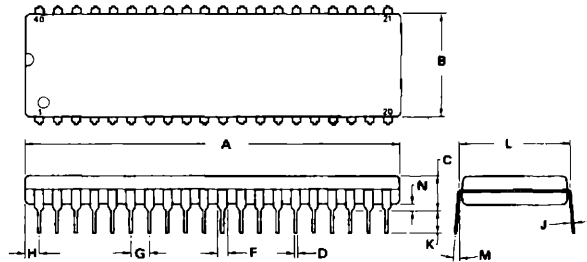
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.56	1.980	2.030
B	14.73	15.49	0.580	0.610
C	1.78	3.05	0.070	0.120
D	0.38	0.58	0.015	0.023
E	1.02	1.65	0.040	0.065
F	2.29	2.80	0.090	0.110
G	0.20	0.38	0.008	0.015
H	3.18	3.81	0.125	0.150
I	14.99	16.51	0.590	0.650
J	0"	10"	0"	10"
K	0.58	1.78	0.020	0.070

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.81	0.014	0.032
E	1.02	1.52	0.040	0.060
F	2.54	BSC	0.100	BSC
G	1.65	2.16	0.065	0.085
H	0.20	0.30	0.008	0.012
I	3.05	3.56	0.120	0.140
J	15.24	BSC	0.600	BSC
K	7"	10"	7"	10"
L	0.51	1.02	0.020	0.040



R6551 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

DESCRIPTION

The Rockwell R6551 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The ACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or at $1/16$ times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at $1/16$ times the external clock rate. The ACIA has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, $1\frac{1}{2}$, or 2 stop bits.

The ACIA is designed for maximum programmed control from the microprocessor (MPU), to simplify hardware implementation. Three separate registers permit the MPU to easily select the R6551's operating modes and data checking parameters and determine operational status.

The Command Register controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{\text{RTS}}$ line, receiver interrupt control, and the state of the $\overline{\text{DTR}}$ line.

The Control Register controls the number of stop bits, word length, receiver clock source, and baud rate.

The Status Register indicates the states of the $\overline{\text{IRQ}}$, $\overline{\text{DSR}}$, and $\overline{\text{DCD}}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing, and Parity Error conditions.

The Transmitter and Receiver Data Registers are used for temporary data storage by the ACIA Transmit and Receiver circuits.

ORDERING INFORMATION

Part No.: R6551	
Temperature Range (T_L to T_H):	
Blank = 0°C to +70°C	
E = -40°C to +85°C	
Frequency Range:	
1 = 1 MHz	
2 = 2 MHz	
Package:	
C = Ceramic	
P = Plastic	

FEATURES

- Compatible with 8-bit microprocessors
- Full duplex operation with buffered receiver and transmitter
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 19,200)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Program reset
- Program-selectable serial echo mode
- Two chip selects
- 2 or 1 MHz operation
- 5.0 Vdc \pm 5% supply requirements
- 28-pin plastic or ceramic DIP
- Full TTL compatibility
- Compatible with R6500, R6500/* and R65C00 micro-processors

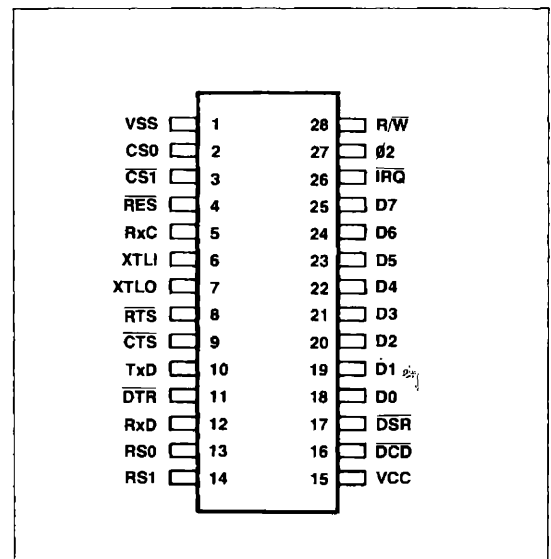


Figure 1. R6551 ACIA Pin Configuration

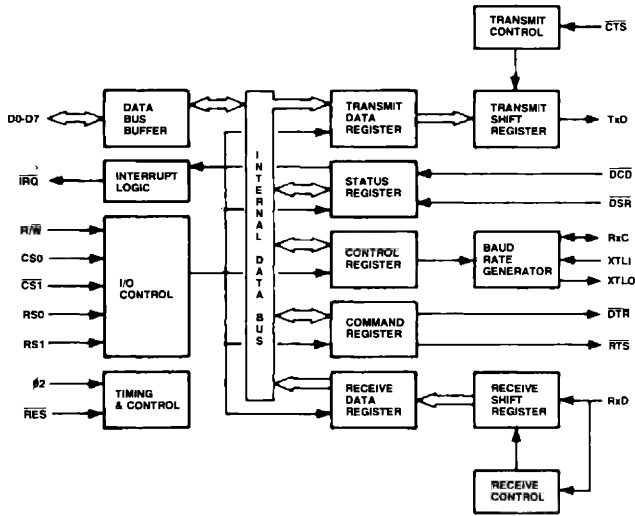


Figure 2. ACIA Internal Organization

FUNCTIONAL DESCRIPTION

A block diagram of the ACIA is presented in Figure 2 followed by a description of each functional element of the device.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the $\overline{R/\overline{W}}$ line is high and the chip is selected, the Data Bus Buffer passes the data from the system data lines to the ACIA internal data bus. When the $\overline{R/\overline{W}}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the internal data bus to the system data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the \overline{IRQ} line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register, if enabled. Bits 5 and 6 correspond to the Data Carrier Detect (DCD) logic and the Data Set Ready (DSR) logic. Bits 3 and 4 correspond to the Receiver Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers in preparation for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Receiver Select (RS1, RS0) and Read/Write ($\overline{R/\overline{W}}$) lines as described later in Table 1.

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus and the registers, the Data Bus Buffer, and the microprocessor data bus, and the hardware reset features.

Timing is controlled by the system $\phi 2$ clock input. The chip will perform data transfers to or from the microcomputer data bus during the $\phi 2$ high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset (\overline{RES}) line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the ACIA Transmitter and Receive Circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write ($\overline{R/\overline{W}}$) line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care".

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

STATUS REGISTER

The Status Register indicates the state of interrupt conditions and other non-interrupt status lines. The interrupt conditions are the Data Set Ready, Data Carrier Detect, Transmitter Data Register Empty and Receiver Data Register Full as reported in bits 6 through 3, respectively. If any of these bits are set, the Interrupt (IRQ) indicator (bit 7) is also set. Overrun, Framing Error, and Parity Error are also reported (bits 2 through 0 respectively).

7	6	5	4	3	2	1	0
IRQ	DSR	DCD	TDRE	RDRE	OVN	FE	PE

Bit 7 Interrupt (IRQ)

- 0 No interrupt
- 1 Interrupt has occurred

Bit 6 Data Set Ready (DSR)

- 0 DSR low (ready)
- 1 DSR high (not ready)

Bit 5 Data Carrier Detect (DCD)

- 0 DCD low (detected)
- 1 DCD high (not detected)

Bit 4 Transmitter Data Register Empty

- 0 Not empty
- 1 Empty

Bit 3 Receiver Data Register Full

- 0 Not full
- 1 Full

Bit 2 Overrun*

- 0 No overrun
- 1 Overrun has occurred

Bit 1 Framing Error*

- 0 No framing error
- 1 Framing error detected

Bit 0 Parity Error*

- 0 No parity error
- 1 Parity error detected

*No interrupt occurs for these conditions

Reset Initialization

7	6	5	4	3	2	1	0	
0	—	—	1	0	0	0	0	Hardware reset
—	—	—	—	0	—	—	—	Program reset

Parity Error (Bit 0), Framing Error (Bit 1), and Overrun (2)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified. These bits are self clearing (i.e., they are automatically cleared after a read of the Receiver Data Register).

Receiver Data Register Full (Bit 3)

This bit goes to a 1 when the ACIA transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a 0 (is cleared) when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a 1 when the ACIA transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a 0 (is cleared) when the processor writes new data onto the Transmitter Data Register.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the DCD and DSR inputs to the ACIA. A 0 indicates a low level (true condition) and a 1 indicates a high level (false). Whenever either of these inputs change state, an immediate processor interrupt (IRQ) occurs, unless bit 1 of the Command Register (IRD) is set to a 1 to disable IRQ. When the interrupt occurs, the status bits indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until the Status Register is interrogated by the processor. At that time, another interrupt will immediately occur and the status bits reflect the new input levels. These bits are not automatically cleared (or reset) by an internal operation.

Interrupt (Bit 7)

This bit goes to a 1 whenever an interrupt condition occurs and goes to a 0 (is cleared) when the Status Register is read.

CONTROL REGISTER

The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.

7	6	5	4	3	2	1	0
SBN	WL		RCS	SBR			
	WL1	WL0		SBR3	SBR2	SBR1	SBR0

Bit 7 Stop Bit Number (SBN)

0	1 Stop bit
1	2 Stop bits
1	1½ Stop bits
	For WL = 5 and no parity
1	1 Stop bit
	For WL = 8 and parity

Bits 6-5 Word Length (WL)

6	5	No. Bits
0	0	8
0	1	7
1	0	6
1	1	5

Bit 4 Receiver Clock Source (RCS)

0	External receiver clock
1	Baud rate

Bits 3-0 Selected Baud Rate (SBR)

3	2	1	0	Baud
0	0	0	0	16x External Clock
0	0	0	1	50
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

Reset Initialization

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-

Hardware reset (\overline{RES})

Program reset

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits select the Transmitter baud rate, which can be at $1/16$ an external clock rate or one of 15 other rates controlled by the internal baud rate generator.

If the Receiver clock uses the same baud rate as the transmitter, then RxC becomes an output and can be used to slave other circuits to the ACIA. Figure 3 shows the Transmitter and Receiver layout.

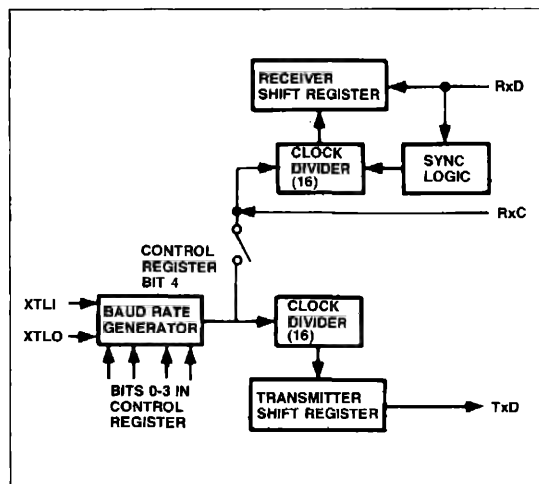


Figure 3. Transmitter/Receiver Clock Circuits

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A 0 causes the Receiver to operate at a baud rate of $1/16$ an external clock. A 1 causes the Receiver to operate at the same baud rate as is selected for the transmitter.

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits).

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A 0 always indicates one stop bit. A 1 indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, or 2 stop bits in all other configurations.

COMMAND REGISTER

The Command Register controls specific modes and functions.

7	6	5	4	3	2	1	0
PMC		PME	REM	TIC		IRD	DTR
PMC1	PMC0			TIC1	TIC0		

Bits 7-6 Parity Mode Control (PMC)

7	6	
0	0	Odd parity transmitted/received
0	1	Even parity transmitted/received
1	0	Mark parity bit transmitted Parity check disabled
1	1	Space parity bit transmitted Parity check disabled

Bit 5 Parity Mode Enabled (PME)

0	Parity mode disabled No parity bit generated Parity check disabled
1	Parity mode enabled

Bit 4 Receiver Echo Mode (REM)

0	Receiver normal mode
1	Receiver echo mode bits 2 and 3 Must be zero for receiver echo mode, RTS will be low.

Bits 3-2 Transmitter Interrupt Control (TIC)

3	2	
0	0	$\overline{\text{RTS}}$ = High, transmit interrupt disabled
0	1	$\overline{\text{RTS}}$ = Low, transmit interrupt enabled
1	0	$\overline{\text{RTS}}$ = Low, transmit interrupt disabled
1	1	$\overline{\text{RTS}}$ = Low, transmit interrupt disabled transmit break on TxD

Bit 1 Interrupt Request Disabled (IRD)

0	$\overline{\text{IRQ}}$ enabled
1	$\overline{\text{IRQ}}$ disabled

Bit 0 Data Terminal Ready (DTR)

0	Data terminal not ready ($\overline{\text{DTR}}$ high)
1	Data terminal ready ($\overline{\text{DTR}}$ low)

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{\text{DTR}}$) line. A 0 indicates the microcomputer system is not ready by setting the $\overline{\text{DTR}}$ line high. A 1 indicates the microcomputer system is ready by setting the $\overline{\text{DTR}}$ line low.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a 1. The Receiver interrupt is enabled when this bit is set to a 0 and Bit 0 is set to a 1.

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send ($\overline{\text{RTS}}$) line and the Transmitter interrupt.

Receiver Echo Mode (Bit 4)

A 1 enables the Receiver Echo Mode and a 0 enables the Receiver Echo Mode. When bit 4 is a 1, bits 2 and 3 must be 0. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by one-half bit time.

Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A 0 disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A 1 bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check).

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset ($\overline{\text{RES}}$)
—	—	—	0	0	0	0	0	Program reset

INTERFACE SIGNALS

Figure 4 shows the ACIA interface signals associated with the microprocessor and the modem.

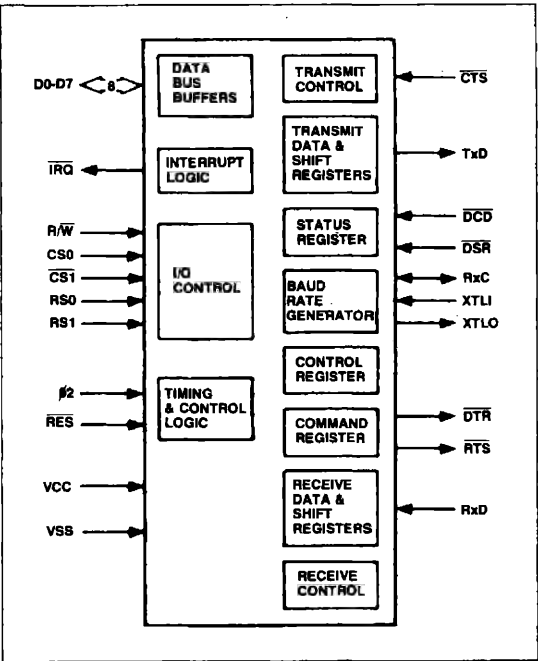


Figure 4. ACIA Interface Diagram

MICROPROCESSOR INTERFACE

Reset (\overline{RES})

During system initialization a low on the \overline{RES} input causes a hardware reset to occur. Upon reset, the Command Register and the Control Register are cleared (all bits set to 0). The Status Register is cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the DSR and DCD lines, and the transmitter Empty bit, which is set. \overline{RES} must be held low for one $\phi 2$ clock cycle for a reset to occur.

Input Clock ($\phi 2$)

The input clock is the system $\phi 2$ clock and clocks all data transfers between the system microprocessor and the ACIA.

Read/Write (R/\overline{W})

The R/\overline{W} input, generated by the microprocessor controls the direction of data transfers. A high on the R/\overline{W} pin allows the processor to read the data supplied by the ACIA, a low allows a write to the ACIA.

Interrupt Request (\overline{IRQ})

The \overline{IRQ} pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common \overline{IRQ} microprocessor input. Normally a high level, \overline{IRQ} goes low when an interrupt occurs.

Data Bus (D0-D7)

The eight data line (D0-D7) pins transfer data between the processor and the ACIA. These lines are bi-directional and are normally high-impedance except during Read cycles when the ACIA is selected.

Chip Selects (CS0, $\overline{CS1}$)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The ACIA is selected when CS0 is high and $\overline{CS1}$ is low. When the ACIA is selected, the internal registers are addressed in accordance with the register select lines (RS0, RS1).

Register Selects (RS0, RS1)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various ACIA internal registers. Table 1 shows the internal register select coding.

Table 1. ACIA Register Selection

RS1	RS0	Register Operation	
		R/\overline{W} = Low	R/\overline{W} = High
L	L	Write Transmit Data Register	Read Receiver Data Register
L	H	Programmed Reset (Data is "Don't Care")	Read Status Register
H	L	Write Command Register	Read Command Register
H	H	Write Control Register	Read Control Register

Only the Command and Control registers can both be read and written. The programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command register and bit 2 in the Status Register. The Control Register is unchanged by a programmed Reset. It should be noted that the programmed Reset is slightly different from the hardware Reset (\overline{RES}); refer to the register description.

ACIA/MODEM INTERFACE

Crystal Pins (XTLI, XTLO)

These pins are normally directly connected to the external crystal (1.8432 MHz) to derive the various baud rates. Alternatively, an externally generated clock can drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

Transmit Data (TxD)

The TxD output line transfers serial nonreturn-to-zero (NRZ) data to the modem. The least significant bit (LSB) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or under control of an external clock. This selection is made by programming the Control Register.

Receive Data (RxD)

The RxD input line transfers serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or under the control of an externally generated receiver clock. The selection is made by programming the Control Register.

Receive Clock (RxC)

The RxC is a bi-directional pin which is either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

Request to Send (RTS)

The RTS output pin controls the modem from the processor. The state of the RTS pin is determined by the contents of the Command Register.

Clear to Send (CTS)

The CTS input pin controls the transmitter operation. The enable state is with CTS low. The transmitter is automatically disabled if CTS is high.

Data Terminal Ready (DTR)

This output pin indicates the status of the ACIA to the modem. A low on DTR indicates the ACIA is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

Data Set Ready (DSR)

The DSR input pin indicates to the ACIA the status of the modem. A low indicates the "ready" state and a high, "not-ready."

Data Carrier Detect (DCD)

The DCD input pin indicates to the ACIA the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

TRANSMITTER AND RECEIVER OPERATION

Continuous Data Transmit

In the normal operating mode, the interrupt request output (\overline{IRQ}) signals when the ACIA is ready to accept the next data word to be transmitted. This interrupt occurs at the beginning of the Start Bit. When the processor reads the Status Register of the ACIA, the interrupt is cleared.

The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted. Figure 5 shows the continuous Data Transmit timing relationship.

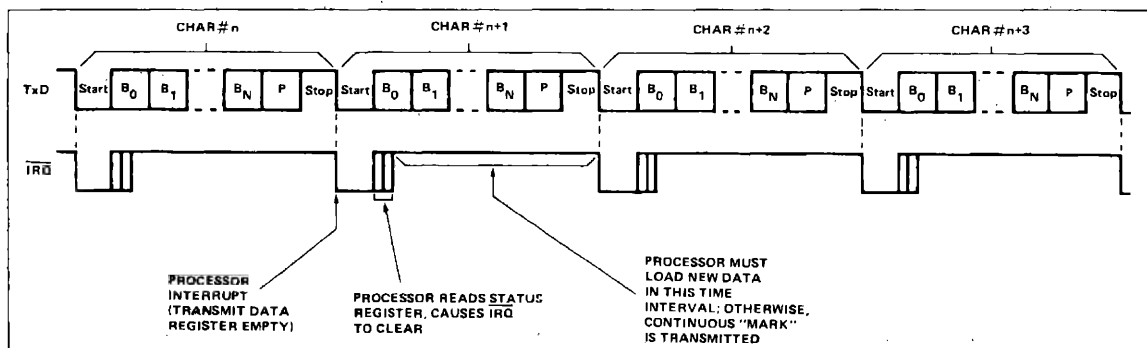


Figure 5. Continuous Data Transmit

Continuous Data Receive

Similar to the Continuous Data Transmit case, the normal operation of this mode is to assert $\overline{\text{IRQ}}$ when the ACIA has received a full data word. This occurs at about $9/16$ point through the Stop Bit. The processor must read the Status Register and

read the data word before the next interrupt, otherwise the Overrun condition occurs. Figure 6 shows the continuous Data Receive Timing Relationship.

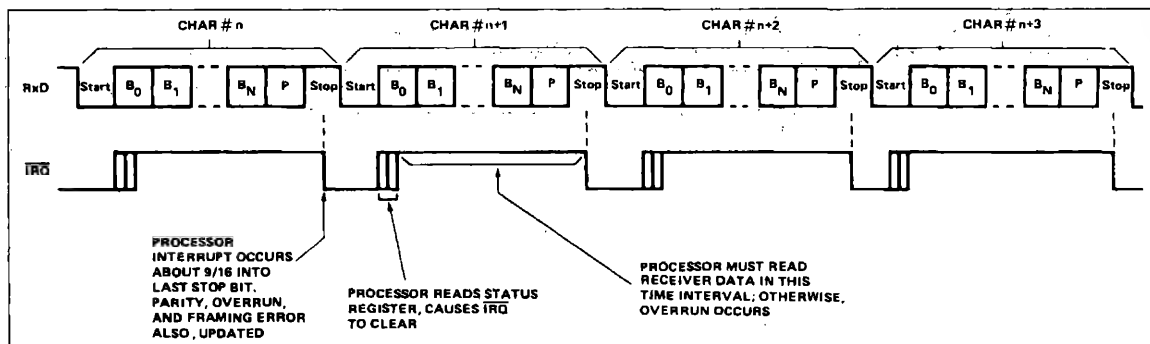


Figure 6. Continuous Data Receive

Transmit Data Register Not Loaded by Processor

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line goes to the "MARK" condition until the data is loaded. $\overline{\text{IRQ}}$ interrupts continue to occur at the same rate as previously, except no data is transmitted.

When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word. Figure 7 shows the timing relationship for this mode of operation.

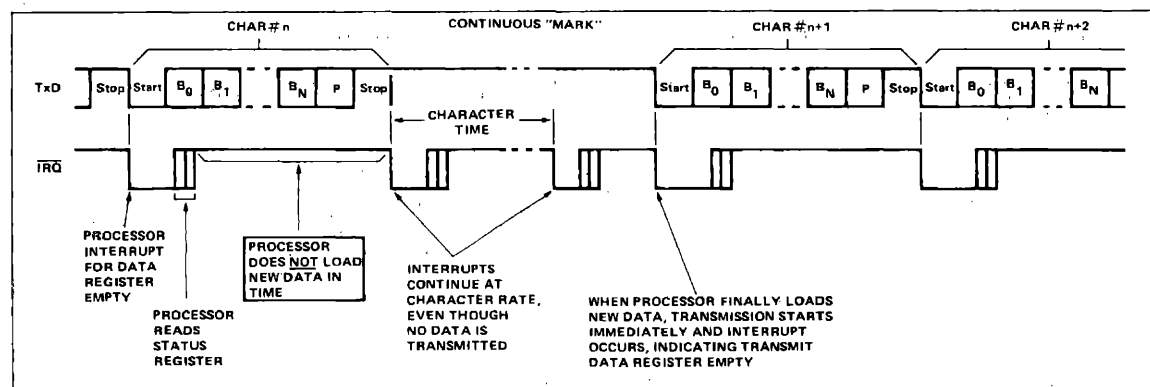


Figure 7. Transmit Data Register Not Loaded by Processor

Effect of CTS on Transmitter

CTS is the Clear-to-Send signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line goes to the "MARK" condition after the entire last character (including parity and stop bit) have been transmitted. Bit 4 in the Status Register

indicates that the Transmitter Data Register is not empty and $\overline{\text{IRQ}}$ is not asserted. CTS is a transmit control line only, and has no effect on the ACIA Receiver Operation. Figure 8 shows the timing relationship for this mode of operation.

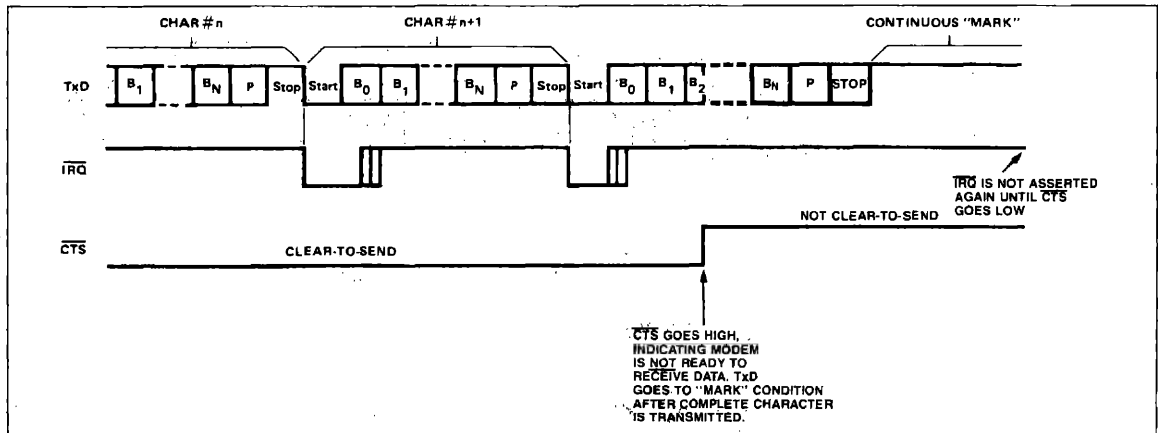


Figure 8. Effect of CTS on Transmitter

Effect of Overrun on Receiver

If the processor does not read the Receiver data Register in the allocated time, then, when the following interrupt occurs, the new data word is not transferred to the Receiver Data Register,

but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost. Figure 9 shows the timing relationship for this mode.

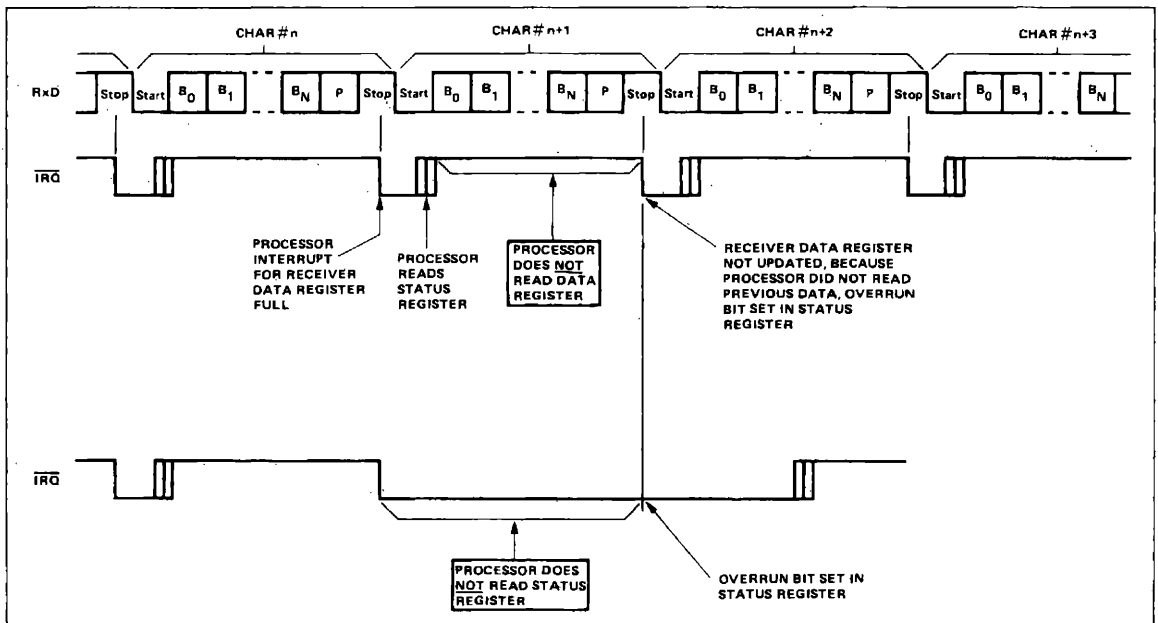


Figure 9. Effect of Overrun on Receiver

Echo Mode Timing

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by 1/2 of the bit time, as shown in Figure 10.

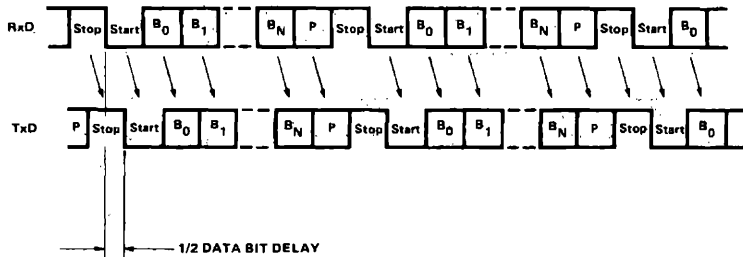


Figure 10. Echo Mode Timing

Effect of CTS on Echo Mode Operation

In Echo Mode, the Receiver operation is unaffected by CTS, however, the Transmitter is affected when CTS goes high, i.e., the TxD line immediately goes to a continuous "MARK" condition. In this case, however, the Status Request indicates that

the Receiver Data Register is full in response to an IRQ, so the processor has no way of knowing that the Transmitter has ceased to echo. See Figure 11 for the timing relationship of this mode.

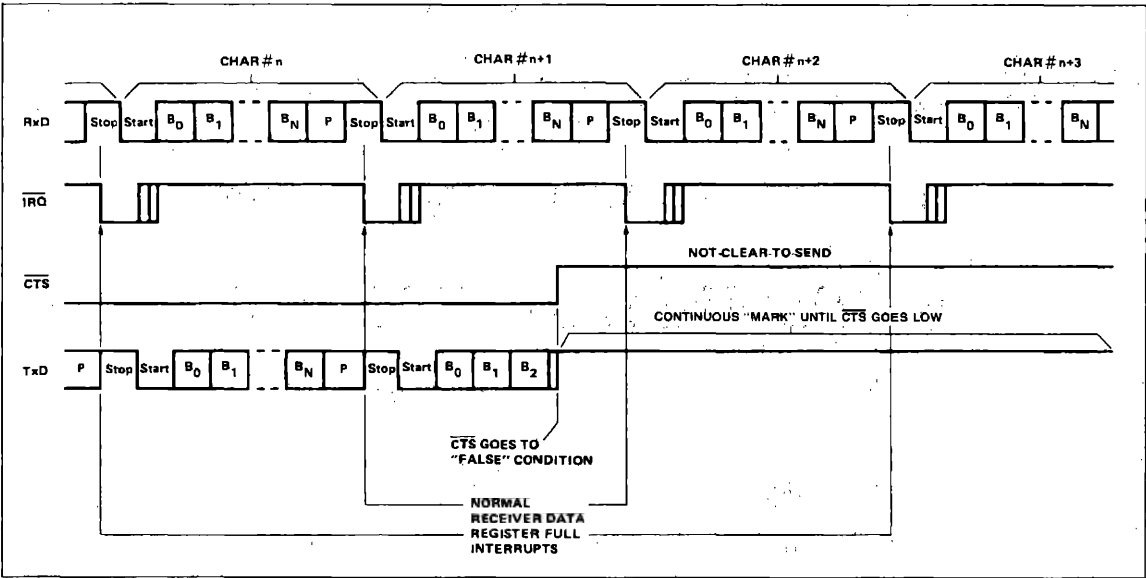


Figure 11. Effect of CTS on Echo Mode

Overflow in Echo Mode

If Overflow occurs in Echo Mode, the Receiver is affected the same way as a normal overflow in Receive Mode. For the re-transmitted data, when overflow occurs, the Tx/D line goes to the

"MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor. Figure 12 shows the timing relationship for this mode.

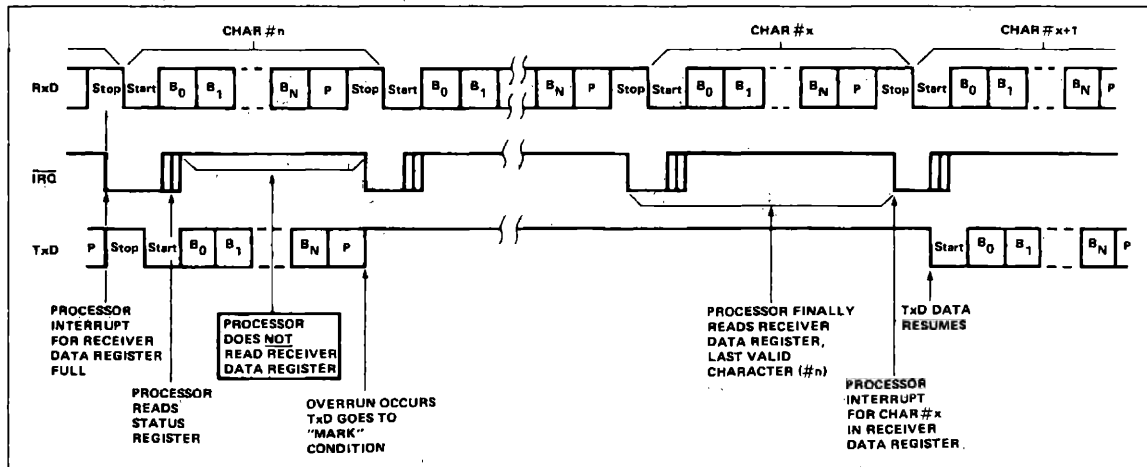


Figure 12. Overflow in Echo Mode

Framing Error

Framing Error is caused by the absence of Stop Bit(s) on received data. A Framing Error is indicated by the setting of bit 4 in the Status Register at the same time the Receiver Data Register Full bit is set, also in the Status Register. In response to IRQ, generated by RDRF, the Status Register can also be

checked for the Framing Error. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received. See Figure 13 for Framing Error timing relationship.

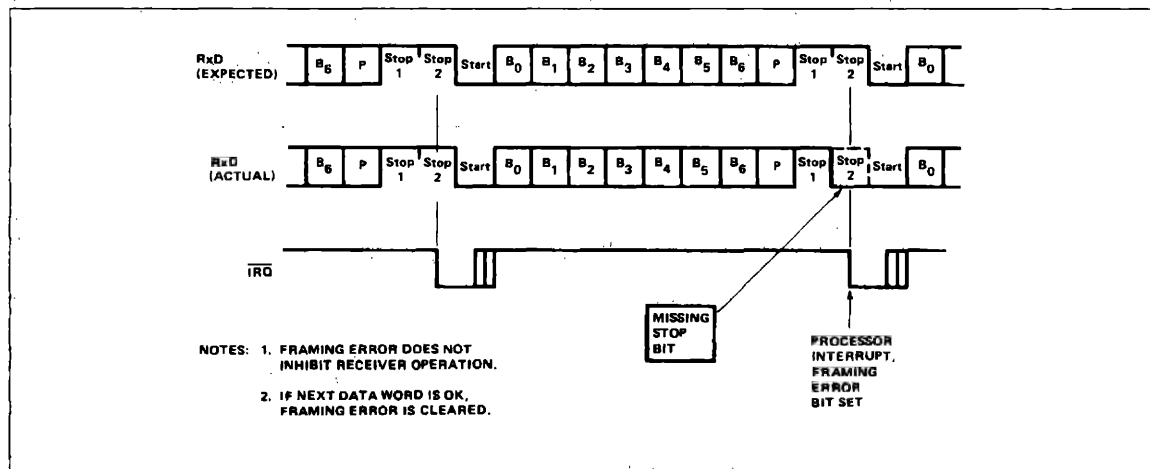


Figure 13. Framing Error

Effect of DCD on Receiver

DCD is a modem output indicating the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data some time later. The ACIA asserts IRQ whenever DCD changes state and indicates this condition via bit 5 in the Status Register.

Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register is read by the processor, the ACIA automatically checks the level of the DCD line, and if it has changed, another IRQ occurs (see Figure 14).

2

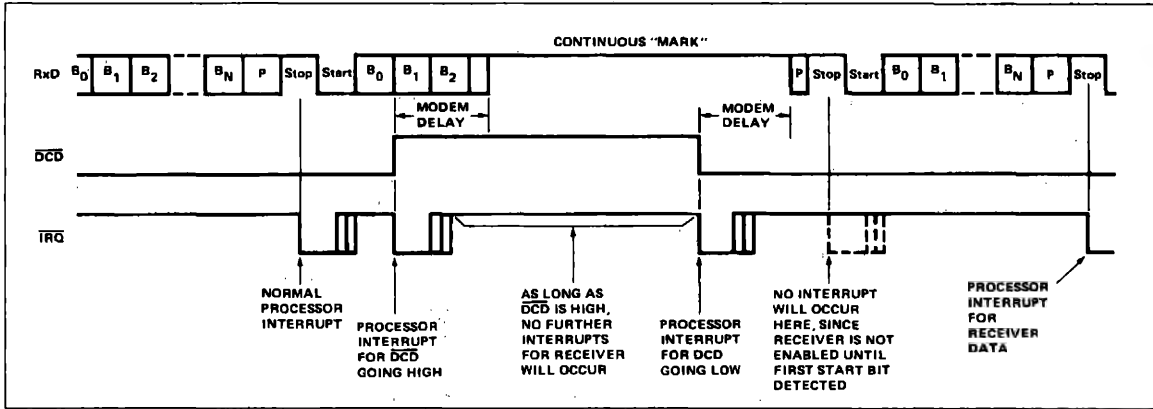


Figure 14. Effect of DCD on Receiver

Timing with 1½ Stop Bits

It is possible to select 1½ Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the IRQ asserted for Receiver Data Register Full occurs halfway through the

trailing half-Stop Bit. Figure 15 shows the timing relationship for this mode.

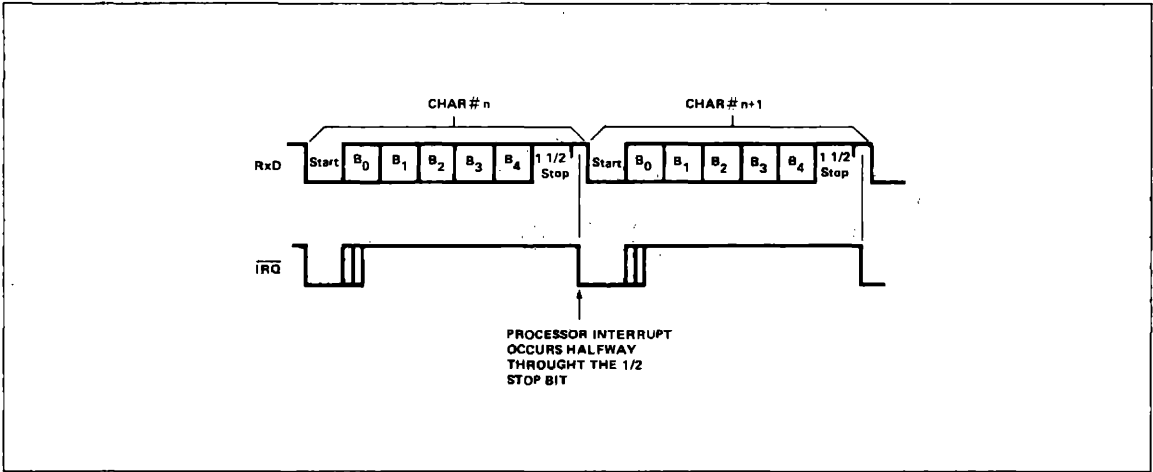


Figure 15. Timing with 1½ Stop Bits

Transmit Continuous "BREAK"

This mode is selected via the ACIA Command Register and causes the Transmitter to send continuous "BREAK" characters, beginning with the next character transmitted. At least one full "BREAK" character will be transmitted, even if the processor quickly re-programs the Command Register transmit mode. Later, when the Command Register is programmed back to normal transmit mode, an immediate Stop Bit will be generated and transmission will resume. Figure 16 shows the timing relationship for this mode.

Note

If, while operating in the Transmit Continuous "BREAK" mode, the CTS should go to a high, the TxD will be overridden by the CTS and will go to continuous "MARK" at the beginning of the next character transmitted after the CTS goes high.

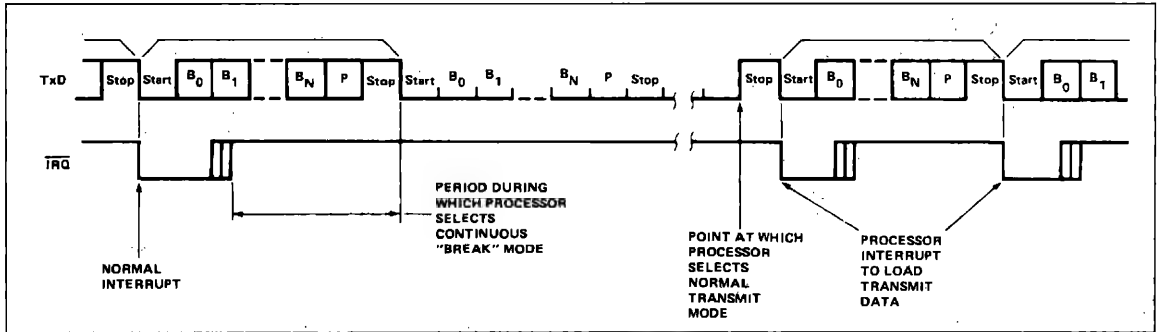


Figure 16. Transmit Continuous "BREAK"

Receive Continuous "BREAK"

In the event the modem transmits continuous "BREAK" characters, the ACIA will terminate receiving. Reception will resume only after a Stop Bit is encountered by the ACIA. Figure 17

shows the timing relationship for continuous "BREAK" characters.

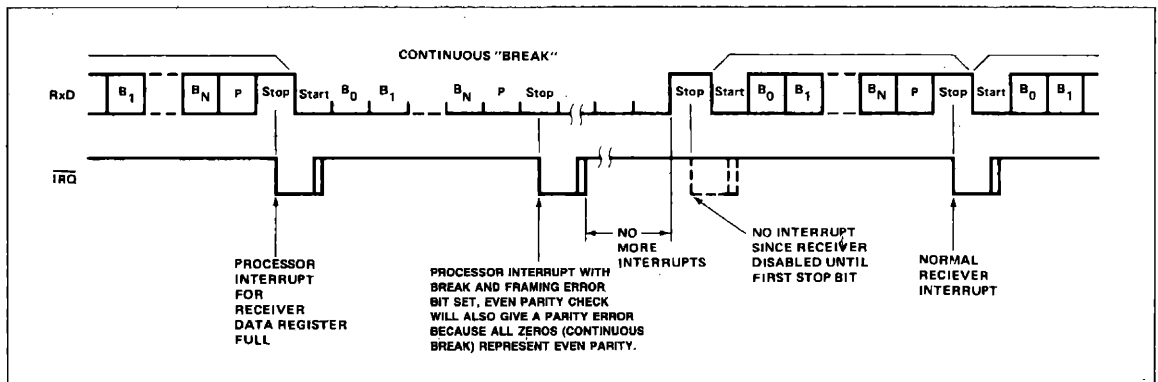


Figure 17. Receive Continuous "BREAK"

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the ACIA should be interrogated, as follows:

1. Read Status Register

This operation automatically clears Bit 7 (\overline{IRQ}). Subsequent transitions on \overline{DCD} and \overline{DSR} will cause another interrupt.

2. Check \overline{IRQ} (Bit 7) in the data read from the Status Register

If not set, the interrupt source is not the ACIA.

3. Check \overline{DCD} and \overline{DSR}

These must be compared to their previous levels, which must have been saved by the processor. If they are both 0 (modern "on-line") and they are unchanged then the remaining bits must be checked.

4. Check RDRF (Bit 3)

Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0-2) if the Receiver Data Register is full.

6. Check TDRE (Bit 4)

Check for Transmitter Data Register Empty.

7. If none of the above conditions exist, then \overline{CTS} must have gone to the false (high) state.

PROGRAM RESET OPERATION

A program reset occurs when the processor performs a write operation to the ACIA with RS0 low and RS1 high. The program reset operates somewhat different from the hardware reset (\overline{RES} pin) and is described as follows:

1. Internal registers are not completely cleared. Check register formats for the effect of a program reset on internal registers.

2. The \overline{DTR} line goes high immediately.

3. Receiver and transmitter interrupts are disabled immediately. If \overline{IRQ} is low when the reset occurs, it stays low until serviced, unless interrupt was caused by \overline{DCD} or \overline{DSR} transition.

4. \overline{DCD} and \overline{DSR} interrupts are disabled immediately. If \overline{IRQ} is low and was caused by \overline{DCD} or \overline{DSR} , then it goes high, also \overline{DCD} and \overline{DSR} status bits subsequently will follow the input lines, although no interrupt will occur.

5. Overrun cleared, if set.

MISCELLANEOUS

1. If Echo Mode is selected, \overline{RTS} goes low.
2. If Bit 0 of Command Register is 0 (disabled), then:
 - a) All interrupts are disabled, including those caused by \overline{DCD} and \overline{DSR} transitions.
 - b) Transmitter is disabled immediately.
 - c) Receiver is disabled, but a character currently being received will be completed first.
3. Odd parity occurs when the sum of all the 1 bits in the data word (including the parity bit) is odd.
4. In the receive mode, the received parity bit does not go into the Receiver Data Register, but generates parity error or no parity error for the Status Register.
5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.
6. If the RxD line inadvertently goes low and then high right after a Stop Bit, the ACIA does not interpret this as a Start Bit, but samples the line again halfway into the bit to determine if it is a true Start Bit or a false one. For false Start Bit detection, the ACIA does not begin to receive data, instead, only a true Start Bit initiates receiver operation.
7. Precautions to consider with the crystal oscillator circuit:
 - a) The external crystal should be a "series" mode crystal.
 - b) The XTALI input may be used as an external clock input. The unused pin (EXTALO) must be floating and may not be used for any other function.
8. \overline{DCD} and \overline{DSR} transitions, although causing immediate processor interrupts, have no effect on transmitter operation. Data will continue to be sent, unless the processor forces transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be terminated either to GND or V_{CC} .

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the ACIA Control Register, as shown in Table 2.

Generating Other Baud Rates

By using a different crystal, other baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the ACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 6) must be the clock input and XTALO (pin 7) must be a no-connect.

Table 2. Divisor Selection

Control Register Bits	Divisor Selected For The Internal Counter	Baud Rate Generated With 1.8432 MHz Crsttal	Baud Rate Generated With a Crystal of Frequency (F)
3 2 1 0			
0 0 0 0	No Divisor Selected	16 × External Clock at Pin Rx/C	16 × External Clock at Pin Rx/C
0 0 0 1	36,864	$\frac{1.8432 \times 10^6}{36,864} = 50$	$\frac{F}{36,864}$
0 0 1 0	24,576	$\frac{1.8432 \times 10^6}{24,576} = 75$	$\frac{F}{24,576}$
0 0 1 1	16,768	$\frac{1.8432 \times 10^6}{16,768} = 109.92$	$\frac{F}{16,768}$
0 1 0 0	13,704	$\frac{1.8432 \times 10^6}{13,704} = 134.51$	$\frac{F}{13,704}$
0 1 0 1	12,288	$\frac{1.8432 \times 10^6}{12,288} = 150$	$\frac{F}{12,288}$
0 1 1 0	6,144	$\frac{1.8432 \times 10^6}{6,144} = 300$	$\frac{F}{6,144}$
0 1 1 1	3,072	$\frac{1.8432 \times 10^6}{3,072} = 600$	$\frac{F}{3,072}$
1 0 0 0	1,536	$\frac{1.8432 \times 10^6}{1,536} = 1,200$	$\frac{F}{1,536}$
1 0 0 1	1,024	$\frac{1.8432 \times 10^6}{1,024} = 1,800$	$\frac{F}{1,024}$
1 0 1 0	768	$\frac{1.8432 \times 10^6}{768} = 2,400$	$\frac{F}{768}$
1 0 1 1	512	$\frac{1.8432 \times 10^6}{512} = 3,600$	$\frac{F}{512}$
1 1 0 0	384	$\frac{1.8432 \times 10^6}{384} = 4,800$	$\frac{F}{384}$
1 1 0 1	256	$\frac{1.8432 \times 10^6}{256} = 7,200$	$\frac{F}{256}$
1 1 1 0	192	$\frac{1.8432 \times 10^6}{192} = 9,600$	$\frac{F}{192}$
1 1 1 1	96	$\frac{1.8432 \times 10^6}{96} = 19,200$	$\frac{F}{96}$

DIAGNOSTIC LOOP-BACK OPERATING MODES

A simplified block diagram for a system incorporating an ACIA is shown in Figure 18.

It may be desirable to include in the system a facility for "loop-back" testing, of which there are two kinds:

1. Local Loop-Back

Loop-back from the point of view of the processor. In this case, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

2. Remote Loop-Back

Loop-back from the point of view of the Data Link and Modem. In this case, the processor, itself, is disconnected and all received data is immediately retransmitted, so the system on the other end of the Data Link may operate independent of the local system.

The ACIA does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry. Figure 19 indicates the necessary logic to be used with the ACIA. The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following:

1. Disables outputs TxD, $\overline{\text{DTR}}$, and $\overline{\text{RTS}}$ (to Modem).
2. Disables inputs RxD, $\overline{\text{DCD}}$, $\overline{\text{CTS}}$, $\overline{\text{DSR}}$ (from Modem).
3. Connects transmitter outputs to respective receiver inputs (i.e., TxD to RxD, $\overline{\text{DTR}}$ to $\overline{\text{DCD}}$, $\overline{\text{RTS}}$ to $\overline{\text{CTS}}$).

LLB may be tied to a peripheral control pin (from an R6520 or R6522, for example) to provide processor control of local loop-

back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

Remote loop-back does not require this circuitry, so LLB must be set low. However, the processor must select the following:

1. Control Register bit 4 must be 1, so that the transmitter clock equals the receiver clock.
2. Command Register bit 4 must be 1 to select Echo Mode.
3. Command Register bits 3 and 2 must be 1 and 0, respectively to disable $\overline{\text{TRQ}}$ interrupt to transmitter.
4. Command Register bit 1 must be 0 to disable $\overline{\text{TRQ}}$ interrupt for receiver.

In this way, the system re-transmits received data without any effect on the local system.

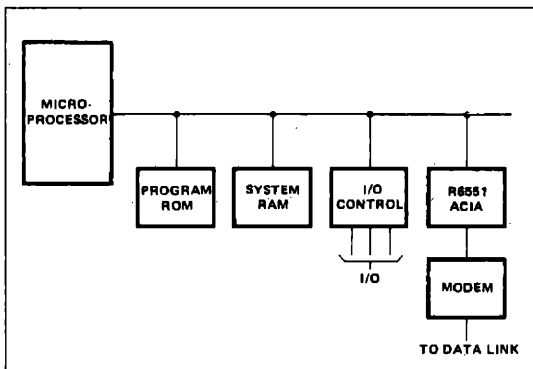


Figure 18. Simplified System Diagram

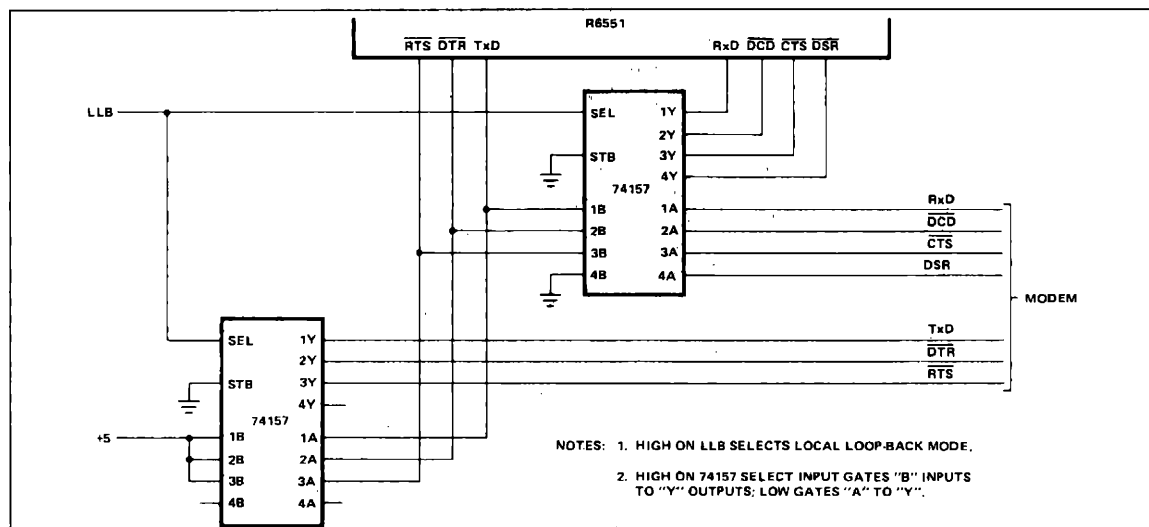


Figure 19. Loop-Back Circuit Schematic

READ TIMING DIAGRAM

Timing diagrams for transmit with external clock, receive with external clock, and $\overline{\text{IRQ}}$ generation are shown in Figures 20, 21 and 22, respectively. The corresponding timing characteristics are listed in Table 3.

Table 3. Transmit/Receive Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	—	400*	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	175	—	ns
Transmit/Receive Clock Low Time	t_{CL}	175	—	175	—	ns
XTLI to TxD Propagation Delay	t_{DD}	—	500	—	500	ns
RTS Propagation Delay	t_{DLY}	—	500	—	500	ns
$\overline{\text{IRQ}}$ Propagation Delay (Clear)	t_{IRQ}	—	500	—	500	ns
Load Capacitance DTR, RTS TxD	C_L	—	130	—	130	pF
		—	30	—	30	pF

Notes:
($t_R, t_F = 10$ to 30 ns)

*The baud rate with external clocking is: $\text{Baud Rate} = \frac{1}{16 \times t_{CCY}}$

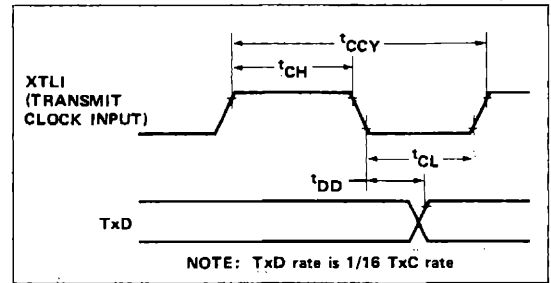


Figure 20. Transmit Timing with External Clock

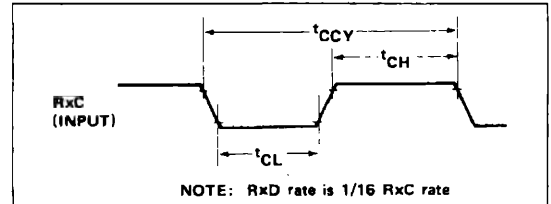


Figure 21. Receive External Clock Timing

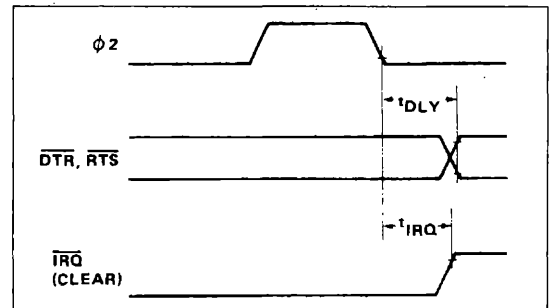


Figure 22. Interrupt and Output Timing

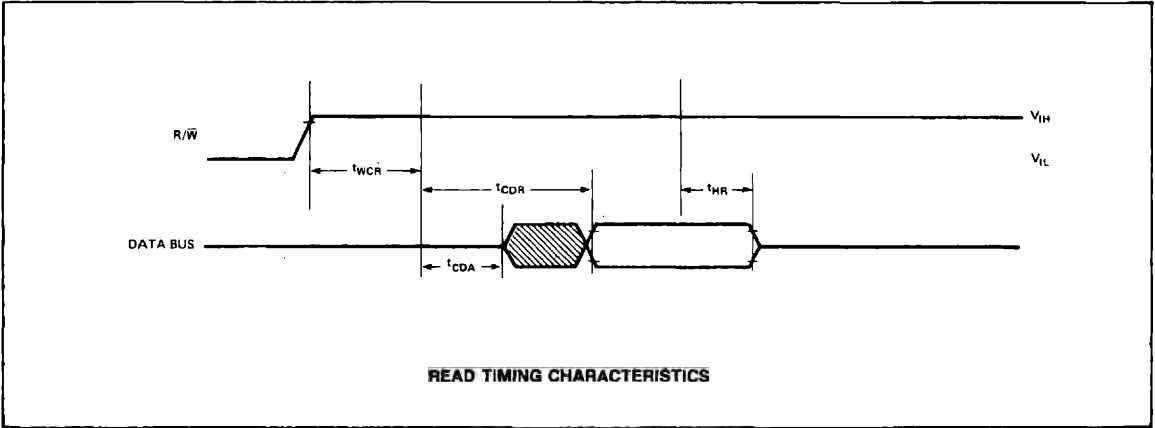
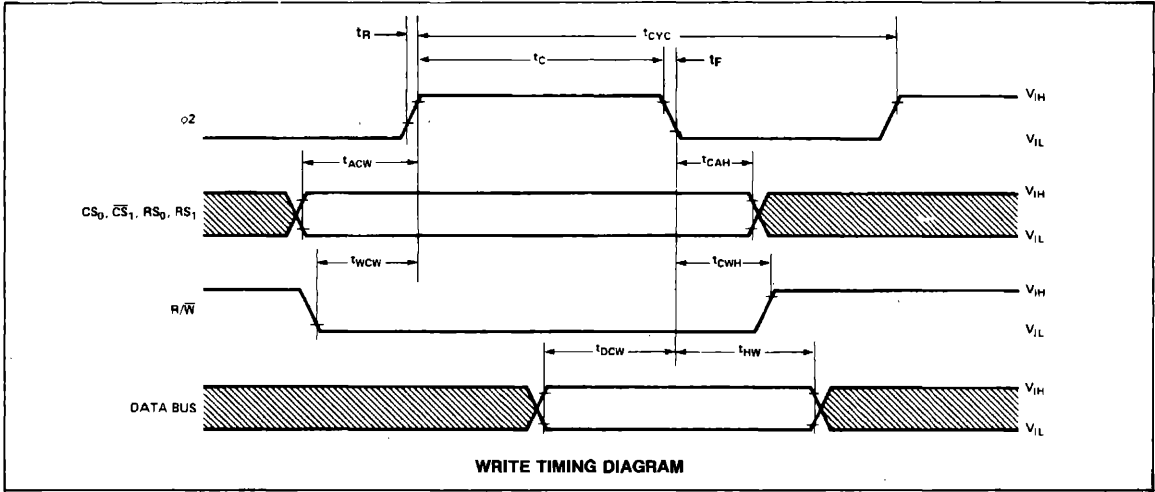
AC CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	t _{CYC}	1.0	40	0.5	40	μs
ø2 Pulse Width	t _C	400	—	200	—	ns
Address Set-Up Time	t _{AC}	120	—	70	—	ns
Address Hold Time	t _{CAH}	0	—	0	—	ns
R/W Set-Up Time	t _{WC}	120	—	70	—	ns
R/W Hold Time	t _{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	t _{DCW}	150	—	60	—	ns
Data Bus Hold Time	t _{HW}	20	—	20	—	ns
Read Access Time (Valid Data)	t _{CDR}	—	200	—	150	ns
Read Hold Time	t _{HR}	20	—	20	—	ns
Bus Active Time (Invalid Data)	t _{CDA}	40	—	40	—	ns

- Notes: 1. V_{CC} = 5.0V ± 5%.
2. T_A = T_L to T_H.
3. t_R and t_F = 10 to 30 ns.
4. D0-D7 load capacitance = 130 pF.

2



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to V_{CC}	Vdc
Output Voltage	V_{OUT}	-0.3 to V_{CC}	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

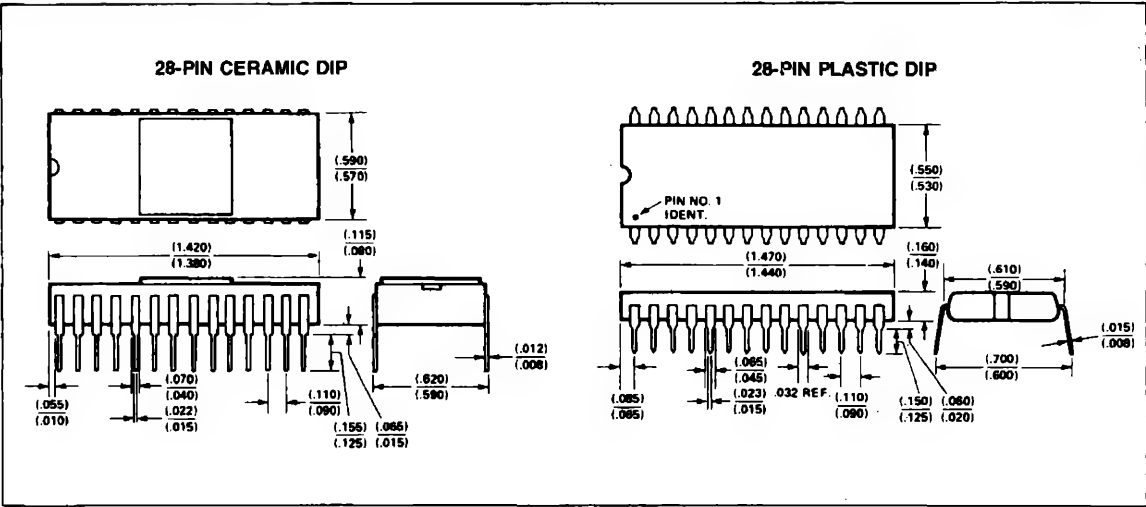
Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V \pm 5%
Temperature Range Commercial Industrial	T_A	0° to 70°C -40°C to +85°C

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0$, $T_A = T_L$ to T_H , unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XT _{LI} and XT _{LO} XT _{LI} and XT _{LO}	V_{IH}	2.0 2.4	— —	V_{CC} V_{CC}	V	
Input Low Voltage Except XT _{LI} and XT _{LO} XT _{LI} and XT _{LO}	V_{IL}	V_{SS} V_{SS}	— —	0.8 0.4	V	
Input Leakage Current Ø2, R/W, RES, CS0, CS1, RS0, RS1, \overline{CTS} , Rx _D , \overline{DCD} , \overline{DSR}	I_{IN}	—	—	2.5	µA	$V_{IN} = 0V$ to 5.25V $V_{CC} = 0V$
Input Leakage Current for High Impedance (Three State Off) D0-D7	I_{TSI}	—	± 2	± 10.0	µA	$V_{IN} = 0.4V$ to 2.4V $V_{CC} = 5.25V$
Output High Voltage D0-D7, Tx _D , Rx _C , \overline{RTS} , \overline{DTR}	V_{OH}	2.4	—	—	V	$I_{LOAD} = -100 \mu A$ $V_{CC} = 4.75V$
Output Low Voltage D0-D7, Tx _D , Rx _C , \overline{RTS} , \overline{DTR} , \overline{IRQ}	V_{OL}	—	—	0.4	V	$V_{CC} = 4.75V$ $I_{LOAD} = 1.6 mA$
Output High Current (Sourcing) D0-D7, Tx _D , Rx _C , \overline{RTS} , \overline{DTR}	I_{OH}	-100	—	—	µA	$V_{OH} = 2.4V$
Output Low Current (Sinking) D0-D7, Tx _D , Rx _C , \overline{RTS} , \overline{DTR} , \overline{IRQ}	I_{OL}	1.6	—	—	mA	$V_{OL} = 0.4V$
Output Leakage Current (off state) \overline{IRQ}	I_{OFF}	—	—	10.0	µA	$V_{OUT} = 5V$
Clock Capacitance (Ø2)	C_{CLK}	—	—	20	pF	$V_{CC} = 5V$ $V_{IN} = 0V$ $f = 1 MHz$ $T_A = 25^\circ C$
Input Capacitance except Ø2	C_{IN}	—	—	10	pF	
Output Capacitance	C_{OUT}	—	—	10	pF	
Power Dissipation	P_D	—	170	300	mW	$T_A = 25^\circ C$

PACKAGE DIMENSIONS





R6565 DOUBLE-DENSITY FLOPPY DISK CONTROLLER (DDFDC)

PRELIMINARY

DESCRIPTION

The R6565 Double-Density Floppy Disk Controller (DDFDC) interfaces up to four floppy disk drives to a 6500/6800 microprocessor-based system. The DDFDC simplifies the system design by minimizing both the number of external hardware components and software steps needed to implement the floppy disk drive (FDD) interface. Control signals supplied by the DDFDC reduce the number of components required in external phase locked loop and write precompensation circuitry. Memory-mapped registers containing commands, status and data simplify the software interface. Built-in functions reduce the software overhead needed to control the FDD interface. The DDFDC supports both the IBM 3740 Single-Density (FM) and IBM System 34 Double-Density (MFM) formats.

The DDFDC interfaces directly to the 6500/6800 synchronous microprocessor bus and operates with 8-bit byte length data transferred on the bus. The DDFDC will operate in either DMA or non-DMA mode. In DMA mode, the CPU need only load the command into the DDFDC and all data transfers occur under DMA control. The R6565 is directly compatible with the MC6844 Direct Memory Access Controller (DMAC). In non-DMA mode, the DDFDC generates an interrupt to the CPU indicating that a byte of data is available.

Controller commands, command or device status, and data are transferred between the DDFDC and the CPU via six internal registers. The Main Status Register (MSR) stores the DDFDC status information while four additional status registers provide result information to the CPU following each controller command. The Data Register (DR) stores actual disk data, parameters, controller commands and FDD status information for use by the CPU.

The R6565 executes 15 separate multi-byte commands:

Read Data	Specify
Write Data	Format a Track
Read Deleted Data	Scan Equal
Write Deleted Data	Scan High or Equal
Read a Track	Scan Low or Equal
Read ID	Sense Interrupt Status
Seek	Sense Drive Status
Recalibrate (Restore to Track 0)	

FEATURES

- Address mark detection circuitry
- Software control of
 - Track stepping rate
 - Head load time
 - Head unload time
- IBM compatible in both single- and double-density recording formats
- Programmable data record lengths: 128, 256, 512, 1024, 2048, 4096 or 8192 bytes/sector
- Multi-sector and multi-track transfer capability
- Controls up to four floppy disk drives
- Data scan capability—will scan a single sector or an entire track of data fields, comparing on a byte-by-byte basis data in the processor's memory with data read from the disk
- Data transfers in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Directly compatible with 6500 and 6800 synchronous microprocessor bus
- Single phase 8 MHz Clock
- Single +5 Volt Power Supply

ORDERING INFORMATION

Part Number	CLK Frequency	Temperature Range
R6565	8 MHz	0°C to 70°C
Package: C = Ceramic P = Plastic		

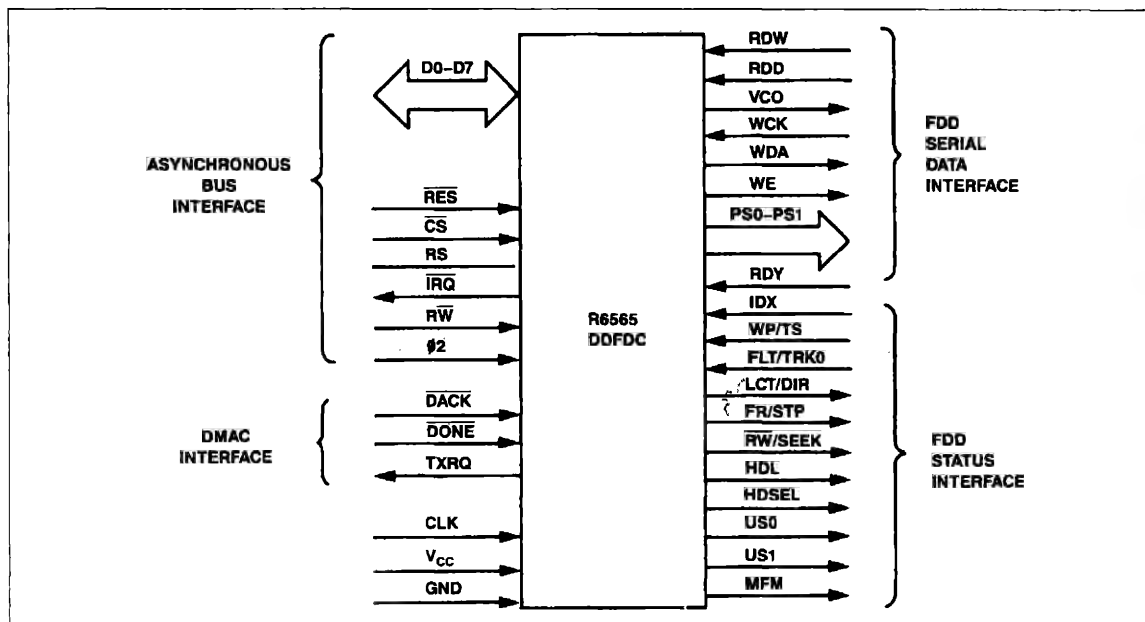


Figure 1. DDFDC Input and Output Signals

PIN DESCRIPTION

Throughout this document signals are presented using the terms active and inactive, or asserted and negated, independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar.

BUS INTERFACE

D0-D7—Data Lines. The bidirectional data lines transfer data between the DDFDC and the 8-bit data bus.

CLK—CLOCK. The clock is a TTL compatible 8 MHz square wave signal.

RES—RESET. This active low input places the DDFDC in the idle state and resets the output lines to the floppy disk drive (FDD) to the low state.

CS—Chip Select. The DDFDC is selected when the CS input is low.

RS—Data/Status Register Select. This input selects the Data or Status Register for reading from or writing to. When RS = high, the Data Register is selected and the state of R/W determines whether it is a read (R/W = high) or a write (R/W = low) operation. When RS = low, the Status Register is selected. This register may only be read (R/W = high); the state R/W = low is invalid when the Status Register is selected.

IRQ—Interrupt Request. This active low output is the interrupt request generated by the DDFDC to the CPU.

R/W—Read/Write. This input defines the data bus transfer as a read or write cycle. When high (read), the data transfer is from the DDFDC to the data bus. When low (write), the data transfer is from the data bus to the DDFDC.

#2—Enable. This input is the synchronous handshake line for the information transfer on the R6500 processor bus. This input signal is the standard enable signal commonly called #2 in R6500 peripheral devices or Enable in 6800 peripheral devices.

DIRECT MEMORY ACCESS CONTROLLER (DMAC) INTERFACE

DACK—DMA Acknowledge. The DMA transfer acknowledge signal is a TTL compatible input generated by the DMA controller (DMAC) controlling the DDFDC. The DMA cycle is active when DACK is low and the DDFDC is performing a DMA transfer.

TXRQ—DMA Request. The transfer request signal is a TTL compatible output generated by the DDFDC to request a data transfer operation under control of the DMAC (in the DMA mode). The request is active when TXRQ = high. The signal is reset inactive when DMA Acknowledge (DACK) is asserted (low).

DONE—DMA Transfer Complete. This input signal is issued to the DDFDC when the DMA transfer for a channel is complete. The signal is active low concurrent with the DACK input when the DMA operation is complete as a result of that transfer.

FDD SERIAL DATA INTERFACE

RDD—Read Data. Read Data input from the floppy disk drive (FDD) containing clock and data bits.

RDW—Read Data Window. Data Window input generated by the Phase Locked Loop (PLL) and used to sample data from the FDD.

VCO—Variable Frequency Oscillator Sync. This output signal inhibits the VCO in the PLL circuit when low and enables the VCO in the PLL circuit when high. This inhibits RDD and RDW from being generated until valid data is detected from the FDD.

WCK—Write Clock. This input clock determines the Write Data rate to the FDD. The data rate is 500 KHz in the FM mode (MFM = low) and 1 MHz in the MFM mode (MFM = high). The pulse width is 250 ns (typical) in both modes.

WDA—Write Data. Serial write data output to the FDD containing both clock and data bits.

WE—Write Enable. This output signal enables the Write Data into the FDD when high.

PS0-PS1—Preshift. These outputs are encoded to convey write compensation status during the MFM mode to determine early, late or normal times as follows:

Write Precompensation Status	Preshift Outputs	
	PS0	PS1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

0 = Low, 1 = High

FDD STATUS INTERFACE

RDY—Ready. An active high input signal indicates the FDD is ready to send data to, or receive data from, the DDFDC.

IDX—Index. An active high input signal from the FDD indicates the index hole is under the index sensor. Index is used to synchronize DDFDC timing.

RW/SEEK—Read Write/Seek. Mode selection signal to the FDD which controls the multiplexer from the multiplexed signals. When RW/SEEK is low, the Read/Write mode is commanded; when RW/SEEK is high, the Seek mode is commanded.

RW/SEEK	Mode	Active FDD Interface Signals
Low	Read/Write	WP, FLT, LCT, FR
High	Seek	TS, TRK0, DIR, STP

WP/TS—Write Protect/Two Side. An active high multiplexed input signal from the FDD. In the Read/Write mode, WP/TS high indicates the media is write-protected. In the Seek mode, WP/TS high indicates the media is two-sided.

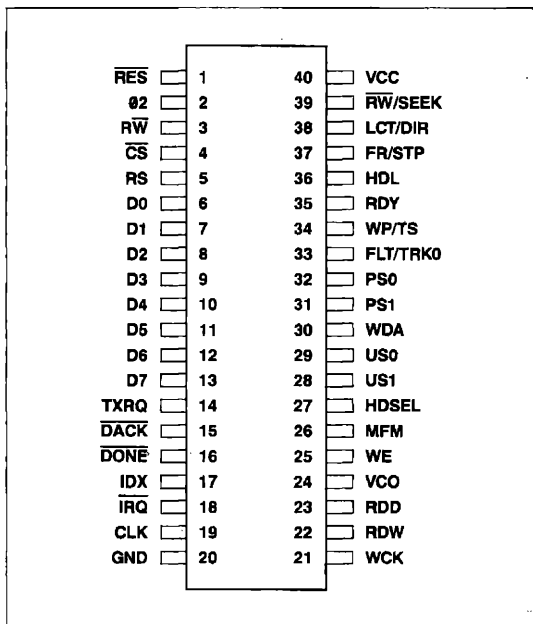
FLT/TRK0—Fault/Track Zero. An active high multiplexed input from the FDD. In the Read/Write mode (RW/SEEK = low), FLT/TRK0 high indicates an FDD fault. In the Seek mode, FLT/TRK0 high indicates that the read/write head is positioned over track zero.

LCT/DIR—Low Current/Direction. A multiplexed output to the FDD. In the Read/Write mode, LCT/DIR is low when the read/write head is to be positioned over the inner tracks and the LCT/DIR is high when the head is to be positioned over the outer tracks. In the Seek mode, LCT/DIR controls the head direction. When LCT/DIR is high, the head steps to the outside of the disk; when LCT/DIR is low, the head steps to the inside of the disk.

FR/STP—Fault Reset/Step. A multiplexed output to the FDD. In the Read/Write mode, FR/STP high resets the fault indicator in the FDD. An FR pulse is issued at the beginning of each read or write command prior to issuing HDL. In the Seek mode, FR/STP provides the step pulses to move the read/write head to another track in the direction indicated by the LCT/DIR signal.

HDL—Head Load. An active high output to notify the FDD that the read/write head should be loaded (placed in contact with the media). A low level indicates the head should be unloaded.

HD—Head Select. An output to the FDD to select the proper read/write head. Head One is selected when HD = high and Head Zero is selected when HD = low.



R6565 DDFDC Pin Diagram

US0-US1—Unit Select. Output signals for floppy disk drive selection as follows:

Unit Select		Floppy Disk Drive Select
US0	US1	
0	0	0
0	1	1
1	0	2
1	1	3

0 = Low, 1 = High

MFM—MFM Mode. Output signal to the FDD to indicate MFM or FM mode. Selects the MFM mode when MFM = high and the FM mode when MFM = low.

VCC—Power. +5V dc.

GND—Ground (V_{SS}).

DDFDC REGISTERS

The DDFDC contains six registers which may be accessed by the processor or DMA controller via the system (i.e., microprocessor) bus: a Main Status Register, a Data Register, and four Result Status Registers. The 8-bit Main Status Register (MSR) contains the status information of the DDFDC, and may be accessed at any time. The 8-bit Data Register, consisting of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, parameters and FDD status information. Bytes of data are read out of, or written into, the Data Register in order to initiate a command or to obtain the results of a command execution.

The read-only Main Status Register facilitates the transfer of data between the system and the DDFDC. The other Status Registers (ST0, ST1, ST2 and ST3) are only available during the result phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

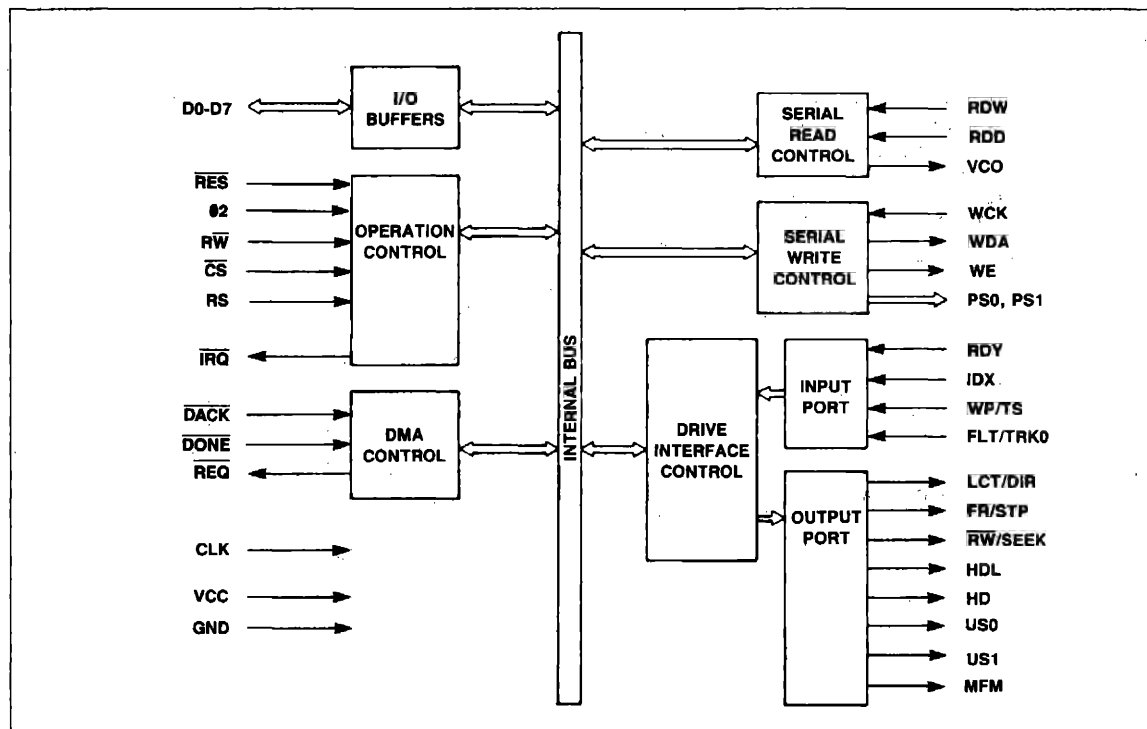


Figure 2. DDFDC Block Diagram

The relationship between the status/data registers and the R/\overline{W} and RS signals is shown below.

RS	R/\overline{W}	Function
0	1	Read Main Status Register
0	0	Illegal
1	1	Read from Data Register
1	0	Write into Data Register
0 = Low, 1 = High		

Table 1 shows each of the status registers used by the DDFDC and each bit assignment within the individual registers. Table 2 defines the symbols used throughout the command definitions. Each register bit symbol is defined in the register descriptions that follow Table 2.

REGISTER DEFINITIONS

Main Status Register (MSR)

7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B

The Main Status Register (MSR) contains the status information of the DDFDC, and must be read by the processor before each byte is written to, or read from, the Data Register during the command or result phase. MSR reads are not required during the execution phase. The Data Input/Output (DIO) and Request for Master (RQM) bits in the MSR indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last R/\overline{W} during command or result phases and the DIO and RQM getting set or reset is 12 μ s. For this reason, every time the MSR is read the processor should wait 12 μ s. The maximum time from the end of the last read in the result phase to when bit 4 (DDFDC Busy) goes low is also 12 μ s.

The DIO and RQM timing chart is shown in Figure 3.

MSR

- 7 RQM —Request for Master.
 0 Data Register is not ready.
 1 Data Register is ready.

MSR

- 6 DIO —Data Input/Output.
 0 Data transfer is from system to the Data Register.
 1 Data transfer is from Data Register to the system.

MSR

- 5 EXM —Execution Mode. (Non-DMA mode only).
 0 Execution phase ended, result phase begun.
 1 Execution phase started.

MSR

- 4 CB —Controller (DDFDC) Busy.
 0 DDFDC is not busy, will accept a command.
 1 DDFDC is busy, will not accept a command.

MSR

- 3 D3B —Floppy Disk Drive (FDD) 3 Busy.
 0 FDD 3 is not busy, DDFDC will accept read or write command.
 1 FDD 3 is busy, DDFDC will not accept read or write command.

MSR

- 2 D2B —FDD 2 Busy.
 0 FDD 2 is not busy, DDFDC will accept read or write command.
 1 FDD 2 is busy, DDFDC will not accept read or write command.

MSR

- 1 D1B —FDD 1 Busy.
 0 FDD 1 is not busy, DDFDC will accept read or write command.
 1 FDD 1 is busy, DDFDC will not accept read or write command.

MSR

- 0 D0B —FDD 0 Busy.
 0 FDD 0 is not busy, DDFDC will accept read or write command.
 1 FDD 0 is busy, DDFDC will not accept read or write command.

Status Register 0 (ST0)

7	6	5	4	3	2	1	0
IC		SE	EC	NR	HD	US	
						US1	US0

The Status Register 0 (ST0) as well as the other status registers (ST1-ST3), are available only during the result phase, and may be read only after completing a command. The particular command executed determines which status registers are used and may be read.

ST0

- 7 6 IC —Interrupt Code.
 0 0 Normal Termination (NT). Command was properly executed and completed.
 0 1 Abnormal Termination (AT). Command execution was started, but was not successfully completed.
 1 0 Invalid Command (IC). Received command was invalid.
 1 1 Abnormal Termination (AT). The Ready (RDY) signal from the FDD changed state during command execution.

ST0

- 5 SE —Seek End.
 0 Seek command is not completed.
 1 Seek command completed by DDFDC.

ST0

- 4 EC —Equipment Check.
 0 No error.
 1 Either a fault signal is received from the FDD or the track 0 signal failed to occur after 256 step pulses (Recalibrate Command).

Table 1. DDFDC Status Register Bit Assignments

Bit Number							
7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B
IC		SE	EC	NR	HD	US	
						US1	US0
EN	0	DE	OR	0	ND	NW	MA
0	CM	DD	WT	SH	SN	BT	MD
FLT	WP	RDY	TRK0	TS	HD	US1	US0

Main Status Register (MSR)

Status Register 0 (ST0)

Status Register 1 (ST1)

Status Register 2 (ST2)

Status Register 3 (ST3)

2

Table 2. Command Symbol Description

Symbol	Name	Description
D	Data	The data pattern which is going to be written into a sector.
D0-D7	Data Bus	8-bit data bus, where D0 is the least significant data line and D7 is the most significant data line.
DTL	Data Length	When N is defined as 00, DTL is the number of data bytes to read from or write into the sector.
EOT	End of Track	The final sector number on a track. During read or write operation, the DDFDC stops data transfer after reading from or writing to the sector equal to EOT.
GPL	Gap Length	The length of Gap 3. During read/write commands this value determines the number of bytes that the VCO will stay low after two CRC bytes. During the Format a Track command it determines the size of Gap 3.
H	Head Address	Head number 0 or 1, as specified in ID field.
HD (H)	Head	A selected head number 0 or 1 which controls the polarity of pin 27. (H = HD in all command words).
HLT	Head Load Time	The head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	The head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	When MF = 0, FM mode is selected; and when MF = 1, MFM mode is selected.
MT	Multi-Track	When MT = 1, a multi-track operation is to be performed. After finishing a read/write operation on side 0, the DDFDC will automatically start searching for sector 1 on side 1.
N	Bytes/Sector	The number of data bytes written in a sector.
ND	Non-DMA Mode	When ND = 1, operation is in the Non-DMA mode; when ND = 0, operation is in the DMA mode.
NTN	New Track Number	A new track number, which will be reached as a result of the Seek command. Desired head position.
PTN	Present Track Number	The track number at the completion of Sense Interrupt Status command. Present head position.
R	Record (Sector)	The sector number to be read or written.
RS	Register Select	Controls selection of Main Status Register (RS = low) or Data Register (RS = high).
R/W	Read/Write	Either read (R) or write (W) signal.
ST	Sectors/Track	The number of sectors per track.
SK	Skip	Skip Deleted Data Address Mark.
SRT	Step Rate Time	The stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by RS = low). ST0-ST3 may be read only after a command has been executed and contain information relevant to that particular command.
STP	Sector Test Process	During a Scan command, if STP = 01, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA controller); and if STP = 02, then alternate sectors are read and compared.
T	Track Number	The current/selected track number of the medium (0-255).
US0,US1	Unit Select	A selected drive number (0-3).

ST0

- 3 NR —Not Ready.
 0 FDD is ready.
 1 FDD is not ready at issue of read or write command. If a read or write command is issued to side 1 of a single-sided drive, this bit is also set.

ST0

- 2 HD —Head Address. (At Interrupt).
 0 Head Select 0.
 1 Head Select 1.

ST0

- 1 0 US —Unit Select. (At Interrupt).
 0 0 FDD 0 selected.
 0 1 FDD 1 selected.
 1 0 FDD 2 selected.
 1 1 FDD 3 selected.

Status Register 1 (ST1)

7	6	5	4	3	2	1	0
EN	0	DE	OR	0	ND	NW	MA

ST1

- 7 EN —End of Track.
 0 No error.
 1 DDFDC attempted to access a sector beyond the last sector of a track.

ST1

- 6 —Not Used. Always Zero.

ST1

- 5 DE —Data Error.
 0 No error.
 1 DDFDC detected a CRC error in ID field or the Data field.

ST1

- 4 OR —Over Run.
 0 No error.
 1 DDFDC was not serviced by the system during data transfers, within a predetermined time interval.

ST1

- 3 —Not Used. Always Zero.

ST1

- 2 ND —No Data.
 0 No error.
 1 3 possible errors.

- DDFDC cannot find sector specified in ID Register during execution of Read Data, Write Deleted Data or Scan commands.
- DDFDC cannot read ID field without an error during Read ID command.
- DDFDC cannot find starting sector during execution of Read a Track command.

ST1

- 1 NW —Not Writable.
 0 No error.
 1 DDFDC detected a write protect signal from FDD during execution of Write Data, Write Deleted Data or Format a Track commands.

ST1

- 0 MA —Missing Address Mark.
 0 No error.
 1 2 possible errors.
- DDFDC cannot detect the ID Address Mark after encountering the index hole twice.
 - DDFDC cannot detect the Data Address Mark or Deleted Data Address Mark. The MD (Missing Address Mark in Data field) of Status Register 2 is also set.

Status Register 2 (ST2)

7	6	5	4	3	2	1	0
0	CM	DD	WT	SH	SN	BT	MD

ST2

- 7 —Not Used. Always Zero.

ST2

- 6 CM —Control Mark.
 0 No error.
 1 DDFDC encountered a sector which contained a Deleted Data Address Mark during execution of a Read Data, Read a Track, or Scan command, or which contained a Data Address Mark during execution of a Read Deleted Data command.

ST2

- 5 DD —Data Error in Data Field.
 0 No error.
 1 DDFDC detected a CRC error in the Data field.

ST2

- 4 WT —Wrong Track.
 0 No error.
 1 Contents of T on the disk is different from that stored in IDR. Bit is related to ND (Bit 2) of Status Register 1.

ST2

- 3 SH —Scan Equal Hit.
 0 No "equal" condition during a scan command.
 1 "Equal" condition satisfied during a scan command.

ST2

- 2 SN —Scan Not Satisfied.
 0 No error.
 1 DDFDC cannot find a sector on the track which meets the scan command condition.

ST2

- 1 **BT** —Bad Track.
 0 No error.
 1 Contents of T on the disk is different from that stored in the IDR and T = FF. Bit is related to ND (Bit 2) of Status Register 1.

ST2

- 0 **MD** —Missing Address Mark in Data Field.
 0 No error.
 1 DDFDC cannot find a Data Address Mark or Deleted Data Address Mark during a data read from the disk.

Status Register 3 (ST3)

7	6	5	4	3	2	1	0
FLT	WP	RDY	TRK0	TS	HD	US1	US0

Status Register 3 (ST3) holds the results of the Sense Drive Status command.

ST3

- 7 **FLT** —Fault.
 0 Fault (FLT) signal from the FDD is low.
 1 Fault (FLT) signal from the FDD is high.

ST3

- 6 **WP** —Write Protect.
 0 Write Protect (WP) signal from the FDD is low.
 1 Write Protect (WP) signal from the FDD is high.

ST3

- 5 **RDY** —Ready.
 0 Ready (RDY) signal from the RDD is low.
 1 Ready (RDY) signal from the FDD is high.

ST3

- 4 **TRK0** —Track 0.
 0 Track 0 (TRK0) signal from the FDD is low.
 1 Track 0 (TRK0) signal is from the FDD is high.

ST3

- 3 **TS** —Two Side.
 0 Two Side (TS) signal from the FDD is low.
 1 Two Side (TS) signal from the FDD is high.

ST3

- 2 **HD** —Head Select.
 0 Head Select (HD) signal to the FDD is low.
 1 Head Select (HD) signal to the FDD is high.

ST3

- 1 **US1** —Unit Select 1.
 0 Unit Select 1 (US1) signal to the FDD is low.
 1 Unit Select 1 (US1) signal to the FDD is high.

ST3

- 0 **US0** —Unit Select 0.
 0 Unit Select 0 (US0) signal to the FDD is low.
 1 Unit Select 0 (US1) signal to the FDD is high.

COMMAND SEQUENCE

The DDFDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer of data from the system. After command execution, the result of the command may be a multi-byte transfer of data back to the system. Because of this multi-byte transfer of information between the DDFDC and the system, each command consists of three phases:

Command Phase—The DDFDC receives all information required to perform a particular operation from the system.

Execution Phase—The DDFDC performs the instructed operation.

Result Phase—After completion of the operation, status and other housekeeping information are made available to the system.

The bytes of data sent to the DDFDC to form a command, and read out of the DDFDC in the result phase, must occur in the order shown for each command sequence. That is, the command code byte must be sent first followed by the other bytes in the specified sequence. All command bytes must be written and all result bytes must be read in each phase. After the last byte of data in the command phase is received by the DDFDC, the execution phase starts. Similarly, when the last byte of data is read out in the result phase, the command is ended and the DDFDC is ready to accept a new command. A command can be terminated by asserting the DONE signal to the DDFDC. This ensures that the processor can always get the DDFDC's attention even if the command in process hangs up in an abnormal manner.

COMMAND DESCRIPTION

READ DATA

A command set of nine bytes places the DDFDC into the Read Data mode. After the Read Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID Address Marks and ID fields from the disk. When the current sector number (R) stored in the ID Register (IDR) matches the sector number read from the disk, the DDFDC transfers data from the disk Data field to the data bus.

After completion of the read operation from the current sector, the DDFDC increments the Sector Number (R) by one, and the data from the next sector is read and output to the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read command terminates after reading the last data byte from sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The Read Data command can also be terminated by a low DONE signal. DONE should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of DONE, the DDFDC stops outputting data to the data bus, but continues to read data from the current sector, checks CRC (Cyclic Redundancy Count) bytes, and then at the end of that sector terminates the Read Data command and sets bits 7 and 6 in ST0 to 0. The amount of data

which can be handled with a single command to the DDFDC depends upon MT (Multi-Track), MF (MFM/FM), and N (Number of Bytes/Sector) values. Table 3 shows the transfer capacity.

The multi-track function (MT) allows the DDFDC to read data from both sides of the disk. For a particular track, data is transferred starting at sector 1, side 0 and completed at sector L, side 1 (sector L = last sector on the side). This function pertains to only one track (the same track) on each side of the disk.

When N = 0 in command byte 6 (FM mode), the Data Length (DTL) in command byte 9 defines the data length that the DDFDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond the DTL is not sent to the data bus. The DDFDC reads (internally) the complete sector, performs the CRC check, and depending upon the manner of command termination, may perform a multi-sector Read operation. When N is non-zero (MFM mode), DTL has no meaning and should be set to FF.

At the completion of the Read Data command, the head is not unloaded until the Head Unload Time (HUT) interval defined in the Specify command has elapsed. The head settling time may be avoided between subsequent reads if the processor issues another command before the head unloads. This time savings is considerable when disk contents are copied from one drive to another.

If the DDFDC detects the Index Hole twice in succession without finding the right sector (indicated in R), then the DDFDC sets the No Data (ND) flag in Status Register 1 (ST1) to a 1, sets Status Register 0 (ST0) bits 7 and 6 to 0 and 1, respectively, and terminates the Read Data command.

After reading the ID and Data fields in each sector, the DDFDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the DDFDC sets the Data Error (DE) flag in ST1 to a 1, sets the Data Error in Data Field (DD) flag in ST2 to a 1 if a CRC error occurs in the Data field, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the DDFDC reads a **Deleted Data Address Mark** from the disk, and the Skip Deleted Data Address Mark bit in the first command byte is not set (SK = 0), then the DDFDC reads all the data in the sector, sets the Control Mark (CM) flag in ST2 to a 1, and terminates the command. If SK = 1, the DDFDC skips the sector with the **Deleted Data Address Mark** and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers from the DDFDC to the system, the DDFDC must be serviced by the system within 27 μ s in the FM mode, and within 13 μ s in the MFM mode, otherwise the DDFDC sets the Over Run (OR) flag in ST1 to a 1, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the processor terminates a read (or write) operation in the DDFDC, then the ID information in the result phase is dependent upon the state of the MT bit in the first command byte and the End of Track (EOT) byte. Table 4 shows the values for Track Number (T), Head Number (H), Sector Number (R), and Number of Data Bytes/Sector (N), when the processor terminates the command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	0	1	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Table 3. DDFDC Transfer Capacity

Multi-Track (MT)	MFM/FM (MF)	Bytes/Sector (N)	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Disk
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 4. DDFDC Command Termination Values

Command Phase ID		Final Sector Transferred to/from Data Bus	Result Phase ID			
Multi-Track (MT)	Head Number (HD)		Track Number (T)	Head Number (H)	Sector Number (R)	No. of Data Bytes (N)
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	T + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	LSB	01	NC

Notes:

1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DATA

A command set of nine bytes places the DDFDC in the Write Data mode. After the Write Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID fields from the disk. When the four bytes (T, H, R, N) loaded during the command match the four bytes of the ID field from the disk, the DDFDC transfers data from the data bus to the disk Data field.

After writing data into the current sector, the DDFDC increments the sector number (R) by one, and writes into the Data field in the next sector. The DDFDC continues this multi-sector write operation until the last byte is written to sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The command can also be terminated by a low on DONE. If DONE is sent to the DDFDC while writing into the current sector, then the remainder of the Data field is filled with 00 (zeros). In this case, ST0 bits 7 and 6 are set to 0 and the command is terminated.

The DDFDC reads the ID field of each sector and checks the CRC bytes. If the DDFDC detects a read error (incorrect CRC) in one

of the ID fields, it terminates the Write Data command, sets the DE flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

The Write Data command operates in much the same manner as the Read Data command. Refer to the Read Data command for the handling of the following items:

- Transfer Capacity
- End of Track (EN) flag
- No Data (ND) flag
- Head Unload Time (HUT) interval
- ID information when the processor terminates command (see Table 4)
- Definition of Data Length (DTL) when N = 0 and when N ≠ 0

In the Write Data mode, data transfers from the data bus to the DDFDC must occur within 27 μs in the FM mode, and within 13 μs in the MFM mode. If the time interval between data transfers is longer than this, then the DDFDC terminates the Write Data command, sets the Over Run (OR) flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	0	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DELETED DATA

The Write Deleted Data command is the same as the Write Data command except a Deleted Data Address Mark is written at the beginning of the Data field instead of the normal Data Address Mark.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ DELETED DATA

The Read Deleted Data command is the same as the Read Data command except that if SK = 0 when the DDFDC detects a **Data Address Mark** at the beginning of a Data field, it reads all the data in the sector and sets the CM flag in ST2 to a 1, and then terminates the command. If SK = 1, then the DDFDC skips the sector with the **Data Address Mark** and reads the next sector.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	1	1	0	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ A TRACK

The Read a Track command is similar to the Read Data command except that this is a continuous read operation where all Data fields from each of the sectors on a track are read and transferred to the data bus. Immediately after encountering the Index Hole, the DDFDC starts reading the Data fields as continuous blocks of data. This command terminates when the number of sectors read is equal to EOT. Multi-track operations are not allowed with this command.

If the DDFDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The DDFDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag in ST1 to a 1 if there is no match.

If the DDFDC does not find an ID Address Mark on the disk after it encounters the Index Hole for the second time it terminates the command, sets the Missing Address Mark (MA) flag in ST1 to a 1, and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	SK	0	0	0	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ ID

The two-byte Read ID command returns the present position of the read/write head. The DDFDC obtains the value from the first ID field it is able to read, sets bits 7 and 6 in ST0 to 0 and terminates the command.

If no proper ID Address Mark is found on the disk before the Index Hole is encountered for the second time then the Missing Address Mark (MA) flag in ST1 is set to a 1, and if no data is found then the ND flag in ST1 is also set to a 1. Bits 7 and 6 in ST0 are set to 0 and 1, respectively and the command is terminated.

During this command there is no data transfer between DDFDC and the data bus except during the result phase.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	0	1	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

FORMAT A TRACK

The six-byte Format a Track command formats an entire track. After the Index Hole is detected, data is written on the disk: Gaps, Address Marks, ID fields and Data fields; all are recorded in either the double-density IBM System 34 format (MF = 1) or the single-density IBM 3740 format (MF = 0). The particular format written is also controlled by the values of Number of Bytes/Sector (N), Sectors/Track (ST), Gap Length (GPL) and Data Pattern (D) which are supplied by the processor during the command phase. The Data field is filled with the data pattern stored in D.

The ID field for each sector is supplied by the processor in response to four data requests per sector issued by the DDFDC. The type of data request depends upon the Non-DMA flag (ND) in the Specify command. In the DMA mode (ND = 0), the DDFDC asserts the DMA Request (TXRQ) output four times per sector. In the Non-DMA mode (ND = 1), the DDFDC asserts Interrupt Request (IRQ) output four times per sector.

The processor must write one data byte in response to each request, sending (in the consecutive order) the Track Number (T), Head Number (H), Sector Number (R) and Number of Bytes/Sector (N). This allows the disk to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for T, H, R, and N to the DDFDC for each sector on the track. For sequential formatting R is incremented by one after each sector is formatted, thus, R contains the total numbers of sectors formatted when it is read during the result phase. This incrementing and formatting continues for the whole track until the DDFDC, upon encountering the Index Hole for the second time, terminates the command and sets bits 7 and 6 in ST0 to 0.

If the Fault (FLT) signal is high from the FDD at the end of a write operation, the DDFDC sets the Equipment Check (EC) flag in ST0 to a 1, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command. Also, a low (RDY) signal at the beginning of a command execution phase causes bits 7 and 6 of ST0 to be set to 0 and 1, respectively.

Table 5 shows the relationship between N, ST, and GPL for various disk and sector sizes.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Number of Bytes per Sector (N)							
	4	Sectors per Track (ST)							
	5	Gap Length (GPL)							
	6	Data Pattern (D)							

Table 5. Standard Floppy Disk Sector Size Relationship

Disk Size	Mode	Sector Size Bytes/Sector	No. of Data Bytes/Sector (N)	No. of Sectors/Tracks (ST)	Gap Length (GPL) ⁴		Remarks
					Read/Write Command ¹	Format Command ²	
8"	FM	128	00	1A	07	1B	IBM Disk 1
		256	01	0F	0E	2A	IBM Disk 2
		512	02	08	1B	3A	
		1024	03	04	47	8A	
		2048	04	02	C8	FF-	
		4096	05	01	C8	FF	
	MFM ³	256	01	1A	0E	36	IBM Disk 2D
		512	02	0F	1B	54	
		1024	03	08	35	74	IBM Disk 2D
		2048	04	04	99	FF	
		4096	05	02	C8	FF	
		8192	06	01	C8	FF	
5¼"	FM	128	00	12	07	09	
		128	00	10	10	19	
		256	01	08	18	30	
		512	02	04	46	87	
		1024	03	02	C8	FF	
		2048	04	01	C8	FF	
	MFM ³	256	01	12	0A	0C	
		256	01	10	20	32	
		512	02	08	2A	50	
		1024	03	04	80	F0	
		2048	04	02	C8	FF	
		4096	05	01	C8	FF	

Notes:

1. Suggested values of GPL in Read or Write Commands to avoid overlapping between Data field and ID field of contiguous sections.
2. Suggested values of GPL in Format a Track command.
3. In MFM mode the DDFDC cannot perform a read/write/format operation with 128 bytes/sector (N = 00).
4. Values of ST and GPL are in hexadecimal.

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)*
	5	Head Number (H)*
	6	Sector Number (R)*
	7	Number of Data Bytes per Sector (N)*

* The ID information has no meaning in this command.

the sector number is incremented ($R + STP - R$), and the scan operation is continued. The scan operation continues until one of the following events occur: the conditions for scan are met (equal, low or equal, or high or equal), the last sector on the track is reached (EOT), or **DONE** is received.

If conditions for scan are met, the DDFDC sets the Scan Hit (SH) flag in ST2 to a 1, and terminates the command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the track (EOT), then the DDFDC sets the Scan Not Satisfied (SN) flag in ST2 to a 1, and terminates the command. The receipt of **DONE** from the processor or DMA controller during the scan operation will cause the DDFDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6 shows the status of bits SH and SN under various conditions of scan.

SCAN COMMANDS

The scan commands compare data read from the disk to data supplied from the data bus. The DDFDC compares the data, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{BUS}$, $D_{FDD} \leq D_{BUS}$, or $D_{FDD} \geq D_{BUS}$ (D = the data pattern in hexadecimal). A magnitude comparison is performed (FF = largest number, 00 = smallest number). The hexadecimal byte of FF either from the bus or from FDD can be used as a mask byte because it always meets the condition of the compare. After a whole sector of data is compared, if the conditions are not met,

If $SK = 0$ and the DDFDC encounters a Deleted Data Address Mark on one of the sectors, it regards that sector as the last sector of the track, sets the Control Mark (CM) bit in ST2 to a 1 and terminates the command. If $SK = 1$, the DDFDC skips the sector with the Deleted Data Address Mark, sets the CM flag to a 1 in order to show that a Deleted Sector has been encountered, and reads the next sector.

Table 6. Scan Status Codes

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{BUS}$
	1	0	$D_{FDD} \neq D_{BUS}$
Scan Low or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} < D_{BUS}$
	1	0	$D_{FDD} > D_{BUS}$
Scan High or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} > D_{BUS}$
	1	0	$D_{FDD} < D_{BUS}$

When either the STP sectors are read (contiguous sectors = 01, or alternate sectors = 02) or MT (Multi-Track) is set, the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and the scan command starts reading at sector 21. Sectors 21, 23, and 25 are read, then the next sector (26) is skipped and the Index Hole is encountered before the EOT value of 26 can be read. This results in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the scan command would be completed in a normal manner.

During a scan command data is supplied from the data bus for comparison against the data read from the disk. In order to avoid having the Over Run (OR) flag set in ST1, data must be available from the data bus in less than 27 μ s (FM mode) or 13 μ s (MFM mode). If an OR occurs, the DDFDC terminates the command and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

The following tables specify the command bytes and describe the result bytes for the three scan commands.

SCAN EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	0	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN LOW OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN HIGH OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SEEK

The three-byte Seek command steps the FDD read/write head from track to track. The DDFDC has two independent Present Track Registers for each drive. They are cleared only by the Recalibrate command. The DDFDC compares the Present Track Number (PTN) which is the current head position with the New Track Number (NTN), and if there is a difference, performs the following operation:

If PTN < NTN: Sets the direction output (LCT/DIR) high and issues step pulses (FR/STP) to the FDD to cause the read/write head to step in.

If PTN > NTN: Sets the direction output (LCT/DIR) low and issues step pulses to the FDD to cause the read/write head to step out.

The rate at which step pulses are issued is controlled by the Step Rate Time (SRT) in the Specify command. After each step pulse is issued, NTN is compared against PTN. When NTN = PTN, then the Seek End (SE) flag in ST0 is set to a 1, bits 7 and 6 in ST0 are set to 0, and the command is terminated. At this point DDFDC asserts IRQ.

The FDD Busy flag (bit 0-3) in the Main Status Register (MSR) corresponding to the FDD performing the Seek operation is set to a 1.

After command termination, all FDD Busy bits set are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the DDFDC sets the Controller Busy (CB) flag in the MSR to 1; but during the execution phase the CB flag is set to 0 to indicate DDFDC non-busy. While the DDFDC is in the non-busy state, another Seek command may be issued, and in this manner parallel seek operations may be performed on all drives at once.

No command other than Seek will be accepted while the DDFDC is sending step pulses to any FDD. If a different command type is attempted, the DDFDC will set bits 7 and 6 in ST0 to a 1 and 0, respectively, to indicate an invalid command.

If the FDD is in a not ready state at the beginning of the command execution phase or during the seek operation, then the DDFDC sets the Not Ready (NR) flag in ST0 to a 1, sets ST0 bits 7 and 6 to 0 and 1, respectively, and terminates the command.

If the time to write the three bytes of the Seek command exceeds 150 μ s, the time between the first two step pulses may be shorter than the Step Rate Time (SRT) defined by the Specify command by as much as 1 ms.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	1	1	1
	2	X	X	X	X	X	0	US1	US0
	3	New Track Number (NTN)							

Result Phase: None.

RECALIBRATE

This two-byte command retracts the FDD read/write head to the Track 0 position. The DDFDC clears the contents of the PTN counters, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal (TRK0) is low, the direction signal (LCT/DIR) output remains low and step pulses are issued on FR/STP. When TRK0 goes high the DDFDC sets the Seek End (SE) flag in ST0 to a 1 and terminates the command. If the TRK0 is still low after 256 step pulses have been issued, the DDFDC sets Seek End (SE) and Equipment Check (EC) flags in ST0 to 1s, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the RDY signal, as described in the Seek command, also applies to the Recalibrate command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	1	1
	2	X	X	X	X	X	0	US1	US0

Result Phase: None.

SENSE INTERRUPT STATUS

Interrupt Request ($\overline{\text{IRQ}}$) is asserted by the DDFDC when any of the following conditions occur:

- Upon entering the result phase of:
 - Read Data command
 - Read a Track command
 - Read ID command
 - Read Deleted Data command
 - Write Data command
 - Format a Track command
 - Write Deleted Data command
 - Scan commands
- Ready (RDY) line from the FDD changes state
- Seek or Recalibrate command termination
- During execution phase in the Non-DMA mode

$\overline{\text{IRQ}}$ caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in Non-DMA mode, bit 5 in the MSR is set to 1. Upon entering result phase this bit is set to 0. Reasons 1 and 4 do not require the Sense Interrupt Status command. The interrupt is cleared by reading or writing data to DDFDC. Interrupts caused by reasons 2 and 3 are identified with the aid of the Sense Interrupt Status command. This command resets $\overline{\text{IRQ}}$ and sets/resets bits 5, 6, and 7 of ST0 to identify the cause of the interrupt. Table 7 defines the seek and interrupt codes.

Neither the Seek or Recalibrate command has a result phase. Therefore, it is mandatory to use the Sense Interrupt Status command after these commands to effectively terminate them and to verify where the head is positioned by checking the Present Track Number (PTN).

Issuing a Sense Interrupt Status command without an interrupt pending is treated as an invalid command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	0	0	0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Present Track Number (PTN)

SPECIFY

The three-byte Specify command sets the initial values for each of the three internal timers. The Head Unload Time (HUT) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (1 = 16 ms, 2 = 32 ms, . . . F = 240 ms).

The Step Rate Time (SRT) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, . . . 0 = 16 ms).

The Head Load Time (HLT) defines the time between the Head Load (HDL) signal going high and the start of the read/write operation. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms, . . . 7F = 254 ms).

The time intervals are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock. If the clock is reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of two.

The choice of DMA or Non-DMA operation is made by the Non-DMA mode (ND) bit. When this bit = 1 the Non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	0	1	1
	2	SRT				HUT			
	3	HLT							ND

SRT — Step Rate Time
 HUT — Head Unload Time
 HLT — Head Load Time
 ND — Non-DMA mode

Result Phase: None.

Table 7. ST0 Seek and Interrupt Code Definition for Sense Interrupt Status

Status Register 0 (ST0) Bits			
Interrupt Code (IC)		Seek End (SE)	Cause
7	6	5	
1	1	0	
0	0	1	
0	1	1	

SENSE DRIVE STATUS

This two-byte command obtains and reports the status of the FDDs. Status Register 3 (ST3) is returned in the result phase and contains the drive status.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	0	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 3 (ST3)
---	---	-------------------------

INVALID COMMAND

If an invalid command (i.e., a command not previously defined) is received by the DDFDC, then the DDFDC terminates the command after setting bits 7 and 6 of ST0 to 1 and 0, respectively. The DDFDC does not generate an interrupt during this condition. Bits 6 and 7 (DIO and RQM) in the MSR are both set to a 1 indicating to the processor that the DDFDC is in the result phase and that ST0 must be read. A hex 80 in ST0 indicates that an invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt, otherwise the DDFDC considers the next command to be an invalid command.

In some applications the user may wish to use this command as a No-Op command, to place the DDFDC in a standby or no operation state.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	Invalid Codes							

Result Phase:

R	1	Status Register 0 (ST0) = 80
---	---	------------------------------

PROCESSOR INTERFACE

During the command or result phases, the Main Status Register (MSR) must be read by the processor before each byte of information is transferred to, or from, the DDFDC Data Register. After each byte of data is written to, or read from, the Data Register, the processor should wait 12 μ s before reading the MSR. Bits 6 and 7 in the MSR must be a 0 and 1, respectively, before each command byte can be written to the DDFDC. During the result phase, bits 6 and 7 of the MSR must both be 1s prior to reading each byte from the Data Register onto the data bus. Note that this status reading of bits 6 and 7 of the MSR before each byte transfer to and from the DDFDC is required in only the command and result phases and not during the execution phase.

During the result phase all bytes shown in the result phase must be read by the processor. The Read Data command, for example, has seven bytes of data in the result phase. All seven bytes must be read to successfully complete the Read Data command. The DDFDC will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

INTERRUPT REQUEST MODE

During the execution phase, the MSR need not be read. The receipt of each data byte from the FDD is indicated by $\overline{\text{IRQ}}$ low on pin 18. When the DDFDC is in Non-DMA mode, $\overline{\text{IRQ}}$ is asserted during the execution phase. When the DDFDC is in the DMA mode, the $\overline{\text{IRQ}}$ is asserted at the result phase. The $\overline{\text{IRQ}}$ signal is reset by a read (R/W high) or write (R/W low) of data to the DDFDC. A further explanation of the $\overline{\text{IRQ}}$ signal is described in the Sense Interrupt Status command on page 16. If the system cannot handle interrupts fast enough (within 13 μ s for MFM mode or 27 μ s for FM mode), it should poll bit 7 (RQM) in the MSR. In this case, RQM in the MSR functions as an Interrupt Request ($\overline{\text{IRQ}}$). If the RQM bit is not set, the Over Run (OR) flag in ST1 will be set to a 1 and bits 7 and 6 of ST0 will be set to a 0 and 1, respectively.

DMA MODE

When the DDFDC is in the DMA mode (ND = 0 in the third command byte of the Specify command), TXRQ (DMA Request) is asserted during the execution phase (rather than $\overline{\text{IRQ}}$) to request the transfer of a data byte between the data bus and the DDFDC.

During a read command, the DDFDC asserts TXRQ as each byte of data is available to be read. The DMA controller responds to this request with DACK low (DMA Acknowledge) and R/W high (read). When DACK goes low the DMA Request is reset (TXRQ low). After the execution phase has been completed (DONE low or the EOT sector is read), $\overline{\text{IRQ}}$ is asserted to indicate the start of the result phase. When the first byte of data is read during the result phase, $\overline{\text{IRQ}}$ is reset high.

During a write command, the DDFDC asserts TXRQ as each byte of data is required. The DMA controller responds to this request with DACK low (DMA Acknowledge) and R/W low (write). When DACK goes low the DMA Request is reset (TXRQ low). After the execution phase has been completed (DONE low or the EOT sector is written), $\overline{\text{IRQ}}$ is asserted. This signals the beginning of the result phase. When the first byte of data is read during the result phase, the $\overline{\text{IRQ}}$ is reset high.

FDD POLLING

After the Specify command has been received by the DDFDC, the Unit Select lines (US0 and US1) begin the polling mode. Between commands (and between step pulses in the Seek Command) the DDFDC polls all the FDD's looking for a change in the RDY line from any of the drives. If the RDY line changes state (usually due to the door opening or closing) then the DDFDC asserts $\overline{\text{IRQ}}$. When Status Register 0 (ST0) is read (after Sense Interrupt Status command is issued), Not Ready (NR = 1) will be indicated. The polling of the RDY line by the DDFDC occurs continuously between commands, thus notifying the processor which drives are on- or off-line. Each drive is polled every 1.024 ms except during read/write commands.

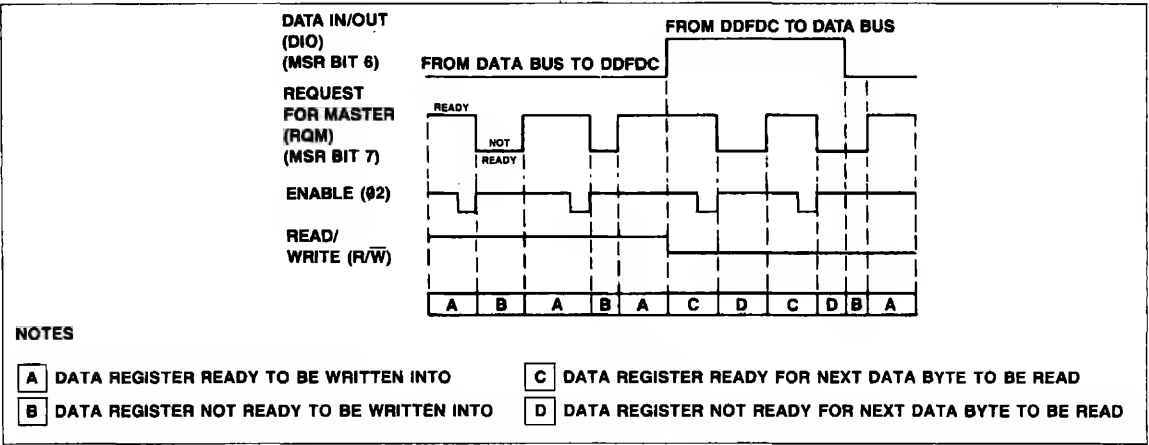


Figure 3. DDFDC and System Data Transfer Timing

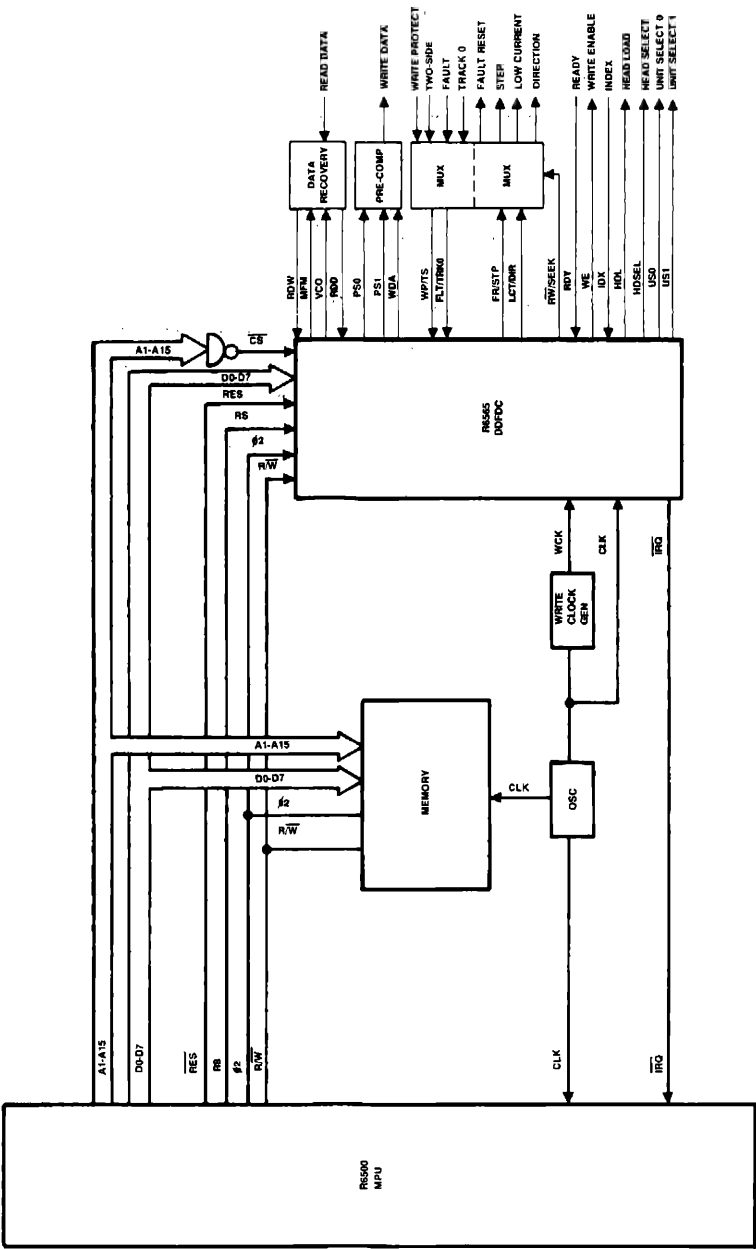


Figure 4. R6565 DDFDC Interface to R6500

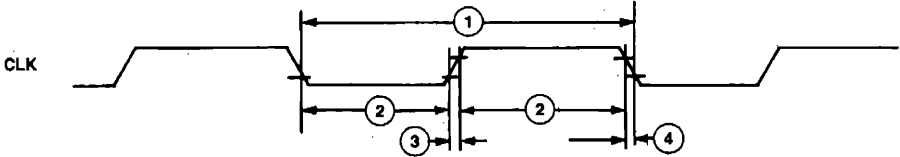


Figure 5. Clock Timing

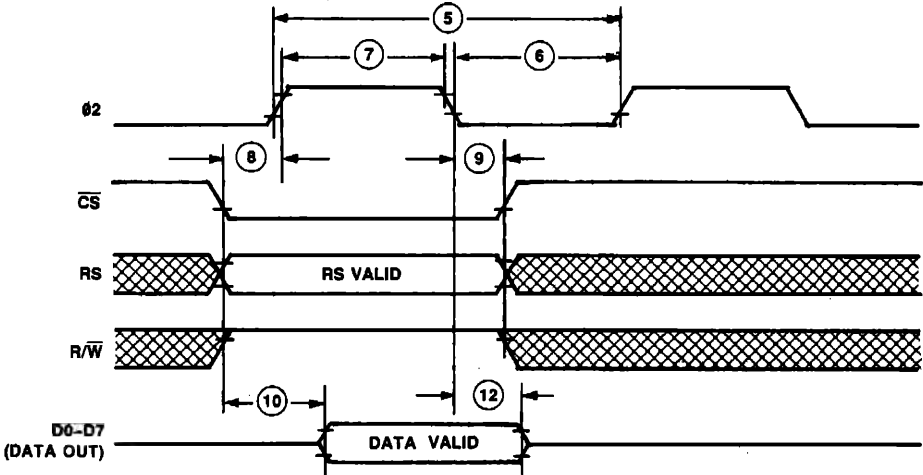


Figure 6. Read Cycle Timing

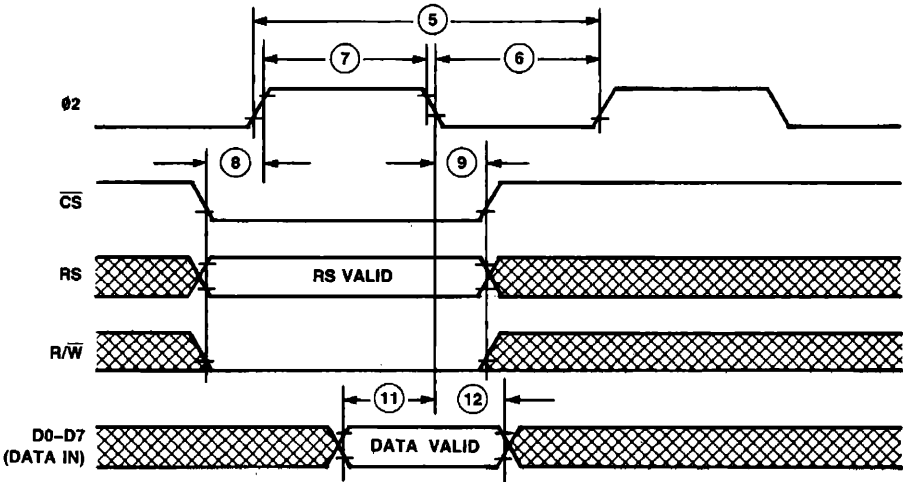


Figure 7. Write Cycle Timing

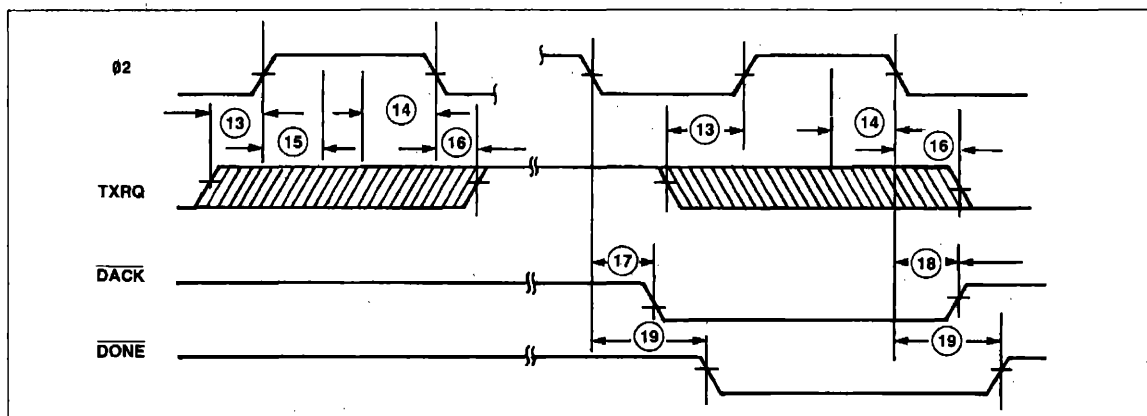


Figure 8. DMA Operation Timing

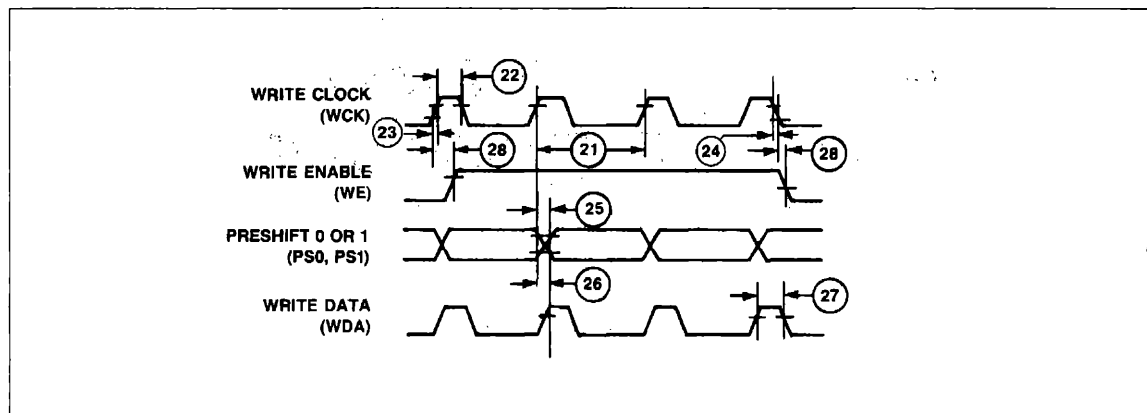


Figure 9. FDD Write Operation Timing

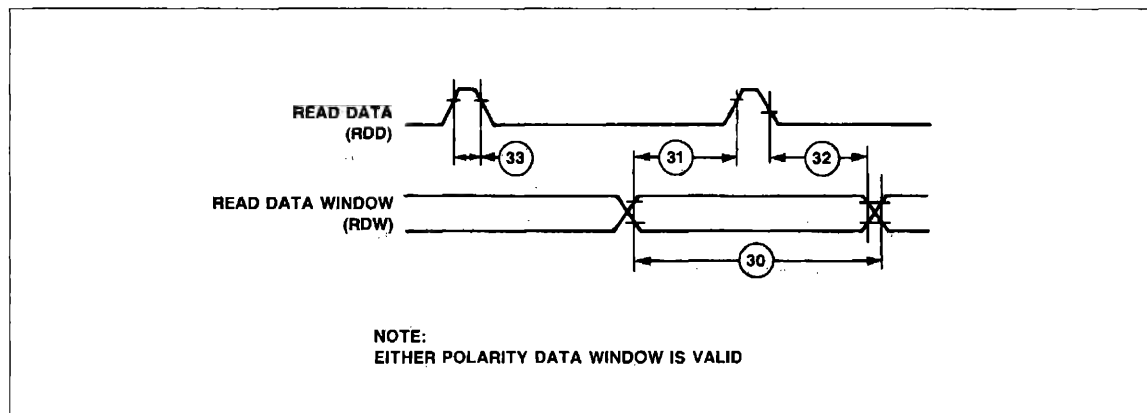


Figure 10. FDD Read Operation Timing

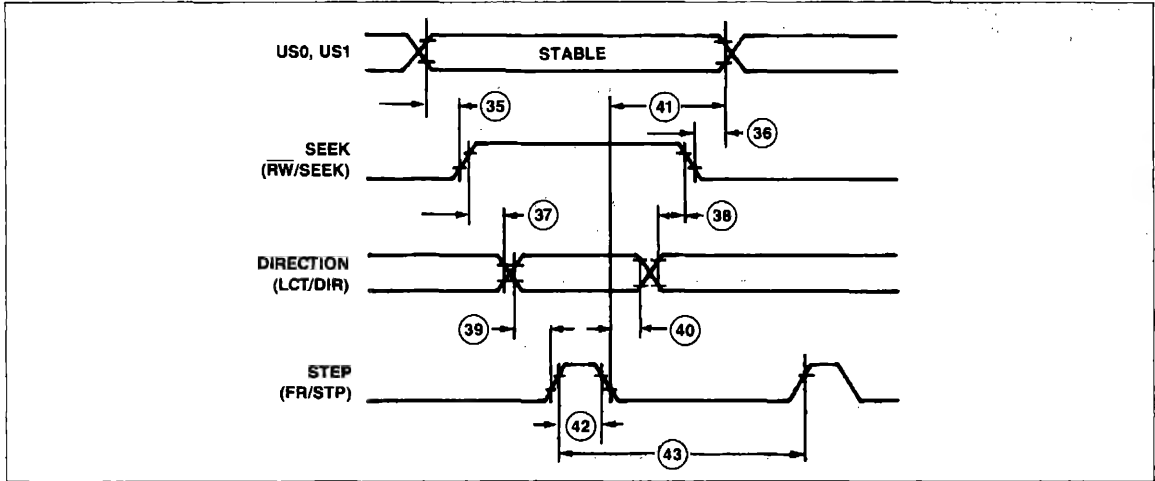


Figure 11. Seek Operation Timing

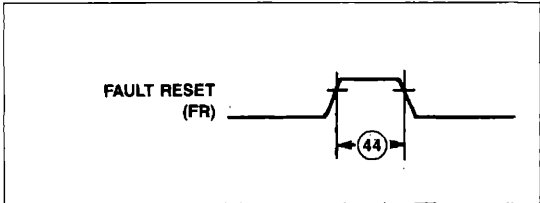


Figure 12. Fault Reset Timing

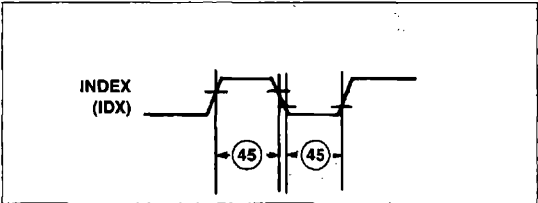


Figure 13. Index Timing

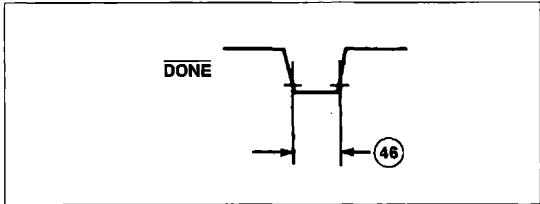


Figure 14. DONE Timing

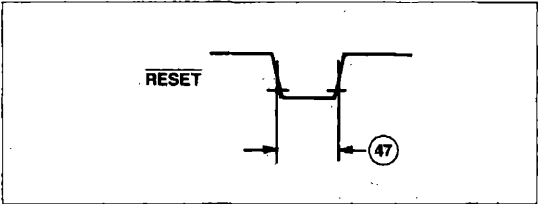


Figure 15. RESET Timing

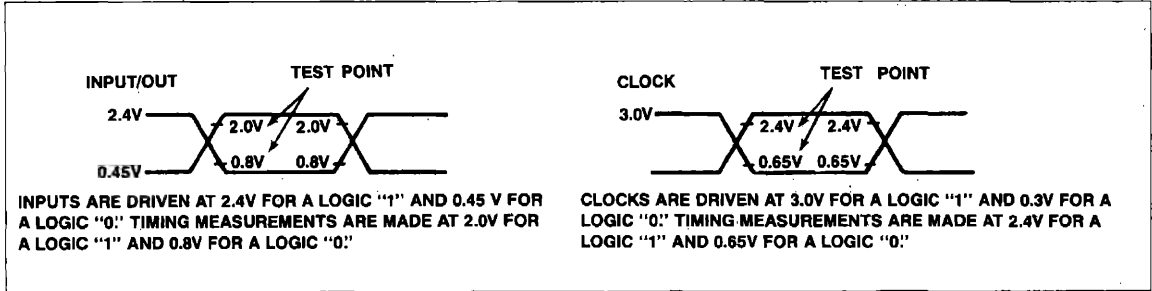


Figure 16. AC Timing Measurement Conditions

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Ref. Fig.	No.	Characteristic	Symbol	Alt. Sym.	Min.	Typ.	Max.	Unit	Test Conditions
5	1	Clock Period	t _{cy}	φ _{cy}	120	125	500	ns	CLK = 8 MHz
	2	Clock High, Low Width	t _{CA}	φ ₀	80	125	—	ns	
	3	Clock Rise Time	t _{CLCH}	φ _r	—	—	—	ns	
	4	Clock Fall Time	t _{CHCL}	φ _f	—	—	—	ns	
6 & 7	5	Ø2 Clock Cycle Time	t _{CCY}	t _{2CY}	500	—	—	ns	C _L = 100 pF
	6	Ø2 Clock Low	t _{CL}	t _{2CL}	210	—	—	ns	
	7	Ø2 Clock High	t _{CH}	t _{2CH}	220	—	—	ns	
	8	Address Setup Time	t _{AVCH}	t _{AS}	70	—	—	ns	
	9	Address Hold Time	t _{CLAX}	t _{AH}	10	—	—	ns	
	10	Data Access Time	t _{AVDX}	t _{ACC}	—	—	250	ns	
	11	Data Setup Time	t _{DVCL}	t _{DS}	60	—	—	ns	
12	12	Data Hold	t _{AXDX}	t _{DH}	10	—	—	ns	
8	13	TXRQ Setup to Ø2 High	t _{TVCH}	t _{TSH}	120	—	—	ns	CLK = 8 MHz
	14	TXRQ Setup to Ø2 Low	t _{TVCL}	t _{TSL}	210	—	—	ns	
	15	TXRQ Hold from Ø2 High	t _{CHTX}	t _{THH}	10	—	—	ns	
	16	TXRQ Hold from Ø2 Low	t _{CLTX}	t _{THL}	10	—	—	ns	
	17	DACK Delay Time	t _{CLAL}	t _{AD}	—	—	150	ns	
	18	DACK Hold Time	t _{CLAH}	t _{AH}	30	—	—	µs	
	19	DONE Delay Time	t _{CLDL}	t _{DD}	—	—	210	µs	
9	21	WCK Cycle Time	t _{WCY}	t _{cy}	—	note 1	—	µs	CLK = 8 MHz
	22	WCK High Width	t _{KHKL}	t ₀	80	250	350	ns	
	23	WCK Rise Time	t _{KUKH}	t _r	—	—	20	ns	
	24	WCK Fall Time	t _{KHKL}	t _f	—	—	20	ns	
	25	WCK High to PS0, PS1 Valid (Delay)	t _{KHPV}	t _{CP}	20	—	100	ns	
	26	PS0, PS1 Valid to WDA High (Delay)	t _{PVDH}	t _{CD}	20	—	100	ns	
	27	WDA High Width	t _{DHDL}	t _{WDD}	t _{WCH} - 50	—	—	ns	
	28	WE High to WCK High or WE Low to WCK Low	t _{EHKH}	t _{WE}	20	—	100	ns	
10	30	RDW Cycle Time	t _{WCY}	t _{wcy}	—	note 2	—	µs	CLK = 8 MHz
	31	RDW Valid to RDD High (Setup)	t _{WVRH}	t _{WRD}	15	—	—	ns	
	32	RDD Low to RDW Invalid (Hold)	t _{RLWI}	t _{RDW}	15	—	—	ns	
	33	RDD High Width	t _{RHRL}	t _{RDD}	40	—	—	ns	
	35	US0, US1 Valid to SEEK High (Setup)	t _{UVSH}	t _{US}	12	—	—	µs	
11	36	SEEK Low to US0, US1 Invalid (Hold)	t _{SLUI}	t _{SU}	15	—	—	µs	CLK = 8 MHz
	37	SEEK High to DIR Valid (Setup)	t _{SHDV}	t _{SD}	7	—	—	µs	
	38	DIR Invalid to SEEK Low (Hold)	t _{DXSL}	t _{DS}	30	—	—	µs	
	39	DIR Valid to STP High (Setup)	t _{DVTH}	t _{DST}	1	—	—	µs	
	40	STP Low to DIR Invalid (Hold)	t _{TLDX}	t _{STD}	24	—	—	µs	
	41	STP Low to US0, US1 Invalid (Hold)	t _{TLUX}	t _{STU}	5	—	—	µs	
	42	STP High Width	t _{HTHL}	t _{STP}	6	7	—	µs	
	43	STP Cycle Time	t _{TCY}	t _{SC}	33 ³	—	note 3	µs	
12	44	FR High Width	t _{FHFL}	t _{FR}	8	—	10	µs	
13	45	IDX High Width	t _{IHIL}	t _{IDX}	10	—	—	t _{cy}	
14	46	DONE Low Width	t _{HTL}	t _{TC}	1	—	—	t _{cy}	
15	47	RES Low Width	t _{RHRL}	t _{AST}	14	—	—	t _{cy}	

Notes:

1.	MFM	Mini	Standard
	0	4 µs	2 µs
	1	2 µs	1 µs

2. For MFM = 0: Typ. = 2 µs

For MFM = 1: Typ. = 1 µs

3. t_{SC} = 33 µs min. is for different drive units. In the case of the same unit, t_{SC} can range from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Output Voltage	V_{OUT}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

OPERATING CONDITIONS

Parameter	Range
V_{CC} Power Supply	5.0V \pm 5%
Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

($V_{CC} = 5.0$ Vdc \pm 5%, $V_{SS} = 0$ Vdc, $T_A = 0^\circ\text{C}$ to 70°C , unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Low Voltage Logic CLK and WCK	V_{IL}	-0.5 -0.5	0.8 0.65	V	
Input High Voltage Logic CLK and WCK	V_{IH}	2.0 2.4	$V_{CC} + 0.5$ $V_{CC} + 0.5$	V	
Output Low Voltage	V_{OL}		0.45	V	$V_{CC} = 4.75\text{V}$, $I_{OL} = 2.0$ mA
Output High Voltage	V_{OH}	2.4	V_{CC}	V	$V_{CC} = 4.75\text{V}$, $I_{OH} = -200$ μA
V_{CC} Supply Current	I_{CC}		150	mA	$V_{CC} = 4.75\text{V}$
Input Load Current All Inputs	I_{IL}		10 -10	μA μA	$V_{IN} = V_{CC}$ $V_{IN} = 0\text{V}$
High Level Output Leakage Current	I_{LOH}		10	μA	$V_{CC} = 0\text{V}$ to 5.25V, $V_{SS} = 0\text{V}$ $V_{OUT} = V_{CC}$
Low Level Output Leakage Current	I_{LOL}		-10	μA	$V_{CC} = 0\text{V}$ to 5.25V, $V_{SS} = 0\text{V}$ $V_{OUT} = +0.45\text{V}$
Internal Power Dissipation	P_{INT}	—	1.0	W	$T_A = 25^\circ\text{C}$

CAPACITANCE

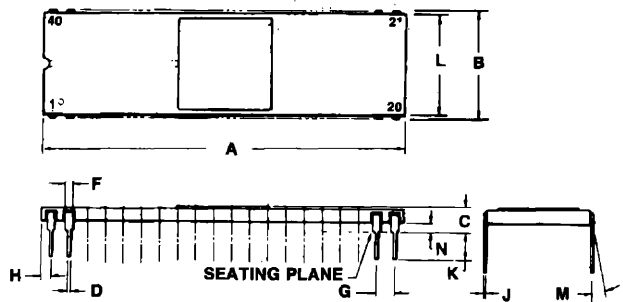
($T_A = 25^\circ\text{C}$; $f_c = 1$ MHz; $V_{CC} = 0\text{V}$)

Parameter	Symbol	Max Limit	Unit
Clock Input	$C_{IN(0)}$	20	pF
Input	C_{IN}	10	pF
Output	C_{OUT}	20	pF

Note: All pins except pin under test tied to ground.

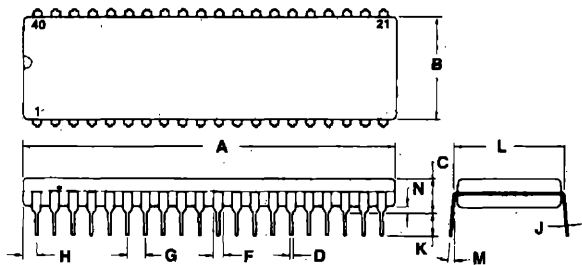
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.065
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.080
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.38	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040



R6592 SINGLE-CHIP PRINTER CONTROLLER

2

INTRODUCTION

The Rockwell R6592 is a single-chip printer controller for eight different EPSON® dot-matrix impact printers, models 210, 220, 240, 511L, 512, 522, 541L, and 542. The R6592 offers the flexibility to support any of these models with a minimum of circuitry. Generation of 96 standard ASCII upper and lower case characters and 6 special characters is provided. In addition, up to 10 ASCII control commands are accepted, depending upon the printer. Logic is included in the R6592 to print up to 26 columns on the 210, 220, and 240 models, and up to 40 columns on the 511L, 512, 522, 541L and 542 models.

Input data may be selected to be in the RS-232 serial format with selectable baud rate from 50 to 7200 bits/second or the parallel format. External circuitry is required to convert RS-232 logic levels to R6592 interface logic levels. An external latch may be required for the R6592 to sample parallel data. If both selectable serial and parallel data interface capability is desired, two external multiplexers are required; one to combine four serial baud select lines and four parallel data interface lines into four R6592 input lines and the other to combine two serial data/control lines and two parallel control lines into two other R6592 input lines.

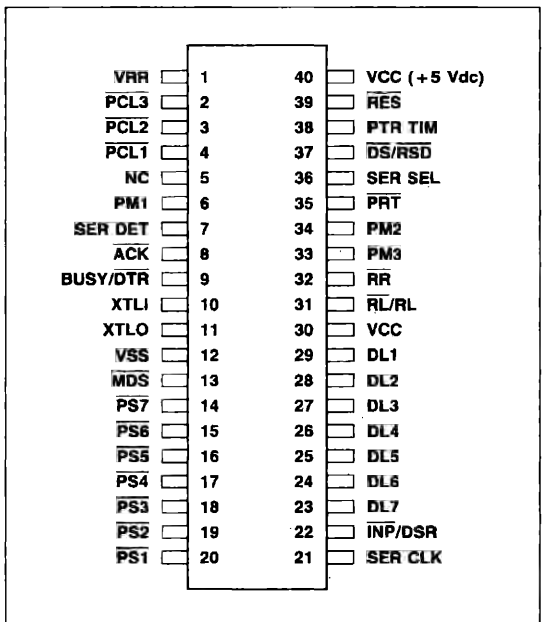
*EPSON is a trade name of Shinshu Seiki Co., Ltd., a member of the Seiko Group. EPSON printers are distributed in the United States by C. Itoh Electronics, Inc. The R6592 meets the printer specifications listed in this data sheet.

FEATURES

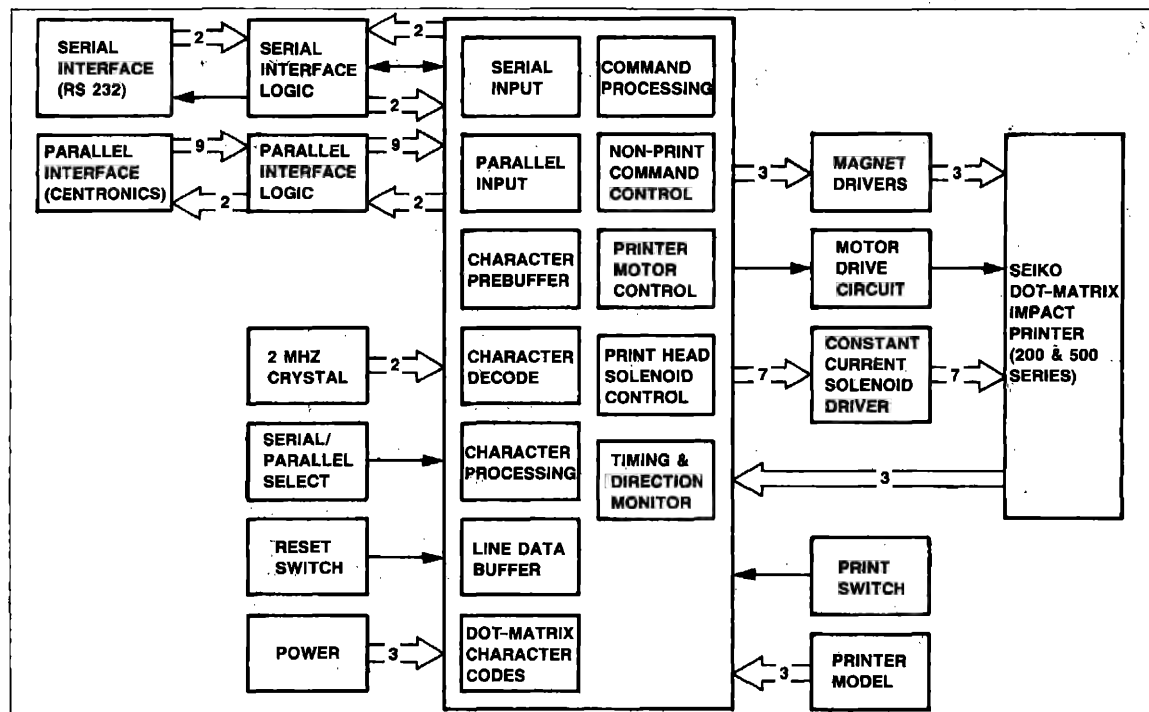
- Controls EPSON Dot-Matrix Impact Printers:

Model 210	Model 512
Model 220	Model 522
Model 240	Model 541L
Model 511L	Model 542
- Minimal Support Circuitry Required
- On-Chip 5 × 7 Dot-Matrix Character Generation
- 96 Standard Upper and Lower Case ASCII Characters (7 Bit Code)

- Six Special ASCII Characters (7 Bit Code)
- Up to 10 ASCII Commands Accepted (Printer Dependent)
- Selectable Serial or Parallel Input Data Operation
- Centronics Standard Parallel Interface
 - Seven Data Lines Plus Data Strobe and Input Drive Input
 - Busy and Acknowledge Output
- RS-232C Serial Interface
 - Baud Rate from 50 to 7200 Bits per Second
 - Received Data and Data Set Ready Input
 - Data Terminal Ready Output
- Single +5V ± 10% power supply
- 40 pin plastic or ceramic DIP
- 1 MHz operation (2 MHz external crystal)



R6592 Pin Configuration



R6592 Interface Diagram

INTERFACE SIGNALS

PRINTER SOLENOID 1 (PS1)
 PRINTER SOLENOID 2 (PS2)
 PRINTER SOLENOID 3 (PS3)
 PRINTER SOLENOID 4 (PS4)
 PRINTER SOLENOID 5 (PS5)
 PRINTER SOLENOID 6 (PS6)

Active low output signals used to command seven constant current print head solenoid drivers. When low, the respective solenoid will be energized to print a dot; and when high, the solenoid will be de-energized to not print a dot. Each solenoid line corresponds to a dot position on the seven row print head. Line PS1 corresponds to the top dot and PS7 corresponds to the bottom dot. The output lines are activated by the positive edge of the timing signal (TIM). The TIM signal should also be used to gate PS1 through PS7 to the current drivers and to de-energize the current driver inputs within $600 \pm 20 \mu\text{sec}$ of the start of the TIM signal by means of a one-shot flip-flop.

PRINTER CONTROL LINE 1 (PCL1)
 PRINTER CONTROL LINE 2 (PCL2)
 PRINTER CONTROL LINE 3 (PCL3)

Active low output control lines used to issue various non-print commands to the printer. These lines are inputs to +24V drivers. When low, these lines cause magnets to be energized in the printer; when high, the magnets are to be de-energized. These lines are assigned to specific signals depending upon printer model:

Printer Model	R6592 Signal Name		
	PCL1	PCL2	PCL3
210	NA	Paper Feed	Change Color
220	Paper Feed (R)	Paper Feed (L)	
240	NA	Paper Feed	Slip Release
511L	NA	Paper Feed	NA
512	NA	Paper Feed	NA
522	Paper Feed (R)	Paper Feed (L)	Stamp and Cut Paper
541L	NA	Paper Feed	Paper Release
542	NA	Paper Feed	Paper Release

NA = Not Assigned

TIMING (TIM)
 RESET LEFT (RL/RL)
 RESET RIGHT (RR/RR)

Input signals used to indicate print cycle Timing. The R6592 initiates a print cycle on the leading edge (positive transition) of the TIM signal information to the R6592. The RESET signals are active low for the 500 series (\overline{RR} and \overline{RL}) and are active high for the 200 series (RL). The printer timing and reset lines are assigned as follows:

Printer Model	R6592 Signal		
	TIM	\overline{RL}/RL	\overline{RR}
210	T Detector	R Detector (RL)	NA
220	T Detector	R Detector (RL)	NA
240	T Detector	R Detector (RL)	NA
511L	Timing Signal	Reset Signal R-L (RL)	NA
512	Timing Signal	Reset Signal R-L (RL)	Reset Signal R-R (\overline{RR})
522	Timing Signal	Reset Signal R-L (RL)	Reset Signal R-R (\overline{RR})
541L	Timing Signal	Reset Signal R-L (RL)	NA
542	Timing Signal	Reset Signal R-L (RL)	Reset Signal R-R (\overline{RR})

See Detail Timing Diagrams in Printer Specifications.

MOTOR DRIVE SIGNAL (\overline{MDS})

Active low output signal used to control application of power from a driver circuit to the printer motor. When high, the motor drive is turned off and when low, the motor drive is turned on. The driver circuit for the 500 series must supply 10 to 30 ma at TTL levels. The driver circuit for the 200 series must additionally provide motor braking.

PRINTER MODEL 1 (PM1)

PRINTER MODEL 2 (PM2)

PRINTER MODEL 3 (PM3)

Encoded input lines used to determine which printer model is connected to the R6592. A connection to GND (low) causes "0" to be read. An open input (high) causes logic "1" to be read. The encoding for the printer model is:

Printer Model	Printer Model Line		
	PM3	PM2	PM1
210	0	0	0
220	0	0	1
240	0	1	0
511L	0	1	1
512	1	0	0
522	1	0	1
541L	1	1	0
542	1	1	1

PRINT (\overline{PRT})

Active low input line used to command R6592 to print a line. When low (GND) print commands will continue to be issued. If the print buffer is partially filled, a line will be printed. Line feeds will subsequently be issued while \overline{PRT} is low. When high (open), print commands will not be issued.

SERIAL SELECT (SER SEL)

Active high input line used to indicate the desired data transmission mode to the R6592. When high (open), input data will be received and processed from the serial interface (RS-232C). When low (GND), input data will be received and processed from the parallel interface (Centronics).

If both transmission modes are to be implemented (but not simultaneously), the SER SEL line should be used to select either serial or parallel signals through multiplexer circuits. If either serial or parallel data transmission is exclusively used, multiplexing of the indicated serial/parallel signals is not required.

DATA LINE 1/BAUD RATE 1 (DL1/BR1)

DATA LINE 2/BAUD RATE 2 (DL2/BR2)

DATA LINE 3/BAUD RATE 3 (DL3/BR3)

DATA LINE 4/BAUD RATE 4 (DL4/BR4)

Active high input signals used as parallel data lines if parallel data transfer mode is selected, or used as baud rate select lines if serial data transfer mode is selected.

If parallel data transfer mode is selected (SER SEL = low) these lines represent four of the seven total data lines (see below). DL1/BR1 represents the least significant bit when ASCII characters are decoded. If serial data transfer mode is selected (SER SEL = high), the data transfer baud rate in bits per second is:

Baud	Data Line/Baud Rate Line			
	DL4/BR4	DL3/BR3	DL2/BR2	DL1/BR1
50	0	0	0	0
75	0	0	0	1
110	0	0	1	0
135	0	0	1	1
150	0	1	0	0
300	0	1	0	1
600	0	1	1	0
1200	0	1	1	1
1800	1	0	0	0
2400	1	0	0	1
3600	1	0	1	0
4800	1	0	1	1
7200*	1	1	0	0

Note: 1 = High (open), 0 = Low (GND).
*Data cannot be sent to the R6592 while the print head is moving.

DATA LINE 5 (DL5)

DATA LINE 6 (DL6)

DATA LINE 7 (DL7)

Active high input signals used as data lines when parallel data transfer mode is selected (SER SEL = low). DL7 represents the most significant bit (MSB) when ASCII characters are decoded. Not used when serial data transfer mode is selected (SER SEL = high).

INPUT PRIME (IP)/DATA SET READY (DSR)

Input line multiplexed between a parallel communications control line (INPUT PRIME) and a serial communications control line (DATA SET READY).

If the parallel data transfer mode is selected (SER SEL = low), this line is assigned to INPUT PRIME (IP). When IP/DSR is high, the R6592 issues print commands to the printer in a normal fashion. When IP/DSR is low, the R6592 will disable printing. This line can, therefore, be used as a print disable line to selected printers in a multiprinter system.

If the serial data transfer mode is selected (SER SEL = high), the line is assigned to DATA SET READY (DSR). When high, DSR indicates that the transmitter is operative and the R6592 will accept data. When low, DSR indicates that the transmitter is not ready to operate and the R6592 will not accept serial data.

DATA STROBE (DS)/RECEIVED SERIAL DATA (RSD)

Input line multiplexed between a parallel communications control line (DATA STROBE) and the serial communications data line (RECEIVED SERIAL DATA).

If the parallel data transfer mode is selected (SER SEL = low), this line is assigned to the DATA STROBE (DS). When DS goes low, the R6592 detects the negative transition, and samples the data on the parallel data lines. The data must be present on the data lines for at least 50 μ sec after DS goes low.

If the serial data transfer mode is selected (SER SEL = high), the line is assigned to RECEIVED SERIAL DATA (RSD). The data is processed in accordance with the selected baud rate. The data must be converted from RS-232 logic levels to R6592 logic levels. The R6592 logic state is inverted from RS-232 logic state.

BUSY DATA TERMINAL READY (BUSY/DTR)

Output line multiplexed between a parallel communication control line (BUSY) and a serial communication control line (DATA TERMINAL READY).

If the parallel data transfer mode is selected (SER SEL = low), this line is assigned to BUSY. When high, BUSY indicates that the R6592 cannot receive data. When low, BUSY indicates that the R6592 is ready to receive data. BUSY is switched high during character print and while non-print commands are being processed.

If the serial data transfer mode is selected (SER SEL = high), this line is assigned to DATA TERMINAL READY (DTR). When high, DTR indicates that the R6592 cannot

receive data. When low, DTR indicates that the R6592 is ready to receive data. DTR is switched high during character print and while non-print commands are being processed.

ACKNOWLEDGE (ACK)

Active low output signal used to inform the parallel data transmitter that an input character has been received. ACK is switched low for 5 μ sec to indicate receipt of a character.

SERIAL CLOCK (SER CLK)

A bi-directional line used to detect the start of the received serial data and to then clock in the serial data bits. When DET ENA is low, this line monitors the input serial data stream for the start bit. When the leading (falling) edge of the start bit is detected, the DET ENA is switched high and this line is switched to an output. Output pulses are generated on this line to clock the received serial data into the R6592 at the selected baud rate.

SERIAL DETECT ENABLE (DET ENA)

Active high output used to enable the received serial data onto the SER CLK line. Upon detection of the received serial start bit, this line is switched low to disable the received serial data from being placed on the SER CLK line.

PRIMARY POWER (VCC)

R6592 primary power supply: +5V \pm 10%. Supplies power to CPU, I/O, timer and supporting circuitry.

RAM POWER (VRR)

R6592 RAM power supply: +5V \pm 10%. Supplies power to the internal R6592 RAM. This line should be connected to VCC power supply.

SIGNAL GROUND (VSS)

R6592 power and signal ground.

XTLI

Input from 2 MHz crystal.

XTLO

Output to 2 MHz crystal.

RESET (RES)

Active low signal used to reset and initialize the R6592. Must be held low for at least 8 μ sec after VCC reaches operating voltage and the clock frequency on XTLO has stabilized.

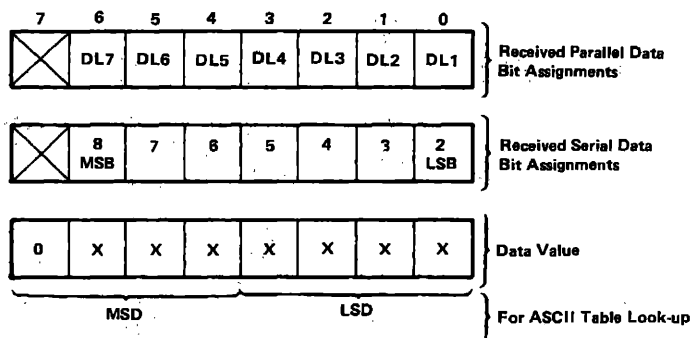
Standard 96 Character 5x7 Matrix Dot Patterns

20	21	22	23	24	25	26	27
28	29	2A	2B	2C	2D	2E	2F
30	31	32	33	34	35	36	37
38	39	3A	3B	3C	3D	3E	3F
40	41	42	43	44	45	46	47
48	49	4A	4B	4C	4D	4E	4F
50	51	52	53	54	55	56	57
58	59	5A	5B	5C	5D	5E	5F
60	61	62	63	64	65	66	67
68	69	6A	6B	6C	6D	6E	6F
70	71	72	73	74	75	76	77
78	79	7A	7B	7C	7D	7E	

Special 6 Character 5x7 Matrix Dot Patterns

5A	5B	5C	5D	5E	5F
YEN	POUND	ONE-HALF	CENT	NO TAX	TAX

R6592 Internal Data Format for 7-Bit ASCII Table Character Look-Up



ASCII 7-Bit Code Character Set Table

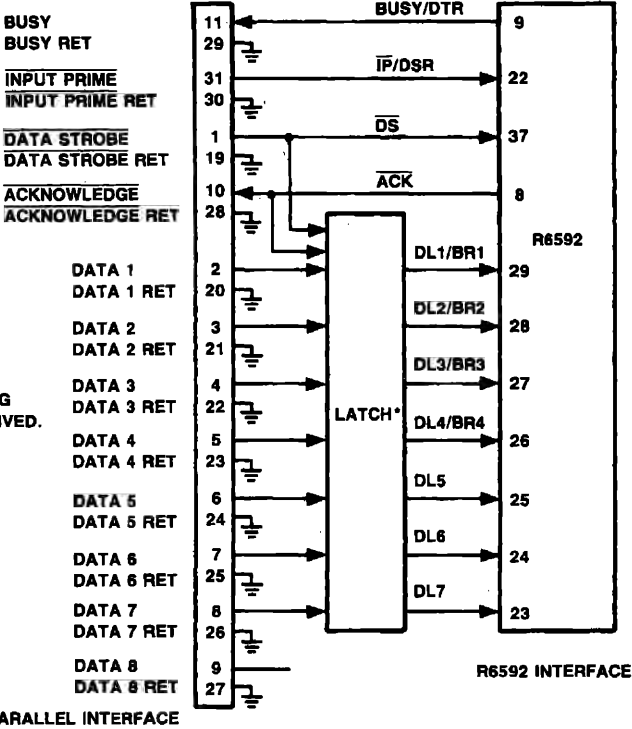
LSD	MSD	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000			SP	0	@	P		p
1	0001		DC1	!	1	A	Q	a	q
2	0010		DC2	"	2	B	R	b	r
3	0011		DC3	#	3	C	S	c	s
4	0100		DC4	\$	4	D	T	d	t
5	0101			%	5	E	U	e	u
6	0110			&	6	F	V	f	v
7	0111			'	7	G	W	g	w
8	1000		CAN	(8	H	X	h	x
9	1001)	9	I	Y	i	y
A	1010	LF	¥	*	:	J	Z	j	z
B	1011	VT	t	+	:	K	[k	{
C	1100	FF	1/2	,	<	L	\	l	
D	1101	CR	¢	-	=	M]	m	}
E	1110		N	.	>	N	^	n	~
F	1111		T	/	?	O	_	o	DEL

LF — Line Feed
 VT — Vertical Tabulation
 FF — Form Feed
 CR — Carriage Return
 DC1 — Device Control 1
 DC2 — Device Control 2
 DC3 — Device Control 3
 DC4 — Device Control 4

CAN — Cancel
 ¥ — Yen
 t — Pound
 ¢ — Cent
 1/2 — One-Half
 N — No Tax
 T — Tax
 X — 4 Tax

Note: Valid control commands are dependent upon printer model.

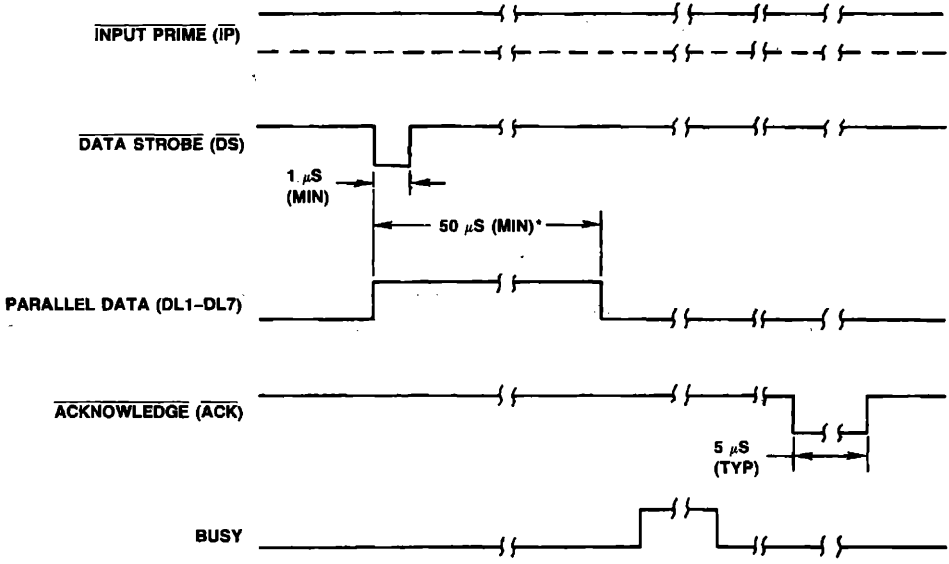
PARALLEL DATA INTERFACE



*NOT REQUIRED IF PARALLEL DATA IS HELD FOR $\geq 50 \mu\text{s}$ AFTER LEADING EDGE OF DS OR UNTIL ACK IS RECEIVED.

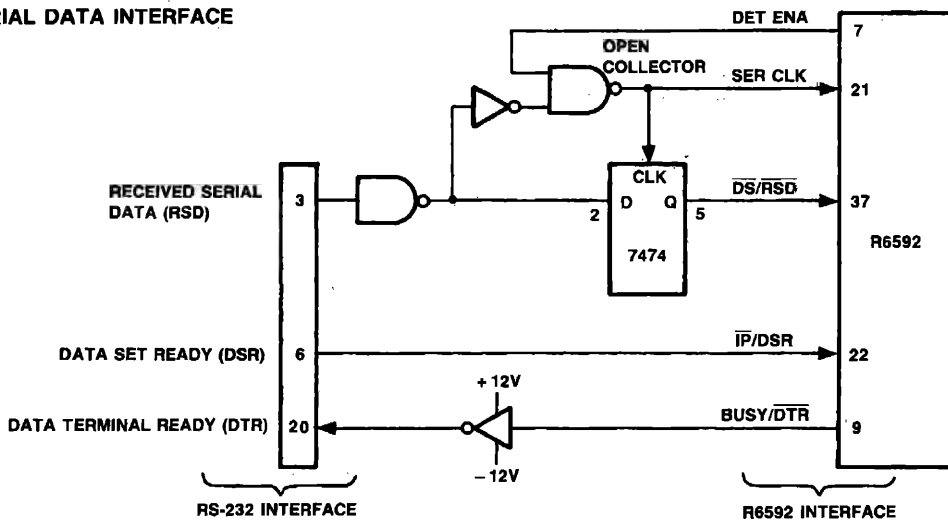
CENTRONICS PARALLEL INTERFACE

PARALLEL DATA TIMING

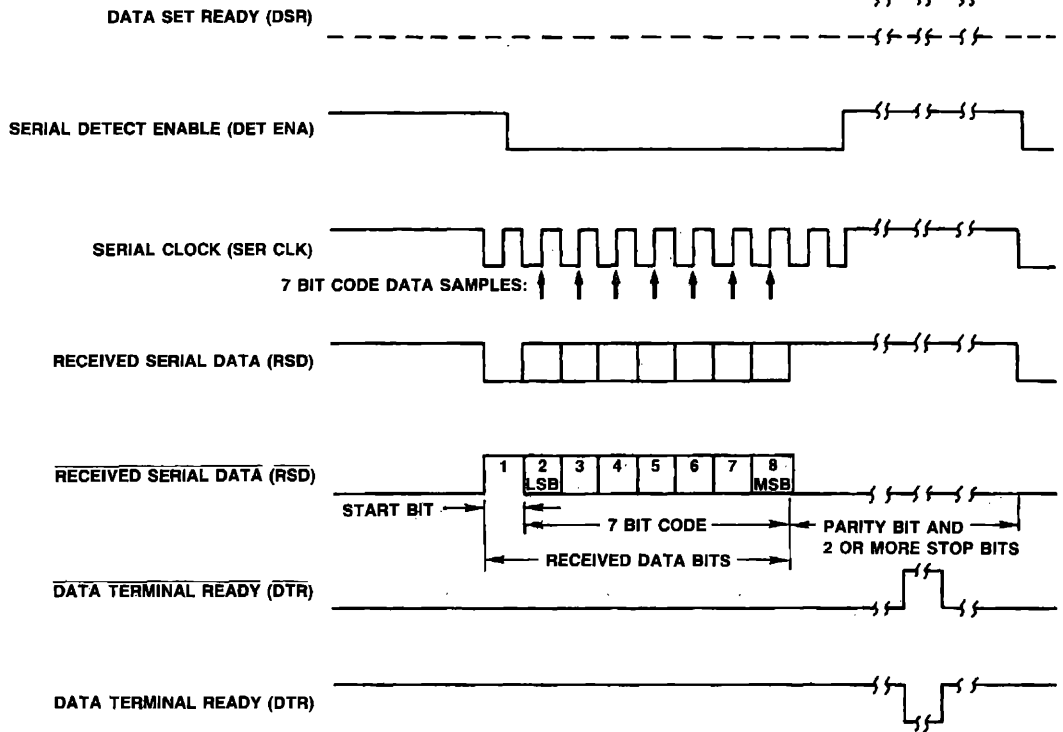


*OR UNTIL $\overline{\text{ACK}}$ IS RECEIVED.

SERIAL DATA INTERFACE



SERIAL DATA TIMING



PRINTER INTERFACE SPECIFICATIONS

The R6592 is designed to meet the interface requirements stated in the following printer specification:

Model-210 Impact Dot Matrix Mini-Printer (Preliminary)
Rev. 4, AUGUST 30, 1978

Model-220 Impact Dot Matrix Mini-Printer,
SEPTEMBER 18, 1978

Model-240 Impact Dot Matrix Mini-Printer,
SEPTEMBER 18, 1978

Model-511L Impact Dot Matrix Printer (Enlarged Character)
Revision 1 JULY 13, 1978

Model 512 Dot-Matrix Impact Printer (P512DF),
APRIL 10, 1978

Model 522 Dot-Matrix Impact Printer (P522DF),
MARCH 1, 1978

Model 541L Impact Dot Matrix Printer (Enlarged Character),
Revision 1, July 19, 1978

Model 542 Dot-Matrix Impact Printer (P542DF),
MARCH 1, 1978

For further printer information, contact:

EPSON America, Inc.
23844 Hawthorne Blvd. Ltd.
Torrance, CA 90505
Phone: (213) 378-2220
TWX: 910-344-7390

C. Itoh Electronics, Inc.
5301 Beethoven Street
Los Angeles, Calif. 90066
Phone: (213) 390-7778
Telex: WU 65-2451

C. Itoh Electronics, Inc.
280 Park Avenue
New York, New York, 10017
Phone: (212) 682-0420
Telex: WUD-12-5059

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	Vdc
Output Voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	Vdc
Operating Temperature Commercial Industrial	T_A	0 to +70 -40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

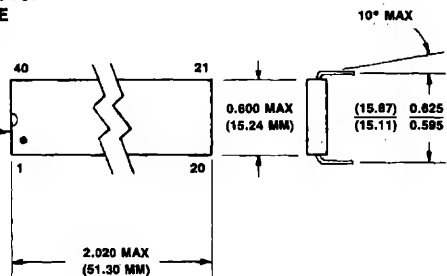
STATIC DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Dissipation (Outputs High)	P_D	—	500	—	mW
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	—	+0.8	Vdc
Input Threshold Voltage	V_{IT}	0.8	—	2.0	Vdc
Input Leakage Current $V_{in} = 0$ to 5.0 Vdc RES	I_{IN}	—	± 1.0	± 2.5	μ Adc
Input High Voltage (XTLI)	V_{IHXT}	+4.0	—	V_{CC}	Vdc
Input Low Voltage (XTLI)	V_{ILXT}	-0.3	—	+0.8	Vdc
Input Low Current ($V_{IL} = 0.4$ Vdc)	I_{IL}	—	-1.0	-1.6	mAdc
Output High Voltage ($V_{CC} = \min$, $I_{Load} = -100 \mu$ Adc)	V_{OH}	2.4	—	—	Vdc
Output Low Voltage ($V_{CC} = \min$, $I_{Load} = 1.6$ mAdc)	V_{OL}	—	—	-0.4	Vdc
Output High Current (Sourcing) ($V_{OH} = 2.4$ Vdc)	I_{OH}	-100	—	—	μ Adc
Output Low Current (Sinking) ($V_{OL} = 0.4$ Vdc)	I_{OL}	1.6	—	—	mAdc
Input Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz) Pins 2-9, 13-29 and 31-38 XTLI, XTLO	C_{in}	— —	— —	10 50	pF
Output Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz)	C_{OUT}	—	—	10	pF
Note: Negative sign indicates outward current flow, positive indicates inward flow.					

PACKAGE DIMENSIONS

DOT OR NOTCH
TO LOCATE
PIN NO. 1

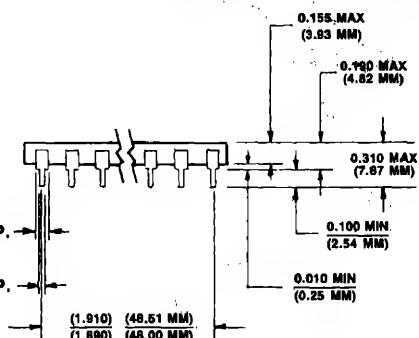


(1.85) 0.065
(1.01) 0.040

TYP.

(0.55) 0.022
(0.45) 0.016

TYP.



19 EQUAL SPACES
0.100 ϕ TOL NONCUM.
(2.54 MM)

NOTE: PIN NO. 1 IS IN LOWER LEFT CORNER WHEN SYMBOLIZATION IS IN NORMAL ORIENTATION.



R65560 MULTI-PROTOCOL COMMUNICATIONS CONTROLLER (MPCC)

PRELIMINARY

DESCRIPTION

The R65560 Multi-Protocol Communications Controller (MPCC) interfaces a single serial communications channel to a 6500/6800 microcomputer-based system using either asynchronous or synchronous protocol. High speed bit rate, automatic formatting, low overhead programming, eight character buffering, and two channel DMA interface optimize MPCC performance to take full advantage of the 6500/6800 processing capabilities.

In synchronous operation, the MPCC supports bit-oriented protocols (BOP), such as SDLC/HDLC, and character-oriented protocols (COP), such as IBM Bisync (BSC) in either ASCII or EBCDIC coding. Formatting, synchronizing, validation and error detection is performed automatically in accordance with protocol requirements and selected options. Asynchronous (ASYNC) and isochronous (ISOC) modes are also supported. In addition, modem interface handshake signals are available for general use.

Control, status and data are transferred between the MPCC and the microcomputer bus via 19 directly addressable registers and a DMA interface. Two first-in first-out (FIFO) registers, addressable through separate receiver and transmitter data registers, each buffer up to eight characters at a time to allow more CPU/MPU processing time to service data received or to be transmitted and to maximize bus throughput, especially during DMA operation. The two-channel Direct Memory Access (DMA) interface operates with the MC6844 DMA Controller.

An on-chip oscillator drives the internal baud rate generator (BRG) and an external clock output with an 8 MHz input crystal or clock frequency. The BRG, in conjunction with two selectable prescalers and 16-bit programmable divisor, provides a data bit rate of DC to 4 MHz.

ORDERING INFORMATION

Part Number	Frequency	Temperature Range
R65560	4 MHz	0°C to 70°C
Package: C = Ceramic P = Plastic		

FEATURES

- Full duplex synchronous/asynchronous receiver and transmitter
- Fully implements IBM Binary Synchronous Communications (BSC) in two coding formats: ASCII and EBCDIC
- Supports other synchronous character-oriented protocols (COP), such as six-bit BSC, X3.28, ISO IS1745, ECMA-16, etc.
- Supports synchronous bit-oriented protocols (BOP), such as SDLC, HDLC, X.25, etc.
- Asynchronous and isochronous modes
- Modem handshake interface
- High speed serial data rate (DC to 4 MHz)
- Internal oscillator and Baud Rate Generator (BRG) with programmable data rate
- Crystal or TTL level clock input and buffered clock output (8 MHz)
- Direct interface to 6500/6800 microprocessor bus
- Eight-character receiver and transmitter buffer registers
- 19 directly addressable registers for flexible option selection, complete status reporting, and data transfer
- Maskable interrupt conditions for receiver, transmitter and serial interface
- Programmable microprocessor bus data transfer: polled, interrupt and two-channel DMA transfer compatible with MC6844
- Clock control register for receiver clock divisor and receiver and transmitter clock routing
- Selectable full/half duplex, autoecho and local loop-back modes
- Selectable parity (enable, odd, even) and CRC (control field enable, CRC-16, CCITT V.41, VRC/LRC)

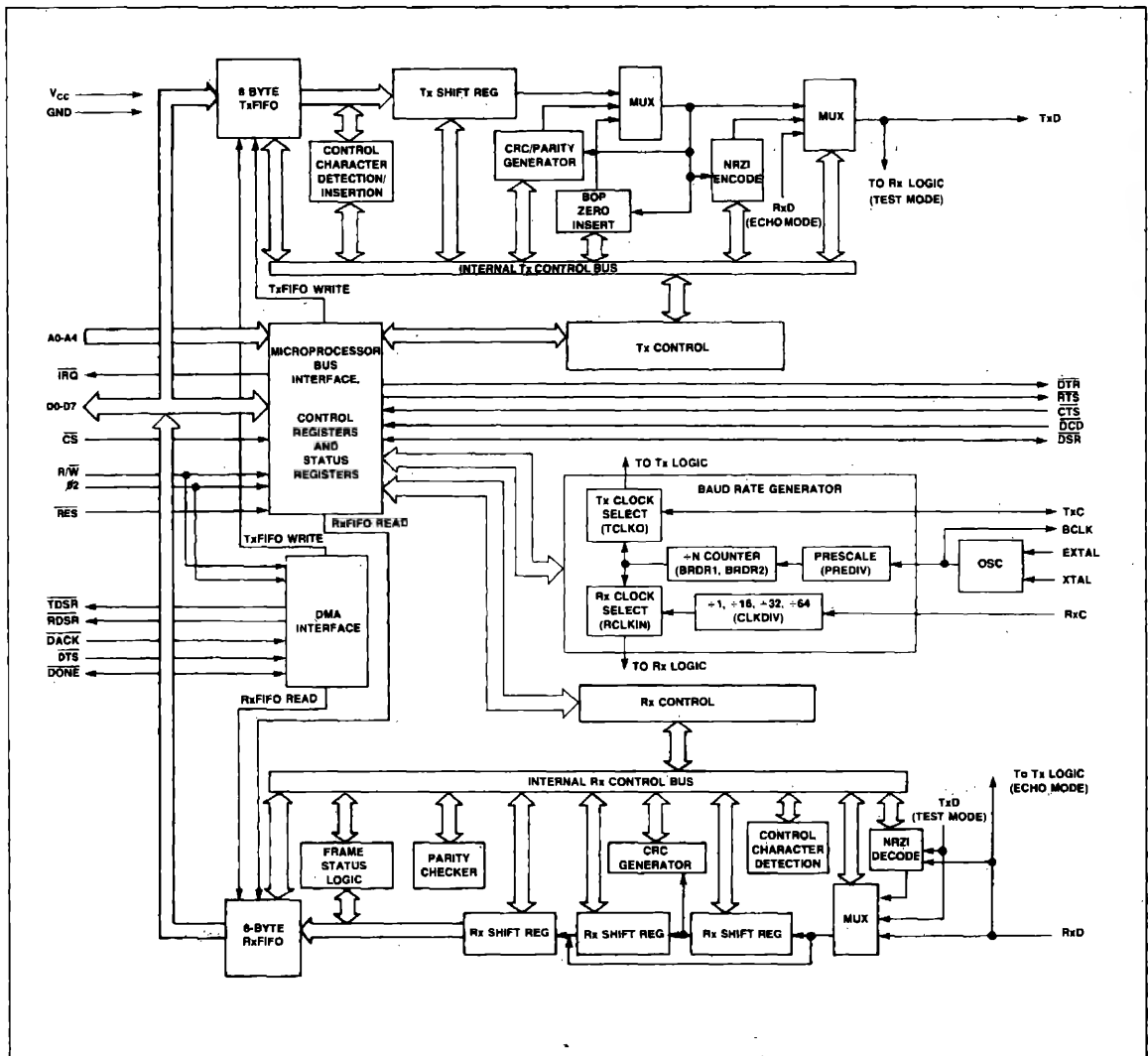


Figure 1. MPCC Block Diagram

PIN DESCRIPTION

Throughout the document, signals are presented using the terms active and inactive or asserted and negated independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar. R/W indicates a write is active low and a read active high.

A0 – A4—Address Lines. A0 – A4 are active high inputs used in conjunction with the CS input to access the internal registers. The address map for these registers is shown in Table 1.

D0 – D7—Data Lines. The bidirectional data lines transfer data between the MPCC and the CPU, memory or other peripheral device. The data bus is tri-stated when CS is inactive. (See exceptions in DMA mode.)

CS—Chip Select. CS low selects the MPCC for programmed transfers with the host. The MPCC is deselected when the CS input is inactive in non-DMA mode.

R/W—Read/Write. R/W controls the direction of data flow through the bidirectional data bus by indicating that the current bus cycle is a read (high) or write (low) cycle.

Ø2—Phase 2. During a write (R/W low), the Ø2 negative transition latches data on data bus lines D0 – D7 into the MPCC. During a read (R/W), Ø2 high enables data from the MPCC to data bus.

IRQ—Interrupt Request. The active low IRQ output requests interrupt service by the CPU. IRQ is driven high after assertion prior to being tri-stated.

TDSR—Transmitter Data Service Request. When Transmitter DMA mode is active, the low TDSR output requests DMA service.

RDSR—Receiver Data Service Request. When receiver DMA mode is active, the low RDSR output requests DMA service.

DACK—DMA Acknowledge. The DACK low input indicates that that the data bus has been acquired by the DMAC and that the requested bus cycle is beginning.

DTS—DMA Transfer Strobe. The DTS low input causes a DMA transfer to occur on the next Ø2 cycle. When R/W is high, data is transferred into the Tx FIFO; when R/W is low, data is transferred from the Rx FIFO.

DONE—Done. DONE is a bidirectional active low signal. The DONE signal is asserted by the DMAC when the DMA transfer count is exhausted and there is no more data to be transferred. DONE will also be asserted by the MPCC, if enabled by bit 5 in the RCR, when the status byte following the last character of a frame (block) is being transferred in response to a RDSR. The DONE signal asserted by the DMAC in response to a TDSR will be stored to track with the data byte through the Tx FIFO.

RES—Reset. RES is an active low, high impedance input that initializes all MPCC functions. RES must be asserted for at least 500 ns to initialize the MPCC.

DTR—Data Terminal Ready. The DTR active low output is general purpose in nature, and is controlled by the DTRLVL bit in the Serial Interface Control Register (SICR).

RTS—Request to Send. The RTS active low output is general

CTS—Clear to Send. The CTS active low input positive transition and level are reported in the CTST and CTS_LVL bits in the Serial Interface Status Register (SISR), respectively.

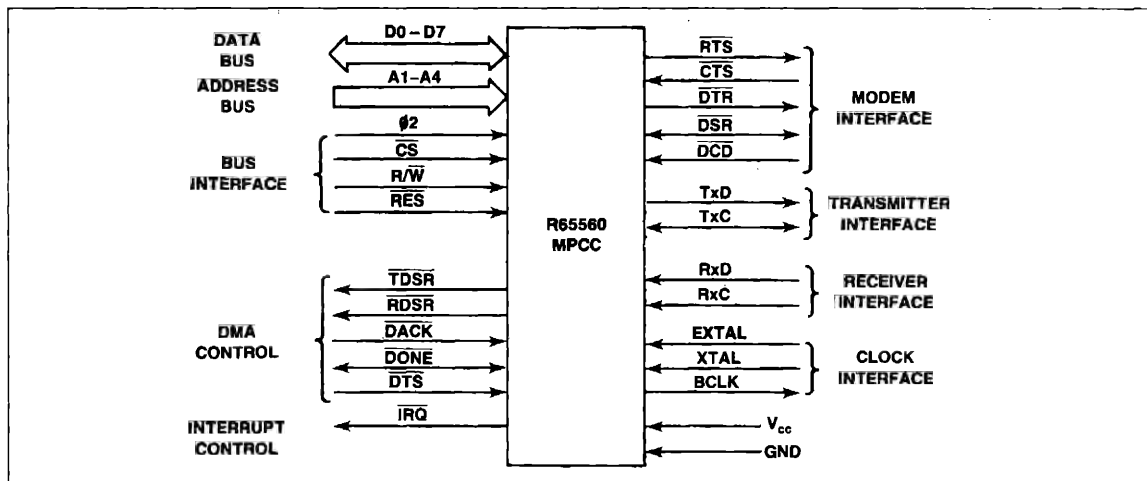


Figure 2. MPCC Input and Output Signals

DSR—Data Set Ready. The $\overline{\text{DSR}}$ active low input negative transition and level are reported in the DSRT and DSRLVL bits in the SISR, respectively. $\overline{\text{DSR}}$ is also an output for RSYN.

DCD—Data Carrier Detect. The $\overline{\text{DCD}}$ active low input positive transition and level are reported in the DCDT and DCDLVL bits in the SISR, respectively.

TxD—Transmitted Data. The MPCC transmits serial data on the TxD output. The TxD output changes on the negative going edge of TxC.

RxD—Received Data. The MPCC receives serial data on the RxD input. The RxD input is shifted into the receiver with the negative going edge of RxC.

TxC—Transmitter Clock. TxC can be programmed to be an input or an output. When TxC is selected to be an input, the transmitter clock must be provided externally. When TxC is programmed to be an output, a clock is generated by the MPCC's internal baud rate generator. The low-to-high transition of the clock signal nominally indicates the center of a serial data present on the TxD output.

RxC—Receiver Clock. RxC provides the MPCC receiver with received data timing information. The clock transition from low-to-high nominally indicates the center of each serial data bit on the RxD input.

EXTAL—Crystal/External Clock Input.

XTAL Crystal Return. EXTAL and XTAL connect an 8 MHz external crystal to the MPCC internal oscillator. The pin EXTAL may also be used as a TTL level input to supply a DC to 8 MHz reference timing from an external clock source. XTAL must be tied to ground when applying an external clock to the EXTAL input.

BCLK—Buffered Clock. BCLK is the internal oscillator buffered output available to other MPCC devices eliminating the need for additional crystals.

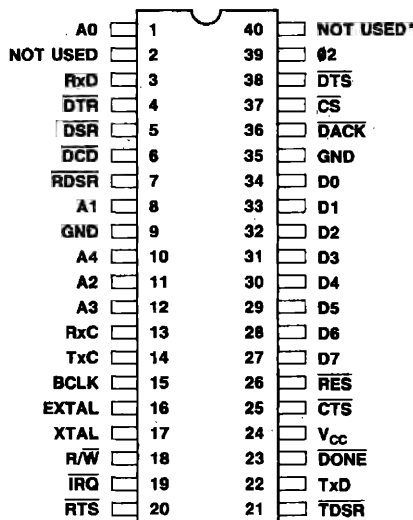
Vcc—Power. 5V \pm 5%.

GND—Ground. Ground (V_{SS}).

MPCC REGISTERS

Nineteen 8-bit registers define, control and monitor the data communications process. These registers and their access are listed in Table 1.

Table 2 summarizes the MPCC register bit assignments and their access. A read from an unassigned location results in a read from a "null register." A null register returns all ones for data and results in a normal bus cycle. Unused bits of a defined register are read as zeros unless otherwise noted.



*Must be connected to V_{CC}.

R65560

Pin Configuration

Table 1. R65560 Accessible Registers

Register(s)	R/W	Addr (Hex.)	Address Lines				
			A4	A3	A2	A1	A0
7	0						
Receiver Status Register (RSR)	R/W	00	0	0	0	0	0
Receiver Control Register (RCR)	R/W	01	0	0	0	0	1
Receiver Data Register (RDR) ¹	R	02	0	0	0	1	0
Receiver Interrupt Enable Register (RIER)	R/W	05	0	0	1	0	1
Transmitter Status Register (TSR)	R/W	08	0	1	0	0	0
Transmitter Control Register (TCR)	R/W	09	0	1	0	0	1
Transmitter Data Register (TDR) ²	W	0A	0	1	0	1	0
Transmitter Interrupt Enable Register (TIER)	R/W	0D	0	1	1	0	1
Serial Interface Status Register (SISR)	R/W	10	1	0	0	0	0
Serial Interface Control Register (SICR)	R/W	11	1	0	0	0	1
Serial Interrupt Enable Register (SIER)	R/W	15	1	0	1	0	1
Protocol Select Register 1 (PSR1)	R/W	18	1	1	0	0	0
Protocol Select Register 2 (PSR2)	R/W	19	1	1	0	0	1
Address Register 1 (AR1)	R/W	1A	1	1	0	1	0
Address Register 2 (AR2)	R/W	1B	1	1	0	1	1
Baud Rate Divider Register 1 (BRDR1)	R/W	1C	1	1	1	0	0
Baud Rate Divider Register 2 (BRDR2)	R/W	1D	1	1	1	0	1
Clock Control Register (CCR)	R/W	1E	1	1	1	1	0
Error Control Register (ECR)	R/W	1F	1	1	1	1	1

Notes:

1. Accessible register of the eight byte Rx FIFO. The data is not initialized, however, $\overline{\text{RES}}$ resets the Rx FIFO pointer to the start of the first byte.
2. Accessible register of the eight byte Tx FIFO. The data is not initialized, however, $\overline{\text{RES}}$ resets the Tx FIFO pointer to the start of the first byte.
3. Reserved registers may contain random bit values.

Table 2. MPCC Register Bit Assignments

R/W Access	Bit Number								Reset** Value	
	7	6	5	4	3	2	1	0		
R/W	RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE	00	Receiver Status Register (RSR)
R/W	0	RDSREN	DONEEN	RSYNEN	STRSYN	2ADCMP	RABTEN	RRES	01	Receiver Control Register (RCR)
R	RECEIVED DATA (Rx FIFO)								— —	Receiver Data Register (RDR)
R/W	RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0	00	Receiver Interrupt Enable Register (RIER)
R/W	TDRA	TFC	0	0	0	TUNRN	TFERR	0	80	Transmitter Status Register (TSR)
R/W	TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES	01	Transmitter Control Register (TCR)
W	TRANSMITTED DATA (Tx FIFO)								— —	Transmitter Data Register (TDR)
R/W	TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	0	00	Transmitter Interrupt Enable Register (TIER)
R/W	CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0	00	Serial Interface Status Register (SISR)
R/W	RTSLVL	DTRLVL	0	0	0	ECHO	TEST	NRZI	00	Serial Interface Control Register (SICR)
R/W	CTS IE	DSR IE	DCD IE	0	0	0	0	0	00	Serial Interrupt Enable Register (SIER)
R/W	0	0	0	0	0	0	CTLEX	ADDEX	00	Protocol Select Register 1 (PSR1)
R/W	0	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL			00	Protocol Select Register 2 (PSR2)
		SB2	SB1	CL2	CL1	PS3	PS2	PS1		
R/W	BOP ADDRESS/BSC & COP PAD								00	Address Register 1 (AR1)
R/W	BOP ADDRESS/BSC & COP SYN								00	Address Register 2 (AR2)
R/W	BAUD RATE DIVIDER (LSH)								01	Baud Rate Divider Register 1 (BRDR1)
R/W	BAUD RATE DIVIDER (MSH)								00	Baud Rate Divider Register 2 (BRDR2)
R/W	0	0	0	PSCDIV	TCLKO	RCLKIN	CLK SEL		00	Clock Control Register (CCR)
							CK2	CK1		
R/W	PAREN	ODDPAR	0	0	CTLCRC	CRCPRE	CRC SEL		04	Error Control Register (ECR)
							CR2	CR1		

Notes:**RESET = Register contents upon power up or RES.

REGISTER DEFINITIONS

RECEIVER REGISTERS

Receiver Status Register (RSR)

7	6	5	4	3	2	1	0
RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE

Reset value = \$00

The Receiver Status Register (RSR) contains the status of the receiver including error conditions. Status bits are cleared by writing a 1 into respective positions, by writing a 1 into the RCR RRES bit or by RES. If an EOF, C/PERR, or FRERR is set in the RSR, the data reflecting the error (the first byte or word in the Rx FIFO) must be read prior to resetting the corresponding status bit in the RSR. The IRQ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the RIER is set.

The RSR format is the same as the frame status format (see below) except as noted.

RSR

- 7 RDA —Receiver Data Available.** (RSR only).
 0 The Rx FIFO is empty (i.e., no received data is available).
 1 Received data is available in the Rx FIFO and can be read via the RDR.

RSR

- 6 EOF —End of Frame.**
 0 No end of frame or block detected.
 1 End of frame or block detected (BOP and BSC).

RSR

- 5 —Not Used.**

RSR

- 4 C/PERR —CRC/Parity Error.**
 0 No CRC or parity error detected.
 1 CRC error detected (BOP, BSC), Parity error detected (ASYNC, ISOC and COP).

RSR

- 3 FRERR —Frame Error.**
 0 No frame error detected.
 1 Short Frame or a closing FLAG detected off boundary (BOP), Frame error (ASYNC, ISOC) or receiver overrun.

RSR

- 2 ROVRN —Receiver Overrun.**
 0 No receiver overrun detected.
 1 Receiver overrun detected. Indicates that receiver data was attempted to be transferred into the Rx FIFO when it was full, resulting in loss of received data. The data that is already in Rx FIFO are not affected and may be read by the processor.

RSR

- 1 RA/B —Receiver Abort/Break.**
 0 Normal Operation.
 1 ABORT detected after an opening flag (BOP), ENQ detected in a block of text data (BSC), or BREAK detected (ASYNC).

RSR

- 0 RIDLE —Receiver Idle.** (RSR only).
 0 Receiver not idle.
 1 15 or more consecutive "1's" have been received and the receiver is in an inactive idle state.

Frame Status (RSR)

7	6	5	4	3	2	1	0
0	EOF	RHW	C/PERR	FRERR	ROVRN	RA/B	0

For the BSC and BOP protocols which have defined message blocks or frames, a "frame status" byte will be loaded into the Rx FIFO following the last data byte of each block (see Figure 3). The EOF status in the RSR is then set when the byte/word containing the frame status is the next byte/word to be read from the Rx FIFO.

In the receiver DMA mode, when the EOF status in the RSR is set, DONE is asserted to the DMAC. Thus the last byte accessed by the DMAC is always a status byte, which the processor may read to check the validity of entire frame.

The frame status contains all the status contained within the RSR with the exception of RDA and RIDLE.

BYTE	D7	D0
M	DATA	
M+1	STATUS	
M+2	NEXT FRAME	

Figure 3. BSC/BOP Block/Frame Status Location

Receiver Control Register (RCR)

7	6	5	4	3	2	1	0
0	RDSREN	DONEEN	RSYNEN	STRSYN	2ADCMP	RABEN	RRES

Reset value = \$01

The Receiver Control Register (RCR) selects receiver control options.

RCR

7 —Not used.

RCR

6 **RDSREN** —Receiver Data Service Request Enable.
 0 Disable receiver DMA mode.
 1 Enable receiver DMA mode.

RCR

5 **DONEEN** —**DONE** Output Enable.
 0 Disable **DONE** output.
 1 Enable **DONE** output. (When the receiver is in the DMA mode, i.e., RDSREN = 1).

RCR

4 **RSYNEN** —**RSYNEN** Output Enable. Selects the DSR signal input or the RSYN SYNC signal output on the DSR pin.
 0 Input DSR on DSR.
 1 Output RSYN on DSR.

RCR

3 **STRSYN** —Strip SYN Character (COP only).
 0 Do not strip SYN character.
 1 Strip SYN character.

RCR

2 **2ADCMP** —One/Two Address Compare (BOP only).
 0 Compare one address byte with the contents of AR1.
 1 Compare two address bytes with the contents of AR1 and AR2.

RCR

1 **RABTEN** —Receiver Abort Enable (BOP only).

0 Do not abort frame upon error detection.
 1 Abort frame upon Rx FIFO overrun (ROVRN bit = 1 in the RSR) or CFCRC error detection (C/PERR bit = 1 in the RSR). If either error occurs, the MPCC ignores the remainder of the current frame and searches for the beginning of the next frame.

RCR

0 **RRES** —Receiver Reset Command.

0 Enable normal receiver operation.
 1 Reset receiver. Resets the receiver section including the Rx FIFO and the RSR (but not the RCR). RRES is set by RES or by writing a 1 into this bit for one write cycle and is cleared by writing a 0 into this bit. RRES requires clearing after RES.

Receiver Data Register (RDR)

7	6	5	4	3	2	1	0
MSB		Received Data (RxFIFO)				LSB	

The receiver has an 8-byte First In First Out (FIFO) register file (Rx FIFO) where received data are stored before being transferred to the bus. The received data is transferred out of the Rx FIFO via the RDR. When the Rx FIFO has a data byte ready to be transferred, the RDA status bit in the RSR is set to 1.

Receiver Interrupt Enable Register (RIER)

7	6	5	4	3	2	1	0
RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	—

Reset value = \$00

The Receiver Interrupt Enable Register (RIER) contains interrupt enable bits for the Receiver Status Register (RSR). When enabled, the IRQ output is asserted when the corresponding condition is detected and reported in the RSR.

RIER

7 RDA IE —Receiver Data Available Interrupt Enable.

- 0 Disable RDA Interrupt.
1 Enable RDA Interrupt.

RIER

6 EOF IE —End of Frame Interrupt Enable.

- 0 Disable EOF Interrupt.
1 Enable EOF Interrupt.

RIER

5 —Not used.

RIER

4 C/PERR IE —CRC/Parity Error Interrupt Enable.

- 0 Disable C/PERR Interrupt.
1 Enable C/PERR Interrupt.

RIER

3 FRERR IE —Frame Error Interrupt Enable.

- 0 Disable FRERR Interrupt.
1 Enable FRERR Interrupt.

RIER

2 ROVRN IE —Receiver Overrun Interrupt Enable.

- 0 Disable ROVRN Interrupt.
1 Enable ROVRN Interrupt.

RIER

1 RA/B IE —Receiver Abort/Break Interrupt Enable.

- 0 Disable RA/B Interrupt.
1 Enable RA/B Interrupt.

RIER

0 —Not used.

TRANSMITTER REGISTERS**Transmitter Status Register (TSR)**

7	6	5	4	3	2	1	0
TDRA	TFC	0	0	0	TUNRN	TFERR	0

Reset value = \$80

The Transmitter Status Register (TSR) contains the transmitter status including error conditions. The transmitter status bits are cleared by writing a 1 into their respective positions, by writing a 1 into the TCR TRES bit, or by RES. The IRQ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the TIER is set.

TSR

7 TDRA —Transmitter Data Register Available.

- 0 The Tx FIFO is full.
1 The Tx FIFO is not full (i.e., available) and data to transmit can be loaded via the TDR.

TSR

6 TFC —Transmitted Frame Complete. (BOP, BSC and COP only).

- 0 Frame not complete.
1 Closing FLAG or ABORT character has been transmitted (BOP), Trailing PAD has been transmitted (BSC), or the last character of a frame or block as defined by TLAST (TCR bit 3) has been transmitted (COP).

TSR

5-3 —Not used.

TSR

2 TUNRN —Transmitter Underrun (BOP, BSC and COP only). A transmitter underrun occurs when the transmitter runs out of data during a transmission. For BOP, the underrun condition is treated as an abort. For BSC and COP, SYN characters are transmitted until more data is available in the Tx FIFO.

- 0 No transmitter underrun occurred.
1 Transmitter underrun occurred.

TSR

1 TFERR —Transmit Frame Error (BOP only).

- 0 No frame error has occurred.
1 No control field was present (short frame).

Transmitter Control Register (TCR)

7	6	5	4	3	2	1	0
TEN	TDSREN	TICS	0	TLAST	TSYN	TABT	TRES

Reset value = \$01

The Transmitter Control Register (TCR) selects transmitter control function.

TCR

7 TEN —Transmitter Enable.

- 0 Disable transmitter. TxD output is idled. The Tx FIFO may be loaded while the transmitter is disabled.
1 Enable transmitter.

TCR

6 TDSREN —Transmitter Data Service Request Enable.

- 0 Disable transmitter DMA mode.
1 Enable transmitter DMA mode.

TCR

5 TICS —Transmitter Idle Character Select. Selects the idle character to be transmitted when the transmitter is in an active idle mode (transmitter enabled or disabled).

0 Mark Idle (TxD output is held high).
1 Content of AR2 (BSC and COP), BREAK condition (ASYN and ISOC), or FLAG character (BOP).

TCR

4 —Not Used. This bit is initialized to 0 by RES and must not be set to 1.

TCR

3 TLAST —Transmit Last Character (BOP, BSC and COP only).

- 0 The next character is not the last character in a frame or block.
1 The next character to be written into the TDR is the last character of the message. The TLAST bit automatically returns to a 0 when the associated word/byte is written to the Tx FIFO. If the transmitter DMA mode is enabled, TLAST is set to a 1 by DONE from the DMAC. In this case the character written into the TDR in the current cycle is the last character.

TCR

2 TSYN —Transmit SYN (BSC and COP only).

- 0 Do not transmit SYN characters.
1 Transmit SYN characters. Causes a pair of SYN characters to be transmitted immediately following the current character. If BSC transparent mode is active, a DLE SYN sequence is transmitted. The TSYN bit automatically returns to a 0 when the SYN character is loaded into the Transmitter Shift Register.

TCR

1 TABT —Transmit ABORT (BOP only).

- 0 Enable normal transmitter operation.
1 Causes an abort by sending eight consecutive 1's. A data word/byte must be loaded into the Tx FIFO after setting this bit in order to complete the command. The TABT bit clears automatically when the subsequent data word/byte is loaded into the Tx FIFO.

TCR

0 TRES —Transmitter Reset Command.

- 0 Enable normal transmitter operation.
1 Reset transmitter. Clears the transmitter section including the Tx FIFO and the TSR (but not the TCR). The TxD output is held in "Mark" condition. TRES is set by RES or by writing a 1 into this bit for one write cycle and is cleared by writing a 0 into this bit. TRES requires clearing after RES.

Transmit Data Register (TDR)

7	6	5	4	3	2	1	0
MSB		Transmitted Data (TxFIFO)				LSB	

The transmitter has an 8-byte FIFO register file (Tx FIFO). Data to be transmitted is transferred from the bus into the Tx FIFO via the TDR. The TDRA status bit in the TSR is set to 1 when the Tx FIFO is ready to accept another data byte.

Transmitter Interrupt Enable Register (TIER)

7	6	5	4	3	2	1	0
TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	—

Reset value = \$00

The Transmitter Interrupt Enable Register (TIER) contains interrupt enable bits for the Transmitter Status Register. When enabled, the IRQ output is asserted when the corresponding condition is detected and reported in the TSR.

TIER

7 TDRA IE —Transmitter Data Register (TDR) Available Interrupt Enable.

- 0 Disable TDRA Interrupt.
1 Enable TDRA Interrupt.

TIER

6 TFC IE —Transmit Frame Complete (TFC) Interrupt Enable.

- 0 Disable TFC Interrupt.
1 Enable TFC Interrupt.

TIER

5-3 —Not used.

TIER

2 TUNRN IE —Transmitter Underrun (TUNRN) Interrupt Enable.

- 0 Disable TUNRN Interrupt.
1 Enable TUNRN Interrupt.

TIER

1 TFERR IE —Transmit Frame Error (TFERR) Interrupt Enable.

- 0 Disable TFERR Interrupt.
1 Enable TFERR Interrupt.

TIER

0 —Not used.

SERIAL INTERFACE REGISTERS

Serial Interface Status Register (SISR)

7	6	5	4	3	2	1	0
CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0

Reset value = \$00

The Serial Interface Status Register (SISR) contains the serial interface status information. The transition status bits (CTST, DSRT and DCDT) are cleared by writing a 1 into their respective positions, or by RESET. The level status bits (CTSLVL, DSRLVL and DCDLVL) reflect the state of their respective inputs and cannot be cleared internally. The IRQ output is asserted if any of the conditions reported by the transition status bits occur and the corresponding interrupt enable bit in the SIER is set.

SISR

- 7 CTST** —Clear to Send Transition Status.
 1 CTS has transitioned positive (from active to inactive). (TRES must be a zero).
 0 CTS has not transitioned positive.

SISR

- 6 DSRT** —Data Set Ready Transition Status.
 1 DSR has transitioned negative (from inactive to active).
 0 DSR has not transitioned negative.

SISR

- 5 DCDT** —Data Carrier Detect Transition Status.
 1 DCD has transitioned positive (from active to inactive).
 0 DCD has not transitioned positive.

SISR

- 4 CTSLVL** —Clear to Send Level.
 0 CTS input level is negated (high).
 1 CTS input level is asserted (low).

SISR

- 3 DSRLVL** —Data Set Ready Level.
 0 DSR input level is negated (high).
 1 DSR input level is asserted (low).

SISR

- 2 DCDLVL** —Data Carrier Detect Level.
 0 DCD input level is negated (high).
 1 DCD input level is asserted (low).

SISR

- 1-0** —Not used.

Serial Interface Control Register (SICR)

7	6	5	4	3	2	1	0
RTSLVL	DTRLVL	—	—	—	ECHO	TEST	NRZI

Reset value = \$00

The Serial Interface Control Register (SICR) controls various serial interface signals and test functions.

SICR

- 7 RTSLVL** —Request to Send Level.
 0 Negate RTS output (high).
 1 Assert RTS output (low).

NOTE

In BOP, BSC, or COP, when the RTSLVL bit is cleared in the middle of data transmission, the RTS output remains asserted until the end of the current frame or block has been transmitted. In ASYNC or ISOC, the RTS output is negated when the Tx FIFO is empty. If the transmitter is idling when the RTSLVL bit is reset, the RTS output is negated within two bit times.

SICR

- 6 DTRLVL** —Data Terminal Ready Level.
 0 Negate DTR output (high).
 1 Assert DTR output (low).

SICR

- 5-3** —Not used. These bits are initialized to 0 by RESET and must not be set to 1.

SICR

- 2 ECHO** —Echo Mode Enable.
 0 Disable Echo mode (enable normal operation).
 1 Enable Echo mode. Received data (RxD) is routed back through the transmitter to Tx D. The contents of the Tx FIFO is undisturbed. This mode may be used for remote test purposes.

SICR

- 1 TEST** —Self-test Enable.
 0 Disable self-test (enable normal operation).
 1 Enable self-test. The transmitted data (Tx D) and clock (Tx C) are routed back through to the receiver through RxD and RxC, respectively (DCD and CTS are ignored). This "loopback" self-test may be used for all protocols. RxC is external regardless of the state of CCR bit 2. CCR bit 3 may be a 0 or a 1.

SICR

- 0 NRZI** —NRZI Data Format Select. Selects the transmit and receive data format to be NRZ or NRZI.
 0 Select NRZ data format. NRZ coding—high = 1 and low = 0.
 1 Select NRZI data format. The serial data remains in the same state to send a binary 1 and switches to the opposite state to send a binary 0. A 1 bit delay is added to the Tx D output to allow for encoding.

Serial Interrupt Enable Register (SIER)

7	6	5	4	3	2	1	0
CTS IE	DSR IE	DCD IE	—	—	—	—	—

Reset value = \$00

The Serial Interrupt Enable Register (SIER) contains interrupt enable bits for the Serial Interface Status Register. When an interrupt enable bit is set, the $\overline{\text{IRQ}}$ output is asserted when the corresponding condition occurs as reported in the SISR.

SIER

<u>7</u>	CTS IE	—Clear to Send (CTS) Interrupt Enable.
0	Disable CTS Interrupt.	
1	Enable CTS Interrupt.	

SIER

<u>6</u>	DSR IE	—Data Set Ready (DSR) Interrupt Enable.
0	Disable DSR Interrupt.	
1	Enable DSR Interrupt.	

SIER

<u>5</u>	DCD IE	—Data Carrier Detect (DCD) Interrupt Enable.
0	Disable DCD Interrupt.	
1	Enable DCD Interrupt.	

SIER

<u>4-0</u>	—Not used.
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GLOBAL REGISTERS

The global registers contain command information applying to different modes of operation and protocols. After changing global register data, TRES in the TCR and RRES in the RCR should be set then cleared prior to performing normal mode processing.

Protocol Select Register 1 (PSR1)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	CTLEX	ADDEX

Reset value = \$00

Protocol Select Register 1 (PSR1) selects BOP protocol related options.

PSR1

<u>7-2</u>	—Not used.
------------	------------

PSR1

<u>1</u>	CTLEX	—Control Field Extend (BOP only).
0	Select 8-bit control field.	
1	Select 16-bit control field.	

PSR1

<u>0</u>	ADDEX	—Address Extend (BOP only).
0	Disable address extension. All eight bits of the address byte are utilized for addressing.	
1	Enable address extension. When bit 0 in the address byte is a 0 the address field is extended by one byte. An exception to the address field extension occurs when the first address byte is all 0's (null address).	

Protocol Select Register 2 (PSR2)

7	6	5	4	3	2	1	0
WD/BYT	STOP BIT SEL	CHAR LEN SEL	PROTOCOL SEL				
	SB2	SB1	CL2	CL1	PS3	PS2	PS1

Reset value = \$00

Protocol Select Register 2 (PSR2) selects protocols, character size, the number of stop bits, and word/byte mode.

PSR2

7

—Not Used. This bit is initialized to 0 by RES and must not be changed to 1.

PSR2

<u>6-5</u>	STOP BIT SEL	—Number of Stop Bits Select.
Selects the number of stop bits transmitted at the end of the data bins in ASYNC and ISOC modes.		

6	5	No. of Stop Bits	
SB2	SB1	ASYNC	ISOC
0	0	1	1
0	1	1-1/2	2
1	0	2	2

PSR2

<u>4-3</u>	CHAR LEN SEL	—Character Length Select. Selects the character length except in BOP and BSC where the character length is always eight bits. Parity is not included in the character length.
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4	3	Character Length
CL2	CL1	
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

PSR2

<u>2-0</u>	PROTOCOL SEL	—Protocol Select. Selects protocol and defines the protocol dependent control bits.
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2	1	0	Protocol
PS3	PS2	PS1	
0	0	0	BOP (Primary)
0	0	1	BOP (Secondary)
0	1	0	Reserved
0	1	1	COP
1	0	0	BSC EBCDIC
1	0	1	BSC ASCII
1	1	0	ASYNC
1	1	1	ISOC

Address Register 1 (AR1)

7	6	5	4	3	2	1	0
BOP ADDRESS/BSC & COP PAD							

Reset value = \$00

Address Register 2 (AR2)

7	6	5	4	3	2	1	0
BOP ADDRESS/BSC & COP SYN							

Reset value = \$00

The protocol selected in PSR2 (BOP, BSC and COP only) determines the function of the two 8-bit Address Registers (AR1 and AR2). As a secondary station in BOP, the contents of the address registers are used for address matching depending on the 2 ADCMP selection in the RCR. In BSC and COP, AR1 and AR2 contain programmable leading PAD and programmable SYN characters, respectively.

Address Register (AR) Contents

Protocol Selected	2ADCMP	AR1	AR2
BOP (Primary)	X	X	X
BOP (Secondary)	0	Address	X
	1	Address	Address
BSC EBCDIC	X	Leading PAD	SYN
BSC ASCII	X	Leading PAD	SYN
COP	X	Leading PAD	SYN
*X = Not used			

Baud Rate Divider Register 1 (BRDR1)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (LSH)							

Reset value = \$01

Baud Rate Divider Register 2 (BRDR2)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (MSH)							

Reset value = \$00

The two 8-bit Baud Rate Divider Registers (BRDR1 and BRDR2) hold the divisor of the Baud Rate Divider circuit. BRDR1 contains the least significant half (LSH) and BRDR2 contains the most significant half (MSH). With an 8.064 MHz EXTAL input, standard bit rates can be selected using the combination of Prescaler Divider (in the CCR) and Baud Rate Divider values shown in Table 3. For isochronous or synchronous protocols, the Baud Rate Divider value must be multiplied by two for the same Prescaler Divider value.

The Baud Rate Divider (BRD) value can be computed for other crystal frequency, prescaler divider and desired baud rate values as follows:

$$BRD = \frac{\text{Crystal Frequency}}{(\text{Prescaler Divider}) (\text{Baud Rate}) (K)}$$

where: K = 1 for isochronous or synchronous
2 for asynchronous

Clock Control Register (CCR)

7	6	5	4	3	2	1	0
—	—	—	PSCDIV	TCLKO	RCLKIN	CLK SEL	
						CK2	CK1

Reset value = \$00

The CCR selects various clock options.

CCR**7-5** —Not used.**CCR**

4 PSCDIV —Prescaler Divider. The Prescaler Divider network reduces the external/oscillator frequency to a value for use by the internal Baud Rate Generator.

0 Divide by 2.

1 Divide by 3.

CCR**3 TCLKO** —Transmitter Clock Output Select.

0 Select TxC to be an input.

1 Select TxC to be an output.

CCR

2 RCLKIN —Receiver Clock Internal Select (ASYNC only).

0 Select External RxC.

1 Select Internal RxC.

CCR

1-0 CLK DIV —External Receiver Clock Divider. Selects the divider of the external RxC to determine the receiver data rate.

CK2	CK1	Divider
0	0	1 (ISOC)
0	1	16
1	0	32
1	1	64

Table 3. Standard Baud Selection (8.064 MHz Crystal)

Desired Baud Rate (Bt Rate)	Prescaler Divider		Baud Rate Divider					
			Asynchronous			Isochronous and Synchronous		
	Decimal Value	PSCDIV (0 to 1)	Decimal Value	Hexadecimal Value		Decimal Value	Hexadecimal Value	
				BRDR2 (MSH)	BRDR1 (LSH)		BRDR2 (MSH)	BRDR1 (LSH)
50	3	1	26,880	69	00	53,760	D2	00
75	2	0	26,880	69	00	53,760	D2	00
110	3	1	12,218	2F	BA	24,436	5F	74
135	2	0	14,933	3A	55	29,866	74	AA
150	3	1	8,960	23	00	17,920	46	00
300	2	0	6,720	1A	40	13,440	34	80
1200	3	1	1,120	04	60	2,240	08	C0
1800	2	0	1,120	04	60	2,240	08	C0
2400	2	0	840	03	48	1,680	06	90
3600	2	0	560	02	30	1,120	04	60
4800	3	1	280	01	18	560	02	30
7200	2	0	280	01	18	560	02	30
9600	3	1	140	00	0C	280	01	18
19200	3	1	70	00	46	140	00	8C
38400	3	1	35	00	23	70	00	46

Error Control Register (ECR)

7	6	5	4	3	2	1	0
PAREN	ODDPAR	—	—	CRCCTL	CRCPRE	CRCSEL	
						CR2	CR1

Reset value = \$04

The Error Control Register (ECR) selects the error detection method used by the MPCC.

ECR

7 PAREN —Parity Enable. (ASYNC, ISOC and COP only).

0 Disable parity generation/checking.

1 Enable parity generation/checking.

ECR

6 ODDPAR —Odd/Even Parity Select (Effective only when PAREN = 1).

0 Generate/check even parity.

1 Generate/check odd parity.

ECR

5-4 —Not used.

ECR

3 CFCRC —Control Field CRC Enable.

0 Disable control field CRC. Enables an intermediate CRC remainder to be appended after the address/control field in transmitted BOP frames and checked in received frames. The CRC generator is reset after control field CRC calculation.

ECR

2 CRCPRE —CRC Generator Preset Select.

0 Preset CRC Generator to 0.

1 Preset CRC Generator to 1 and transmit the 1's complement of the resulting remainder.

ECR

1-0 CRCSEL —CRC Polynomial Select. Selects one of the RC polynomials.

1	0	
CR2	CR1	Polynomial
0	0	$x^{16} + x^{12} + x^5 + 1$ (CCITT V.41)
0	1	$x^{16} + x^{15} + x^2 + 1$ (CRC-16)
1	0	$x^8 + 1$ (VRC/LRC)*
1	1	Not used.

*VRC: Odd-parity check is performed on each character including the LRC character.

INPUT/OUTPUT FUNCTIONS

MPU INTERFACE

Transfer of data between the MPCC and the system bus involves the following signals: Address lines A0 through A4, Data Bus Lines D0 through D7, and control signals consisting of R/W, \overline{CS} , and $\phi 2$. Figures 10 and 11 show typical interface connections.

Read/Write Operation

The R/W input controls the direction of data flow on the data bus. \overline{CS} (Chip Select) enables the MPCC for access to the internal registers and other operations. When \overline{CS} is asserted, the data I/O buffer acts as an output driver during a read operation and as an input buffer during a write operation.

When the MPCC is selected (\overline{CS} low) during a read (R/W high), eight bits of register data are placed on data bus lines D0 – D7 when $\phi 2$ is asserted. When the MPCC is selected (\overline{CS} low) for a write (R/W low), $\phi 2$ strobes data from the D0 – D7 data lines into the selected register. Figures 12 and 13 show the read and write timing relationships.

DMA INTERFACE

The MPCC is capable of providing DMA data transfers up to 2 Mbytes per second when used with the MC68440 DMAC in the single address mode. Based on 4 Mb/s serial data rate and 5 bits/character, the maximum DMA required transfer rate is 800 Kbytes per second.

The MPCC has separate DMA enable bits for the transmitter and receiver, each of which requires a DMA channel. Both the transmitter and receiver data are implicitly addressed (TDR or RDR) therefore addressing of the data register is not required before data may be transferred. Communication between the MPCC and the DMAC is accomplished by a two-signal request/acknowledge handshake. Since the MPCC has only one acknowledge input (\overline{DACK}) for its two DMA request lines, an external OR function must be provided to combine the two DMA acknowledge signals. The MPCC uses the R/W input to distinguish between the Transmitter Data Service Request (\overline{TDSR}) acknowledge and the Receiver Data Service Request (\overline{RDSR}) acknowledge.

Receiver DMA Mode

The receiver DMA mode is enabled when the RDSREN bit in the RCR is set to 1. When data is available in the Rx FIFO, Receiver Data Service Request (\overline{RDSR}) is asserted for one receiver clock period to initiate the MPCC to memory DMA transfer. The next \overline{RDSR} cycle may be initiated as soon as the current \overline{RDSR} cycle is completed (i.e., a full sequence of \overline{DACK} , $\phi 2$, and \overline{DTS}).

In response to \overline{RDSR} assertion, the DMAC sets the R/W line to write and asserts the memory address, DMA transfer strobe (\overline{DTS}), and DMA acknowledge (\overline{DACK}). The MPCC outputs data from the Rx FIFO to the data bus during $\phi 2$. The memory latches the data to complete the data transfer. Figure 13 shows the timing relationships for the receiver DMA mode.

\overline{RDSR} is inhibited when either RDSREN is reset to 0 or RRES is set to 1 (both in the RCR), or when \overline{RES} is asserted.

Transmitter DMA Mode

The transmitter DMA mode is enabled when the TDSREN bit in the TCR is set to 1. When the Tx FIFO is available, Transmitter Data Service Request (\overline{TDSR}) is asserted for one transmitter clock period to initiate the memory to MPCC DMA transfer. The next \overline{TDSR} cycle may be initiated as soon as the current \overline{TDSR} cycle is completed.

In the transmitter DMA mode, the Tx FIFO is implicitly addressed. That is, when the transfer is from memory to the Tx FIFO, only the memory is addressed. In response to \overline{TDSR} assertion, the DMAC sets the R/W line to read and asserts the memory address, DMA transfer strobe (\overline{DTS}) and DMA acknowledge (\overline{DACK}). The memory places data on the data bus and the MPCC loads the data into the Tx FIFO to complete the data transfer. A timing diagram for the transmitter DMA mode is shown in Figure 15.

\overline{TDSR} is inhibited when either TDSREN is reset to 0 or TRES is set to 1 (both in the TCR), or when \overline{RES} is asserted.

DONE Signal

When the DMA transfer count is exhausted in transmitter DMA mode, the DMAC asserts \overline{DONE} which sets the \overline{LAST} bit in the TCR to indicate that the last word/byte has been transferred. In the receiver DMA mode, \overline{DONE} is asserted by the MPCC when the last character of the frame/block is being transferred from the Rx FIFO to the data bus if the \overline{DONEEN} bit is set to a 1 in the RCR.

INTERRUPTS

There are three possible sources of an interrupt request (\overline{IRQ}): the receiver section (as reported in the RSR), the transmitter section (as reported in the TSR), and the serial interface (as reported in the SISR). When an interrupt generating status occurs and the interrupt is enabled by a corresponding bit in the associated interrupt enable register, \overline{IRQ} is asserted. The interrupt processing software must examine all status registers that have interrupt status bits enabled to determine the cause of the interrupt and perform the required processing to clear the interrupt. \overline{IRQ} will remain asserted until all interrupt causing conditions reported in status registers have been cleared.

SERIAL INTERFACE

The MPCC is a high speed, high performance device supporting the more popular bit and character oriented data protocols. The lower speed asynchronous (ASYNC) and isochronous (ISOCH) modes are also supported. An on-chip clock oscillator and baud rate generator provide an output data clock at a frequency of DC to 4 MHz. The clock can also be used in the ASYNC mode to provide a receive clock for the incoming data. The serial interface consists of the following signals:

RTS (Request to Send) Output

The **RTS** output to the DCE is controlled by the **RTSLVL** bit in the **SICR** in conjunction with the state of the transmitter section. When the **RTSLVL** bit is set to 1, the **RTS** output is asserted. When the **RTSLVL** bit is reset to 0, the **RTS** output remains asserted until the **TxFIFO** becomes empty or the end of the message (or frame), complete with CRC code if any, has been transmitted. **RTS** also is negated when the **RTSLVL** bit is reset during transmitter idle, or when the **RES** input is asserted.

CTS (Clear to Send) Input

The **CTS** input signal is normally generated by the DCE to indicate whether or not the data set is ready to transmit data. The **CTST** bit in the **SISR** reflects the transition status of the **CTS** input while the **CTSLVL** bit in the **SISR** reflects the current level. A positive transition on the **CTS** pin asserts **IRQ** if the **CTS IE** bit in the **SIER** is set. The **CTS** input in an inactive state disables the start of transmission.

DCD (Data Carrier Detect) Input

The **DCD** input signal is normally generated by the DCE and indicates that the DCE is receiving a data carrier signal suitable for demodulation. The **DCDT** bit in the **SISR** reports the transition status of the **DCD** input while the **DCDLVL** bit in the **SISR** contains the current level. A positive transition on the **DCD** pin asserts the **IRQ** output if the **DCD IE** bit in the **SIER** is set. A negated **DCD** input disables the start of the receiver.

DSR (Data Set Ready) Input/RSYN Output

The **DSR** input from the DCE indicates the status of the local data set. The **DSRT** bit in the **SISR** contains the transition status of the **DSR** input while the **DSRLVL** bit in the **SISR** reports the current level. A negative transition on the **DSR** pin asserts the **IRQ** output if the **DSR IE** bit in the **SIER** is set.

When the **RSYN** bit in the **RCR** is set to 1, the frame synchronization signal (**RSYN**) in the receiver is output on the **DSR** pin. In this mode, **DSR** output low indicates detection of **SYN** in **BSC** or **COP**, or an address match in **BOP**.

DTR (Data Terminal Ready) Output

The **DTR** output is general purpose in nature and can be used to control switching of the DCE. The **DTR** output is controlled by the **DTRLVL** bit in the **SICR**.

TxC (Transmitter Clock) Input/Output

The transmitter clock (**TxC**) may be programmed to be input or an output. When the **TCLKO** control bit in the **CCR** is set to a 1, the **TxC** pin becomes an output and provides the DCE with a clock whose frequency is determined by the internal baud rate generator. When the **TCLKO** control bit is reset, **TxC** is an input and the transmitter shift timing must be provided externally. The **TxD** output changes state on the negative-going edge of the transmitter clock. In the asynchronous mode when **TCLKO** = 0 in the **CCR**, the **TxC** input frequency must be two times the desired baud rate.

TxD (Transmitted Data) Output

The serial data transmitted from the MPCC is coded in **NRZ** or **NRZI** (zero complement) data format as selected by the **NRZI** control bit in the **SICR**.

RxC (Receiver Clock) Input

The receiver latches data on the negative transition of the **RxC**.

RxD (Received Data) Input

The serial data received by the MPCC can be coded in **NRZ** or **NRZI** data format. The MPCC will decode the received data in accordance with the **NRZI** control bit setting in the **SICR**.

Serial Interface Timing

The timing for the serial interface clock and data lines is shown in Figure 16. The MPCC supports high speed synchronous operation. As shown, the **TxD** output changes with the negative-going edge of **TxC** and the received data on **RxD** is latched on the negative edge of **RxC**. This assures high speed two-way operation between two MPCCs connected as shown in Figure 18.

For low speed operation between the MPCC and a modem or **RS-232C** Data Communications Equipment (DCE), an inverter can be used in the **TxC** output lines as shown in Figure 18. **RS-232** and **RS-423** (covering serial data interface up to 100K baud) require that data be centered $\pm 25\%$ about the negative-going edge of the **RxC**. This criteria is met for frequencies up to 1.25 MHz using the inverter. Use of the inverter also allows MPCC to MPCC operation up to 2.17 MHz.

SERIAL COMMUNICATION MODES AND PROTOCOLS**ASYNCHRONOUS AND ISOCRONOUS MODES**

Asynchronous and isochronous data are transferred in frames. Each frame consists of a start bit, 5 to 8 data bits plus optional even or odd parity, and 1, 1½, or 2 stop bits. The data character is transmitted with the least significant bit (**LSB**) first. The data line is normally held high (**MARK**) between frames, however, a **BREAK** (minimum of one frame length for which the line is held low) is used for control purposes. Figure 4 illustrates the frame format supported by the MPCC.

Asynchronous Receive

In the asynchronous (**ASYN**) mode, data received on **RxD** occurs in three phases: (1) detection of the start bit and bit synchronization, (2) character assembly and optional parity check, and (3) stop bit detection. The receiver bit stream may be synchronized by the internal baud rate generator clock or by an external clock on **RxC**. When **RCLKIN** in the **CCR** is set to 0, an external clock with a frequency of 16, 32, or 64 times the data rate establishes the data bit midpoint and maintains bit synchronization. The character assembly process does not start if the start bit is less than one-half bit time. Framing and parity errors are detected and buffered along with the character on which errors occurred. They are passed on to the **RxFIFO** and set appropriate status bits in the **RSR** when the character with an error reaches the last **RxFIFO** register where it is ready to be transferred onto the data bus via the **RDR**.

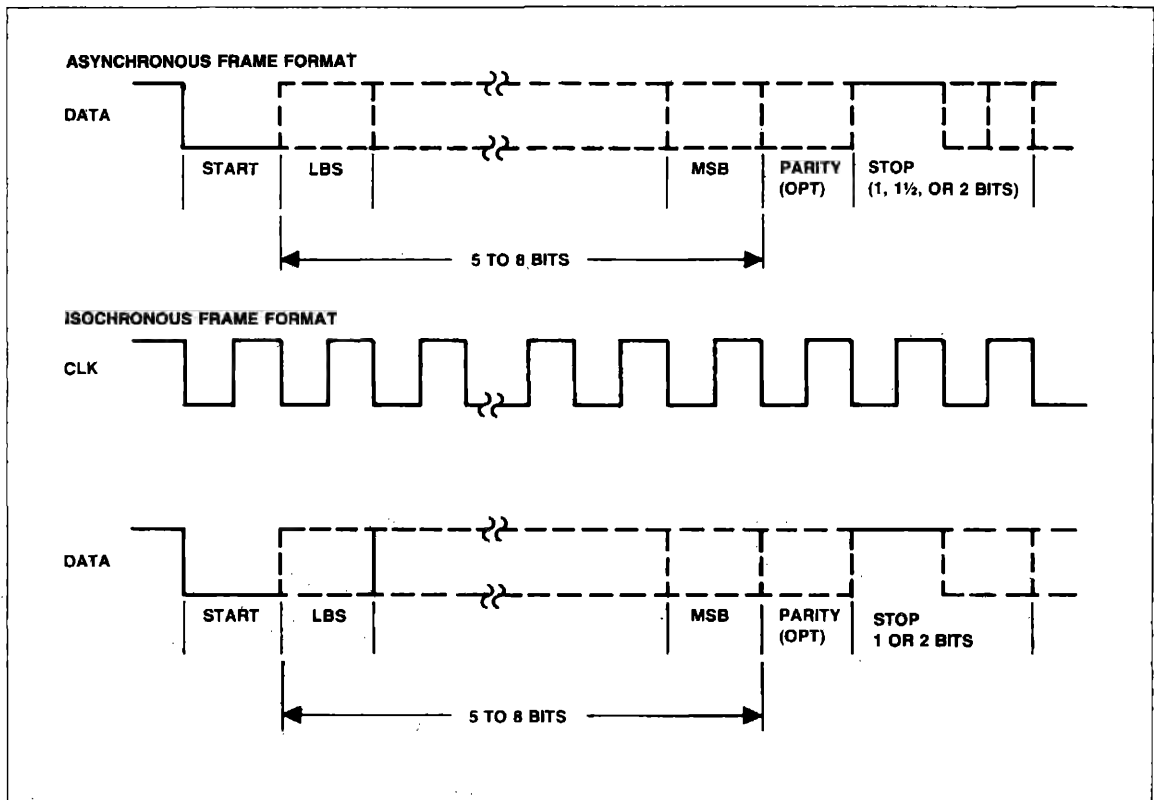


Figure 4. Asynchronous and Isochronous Frame Format

Isochronous Receive

In the isochronous (ISOC) mode, a 1 times clock on RxC is required with the data on RxD and the serial data bit is latched on the falling edge of each clock pulse. The requirement for the detection of a valid start bit, or the beginning of a break, is satisfied by the detection of a high-to-low transition on the serial data input line. Error detection and status indication are the same as the asynchronous mode.

Asynchronous and Isochronous Transmit

In asynchronous and isochronous transmit modes, output data transmission on TxD begins with the start bit. This is followed by the data character which is transmitted LSB first. If parity generation is enabled, the parity bit is transmitted after the MSB of the character.

SYNCHRONOUS MODES

In synchronous modes, a one-times clock is provided along with the data. Serial output data is shifted out and input data is latched on the falling edge of the clock.

BIT ORIENTED PROTOCOLS (BOP)

In bit oriented protocols (BOP), messages (data) are transmitted and received in frames. Each frame contains an opening flag, address field, control field, frame check sequence, and a closing flag. A frame may also contain an information field. (See Figure 5).

The opening flag is a special character whose bit pattern is 01111110. It marks the frame boundaries and is the interframe fill character. The address field of a frame contains the address of the secondary station which is receiving or responding to a command. The address field may be one or more bytes long. The address field can be extended by setting the ADDEX bit to a 1 in PSR1. In this case, the address field will be extended until the occurrence of an address byte with a 1 in bit 0. Up to two bytes of the address field may be automatically checked when the MPCC is programmed to be a secondary station in BOP. An automatic check for global (11111111) or null (00000000) address is also made. The control field of one or two bytes is transparent to the MPCC and sent directly to the host without interpretation.

The optional information field consists of 8-bit characters. Cyclic redundancy checking is used for error detection and the CRC remainder resulting from the calculation is transmitted as the frame check sequence field. For BOP, the polynomial $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) should be used, i.e., selected in the CRC SEL bits in the ECR. The registers representing the CRC-CCITT polynomial are generally preset to all 1s, and the 1s complement of the resulting remainder is transmitted. (See X.25 Recommendation.)

Zero insertion/deletion is employed to prevent valid frame data from being confused with the special characters. A 0 is inserted by the transmitter after every fifth consecutive 1 in the data stream. These inserted zeros are removed by the receiver to restore the data to its original form. The inserted zeros are not included in the CRC calculation.

The end of the frame is determined by the detection of the closing Flag special character which is the same as the opening Flag.

With the control options offered by the MPCC, commonly used bit oriented protocols such as SDLC, HDLC and X.25 standards can be supported. Figure 6 compares the requirements of these options.

BOP Receiver Operation

In BOP, the receiver starts assembling characters and accumulating CRC immediately after the detection of a Flag. The receiver also continues to search for additional Flag, or Abort, characters on a bit-by-bit basis. Zero deletion is implemented in the Receiver Shift Register after the Flag detection logic and before the CRC circuitry. The receiver recognizes the shared flag (the closing flag for one frame serves as the opening flag for the next frame) and the shared zero (the ending 0 of a closing flag serves as the beginning 0 of an opening flag forming the pattern "0111110111110."

Character assembly and CRC accumulation are stopped when a closing Flag or Abort is detected. The CRC accumulation includes all the characters between the opening Flag and the closing Flag. The contents of the CRC register are checked

at the close of a frame and the C/PERR bit in the RSR is updated. The FCS and the Flag are not passed on to the RxFIFO.

If the Flag is a closing flag, checks for short frame (no control field) and CRC error conditions are made and the appropriate status is updated. When an Abort (seven 1s) is detected, the remaining frame is discarded and the FA/B bit is set in the RSR. When a link idle (15 or more consecutive 1s) is detected, the RIDLE status bit is set in the RSR. The zeros that have been inserted to distinguish data from special characters are detected and deleted from the data stream before characters are assembled. The MPCC programmed as a secondary station provides automatic address matching of up to two bytes. If there is no address match, the receiver (secondary station) ignores the remainder of the frame by searching for the Flag. If there is a match, the address bytes are transferred to the RxFIFO as they are assembled.

For the control field, one or two bytes are assembled and passed on to the RxFIFO depending on the state of the extended control field bit.

If the CFCRC bit in the ECR is set to 1, an intermediate CRC check will be made after the address and control field. The Frame Check Sequence is still calculated over the remainder of the frame.

BOP Transmitter Operation

In BOP, the TxFIFO can be preloaded through the TDR while the transmitter is disabled (TEN = 0 in the TCR). When the transmitter is enabled (TEN = 1 in the TCR), the leading FLAG is automatically sent prior to transmitting data from the TxFIFO. The TDRA bit is set to 1 in the TSR as long as TxFIFO is not full. If an underrun occurs, the TUNRN bit in the TSR is set to a 1 and an ABORT (1111111) is transmitted followed by continuous FLAGs or marks until a new sequence is initiated.

The TLAST bit in the TCR must be set prior to loading the last character of the message to signal the transmitter to append the two-byte Frame Check Sequence (FCS) following the last character. If the transmitter DMA mode is selected (the TDSREN bit set to 1 in the TCR) the TLAST bit is set by the DONE signal from the DMAC.

FLAG 01111110	ADDRESS 1 OR N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES (OPTIONAL)	FCS 2 BYTES	FLAG 01111110
------------------	----------------------------	----------------------------	--------------------------------------	----------------	------------------

Figure 5. Bit Oriented Protocol (BOP) Frame Format

IBM SDLS FRAME FORMAT

FLAG 01111110	ADDRESS 1 BYTE	CONTROL 1 BYTE	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110
------------------	-------------------	-------------------	------------------------	----------------	------------------

ADCCP/HDLC FRAME FORMAT

FLAG 01111110	ADDRESS N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110
------------------	--------------------	----------------------------	------------------------	----------------	------------------

Figure 6. Implemented Bit Oriented Protocols

A message may be terminated at any time by setting the TABT bit in the TCR to 1. This causes the transmitter to send an Abort character followed by the remainder of the current frame data in the TxFIFO.

The serial data from the Transmitter Shift Register is continuously monitored for five consecutive 1s, and a 0 is inserted in the data stream each time this condition occurs (excluding Flag and Abort characters).

CRC accumulation begins with the first non-Flag character and includes all subsequent characters. The CRC remainder is transmitted as the FCS following the last data character. If the CTLCRC bit in the ECR is set to 1, an intermediate CRC remainder is appended after the Address and Control field. The final Frame Check Sequence is calculated over the balance of the frame.

BISYNC (BSC)

The structure of messages utilizing the IBM Binary Synchronous Communications (BSC) protocol, commonly called Bisync, is shown in Figure 7. The MPCC can process both transparent and nontransparent messages using either the EBCDIC or the ASCII codes. The CRC-16 polynomial should be selected by setting the appropriate CRCSEL bits in the ECR for both transparent and non-transparent EBCDIC and for transparent ASCII coded messages. VRC/LRC should be selected for non-transparent ASCII coded messages. BSC messages are formatted using defined data-link control characters. Data-link control characters generated and recognized by the MPCC are listed in Table 4.

Table 4. BSC Data-Link Control Characters

ASCII			EBCDIC		
Command	Byte 1	Byte 2	Command	Byte 1	Byte 2
SYN	16*	—	SYN	32*	—
SOH	01	—	SOH	01	—
STX	02	—	STX	02	—
ETB	17	—	EOB (ETB)	26	—
ETX	03	—	ETX	03	—
ENQ	05	—	ENQ	2D	—
DLE	10	—	DLE	10	—
ITB	1F	—	ITB	1F	—
EOT	04	—	EOT	37	—
ACK N*	10	30-37	ACK 0	10	70
NAK	15	—	ACK 1	10	61
WACK	10	3B	NAK	3D	—
RVI	10	3C	WACK	10	6B
			RVI	10	7C

Note: *Programmable

A heading is a block of data starting with an SOH and containing one or more characters that are used for message control (e.g., message identification, routing, and priority). The SOH initiates the block-check-character (BCC) accumulation, but is not included in the accumulation. The heading is terminated by STX when it is part of a block containing both heading and text. A block containing only a heading is terminated with an ITB or an ETB followed by the BCC. Only the first SOH or STX in a transmission block following a line turnaround causes the BCC to reset. All succeeding STX or SOH characters are included in the BCC. This permits the entire transmission (excluding the first SOH or STX) to be block-checked.

The text data is transmitted in complete units called messages, which are initiated by STX and concluded with ETX. A message can be subdivided into smaller blocks for ease in processing and more efficient error control. Each block starts with STX and ends with ETB (except for the last block of a message, which ends with ETX). A single transmission can contain any number of blocks (ending with ETB) or messages (ending with ETX). An EOT following the last ETX block indicates a normal end of transmission. Message blocking without line turnaround can be accomplished by using ITB (see the Additional Data Link Capabilities section, IBM GA 27-3004-2).

Two modes of data transfers are used in BSC. In non-transparent mode, data link control characters may not appear as text data. In transparent mode, each control character is preceded by a data link escape (DLE) character to differentiate it from the text data. Table 5 indicates which control characters are excluded in the CRC generation. All characters not shown in the table are included in the CRC generation. Figure 8 shows various formats for Control/Response Blocks and Heading and Text Blocks.

Table 5. BSC Control Sequences — Inclusion in CRC Accumulation

Character of Sequence	Included in CRC Accumulation	
	Yes	No
TSYN	—	DLESYN
TSOH	—	DLESOH
TSTX*	—	DLESTX
TETB	ETB	DLE
TETX	ETX	DLE
TDLE	(DLE)DLE	DLE(DLE)

* If not preceded within the same block by transparent heading information.

LEADING PAD 1 BYTE (AR1)	SYN 1 BYTE (AR2)	SYN 1 BYTE (AR2)	BODY	BCC	TRAILING PAD 11111111
--------------------------------	------------------------	------------------------	------	-----	-----------------------------

Figure 7. BSC Block Format

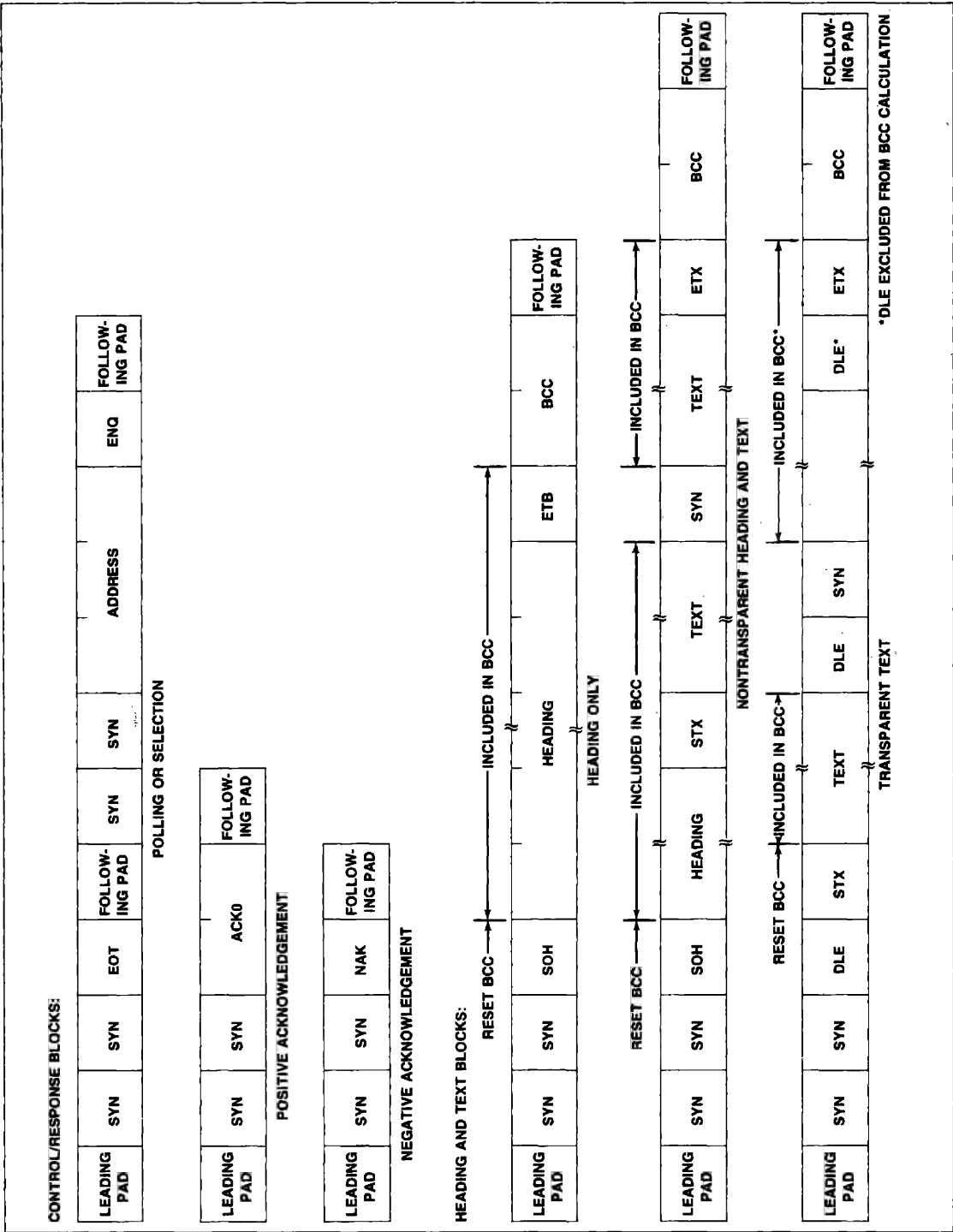


Figure 8. BSC Message Format Examples

BSC Receiver Operation

Character length defaults to eight bits in BSC mode. When ASCII is selected, the eighth bit is used for parity provided that VRC/LRC polynomial is selected. Character assembly starts after the receipt of two consecutive SYN characters. Serial data bits are shifted through the Receiver Shift Register into the Serial-to-Parallel Register and transferred to the RxFIFO. The RDA status bit in the RSR is set to 1 each time data is transferred to the RxFIFO. The SYN character in non-transparent mode and DLE-SYN pairs in transparent mode are discarded.

The receiver starts each block in the non-transparent mode. It switches to transparent mode if a block begins with a DLE-SOH or DLE-STX pair. The receiver remains in transparent mode until a DLE-ITB, DLE-ETB, DLE-ETX or DLE-ENQ pair is received. BCC accumulation begins after an opening SOH, STX, or DLE-STX. SYN characters in non-transparent mode or DLE-SYN pairs in transparent mode are excluded from the BCC accumulation. The first DLE of a DLE-DLE sequence is not included in the BCC accumulation and is discarded. The BCC is checked after receipt of an ITB, ETB, or ETX in non-transparent mode or DLE-ITB, DLE-ETB, DLE-ETX in transparent mode. If a CRC error is detected, the C/PERR and EOF bits in the RSR are set to 1. If no error is detected only the EOF bit is set. If the closing character was an ITB, BCC accumulation and character assembly starts again on the first character following the BCC.

BSC Transmitter Operation

BSC transmission begins with the sending of an opening pad (PAD) and two sync (SYN) characters. These characters are programmable and stored in AR1(PAD) and AR2(SYN). SOH or STX initiates the block-check-character (BCC) accumulation. An initial SOH or STX is not included in the BCC accumulation. Should an underrun condition occur, the content of AR2 (normally SYN character) is transmitted until new characters become available.

The message is terminated by the transmission of the BCC followed by a closing pad when an ETB, ITB, or ETX is fetched from the TxFIFO. The closing PAD is generated by the MPCC.

In transparent mode, the BCC accumulation is initiated by DLE-STX and is terminated by the sequences DLE-ETX, DLE-ETB, or DLE-ITB. See Table 5 for character sequence and inclusion in CRC accumulation. If an underrun occurs, DLE-SYN characters will be transmitted until new characters are available in the TxFIFO, ETC, ETX, ITB, or ENQ with a TLAST tag is treated as a control character and the MPCC automatically inserts a DLE immediately preceding these characters, DLE-ETB, DLE-ETX, DLE-ITB, or DLE-ENQ terminates a block of transparent text, and returns the data link to normal mode. BCC generation is not used for messages beginning with characters other than SOH, STX, DLE-SOH, or DLE-STX. On all message types, if the TSYN bit is set to 1 in the TCR, a SYN-SYN (DLE-SYN sequence on transparent messages) sequence is transmitted before the next character is fetched from the TxFIFO.

CHARACTER ORIENTED PROTOCOLS

The character oriented protocol (COP) option uses the format shown in Figure 9. It may be used for various character oriented protocols with 5-8 bit character sizes and optional parity checking. The input data is checked on a bit-by-bit basis for a pair of consecutive SYN characters to establish character synchronization. These SYN characters are discarded after detection. The PAD and SYN characters may be 5-8 bits long and are user programmable as stored in AR1 and AR2, respectively.

If parity checking is enabled the characters assembled after character sync are checked for parity errors. If STRSYN is set in the RCR, all SYN characters detected within the message will be discarded and will not be passed on to the RxFIFO. If STRSYN is reset, SYNs detected within the message will be treated as data.

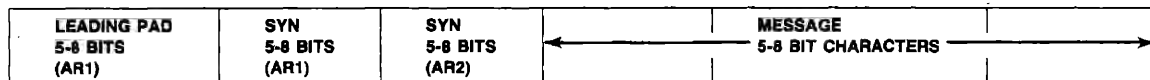


Figure 9. Character Oriented Protocol Format

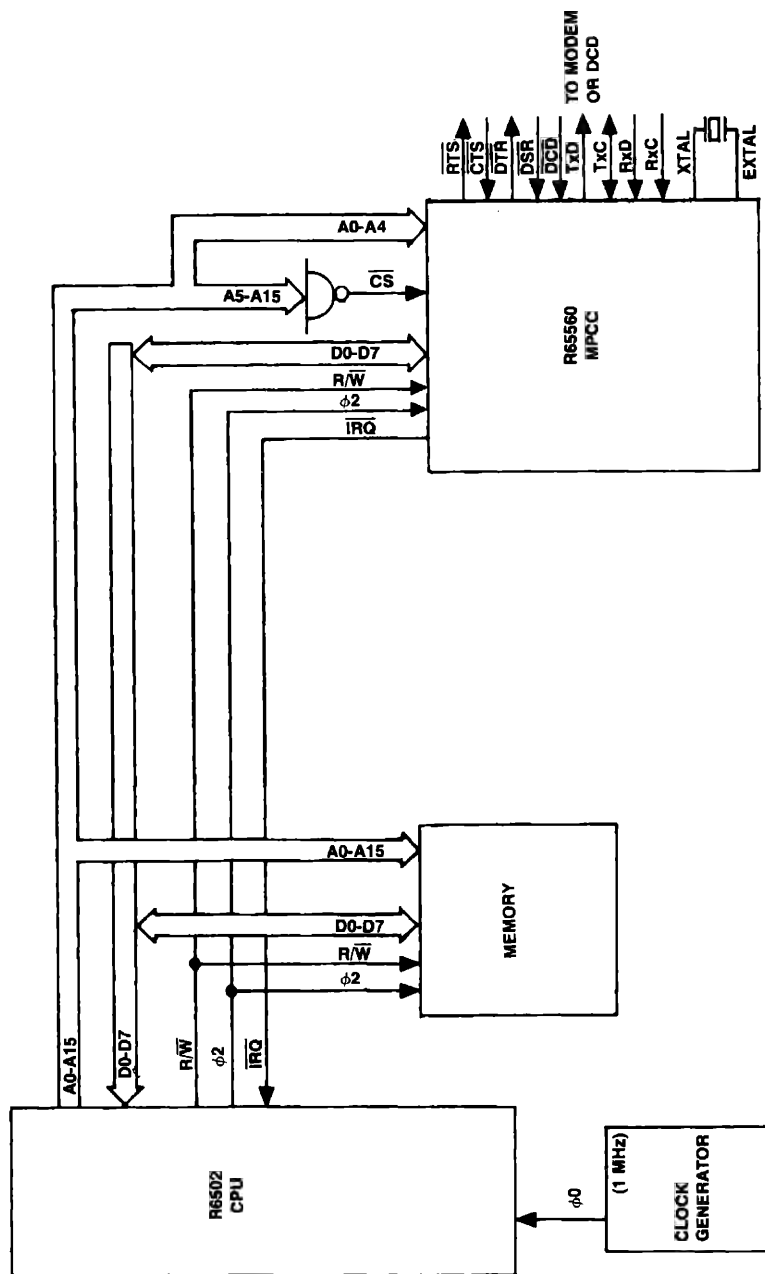


Figure 10. Typical Interface to 6500-Based System

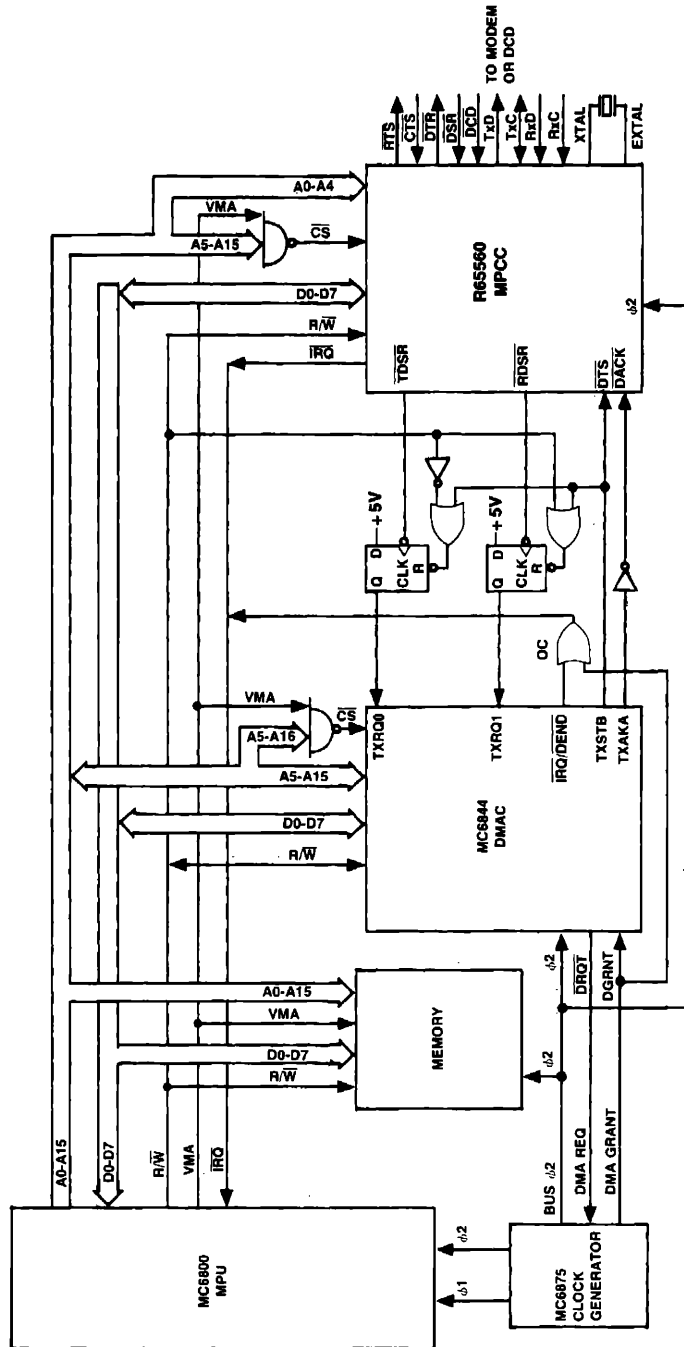
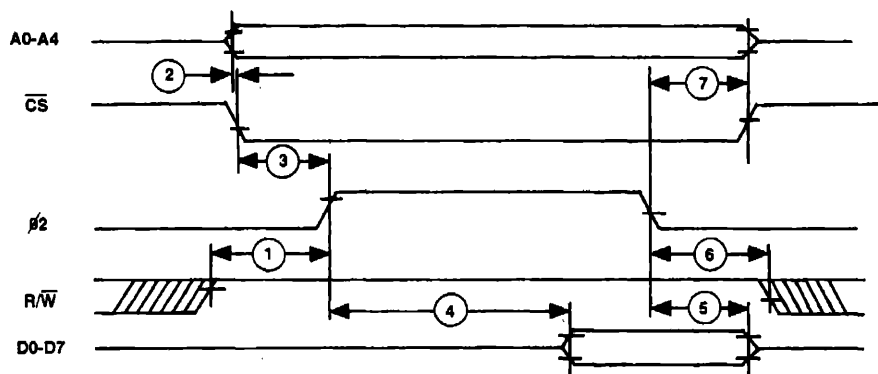
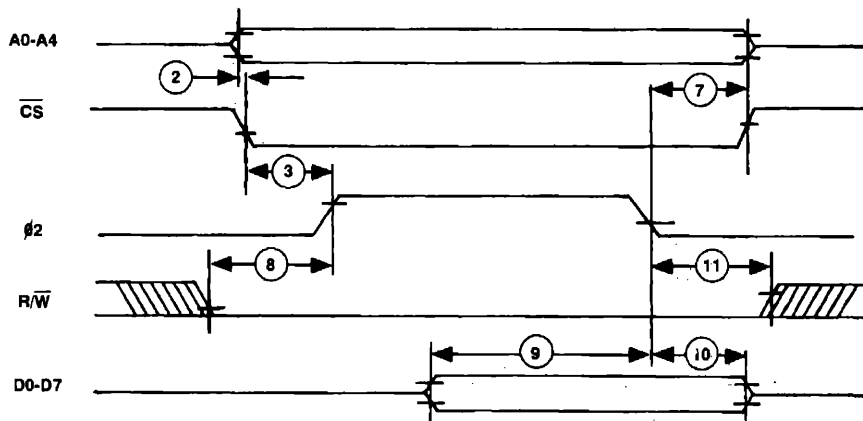


Figure 11. Typical Interface to 6800-Based System



NOTES: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 12. MPCC Read Cycle Timing



NOTES: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 13. MPCC Write Cycle Timing

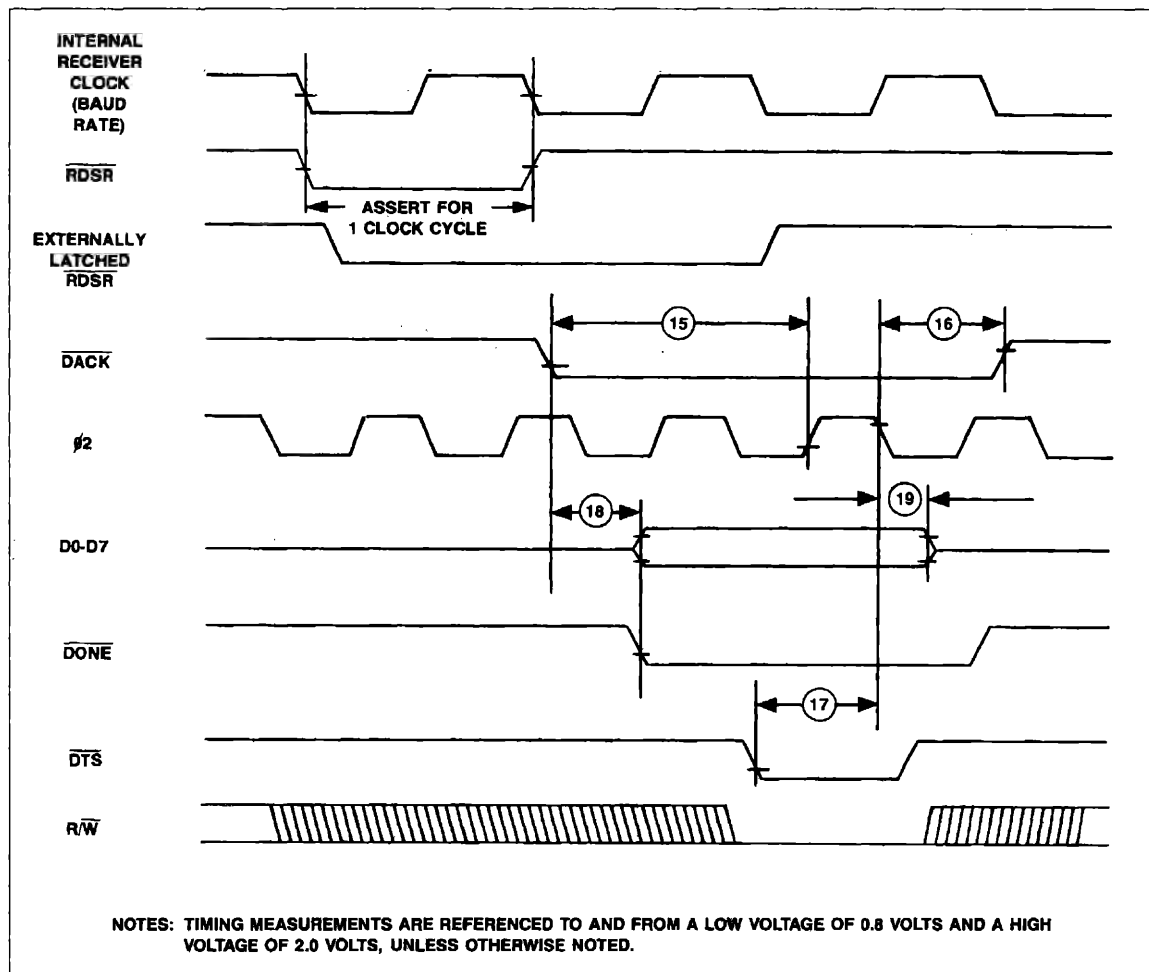


Figure 14. MPCC to Memory DMA Transfer Cycle Timing (Receiver DMA Mode).

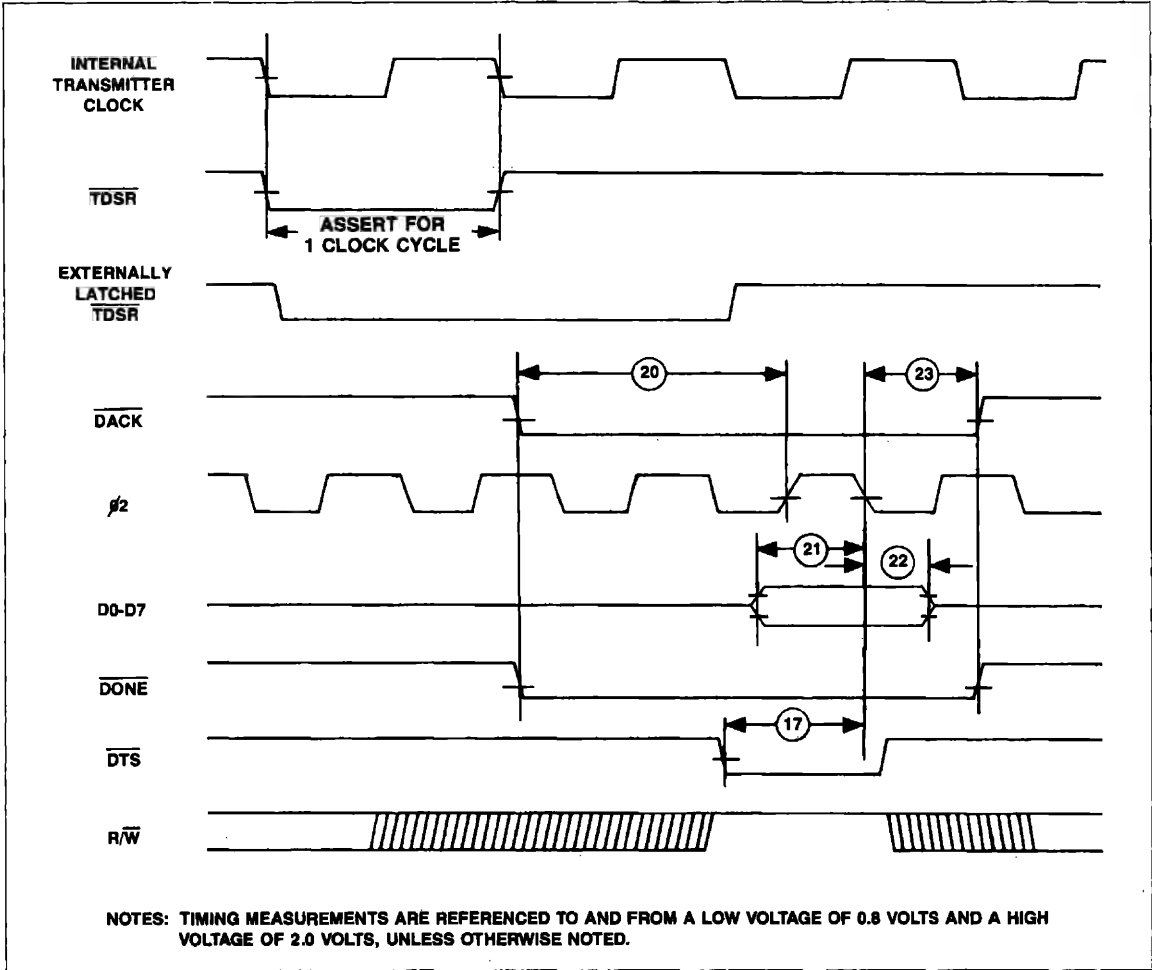


Figure 15. Memory to MPCC DMA Transfer Cycle Timing (Transmitter DMA Mode).

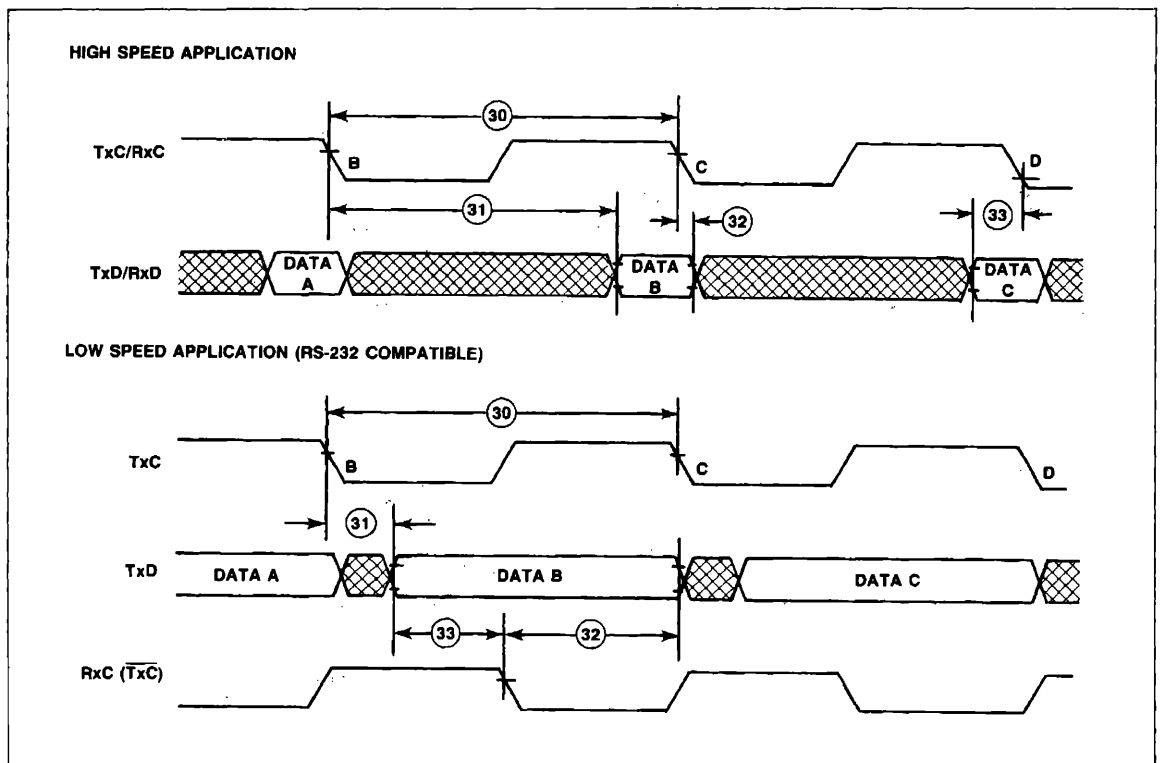


Figure 16. Serial Interface Timing

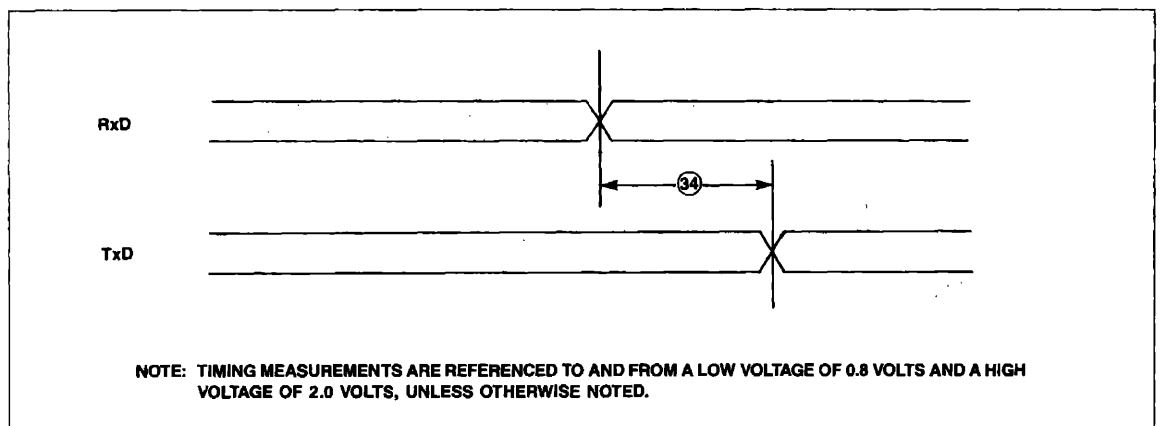


Figure 17. Serial Interface Echo Mode Timing

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Number	Parameter	Symbol	Min	Max	Unit
1	R/W High to $\overline{\text{O2}}$ High	t_{RH2H}	0	—	ns
2	Address Valid to $\overline{\text{CS}}$ Low	t_{AVSL}	30	—	ns
3	$\overline{\text{CS}}$ Low to $\overline{\text{O2}}$ High	t_{SL2H}	30	—	ns
4	$\overline{\text{O2}}$ High to Data Valid	t_{2HDV}	0	140	ns
5	$\overline{\text{O2}}$ Low to Data Invalid	t_{2LDXR}	10	150	ns
6	$\overline{\text{O2}}$ Low to R/W Low	t_{2LRL}	20	—	ns
7	$\overline{\text{O2}}$ Low to Address Invalid	t_{2LAI}	20	—	ns
8	R/W Low to $\overline{\text{O2}}$ High	t_{RL2H}	0	—	ns
9	Data Valid to $\overline{\text{O2}}$ Low	t_{DV2L}	60	—	ns
10	$\overline{\text{O2}}$ Low to Data Invalid	t_{2LDXW}	0	—	ns
11	$\overline{\text{O2}}$ Low to R/W High	t_{2LRH}	20	—	ns
15	$\overline{\text{DACK}}$ Low to $\overline{\text{O2}}$ High	t_{AL2H}	125	—	ns
16	$\overline{\text{O2}}$ Low to $\overline{\text{DACK}}$ High	t_{2LAH}	65	—	ns
17	$\overline{\text{DTS}}$ Low to $\overline{\text{O2}}$ Low	t_{SL2L}	60	—	ns
18	$\overline{\text{DACK}}$ Low to Data Valid, $\overline{\text{DONE}}$ Low	t_{ALDV}	0	140	ns
19	$\overline{\text{O2}}$ Low to Data Invalid	t_{2LDXDR}	10	150	ns
20	$\overline{\text{DACK}}$, $\overline{\text{DONE}}$ Low to $\overline{\text{O2}}$ High	t_{AL2H}	125	—	ns
21	Data Valid to $\overline{\text{O2}}$ Low	t_{DV2L}	60	—	ns
22	$\overline{\text{O2}}$ Low to Data Invalid	t_{2LDXDW}	0	—	ns
23	$\overline{\text{O2}}$ Low to $\overline{\text{DACK}}$, $\overline{\text{DONE}}$ High	t_{2LDH}	65	—	ns
30	RxC and Tx C Period	t_{CP}	248	—	ns
31	TxC Low to Tx D Delay	t_{TCLTD}	0	200	ns
32	RxC Low to Rx D Transition (Hold)	t_{RCLRD}	0	—	ns
33	RxD Transition to Rx C Low (Setup)	t_{RDRCL}	30	—	ns
34	RxD to Tx D Delay (Echo Mode)	t_{RDTD}	—	200	ns

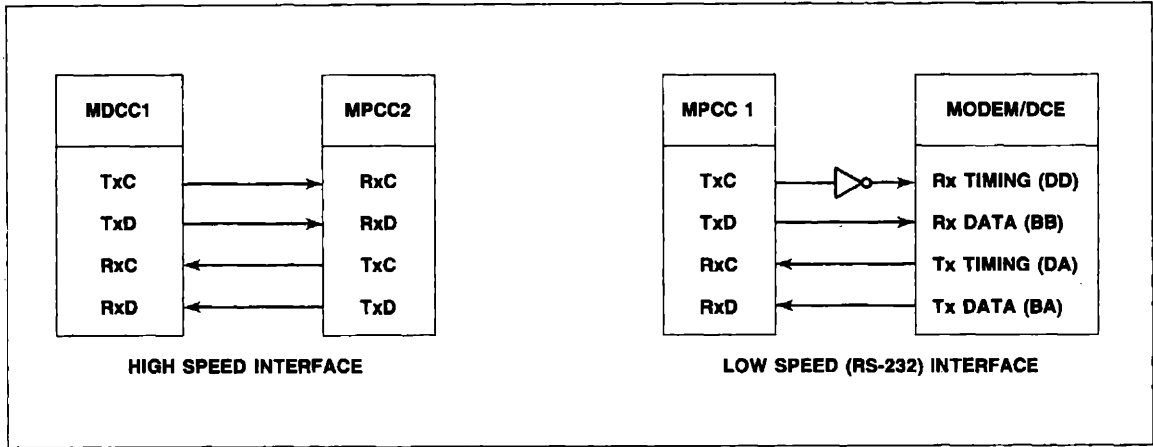


Figure 18. Serial Interface

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Rating
Thermal Resistance	θ_{JA}		°C/W
Ceramic		50	
Plastic		68	

OPERATING CONDITIONS

Parameter	Range
V_{CC} Power Supply	5.0V $\pm 5\%$
Operating Temperature	0°C to 70°C

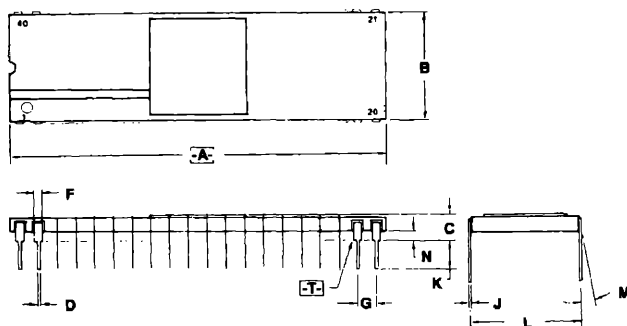
DC CHARACTERISTICS

($V_{CC} = 5.0 \text{ Vdc} \pm 5\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = 0^\circ\text{C}$ to 70°C unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input High Voltage All Inputs	V_{IH}	+2.0	V_{CC}	V	
Input Low Voltage All Inputs	V_{IL}	-0.3	+0.8	V	
Input Leakage Current R/W, RES, CS	I_{IN}	—	10.0	μA	$V_{IN} = 0$ to 5.25V $V_{CC} = 0$
Three-State (Off State) Input Current IRQ, D0-D7	T_{TSI}	—	10.0	μA	$V_{IN} = 0.4$ to 2.4V $V_{CC} = 5.0\text{V}$
Output High Voltage RDSR, TDSR, IRQ, D0-D7, DSR, DTR, RTS, Tx0, Tx0	V_{OH}	$V_{SS} + 2.4$	—	V	$V_{CC} = 4.75\text{V}$ $I_{LOAD} = -400\mu\text{A}$, $C_{LOAD} = 130 \text{ pF}$
BCLK	V_{OH}	$V_{SS} + 2.4$	—	V	$V_{CC} = 4.75\text{V}$ $I_{LOAD} = 0$ $C_{LOAD} = 30 \text{ pF}$
Output Low Voltage RDSR, TDSR, IRQ, D0-D7, DSR, DTR, RTS, Tx0, Tx0, BCLK	V_{OL}	—	0.5	V	$V_{CC} = 4.75\text{V}$ $I_{LOAD} = 3.2 \text{ mA}$
DONE					$V_{CC} = 4.75\text{V}$ $I_{LOAD} = 8.8 \text{ mA}$
Internal Power Dissipation	P_{INT}	—	1	W	$T_A = 25^\circ\text{C}$
Input Capacitance	C_{IN}	—	13	pF	$V_{IN} = 0\text{V}$ $T_A = 25^\circ\text{C}$ $f = 1 \text{ MHz}$

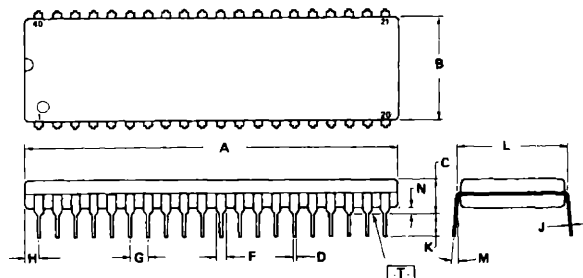
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.56	1.980	2.030
B	14.73	15.49	0.580	0.610
C	1.78	3.05	0.070	0.120
D	0.38	0.58	0.015	0.023
F	1.02	1.65	0.040	0.065
G	2.29	2.80	0.090	0.110
J	0.20	0.38	0.008	0.015
K	3.18	3.81	0.125	0.150
L	14.99	16.51	0.590	0.650
M	0"	10"	0"	10"
N	0.58	1.78	0.020	0.070

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC	0.100 BSC		
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC	0.600 BSC		
M	7"	10"	7"	10"
N	0.51	1.02	0.020	0.040



R65C02, R65C102, AND R65C112 R65C00 MICROPROCESSORS (CPU)

DESCRIPTION

The 8-bit R65C00 microprocessor family of devices are produced using CMOS silicon gate technology which provides advanced system architecture for performance speed and system cost-effectiveness enhancements over their NMOS counterparts, the R6500 family of microprocessor devices.

Three CPU devices are available. All are software-compatible and provide 64K bytes of addressable memory, interrupt input, and on-chip clock oscillators and drivers options. All are bus-compatible with the NMOS R6500 family devices.

The CMOS family includes two microprocessors (R65C02 and R65C102) with on-board clock oscillators and drivers and one microprocessor (R65C112) driven by external clocks. The on-chip clock versions are aimed at high performance, low-cost applications where single phase inputs, crystal or RC inputs provide the time base. The slave processor version is geared for multiprocessor system applications where maximum timing control is mandatory. All R65C00 microprocessors are available in ceramic and plastic packaging, operating frequency of 1 MHz, 2 MHz, 3 MHz and 4 MHz, and commercial and industrial temperature versions. All three devices are housed in 40-pin packages.

ENHANCEMENTS OVER R6502

The CMOS family of microprocessor devices has been designed with many enhancements over the R6502 NMOS device while maintaining software compatibility. Besides the increased speed and lower power consumption inherent in CMOS technology, the R65C00 family has added the following characteristics.

- 12 new instructions for a total of 68
- 59 new op codes, for a total of 210
- Two new addressing modes
- Seven software/operational enhancements
- Two hardware enhancements

FEATURES

- CMOS silicon gate technology
- Low Power (4mA/MHz)
- Software compatible with R6502
- Single 5V +5% power supply requirements
- Eight bit parallel processing
- Decimal and binary arithmetic
- True indexing capability
- Programmable stack pointer
- Interrupt capability
- Non-maskable interrupt
- Eight-bit bidirectional data bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct memory access (DMA) capability
- Memory lock output
- 1 MHz, 2 MHz, 3 MHz, and 4 MHz versions
- Choice of external or on-chip clocks
- On-chip clock options
 - External single clock input
 - Direct crystal input (+ 4)
- Commercial and industrial temperature versions
- Pipeline architecture
- Slave processor version (R65C112)

ORDERING INFORMATION

Part Number:

R65C02 _ _ _

R65C102 _ _ _

R65C112 _ _ _

Temp. Range (T_L to T_H)
Blank = 0°C to +70°C
E = -40°C to +85°C

Frequency Range

1 = 1 MHz
2 = 2 MHz
3 = 3 MHz
4 = 4 MHz

Package

C = Ceramic
P = Plastic

FUNCTIONAL DESCRIPTION

With the exception of a crystal oscillator, clock signals, Memory Latch (ML), and Bus Enable (BE) signals, the internal architecture of the three members of the R65C00 CPU of devices is identical. Figure 1 shows the block diagram of the R65C00 CPU

internal architecture for all three devices. This block diagram supports the following text that describes the function of each of the device's major elements.

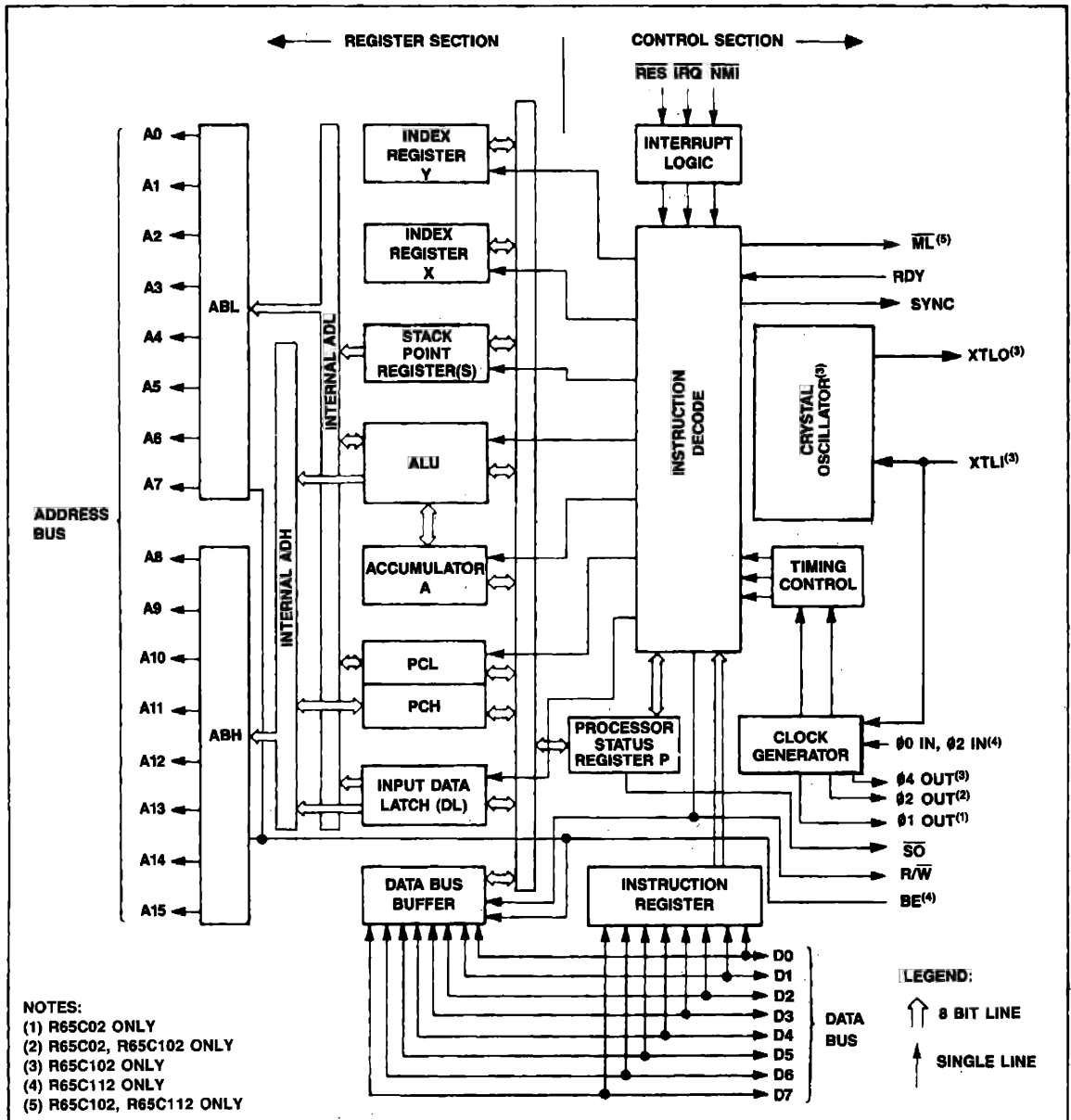


Figure 1. R65C00 Internal Architecture

CRYSTAL OSCILLATOR (R65C102 Only)

The crystal oscillator, driven by a crystal across XTLO and XTAL, divides the crystal frequency by four to provide the basic $\phi 2$ clock signal that drives the internal clock generator.

CLOCK GENERATOR

The clock generator develops all internal clock signals, and (where applicable) external clock signals, associated with the device. It is the clock generator that drives the timing control unit and the external timing for slave mode operations.

TIMING CONTROL

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

PROGRAM COUNTER

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

INSTRUCTION REGISTER AND DECODE

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

ACCUMULATOR

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations, and in addition, the accumulator usually contains one of the two data words used in these operations.

INDEX REGISTERS

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address,

and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

STACK POINTER

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts (NMI and IRQ). The stack allows simple implementation of nested sub-routines and multiple level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

PROCESSOR STATUS REGISTER

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The R65C00 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

HARDWARE ENHANCEMENTS

The R65C00 family of CPU devices have incorporated hardware enhancements over their NMOS counterpart, the R6502. These hardware enhancements are:

- The NMOS device would ignore the assertion of a Ready (RDY) during a write operation. The CMOS family will stop the processor during $\phi 2$ clock if RDY is asserted during a write operation.
- On the NMOS device, unused input-only pins ($\overline{\text{IRQ}}$, NMI, RDY, RES, and SO) must be connected to a low impedance signal to avoid noise problems. These unused pins on the CMOS devices are internally connected by a high impedance to V_{CC} (approximately 250K ohms).

MAJOR FEATURES AND DIFFERENCES

The functional aspects of and differences between the microprocessor configurations are shown in Table 1.

Table 1. Family Comparison Chart

Feature	R65C02	R65C102	R65C112
Pin compatible with NMOS R6502	X		
64K addressable bytes of memory	X	X	X
IRQ interrupt	X	X	X
On-chip clock oscillator	X	X	
External clock only			X
TTL level single phase clock input	X	X	
RC time base clock input	X	X	
Crystal time base clock input	X	X	
Single phase clock input			X
Two phase output clock	X	X	
SYNC and RDY signals	X	X	X
Bus Enable (BE) signal		X	X
Memory Lock (ML) output signal		X	X
Direct Memory Access (DMA) capacity		X	X
NMI interrupt signal	X	X	X

PIN ASSIGNMENTS

Figure 2 shows the pin assignments for the three members of the R65C00 CPU family. All three devices are housed in 40-pin, dual-in-line, ceramic or plastic packages.

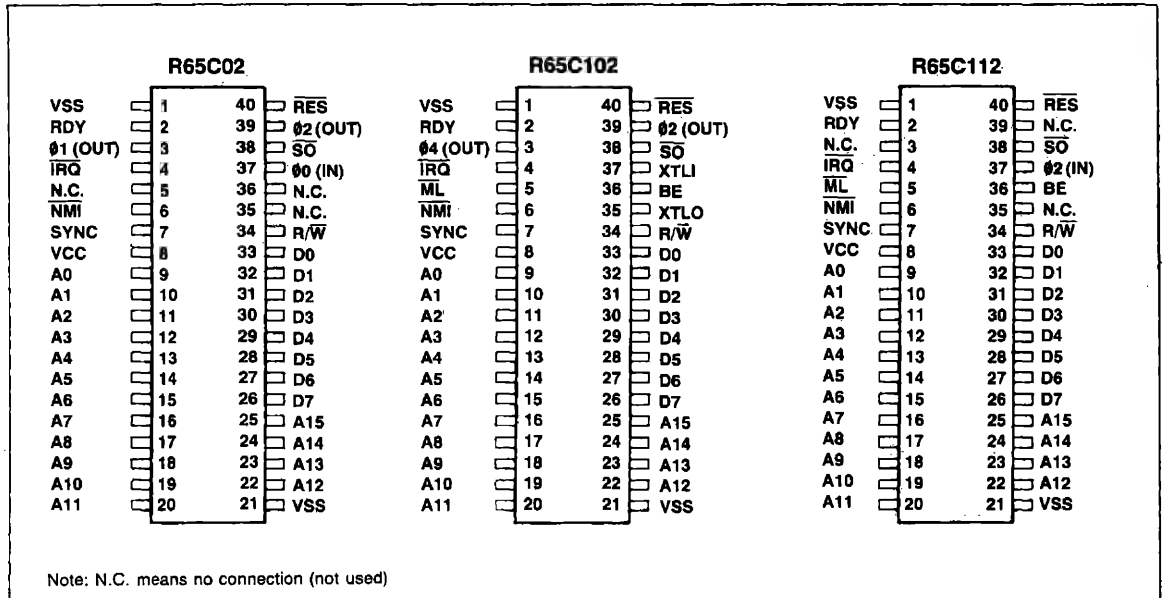


Figure 2. Pin Assignments

SIGNAL DESCRIPTIONS

Reference the timing diagrams for the particular device in the following discussion.

CLOCK SIGNALS (R65C02)

The R65C02 requires an external Ø0 clock. Ø0 is a TTL level input that is used to generate the internal clocks of the R65C02. Two full level output clocks are generated by the R65C02. The Ø2 clock is in phase with Ø0. The Ø1 clock output is 180° out of phase with Ø0. When the input clock is stopped, the CPU is in the standby mode.

For non-critical timing configurations, a simple RC or crystal network may be strapped between Ø0 (IN) and Ø1 (OUT).

CLOCK SIGNALS (R65C102)

The R65C102 internal clocks may be generated by a TTL level single phase input, an RC time base input, or a crystal time base input ($\div 4$) using the XTLO and XTLI input pins. Two full level output clocks are generated by the R65C102. The Ø2 clock output provides timing for external R/W operations. Addresses are valid after the address setup time (t_{ADS}) referenced to the falling edge of Ø2 (OUT). The Ø4 output is a quadrature output clock that is delayed from the falling edge of the Ø2 clock by delay time t_{AVS} . Using the Ø4 clock, addresses are valid at the rising edge of Ø4.

CLOCK SIGNALS (R65C112)

All internal clock signals for the R65C112 are generated by the input clock signal Ø2 (IN). Since this device is intended to be operated in the slave mode it does not have internal clock generation, but rather requires the external clock Ø2 (IN) from a host device.

ADDRESS BUS (A0-A15)

A0-A15 forms a 16-bit address bus for memory and I/O exchanges on the data bus. The output of each address line is TTL compatible, capable of driving one standard TTL load and 130pF.

DATA BUS (D0-D7)

The data lines (D0-D7) constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are tri-state buffers capable of driving one TTL load and 130pF.

BUS ENABLE (BE)

This signal allows external control of the data and the address output buffers and R/W. For normal operation, BE is high causing the address buffers and R/W to be active and the data buffers to be active during a write cycle. For external control, BE is held low to disable the buffers. BE is an asynchronous signal and therefore not related to, or controlled by the CPU internal clock signals.

INTERRUPT REQUEST ($\overline{\text{IRQ}}$)

This TTL compatible input requests that an interrupt sequence begin within the microprocessor. The $\overline{\text{IRQ}}$ is sampled during $\Phi 2$ operation; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during $\Phi 1$. The program counter and processor status register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further $\overline{\text{IRQ}}$ s may occur. At the end of this cycle, the program counter low byte will be loaded from address FFFE, and program counter high byte from location FFFF, thus transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K ohm external resistor should be used for proper wire OR operation.

MEMORY LOCK ($\overline{\text{ML}}$)

In a multiprocessor system, the $\overline{\text{ML}}$ output indicates the need to defer the re-arbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. $\overline{\text{ML}}$ goes low during ASL, DEC, INC, LSR, ROL, ROR, TRB, TSB memory referencing instructions. This signal is low for the modify and write cycles.

NON-MASKABLE INTERRUPT ($\overline{\text{NMI}}$)

A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The $\overline{\text{NMI}}$ is sampled during $\Phi 2$; the current instruction is completed and the interrupt sequence begins during $\Phi 1$. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine.

NOTE

Since this interrupt is non-maskable, another $\overline{\text{NMI}}$ can occur before the first is finished. Care should be taken when using $\overline{\text{NMI}}$ to avoid this.

READY (RDY)

This input allows the user to single-cycle the microprocessor on all cycles including write cycles. A negative transition to the low state, during or coincident with $\Phi 1$, will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent

$\Phi 2$ in which the ready signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).

READ/WRITE (R/ $\overline{\text{W}}$)

This signal is normally in the high state indicating that the microprocessor is reading data from memory or I/O bus. In the low state the data bus has valid data from the microprocessor to be stored at the addressed memory location.

SET OVERFLOW ($\overline{\text{SO}}$)

A negative transition on this line sets the overflow bit (V) in the processor status register. The signal is sampled prior to the leading edge of $\Phi 2$ by the processor control time (t_{AWS}).

RESET ($\overline{\text{RES}}$)

This input resets the microprocessor. Reset must be held low for at least two clock cycles after V_{CC} reaches operating voltage from a power down. A positive transition on this pin will then cause an initialization sequence to begin. Likewise, after the system has been operating, a low on this line of at least two cycles will cease microprocessing activity, followed by initialization after the positive edge on $\overline{\text{RES}}$.

When a positive edge is detected, there is an initialization sequence lasting six clock cycles. Then the interrupt mask flag is set, the decimal mode is cleared, and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation.

SYNCHRONIZE (SYNC)

This output line identifies those cycles during which the microprocessor is fetching the instruction operation code (OP CODE). The SYNC line goes high during $\Phi 1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\Phi 1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

OPERATIONAL ENHANCEMENTS

Table 2 lists the operational enhancements that have been added to the CMOS family of CPU devices and compares the results with their NMOS R6502 counterpart.

Table 2. CMOS Operational Enhancements

Function	NMOS R6502 Microprocessor	CMOS R65C00 Family Microprocessor
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.
Execution of invalid op codes.	Some terminate only by reset. Results are undefined.	All are NOPs (reserved for future use).
Jump indirect, operand = XXFF.	Page address does not increment.	Page address increments and adds one additional cycle.
Read/modify/write instructions at effective address.	One read and two write cycles.	Two read and one write cycle.
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D=0) after reset and interrupts.
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flag adds one additional cycle.
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded, BRK vector is ignored.	BRK is executed, then interrupt is executed.

ADDRESSING MODES

The R65C00 CPU family has 15 addressing modes (two more than the NMOS equivalent family). In the following discussion of these addressing modes, a bracketed expression follows the title of the mode. This expression is the term used in the Instruction Set Op Code Matrix table (later in this product description) to make it easier to identify the actual addressing mode used by the instruction.

ACCUMULATOR ADDRESSING [Accum]—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING [IMM]—In immediate addressing, the second byte of the instruction contains the operand, with no further memory addressing required.

ABSOLUTE ADDRESSING [ABS]—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING [ZP]—The zero page instructions allow for shorter code and execution times by fetching only the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

ZERO PAGE INDEXED ADDRESSING [ZP, X or Y]—(X, Y indexing)—This form of addressing is used with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur.

ABSOLUTE INDEXED ADDRESSING [ABS, X or Y]—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X" and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields, resulting in reduced coding and execution time.

INDEXED ABSOLUTE INDIRECT [(ABS, X)]*

The contents of the second and third instruction bytes are added to the X-register. The sixteen-bit result is a memory address containing the effective address. (JMP (ABS, X) only).

IMPLIED ADDRESSING [Implied]—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING [Relative]—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING [(IND, X)]—In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents are the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING [(IND), Y]—In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT [(ABS)]—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter. (JMP (ABS) only.)

INDIRECT [(IND)]*—The second byte of the instruction contains a zero page address serving as the indirect pointer.

NOTE

*These addressing modes are not available to the NMOS CPU family (e.g., the R6502).

2

INSTRUCTION SET

Table 3 lists the instruction set for the CMOS CPU family in alphabetic order according to mnemonic. Table 4 lists the hexadecimal codes for each of the instructions that are new to the CMOS family and were not available in the NMOS R6502 device

family. Table 5 lists those instructions that were available on the NMOS family, but have been assigned new addressing modes in the CMOS CPU family.

Table 3. Alphabetic Listing of Instruction Set

Mnemonic	Function	Mnemonic	Function
(2) ADC	Add Memory to Accumulator with Carry	NOP	No Operation
(2) AND	"AND" Memory with Accumulator	(2) ORA	"OR" Memory with Accumulator
ASL	Shift Left One Bit (Memory or Accumulator)	PHA	Push Accumulator on Stack
(1) BBR	Branch on Bit Reset	PHP	Push Processor Status on Stack
(1) BBS	Branch on Bit Set	(1) PHX	Push X Register on Stack
BCC	Branch on Carry Clear	(1) PHY	Push Y Register on Stack
BCS	Branch on Carry Set	PLA	Pull Accumulator from Stack
BEQ	Branch on Result Zero	PLP	Pull Processor Status from Stack
(2) BIT	Test Bits in Memory with Accumulator	(1) PLX	Pull X Register from Stack
BMI	Branch on Result Minus	(1) PLY	Pull Y Register from Stack
BNE	Branch on Result not Zero	(1) RMB	Reset Memory Bit
BPL	Branch on Result Plus	ROL	Rotate One Bit Left (Memory or Accumulator)
(1) BRA	Branch Always	ROR	Rotate One Bit Right (Memory or Accumulator)
BRK	Force Break	RTI	Return from Interrupt
BVC	Branch on Overflow Clear	RTS	Return from Subroutine
BVS	Branch on Overflow Set	SBC	Subtract Memory from Accumulator with Borrow
CLC	Clear Carry Flag	SEC	Set Carry Flag
CLD	Clear Decimal Mode	SED	Set Decimal Mode
CLI	Clear Interrupt Disable Bit	SEI	Set Interrupt Disable Status
CLV	Clear Overflow Flag	(1) SMB	Set Memory Bit
(2) CMP	Compare Memory and Accumulator	(2) STA	Store Accumulator in Memory
CPX	Compare Memory and Index X	STX	Store Index X in Memory
CPY	Compare Memory and Index Y	STY	Store Index Y in Memory
(2) DEC	Decrement Memory by One	(1) STZ	Store Zero
DEX	Decrement Index X by One	TAX	Transfer Accumulator to Index X
DEY	Decrement Index Y by One	TAY	Transfer Accumulator to Index Y
(2) EOR	"Exclusive-OR" Memory with Accumulator	(1) TRB	Test and Reset Bits
(2) INC	Increment Memory by One	(1) TSB	Test and Set Bits
INX	Increment Index X by One	TSX	Transfer Stack Pointer to Index X
INY	Increment Index Y by One	TXA	Transfer Index X to Accumulator
(2) JMP	Jump to New Location	TXS	Transfer Index X to Stack Register
JSR	Jump to New Location Saving Return Address	TYA	Transfer Index Y to Accumulator
(2) LDA	Load Accumulator with Memory		
LDX	Load Index X with Memory		
LDY	Load Index Y with Memory		
LSR	Shift One Bit Right (Memory or Accumulator)		

Notes:

(1) Instruction not available on the NMOS family.

(2) R6502 instruction with additional addressing mode(s).

Table 4. Hexadecimal Codes For New Instructions in The CMOS Family

Hex	Mnemonic	Description
80	BRA	Branch relative always [Relative]
3A	DEC	Decrement accumulator [Accum]
1A	INC	Increment accumulator [Accum]
DA	PHX	Push X on stack [Implied]
5A	PHY	Push Y on stack [Implied]
FA	PLX	Pull X from stack [Implied]
7A	PLY	Pull Y from stack [Implied]
9C	STZ	Store zero [Absolute]
9E	STZ	Store zero [ABS, X]
64	STZ	Store zero [ZP]
74	STZ	Store zero [ZP, X]
1C	TRB	Test and reset memory bits with accumulator [ABS]
14	TRB	Test and reset memory bits with accumulator [ZP]
0C	TSB	Test and set memory bits with accumulator [ABS]
04	TSB	Test and set memory bits with accumulator [ZP]
89	BIT	Test Immediate with accumulator [IMM]
0F-7F ⁽¹⁾	BBR	Branch on bit reset [Bit Manipulation, ZP, REL]
8F-FF ⁽¹⁾	BBS	Branch on bit set [Bit Manipulation, ZP, REL]
07-77 ⁽¹⁾	RMB	Reset memory bit [Bit Manipulation, ZP]
87-F7 ⁽¹⁾	SMB	Set memory bit [Bit Manipulation, ZP]

Note:
1. Most significant digit change only.

Table 5. Hexadecimal Codes For Instructions With New CMOS Addressing Modes

Hex	Mnemonic	Description
72	ADC	Add memory to accumulator with carry [(IND)]
32	AND	AND memory with accumulator [(IND)]
3C	BIT	Test memory bits with accumulator [ABS, X]
34	BIT	Test memory bits with accumulator [ZP, X]
D2	CMP	Compare memory and accumulator [(IND)]
52	EOR	Exclusive Or memory with accumulator [(IND)]
7C	JMP	Jump (New addressing mode) [(ABS, X)]
B2	LDA	Load accumulator with memory [(IND)]
12	ORA	OR memory with accumulator [(IND)]
F2	SBC	Subtract Memory from accumulator with borrow [(IND)]
92	STA	Store accumulator in memory [(IND)]

INSTRUCTION SET OP CODE MATRIX

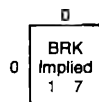
The following matrix shows the 210 Op Codes associated with the R65C00 family of CPU devices. The matrix identifies the hexadecimal code, the mnemonic code, the addressing mode,

the number of instruction bytes, and the number of machine cycles associated with each Op Code. Also, refer to the instruction set summary for additional information on these Op Codes.

MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BRK Implied 1 7	ORA (IND, X) 2 6			TSB ZP 2 5	ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2		TSB ABS 3 6	ORA ABS 3 4	ASL ABS 3 6	BBS0 ZP 3 5**
1	BPL Relative 2 2**	ORA (IND), Y 2 5*	ORA (IND) 2 5		TRB ZP 2 5	ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*	INC Accum 1 2		TRB ABS 3 6	ORA ABS, X 3 4*	ASL ABS, X 3 7	BBS1 ZP 3 5**
2	JSR ABS 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBS2 ZP 3 5**
3	BMI Relative 2 2**	AND (IND), Y 2 5*	AND (IND) 2 5		BIT ZP, X 2 4	AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*	DEC Accum 1 2		BIT ABS, X 3 4*	AND ABS, X 3 4*	ROL ABS, X 3 7	BBS3 ZP 3 5**
4	RTI Implied 1 6	EOR (IND, X) 2 6			EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2			JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBS4 ZP 3 5**
5	BVC Relative 2 2**	EOR (IND), Y 2 5*	EOR (IND) 2 5		EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*	PHY Implied 1 3			EOR ABS, X 3 4*	LSR ABS, X 3 7		BBS5 ZP 3 5**
6	RTS Implied 1 6	ADC (IND, X) 2 6†			STZ ZP 2 3	ADC ZP 2 3†	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2†	ROR Accum 1 2		JMP (ABS) 3 6	ADC ABS 3 4†	ROR ABS 3 6	BBS6 ZP 3 5**
7	BVS Relative 2 2**	ADC (IND), Y 2 5†	ADC (IND) 2 5†		STZ ZP, X 2 4	ADC ZP, X 2 4†	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4†	PLY Implied 1 4		JMP (ABS, X) 3 6	ADC ABS, X 3 4†	ROR ABS, X 3 7	BBS7 ZP 3 5**
8	BRA Relative 2 3*	STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2	BIT IMM 2 2	TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**
9	BCC Relative 2 2**	STA (IND), Y 2 6	STA (IND) 2 5		STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 5	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2		STZ ABS 3 4	STA ABS, X 3 5	STZ ABS, X 3 5	BBS1 ZP 3 5**
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**
B	BCS Relative 2 2**	LDA (IND), Y 2 5*	LDA (IND) 2 5		LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**
D	BNE Relative 2 2**	CMP (IND), Y 2 5*	CMP (IND) 2 5		CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*	PHX Implied 1 3			CMP ABS, X 3 4*	DEC ABS, X 3 7		BBS5 ZP 3 5**
E	CPX IMM 2 2	SBC (IND, X) 2 6†			CPX ZP 2 3	SBC ZP 2 3†	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2†	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4†	INC ABS 3 6	BBS6 ZP 3 5**
F	BEQ Relative 2 2**	SBC (IND), Y 2 5†	SBC (IND) 2 5†		SBC ZP, X 2 4†	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4†	PLX Implied 1 4			SBC ABS, X 3 4†	INC ABS, X 3 7		BBS7 ZP 3 5**
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F



— New Opcode



—OP Code
—Addressing Mode
—Instruction Bytes; Machine Cycles

†Add 1 to N if in decimal mode.

*Add 1 to N if page boundary is crossed.

**Add 1 to N if branch occurs to same page;

Add 2 to N if branch occurs to different page.

INSTRUCTION SET SUMMARY

MNEMONIC	OPERATION	ADDRESSING MODES																												PROCESSOR STATUS CODES																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																							
		IMMEDIATE		ABSOLUTE		ZERO PAGE		JP REL		ACCUM.		IMPLIED		(IND. X)		(IND. Y)		PAGE X		ABS. X		ABS. Y		RELATIVE		(RD)		PAGE Y		PROCESSOR STATUS CODES																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																							
		Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n	Op	n

LEGEND

X = Index X
Y = Index Y
A = Accumulator
M = Memory per effective address
M_n = Memory per stack pointer
n = Selector zero page memory bit
= Memory Bit 7

Notes:

1. Add 1 to N if page boundary is crossed.
2. Add 1 to N if branch occurs to same page.
3. Add 2 to N if branch occurs to different page.
4. Carry not (C) = Borrow.
5. Effects e-bit data field of the specified zero page address.
6. On the BII immediate instruction, the results of the M_n and V flags are indeterminate and should be considered invalid.
7. If in Decimal Mode, Z flag is invalid. Accumulator must be checked for zero result.
8. JMP (OP Code 9C) is an Absolute Indirect Addressing Mode (ABS).

AC CHARACTERISTICS

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	

CLOCK TIMING

Ø2 Cycle Time	t_{CYC}	1000	Note 1	500	Note 1	333	Note 1	250	Note 1	ns
Ø2 Low Pulse Width	t_{CL}	430	5000	210	5000	150	5000	100	5000	ns
Ø2 High Pulse Width	t_{CH}	450	—	220	—	160	—	110	—	ns
Ø0 Low to Ø2 Low Skew ⁽²⁾	t_{SK2}	—	50	—	50	—	40	—	30	ns
Ø2 Low to Ø1 High Skew ⁽³⁾	t_{SK1}	-20	20	-20	20	-20	20	-20	20	ns
XTL1 High to Ø2 Low ⁽⁴⁾	t_{DXI}	—	100	—	100	—	100	—	100	ns
XTLO Low to Ø2 Low ⁽⁴⁾	t_{DXO}	—	75	—	75	—	75	—	75	ns
Ø2 Low to Ø4 High Delay ⁽⁴⁾	t_{AVS}	250	—	125	—	85	—	65	—	ns
Ø4 Low Pulse Width ⁽⁴⁾	$t_{Ø4L}$	430	—	210	—	150	—	100	—	ns
Ø4 High Pulse Width ⁽⁴⁾	$t_{Ø4H}$	450	5000	220	5000	160	5000	110	5000	ns
Clock Rise and Fall Times	t_{RI}, t_F	—	25	—	20	—	15	—	12	ns

READ/WRITE TIMING

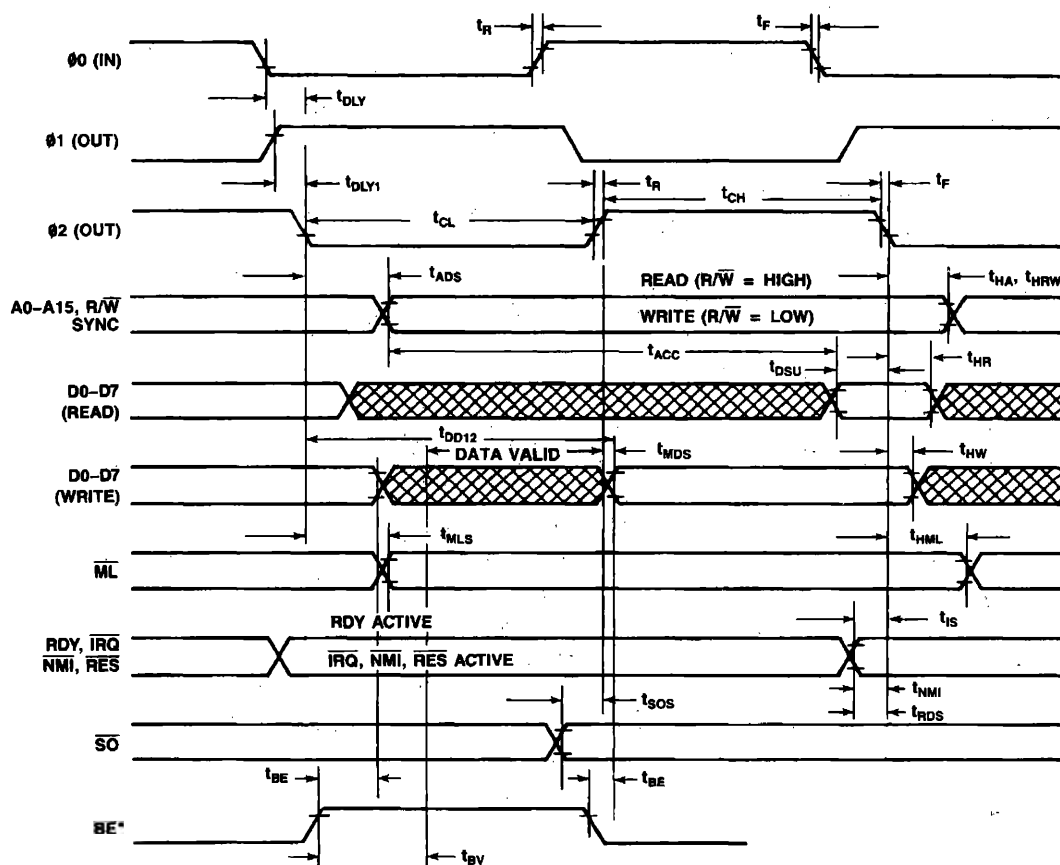
R/W Setup Time	t_{RWS}	—	125	—	100	—	75	—	60	ns
R/W Hold Time	t_{HRW}	15	—	15	—	15	—	15	—	ns
Address Setup Time	t_{ADS}	—	125	—	100	—	75	—	60	ns
Address Valid to Ø4 High ⁽⁴⁾	$t_{AØ4}$	100	—	25	—	10	—	0	—	ns
Address Hold Time	t_{HA}	15	—	15	—	15	—	15	—	ns
Read Access Time	t_{ACC}	775	—	340	—	215	—	160	—	ns
Read Data Setup Time	t_{DSU}	100	—	60	—	40	—	30	—	ns
Read Data Hold Time	t_{HR}	10	—	10	—	10	—	10	—	ns
Write Data Delay Time ⁽²⁾	t_{MDS}	—	200	—	110	—	85	—	55	ns
Write Data Delay Time ⁽⁴⁾	t_{DDW}	—	200	—	110	—	85	—	55	ns
Write Data Delay Time ⁽⁶⁾	t_{DD12}	—	450	—	235	—	170	—	120	ns
Write Data Hold Time	t_{HW}	30	—	30	—	30	—	30	—	ns

CONTROL LINE TIMING

SYNC Delay	t_{SYS}	—	125	—	100	—	75	—	60	ns
RDY Setup Time	t_{RDS}	200	—	110	—	80	—	60	—	ns
SO Setup Time	t_{SOS}	75	—	50	—	40	—	30	—	ns
ML Delay Time ⁽⁵⁾	t_{MLS}	—	125	—	100	—	75	—	60	ns
ML Hold Time ⁽⁴⁾	t_{MLH}	10	—	10	—	10	—	10	—	ns
ML Hold Time ⁽⁶⁾	t_{MLH}	15	—	15	—	15	—	15	—	ns
BE Delay Time ⁽⁵⁾⁽⁹⁾	t_{BE}	—	40	—	40	—	40	—	40	ns
BE Setup Time ⁽⁵⁾⁽⁹⁾	t_{BV}	—	60	—	60	—	60	—	60	ns
IRQ, RES Setup Time	t_{IS}	200	—	110	—	80	—	60	—	ns
NMI Setup Time	t_{NMI}	200	—	150	—	100	—	70	—	ns

Notes:

1. R65C02 and R65C102 minimum operating frequency is limited by Ø2 low pulse width. All processors can be stopped with Ø2 held high.
2. R65C02 only.
3. R65C02 and R65C102 only.
4. R65C102 only.
5. R65C102 and R65C112 only.
6. R65C112 only.
7. Voltage levels shown are $V_L \leq 0.4V$ and $V_H \geq 2.4V$ unless otherwise stated.
8. Measurement points shown are 0.8V (low) and 2.0V (high) for inputs and 1.5V (low and high) for outputs, unless otherwise specified.
9. BE signal is asynchronous.



2

NOTE: ALL TIMING IS REFERENCED FROM A HIGH VOLTAGE OF 2.4 VOLTS AND A LOW OF 0.5 VOLTS.

* ML (MEMORY LOCK) AND BE (BUS ENABLE) NOT APPLICABLE TO R65C02.

Figure 3. Timing Diagram for the R65C02 and R65C112

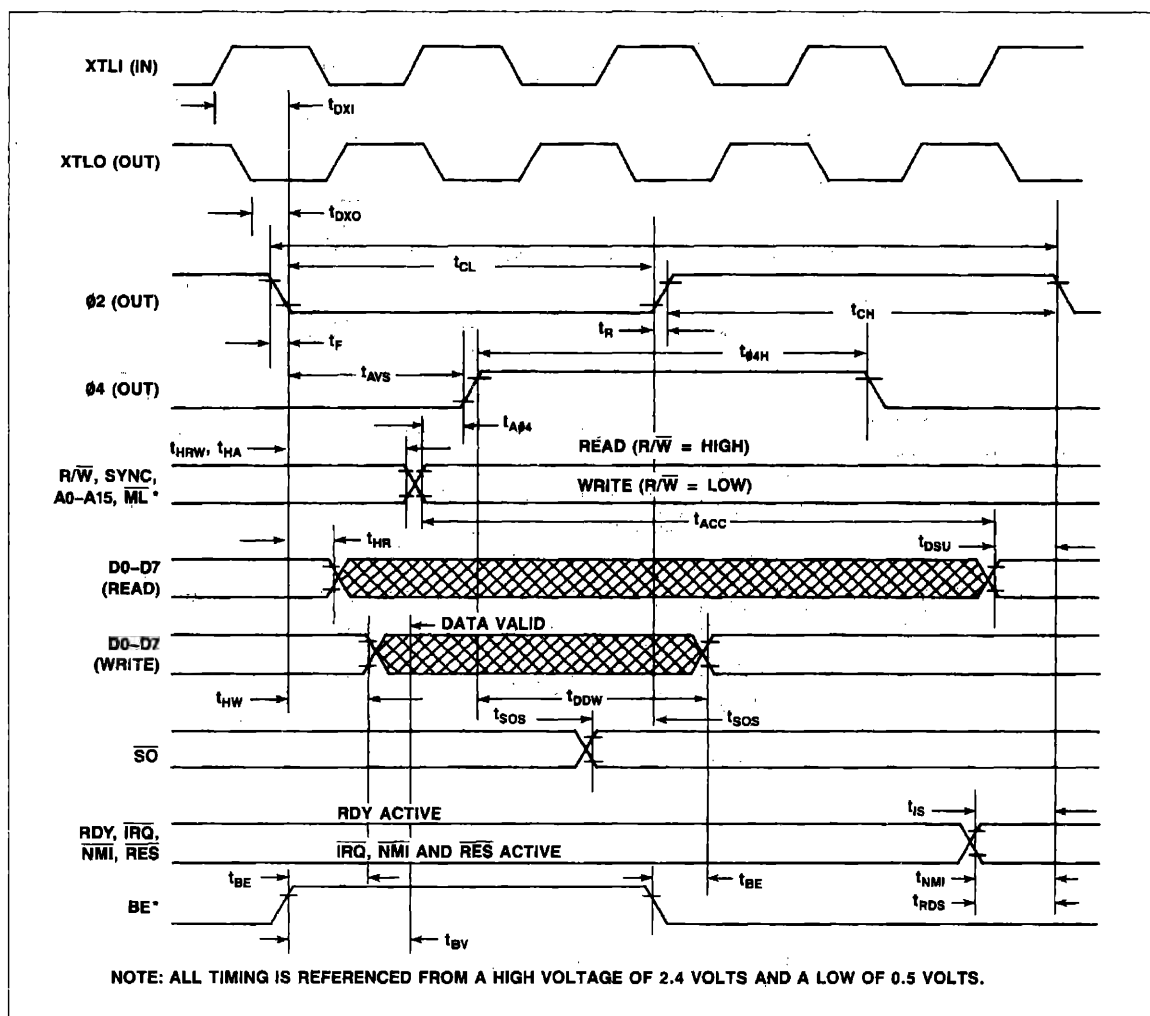


Figure 4. Timing Diagram for the R65C102

CRYSTAL/CLOCK CONSIDERATIONS

CRYSTAL/CLOCK CIRCUITS

Figure 5 shows a time base generation scheme, for 4 MHz operation of the R65C02, that has been tested and proven reliable for normal environments. As with any clock oscillator circuit, stray capacitance due to board layout can cause unpredictable results requiring "fine tuning" of the circuit. Figure 6 shows a possible external clock scheme for a R65C102 and R65C112 master/slave configuration. Table 6 identifies nominal crystal parameters for five crystal frequencies.

Table 6. Nominal Crystal Parameters

FREQ	3.58	4.0	6.0	8.0	16.0	MHz
RS	60	50	30-50	20-40	10-30	Ω
C0	3.5	6.5	4-6	4-6	3-5	pF
C1	.015	.025	.01-.02	.01-.02	.01-.02	pF
Q	740K	730K	720K	720K	720K	K

Note: These represent at-cut crystal parameters only. Others may be used.

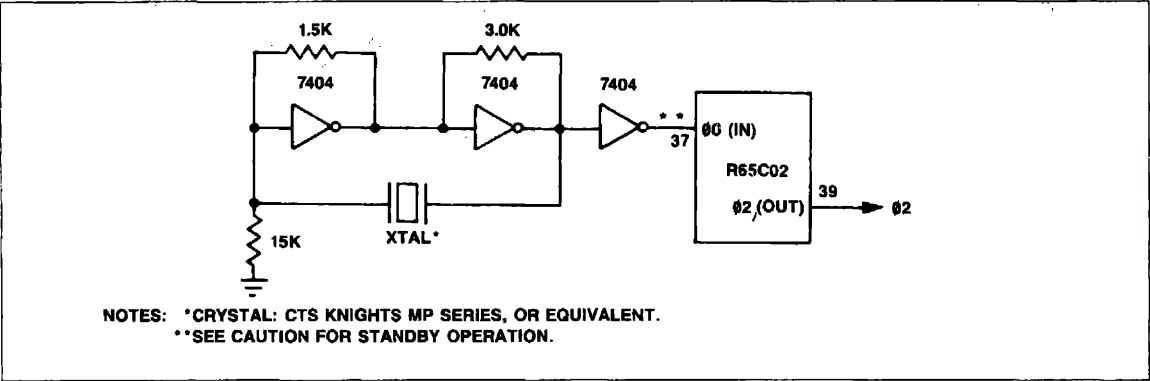


Figure 5. Example of R65C02 Time Base Generation

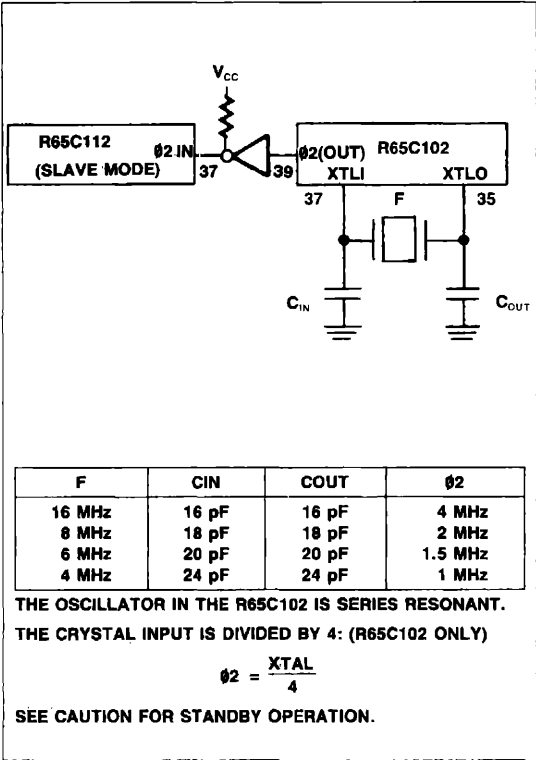


Figure 6. Example of External Clock for R65C102

STOPPING THE CLOCK-STANDBY MODE

Caution must be exercised when configuring the R65C02 or R65C112 in the standby mode (i.e., #0 IN or #2 IN clock stopped). The input clock can be held in the high state indefinitely; however, if the input clock is held in the low state longer than 5 microseconds, internal register and data status can be lost. Figure 7 shows a circuit that will stop the #0 IN (R65C02) or #2 IN (R65C112) clock in the high state during standby mode.

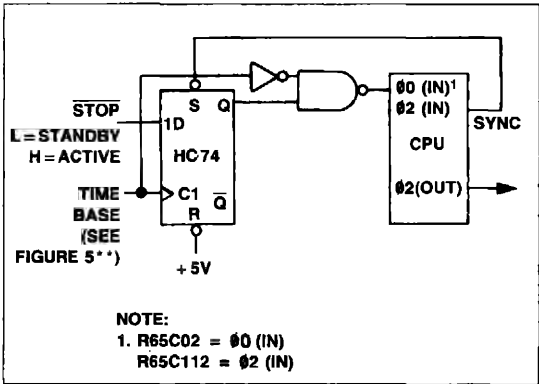


Figure 7. Standby Mode Circuit

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	Vdc
Output Voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	Vdc
Operating Temperature Commercial Industrial	T_A	0 to +70 -40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*Note

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V \pm 5%
Temperature Range Commercial Industrial	T_A	0° to 70°C -40°C to +85°C

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage All Other Input Pins 00 on R65C02 02 on R65C112	V_{IH}	2.0 2.4 $V_{CC} - 0.4$		$V_{CC} + 0.3$ $V_{CC} + 0.3$ $V_{CC} + 0.3$	V	
Input Low Voltage All Other Input Pins 00 on R65C02 02 on R65C112	V_{IL}	-0.3 -0.3 -0.3		+0.8 +0.4 +0.4	V	
Input Leakage Current NMI, \overline{IRQ} , BE, RDY, \overline{RES} , \overline{SO} 02 IN, 00 IN, XTLI	I_{IN}	— —		-50 1.0	μ A	$V_{IN} = 0V$ to 5.25V $V_{CC} = 0V$
Three-State (Off State) Input Current Data Lines	I_{TSI}	—		10	μ A	$V_{IN} = 0.4V$ to 2.4V $V_{CC} = 5.25V$
Output High Voltage SYNC, Data, A0-A15, R/W, 01, 02, 04, \overline{ML}	V_{OH}	2.4		—	V	$V_{CC} = 4.75V$ $I_{LOAD} = -100 \mu A$
Output Low Voltage SYNC, Data, A0-A15, R/W, 01, 02, 04, \overline{ML}	V_{OL}	—		+0.4	V	$V_{CC} = 4.75V$ $I_{LOAD} = 1.6 \mu A$
Supply Current Standby ¹ Active (R65C02) Active (R65C102) Active (R65C112) Low Power (R65C02) Low Power (R65C102) Low Power (R65C112)	I_{CC}	— — — — — — —	2 2.6 5 2 1.1 3 0.7	10 4 7 4 2 4 1	μ A mA/MHz mA/MHz mA/MHz mA/MHz mA/MHz mA/MHz	$V_{CC} = 5.0V$ RDY = 0 RDY = 0
Capacitance NMI, \overline{IRQ} , \overline{SO} , BE, RDY Data, 01, 02, 04, \overline{ML} , XTLO A0-A15, R/W, SYNC 00 (IN), XTLI 02 (IN)	C C_{IN} C_{OUT} C_0 C_2	— — — —		7 10 10 30	pF	$V_{CC} = 5.0V$ $V_{IN} = 0V$ $f = 1 MHz$ $T_A = 25^\circ C$

Notes:

1. All units are direct current (dc).
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. \overline{IRQ} and NMI require external pull-up resistor.
4. Typical values are shown for $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.



R65C21 PERIPHERAL INTERFACE ADAPTER (PIA)

PRELIMINARY

2

DESCRIPTION

The R65C21 Peripheral Interface Adapter (PIA) is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the R6500, R6500/* or R65C00 family of microprocessors, the R65C21 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or to "handshake" data between the processor and a peripheral device.

ORDERING INFORMATION

The R65C21 is available in both a ceramic and a plastic 40-pin package, a commercial or industrial operating temperature range, and operating frequencies of 1, 2, 3, or 4 MHz. These versions are coded into the part number as follows:

Part Number:

R65C21

Temperature Range (T_L to T_H):

Blank = 0°C to +70°C

E = -40°C to +85°C

Frequency Range:

1 = 1 MHz

2 = 2 MHz

3 = 3 MHz

4 = 4 MHz

Package:

C = Ceramic

P = Plastic

FEATURES

- Low power CMOS N-well silicon gate technology
- Direct replacement for NMOS R6520 or MC6821 PIA
- Two 8-bit bidirectional I/O ports with individual data direction control
- Automatic "Handshake" control of data transfers
- Two interrupts (one for each port) with program control
- 1, 2, 3, and 4 MHz versions
- Commercial and industrial temperature range versions
- 40-pin plastic and ceramic versions
- 5 volt $\pm 5\%$ supply requirements
- Compatible with the R6500, R6500/* and R65C00 family of microprocessors

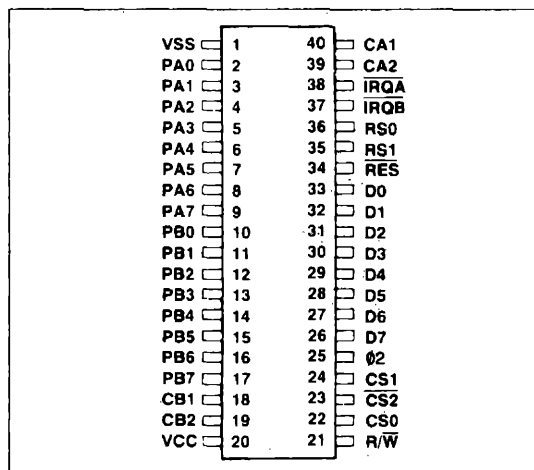


Figure 1. R65C21 Pin Configuration

FUNCTIONAL DESCRIPTION

The R65C21 PIA is organized into two independent sections referred to as the A Side and the B Side. Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control (ISCA, ISCB), and the buffers necessary to drive the Peripheral Interface buses. Data Bus Buffers (DBB) interface

data from the two sections to the data bus, while the Data Input Register (DIR) interfaces data from the DBB to the PIA registers. Chip Select and R/W control circuitry interface to the processor bus control lines. Figure 2 is a block diagram of the R65C21 PIA.

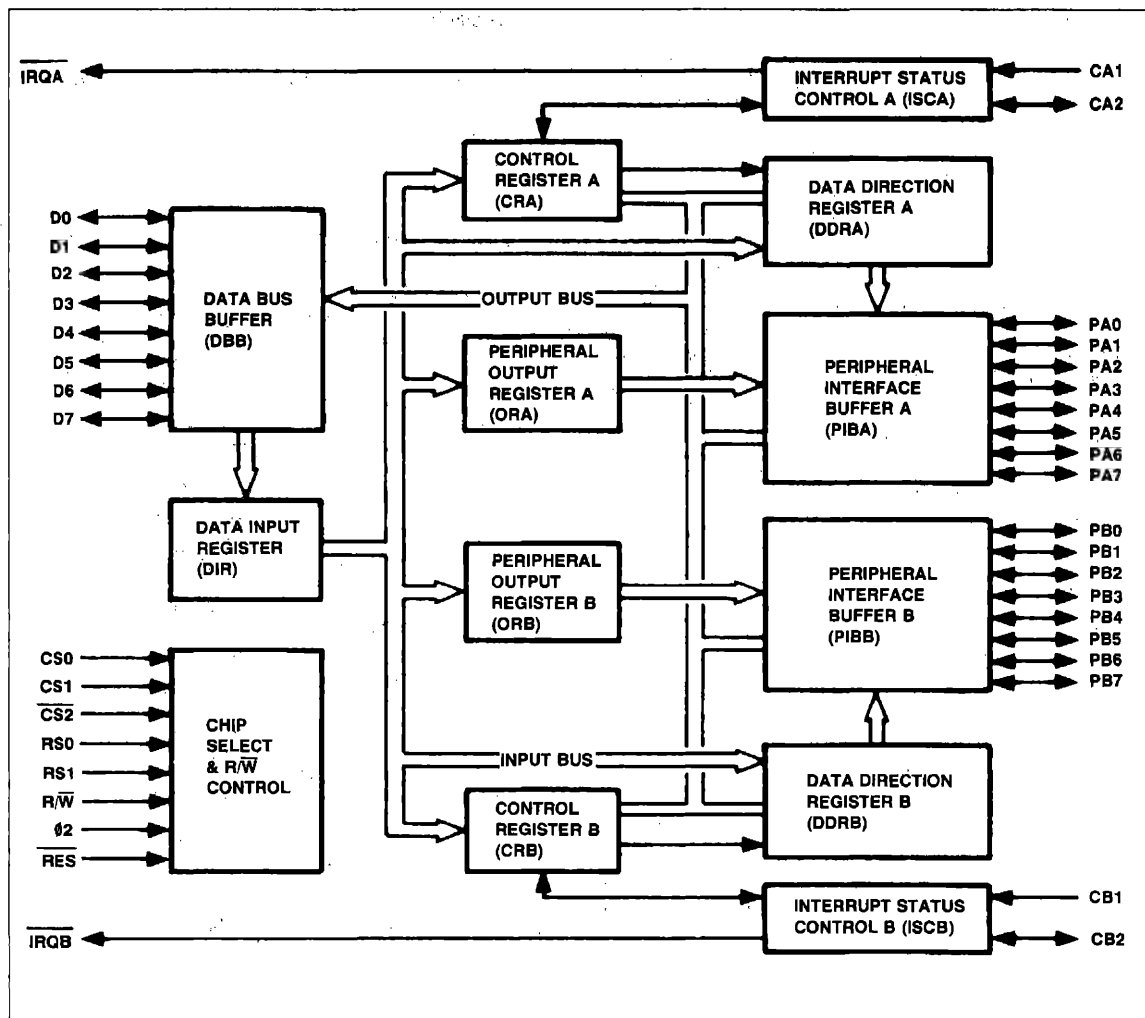


Figure 2. R65C21 PIA Block Diagram

DATA INPUT REGISTER (DIR)

When the microprocessor writes data into the PIA, the data which appears on the data bus during the $\phi 2$ clock pulse is latched into the Data Input Register (DIR). The data is then transferred into one of six internal registers of the PIA after the trailing edge of the $\phi 2$ clock. This assures that the data on the peripheral output lines will make smooth transitions from high to low (or from low to high) and the voltage will remain stable except when it is going to the opposite polarity.

CONTROL REGISTERS (CRA AND CRB)

Table 1 illustrates the bit designation and functions in the two control registers. The control registers allow the microprocessor to control the operation of the Interrupt Control Inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) in each control register indicate the status of the Interrupt Input lines (CA1, CA2, CB1, CB2). These Interrupt Status bits (IRQA1, IRQA2 or IRQB1, IRQB2) are normally interrogated by the microprocessor during the IRQ interrupt service routine to determine the source of the interrupt.

DATA DIRECTION REGISTERS (DDRA, DDRB)

The Data Direction Registers (DDRA, DDRB) allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Writing a "0" in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

Bit 2 (DDRA, DDRB) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a "1," a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a "0," a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines RS0, RS1) selects the various internal registers as shown in Table 2.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

PERIPHERAL OUTPUT REGISTERS (ORA, ORB)

The Peripheral Output Registers (ORA, ORB) store the output data from the Data Bus Buffers (DBB) which appears on the Peripheral I/O port. If a line on the Peripheral A Port is programmed as an output by the DDRA, writing a 0 into the corresponding bit in the ORA causes that line to go low (<0.4 V); writing a 1 causes the line to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

INTERRUPT STATUS CONTROL (ISCA, ISCB)

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register and detects active transitions on the interrupt inputs.

PERIPHERAL I/O PORTS (PA0-PA7, PB0-PB7)

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by writing data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a 1 in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A 0 in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-up devices. These pull-up devices are resistive in nature and therefore allow the output voltage to go to VCC for a logic 1. The switches can sink a full 3.2 mA, making these buffers capable of driving two standard TTL loads.

In the input mode, the pull-up devices are still connected to the I/O pin and still supply current to this pin. For this reason, these lines also represent two standard TTL loads in the input mode.

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output is similar to the Peripheral A port, as is the effect of reading or writing this port. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

Table 1. Control Registers Bit Designations

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

The Peripheral B I/O port buffers are push-pull devices i.e., the pull-up devices are switched OFF in the 0 state and ON for a logic 1. Since these pull-ups are active devices, the logic 1 voltage will not go higher than +2.4V.

Another difference between the PA0-PA7 lines and the PB0 through PB7 lines is that they have three-state capability which allows them to enter a high impedance state when programmed to be used as input lines. In addition, data on these lines will be read properly, when programmed as output lines, even if the data signals fall below 2.0 volts for a "high" state or are above 0.8 volts for a "low" state. When programmed as output, each line can drive at least a two TTL load and may also be used as a source of up to 3.2 milliamperes at 1.5 volts to directly drive the base of a transistor switch, such as a Darlington pair.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic is the high-impedance input state which is a function of the Peripheral B push-pull buffers. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

DATA BUS BUFFERS (DBB)

The Data Bus Buffers are 8-bit bidirectional buffers used for data exchange, on the D0-D7 Data Bus, between the microprocessor and the PIA. These buffers are tri-state and are capable of driving a two TTL load (when operating in an output mode) and represent a one TTL load to the microprocessor (when operating in an input mode).

INTERFACE SIGNALS

The PIA interfaces to the R6500, R6500/* or the R65C00 microprocessor family with a reset line, a $\phi 2$ clock line, a read/write line, two interrupt request lines, two register select lines, three chip select lines, and an 8-bit bidirectional data bus.

The PIA interfaces to the peripheral devices with four interrupt/control lines and two 8-bit bidirectional data buses.

Figure 1 (on the front page) shows the pin assignments for these interface signals and Figure 3 shows the interface relationship of these signals as they pertain to the CPU and the peripheral devices.

CHIP SELECT ($\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$)

The PIA is selected when $\overline{CS0}$ and $\overline{CS1}$ are high and $\overline{CS2}$ is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits. When the PIA is selected, data will be transferred between the data lines and PIA registers, and/or peripheral interface lines as determined by the $\overline{R/\overline{W}}$, $\overline{RS0}$, and $\overline{RS1}$ lines and the contents of Control Registers A and B.

RESET SIGNAL (\overline{RES})

The Reset (\overline{RES}) input initializes the R65C21 PIA. A low signal on the \overline{RES} input causes all internal registers to be cleared.

CLOCK SIGNAL ($\phi 2$)

The Phase 2 Clock Signal ($\phi 2$) is the system clock that triggers all data transfers between the CPU and the PIA. $\phi 2$ is generated by the CPU and is therefore the synchronizing signal between the CPU and the PIA.

READ/WRITE SIGNAL ($\overline{R/\overline{W}}$)

Read/Write ($\overline{R/\overline{W}}$) controls the direction of data transfers between the PIA and the data lines associated with the CPU and the peripheral devices. A high on the $\overline{R/\overline{W}}$ line permits the peripheral devices to transfer data to the CPU from the PIA. A low on the $\overline{R/\overline{W}}$ line allows data to be transferred from the CPU to the peripheral devices from the PIA.

REGISTER SELECT ($\overline{RS0}$, $\overline{RS1}$)

The two Register Select lines ($\overline{RS0}$, $\overline{RS1}$), in conjunction with the Control Registers (CRA, CRB) Data Direction Register access bits (see Table 1, bit 2) select the various R65C21 registers to be accessed by the CPU. $\overline{RS0}$ and $\overline{RS1}$ are normally connected to the microprocessor (CPU) address output lines. Through control of these lines, the CPU can write directly into the Control

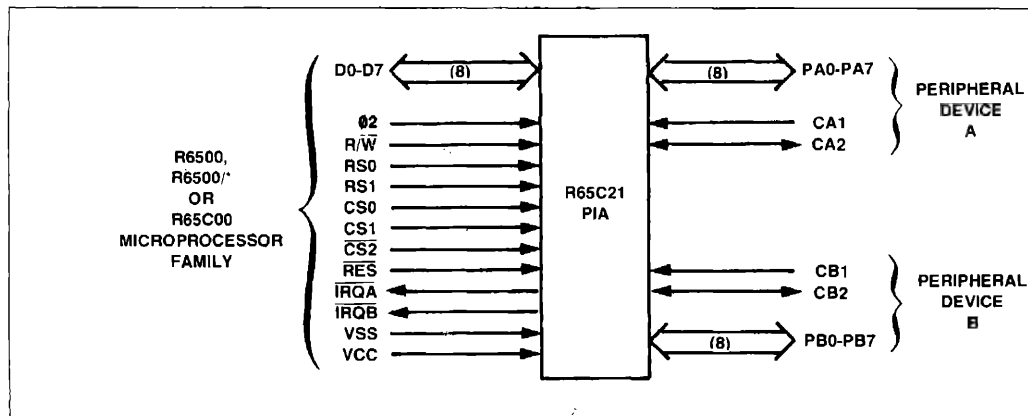


Figure 3. Interface Signals Relationship

Registers (CRA, CRB) the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore are shown separately in Table 2.

Table 2. ORA and ORB Register Addressing

Register Address (Hex)	Register Select Lines		Data Direction Control		Register Operation	
	RS1	RS0	CRA (Bit 2)	CRB (Bit 2)	R \overline{W} =H	R \overline{W} =L
0	L	L	1	—	Read PIBA	Write ORA
0	L	L	0	—	Read DDRA	Write DDRA
1	L	H	—	—	Read CRA	Write CRA
2	H	L	—	1	Read PIBB	Write ORB
2	H	L	—	0	Read DDRB	Write DDRB
3	H	H	—	—	Read CRB	Write CRB

INTERRUPT REQUEST LINES (\overline{IRQA} , \overline{IRQB})

The active low Interrupt Request lines (\overline{IRQA} and \overline{IRQB}) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are open drain and are capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a wired-OR configuration. The A and B in the titles of these lines correspond to the peripheral port A and the peripheral port B so that each Interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers (CRA, CRB). These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2). The four interrupt flags are set (enabled) by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

CRA bit 7 ($\overline{IRQA1}$) is always set by an active transition of the CA1 interrupt input signal. However, \overline{IRQA} can be disabled by setting bit 0 in CRA to a 0. Likewise, CRA bit 6 ($\overline{IRQA2}$) can be set by an active transition of the CA2 interrupt input signal and \overline{IRQA} can be disabled by setting bit 3 in CRA to a 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the read/write, proper data direction register and register select signals are provided to allow the processor to read the Peripheral A I/O port. A summary of \overline{IRQA} control is shown in Table 3.

Control of \overline{IRQB} is performed in exactly the same manner as that described above for \overline{IRQA} . Bit 7 in CRB ($\overline{IRQB1}$) is set by an active transition on CB1 and \overline{IRQB} from this flag is controlled

by CRB bit 0. Likewise, bit 6 ($\overline{IRQB2}$) in CRB is set by an active transition on CB2, and \overline{IRQB} from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 of CRB are reset by a "Read Peripheral B Output Register" operation. A summary of \overline{IRQB} control is shown in Table 3.

Table 3. \overline{IRQA} and \overline{IRQB} Control Summary

Control Register Bits	Action
CRA-7=1 and CRA-0=1	\overline{IRQA} goes low (Active)
CRA-6=1 and CRA-3=1	\overline{IRQA} goes low (Active)
CRB-7=1 and CRB-0=1	\overline{IRQB} goes low (Active)
CRB-6=1 and CRB-3=1	\overline{IRQB} goes low (Active)
Note:	
The flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.	

INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 4 summarizes the operation of these control lines.

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

NOTE:

A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

CA2 can act as a totally independent interrupt or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupt.

In the output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a 0 and CRA, bit 3 to a 1. This pulse output can be used to control the counters, shift registers, etc., which make sequential data available on the Peripheral input lines.

CONTROL REGISTER A (CRA)

CA2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQA1 FLAG	IRQA2 FLAG	CA2 INPUT MODE SELECT (=0)	IRQA2 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA2	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			IRQA/IRQA2 CONTROL			$\overline{\text{IRQA}}/\text{IRQA1}$ CONTROL	

CA2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQA1 FLAG	0	CA2 OUTPUT MODE SELECT (=1)	CA2 OUTPUT CONTROL	CA2 RESTORE CONTROL	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			CA2 CONTROL			$\overline{\text{IRQA}}/\text{IRQA1}$ CONTROL	

CA2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7	IRQA1 FLAG
1	A transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria. This bit is cleared by a read of Output Register A or by RES.
0	No transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria.
Bit 2	OUTPUT REGISTER A SELECT
1	Select Output Register A.
0	Select Data Direction Register A.
Bit 1	IRQA1 POSITIVE TRANSITION
1	Set IRQA1 Flag (bit 7) on a positive (low-to-high) transition of CA1.
0	Set IRQA1 Flag (bit 7) on a negative (high-to-low) transition of CA1.
Bit 0	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
1	Enable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.
0	Disable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.

CA2 INPUT MODE (BIT 5 = 0)

Bit 6	IRQA2 FLAG
1	A transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria. This flag is cleared by a read of Output Register A or by RES.
0	No transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria.
Bit 5	CA2 MODE SELECT
0	Select CA2 Input Mode.
Bit 4	IRQA2 POSITIVE TRANSITION
1	Set IRQA2 Flag (bit 6) on a positive (low-to-high) transition of CA2.
0	Set IRQA2 Flag (bit 6) on a negative (high-to-low) transition of CA2.
Bit 3	$\overline{\text{IRQA}}$ ENABLE FOR IRQA2
1	Enable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.
0	Disable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.

CA2 OUTPUT MODE (BIT 5 = 1)

Bit 6	NOT USED
0	Always zero.
Bit 5	CA2 MODE SELECT
1	Select CA2 Output Mode.
Bit 4	CA2 OUTPUT CONTROL
1	CA2 goes low when a zero is written into CRA bit 3. CA2 goes high when a one is written into CRA bit 3.
0	CA2 goes low on the first negative (high-to-low) $\phi 2$ clock transition following a read of Output Register A. CA2 returns high as specified by bit 3.
Bit 3	CA2 READ STROBE RESTORE CONTROL (4 = 0)
1	CA2 returns high on the next $\phi 2$ clock negative transition following a read of Output Register A.
0	CA2 returns high on the next active CA1 transition following a read of Output Register A as specified by bit 1.

Figure 4. Control Line Operations Summary (1 of 2)

CONTROL REGISTER B (CRB)

CB2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQB1 FLAG	IRQB2 FLAG	CB2 INPUT MODE SELECT (=0)	IRQB2 POSITIVE TRANSITION	IRQB ENABLE FOR IRQB2	ORB SELECT	IRQB1 POSITIVE TRANSITION	IRQB ENABLE FOR IRQB1
			IRQB/IRQB2 CONTROL			IRQB/IRQB1 CONTROL	

CB2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQB1 FLAG	0	CB2 OUTPUT MODE SELECT (=1)	CB2 OUTPUT CONTROL	CB2 RESTORE CONTROL	ORB SELECT	IRQB1 POSITIVE TRANSITION	IRQB ENABLE FOR IRQB1
			CB2 CONTROL			IRQB/IRQB1 CONTROL	

CB2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7	IRQB1 FLAG
1	A transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria. This bit is cleared by a read of Output Register B or by RES.
0	No transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria.
Bit 2	OUTPUT REGISTER B SELECT
1	Select Output Register B.
0	Select Data Direction Register B.
Bit 1	IRQB1 POSITIVE TRANSITION
1	Set IRQB1 Flag (bit 7) on a positive (low-to-high) transition of CB1.
0	Set IRQB1 Flag (bit 7) on a negative (high-to-low) transition of CB1.
Bit 0	IRQB ENABLE FOR IRQB1
1	Enable assertion of IRQB when IRQB1 Flag (bit 7) is set.
0	Disable assertion of IRQB when IRQB1 Flag (bit 7) is set.

CB2 INPUT MODE (BIT 5 = 0)

Bit 6	IRQB2 FLAG
1	A transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria. This flag is cleared by a read of Output Register B or by RES.
0	No transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria.
Bit 5	CB2 MODE SELECT
0	Select CB2 Input Mode.
Bit 4	IRQB2 POSITIVE TRANSITION
1	Set IRQB2 Flag (bit 6) on a positive (low-to-high) transition of CB2.
0	Set IRQB2 Flag (bit 6) on a negative (high-to-low) transition of CB2.
Bit 3	IRQB ENABLE FOR IRQB2
1	Enable assertion of IRQB when IRQB2 Flag (bit 6) is set.
0	Disable assertion of IRQB when IRQB2 Flag (bit 6) is set.

CB2 OUTPUT MODE (BIT 5 = 1)

Bit 6	NOT USED
0	Always zero.
Bit 5	CB2 MODE SELECT
1	Select CB2 Output Mode.
Bit 4	CB2 OUTPUT CONTROL
1	CB2 goes low when a zero is written into CRB bit 3.
0	CB2 goes high when a one is written into CRB bit 3.
	CB2 goes low on the first negative (high-to-low) #2 clock transition following a write to Output Register B. CB2 returns high as specified by bit 3.
Bit 3	CB2 WRITE STROBE RESTORE CONTROL (BIT 4 = 0)
1	CB2 returns high on the next #2 clock negative transition following a write to Output Register B.
0	CB2 returns high on the next active CB1 transition following a write to Output Register B as specified by bit 1.

Figure 4. Control Line Operations Summary (2 of 2)

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0 respectively.

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

READING THE PERIPHERAL A I/O PORT

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly

transfers the data on the Peripheral A I/O lines to the data bus. In this situation, the data bus will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read by the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

READING THE PERIPHERAL B I/O PORT

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back to the processor on a Read operation.

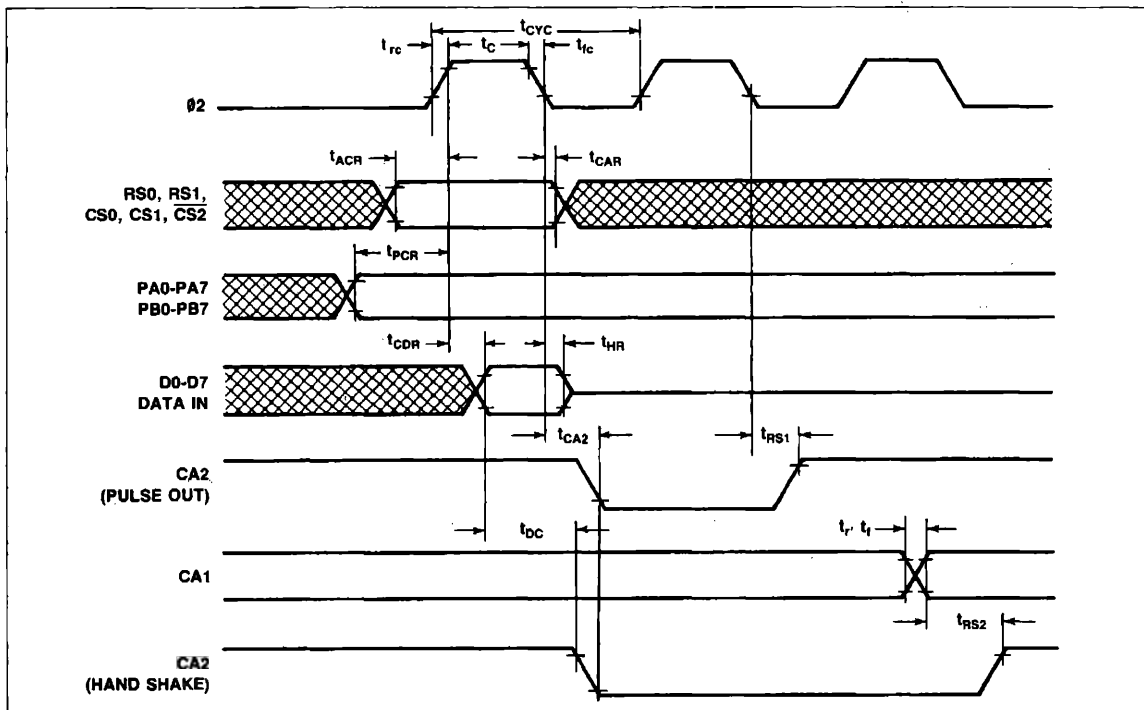


Figure 5. Read Timing Waveforms

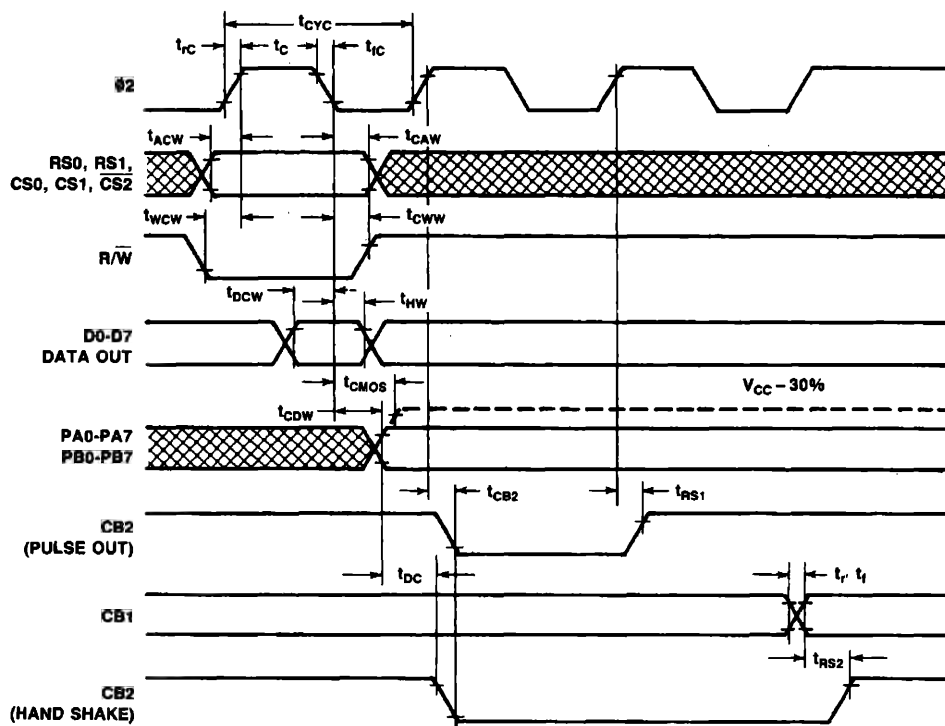


Figure 6. Write Timing Waveforms

BUS TIMING CHARACTERISTICS

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Ø2 Cycle	t_{CYC}	1.0	—	0.5	—	0.33	—	0.25	—	μs
Ø2 Pulse Width	t_C	480	—	240	—	180	—	120	—	ns
Ø2 Rise and Fall Time	t_{rC}, t_{fC}	—	25	—	15	—	12	—	10	ns

READ TIMING

Address Set-Up Time	t_{ACR}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	0	—	0	—	ns
Peripheral Data Set-Up Time	t_{PCR}	300	—	150	—	110	—	75	—	ns
Data Bus Delay Time	t_{CDR}	—	395	—	190	—	100	—	75	ns
Data Bus Hold Time	t_{HR}	20	—	20	—	20	—	20	—	ns

WRITE TIMING

Address Set-Up Time	t_{ACW}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAW}	0	—	0	—	0	—	0	—	ns
R/W Set-Up Time	t_{WCW}	180	—	90	—	67	—	45	—	ns
R/W Hold Time	t_{CWW}	0	—	0	—	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	180	—	90	—	67	—	45	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	10	—	10	—	ns
Peripheral Data Delay Time	t_{CPW}	—	1.0	—	0.5	—	0.33	—	0.25	μs
Peripheral Data Delay Time to CMOS Level	t_{CMOS}	—	2.0	—	1.0	—	0.7	—	0.5	μs

PERIPHERAL INTERFACE TIMING

Peripheral Data Set-Up	t_{PCR}	300	—	150	—	110	—	75	—	ns
Ø2 Low to CA2 Low Delay	t_{CA2}	—	1.0	—	0.5	—	0.33	—	0.25	μs
Ø2 Low to CA2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	μs
CA1 Active to CA2 High Delay	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.5	μs
Ø2 High to CB2 Low Delay	t_{CB2}	—	1.0	—	0.5	—	0.33	—	0.25	μs
Peripheral Data Valid to CB2 Low Delay	t_{DC}	0	1.5	0	0.75	0	0.5	0	0.37	μs
Ø2 High to CB2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	μs
CB1 Active to CB2 High Delay	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.5	μs
CA1, CA2, CB1 and CB2 Input Rise and Fall Time	t_r, t_f	—	1.0	—	1.0	—	1.0	—	1.0	μs

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	Vdc
Output Voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	Vdc
Operating Temperature Range Commercial Industrial	T_A	0 to +70 -40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V \pm 5%
Temperature Range Commercial Industrial	T_A	0°C to 70°C -40°C to +85°C

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0$, $T_A = T_L$ to T_H , unless otherwise noted)

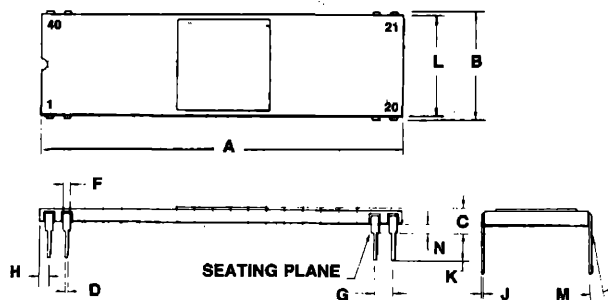
Parameter	Symbol	Min.	Typ. ³	Max.	Unit ²	Test Conditions
Input High Voltage All except PB0-PB7, RES PB0-PB7, RES	V_{IH}	+2.0 +2.4	— —	V_{CC} V_{CC}	V V	
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V	
Input Leakage Current R/W, RES, RS0, RS1, CS0, CS1, CS2, CA1, CB1, \emptyset 2	I_{IN}	—	± 1	± 2.5	μA	$V_{IN} = 0V$ to V_{CC} $V_{CC} = 5.25V$
Input Leakage Current for Three-State Off D0-D7, PB0-PB7, CB2	I_{TSI}	—	± 2	± 10	μA	$V_{IN} = 0.4V$ to $2.4V$ $V_{CC} = 5.25V$
Input High Current PA0-PA7, CA2	I_{IH}	-200	-300	—	μA	$V_{IH} = 2.4V$
Input Low Current PA0-PA7, CA2	I_{IL}	—	-2	-3.2	mA	$V_{IL} = 0.4V$
Output High Voltage Logic PB0-PB7, CB2 (Darlington Drive)	V_{OH}	2.4 1.5	— —	— —		$V_{CC} = 4.75V$ $I_{LOAD} = -200\mu A$ $I_{LOAD} = -3.2mA$
Output Low Voltage PA0-PA7, CA2, PB0-PB7, CB2 D0-D7, IRQA, IRQB	V_{OL}	—	—	+0.4	V	$V_{CC} = 4.75V$ $I_{LOAD} = 3.2 mA$ $I_{LOAD} = 1.6 mA$
Output High Current (Sourcing) Logic PB0-PB7, CB2 (Darlington Drive)	I_{OH}	-200 -3.2	-1500 -6	— —	μA mA	$V_{OH} = 2.4V$ $V_{OH} = 1.5V$
Output Low Current (Sinking) PA0-PA7, PB0-PB7, CB2, CA2 D0-D7, IRQA, IRQB	I_{OL}	3.2 1.6	— —	— —	mA mA	$V_{OL} = 0.4V$
Output Leakage Current (Off State) IRQA, IRQB	I_{OFF}	—	1	± 10	μA	$V_{OH} = 2.4V$ $V_{CC} = 5.25V$
Power Dissipation	P_D		7	10		mW/MHz
Input Capacitance D0-D7, PA0-PA7, PB0-PB7, CA2, CB2 R/W, RES, RS0, RS1, CS0, CS1, CS2 CA1, CB1, \emptyset 2	C_{IN}	— — —	— — —	10 7 20	pF pF pF	$V_{CC} = 5.0V$ $V_{IN} = 0V$ $f = 2 MHz$ $T_A = 25^\circ C$
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:

1. All units are direct current (dc) except capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.

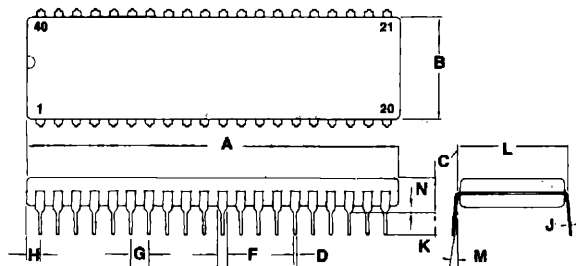
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0"	10"	0"	10"
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7"	10"	7"	10"
N	0.51	1.02	0.020	0.040



R65C24 PERIPHERAL INTERFACE ADAPTER/TIMER (PIAT)

PRELIMINARY

2

DESCRIPTION

The R65C24 Peripheral Interface Adapter/Timer (PIAT) is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the R6500, R6500/* or R65C00 family of microprocessors, the R65C24 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or to "handshake" data between the processor and a peripheral device.

The PIAT also contains one 16-bit Counter/Timer comprised of a 16-bit counter, two 8-bit latches associated with the counter, and an 8-bit snapshot latch for the upper half of the counter. A counter mode control register, under software direction, selects any one of eight counter modes of operation, and the status register contains an underflow flag to report counter time-out. A maskable interrupt request allows immediate CPU notification upon counter time-out.

ORDERING INFORMATION

The R65C24 is available in both a ceramic and a plastic 40-pin package, a commercial or industrial temperature range, and operating frequencies of 1, 2, 3, or 4 MHz. These versions are coded into the part number as follows:

Part Number:

R65C24

Temperature Range:

Blank = 0°C to +70°C

E = -40°C to +85°C

Frequency Range:

1 = 1 MHz

2 = 2 MHz

3 = 3 MHz

4 = 4 MHz

Package:

C = Ceramic

P = Plastic

FEATURES

- Low power CMOS N-well silicon gate technology
- Two 8-bit bidirectional I/O ports with individual data direction control
- Programmable 16-bit Counter/Timer with eight modes of operation
- Three 8-bit latches associated with the Counter/Timer
- Selectable divide-by-sixteen prescaler for all modes
- Automatic "Handshake" control of data transfers
- Two interrupts (one for each port) with program control
- 1, 2, 3, and 4 MHz versions
- Commercial and industrial temperature range versions
- 40-pin plastic and ceramic versions
- Single 5V \pm 5% supply requirements
- Compatible with the R6500, R6500/* and R65C00 family of microprocessors

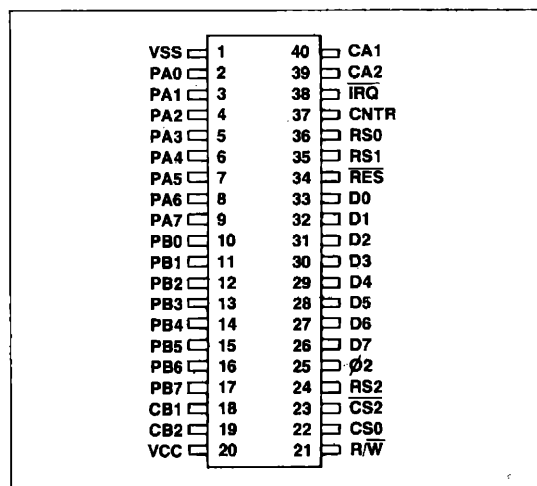


Figure 1. R65C24 Pin Configuration

FUNCTIONAL DESCRIPTION

The R65C24 PIAT is organized into three independent sections referred to as the A Side, the B Side, and a Counter/Timer. The A Side and B Side each consist of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control (ISCA, ISCB), and the buffers necessary to drive the Peripheral Interface buses. Data Bus Buffers (DBB) interface data from the two sections to the data bus, while the Data Input Register (DIR) interfaces data

from the DBB to the PIAT registers. Chip Select and R/W control circuitry interface to the processor bus control lines. The Counter/Timer consists of a 16-bit counter; i.e., an 8-bit Upper Counter (UC) and 8-bit Lower Counter (LC), an 8-bit Upper Latch (UL), an 8-bit Lower Latch (LL), an 8-bit Snapshot Latch (SL), and a Status Register (SR). A Counter Mode Control Register (CMCR) selects the Counter/Timer mode of operation. Figure 2 is a block diagram of the R65C24 PIAT.

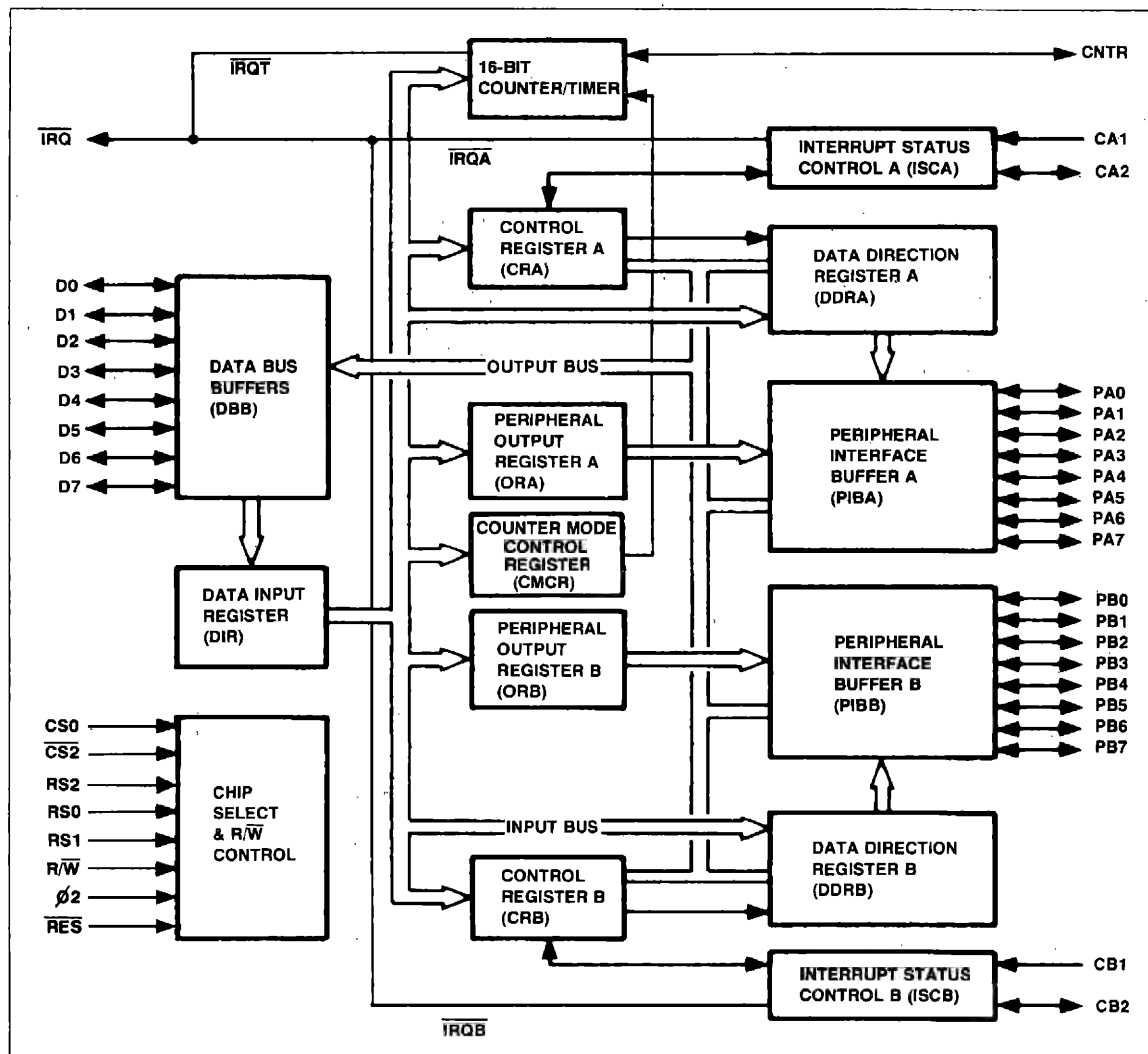


Figure 2. R65C24 PIAT Block Diagram

DATA INPUT REGISTER (DIR)

When the microprocessor writes data into the PIAT, the data which appears on the data bus during the $\phi 2$ clock pulse is latched into the Data Input Register (DIR). The data is then transferred into one of six internal registers of the PIAT after the trailing edge of the $\phi 2$ clock. This assures that the data on the peripheral output lines will make smooth transitions from high to low (or from low to high) and the voltage will remain stable except when it is going to the opposite polarity.

CONTROL REGISTERS (CRA AND CRB)

Table 1 illustrates the bit designation and functions in the two control registers. The control registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) in each control register indicate the status of the Interrupt input lines (CA1, CA2, CB1, CB2). These Interrupt Status bits (IRQA1, IRQA2 or IRQB1, IRQB2) are normally interrogated by the microprocessor during the IRQ interrupt service routine to determine the source of the interrupt.

DATA DIRECTION REGISTERS (DDRA, DDRB)

The Data Direction Registers (DDRA, DDRB) allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Writing a "0" in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

Bit 2 (DDRA, DDRB) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a "1," a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a "0," a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1 and RS2) selects the various internal registers as shown in Table 2.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

PERIPHERAL OUTPUT REGISTERS (ORA, ORB)

The Peripheral Output Registers (ORA, ORB) store the output data from the Data Bus Buffers (DBB) which appears on the Peripheral I/O port. If a line on the Peripheral A Port is programmed as an output by the DDRA, writing a 0 into the corresponding bit in the ORA causes that line to go low (<0.4 V); writing a 1 causes the line to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

INTERRUPT STATUS CONTROL (ISCA, ISCB)

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register and detects active transitions on the interrupt inputs.

PERIPHERAL I/O PORTS (PA0-PA7, PB0-PB7)

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by writing data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a 1 in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A 0 in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-up devices. These pull-up devices are resistive in nature and therefore allow the output voltage to go to VCC for a logic 1. The switches can sink a full 3.2 mA, making these buffers capable of driving two standard TTL loads.

In the input mode, the pull-up devices are still connected to the I/O pin and still supply current to this pin. For this reason, these lines also represent two standard TTL loads in the input mode.

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output is similar to the Peripheral A port, as is the effect of reading or writing this port. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

Table 1. Control Registers Bit Designations

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

The Peripheral B I/O port buffers are push-pull devices i.e., the pull-up devices are switched OFF in the 0 state and ON for a logic 1. Since these pull-ups are active devices, the logic 1 voltage will not go higher than +2.4V.

Unlike the PA0-PA7 lines (which have pull-up devices), the PB0 through PB7 lines have three-state capability which allows them to enter a high impedance state when programmed to be used as input lines. In addition, data on these lines will be read properly, when programmed as output lines, even if the data signals fall below 2.0 volts for a "high" state or are above 0.8 volts for a "low" state. When programmed as output, each line can drive at least a two TTL load and may also be used as a source of up to 3.2 milliamperes at 1.5 volts to directly drive the base of a transistor switch, such as a Darlingon pair.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic is the high-impedance input state which is a function of the Peripheral B push-pull buffers. When the

Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

DATA BUS BUFFERS (DBB)

The Data Bus Buffers are 8-bit bidirectional buffers used for data exchange, on the D0-D7 Data Bus, between the microprocessor and the PIAT. These buffers are tri-state and are capable of driving a two TTL load (when operating in an output mode) and represent a one TTL load to the microprocessor (when operating in an input mode).

COUNTER/TIMER

The Counter/Timer includes a 16-bit counter and three 8-bit data latches. It also includes an 8-bit Counter Mode Control Register (CMCR) to select the Counter/Timer operating mode and options and an 8-bit Status Register to report time-out condition as well as peripheral data port interrupt conditions. Figure 3 illustrates the Timer/Counter.

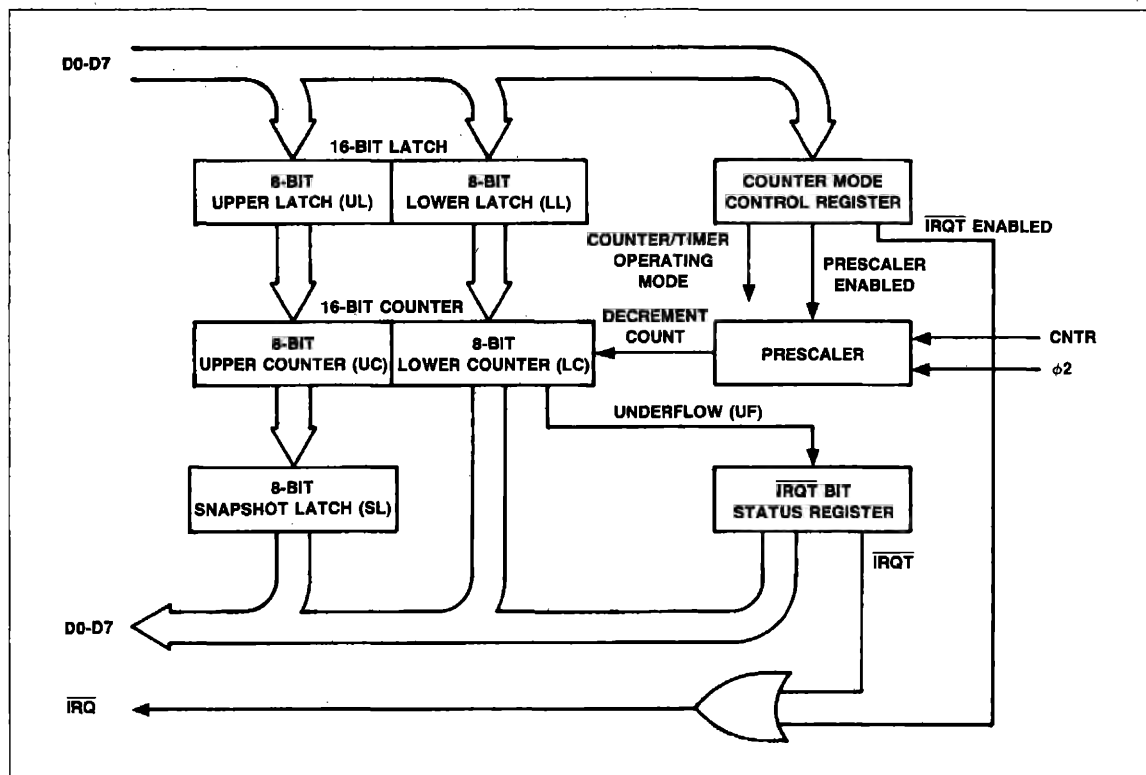


Figure 3. Counter/Timer

Counter/Latches—The Upper Counter (UC) and Lower Counter (LC) form a 16-bit down-counter that counts either $\phi/2$ clock pulses from the processor bus or external events from input line CNTR, depending on the mode selected. The Upper Latch (UL) and Lower Latch (LL) hold the initial higher- and lower-order count values to be loaded into the counter. The Snapshot Latch (SL) is loaded with the value of the UC when the LC is read or the LL is written into by the PIAT. After a read of the LC, the Snapshot Latch is read to provide the current 16-bit value of the counter. The Underflow Flag (UF) in the Status Register (SR) is set to a 1 whenever the counter (UC, LC) decrements past \$0000. A Prescaler can be program activated to divide-by-sixteen rather than divide-by-one for any of the Counter/Timer modes.

Counter Mode Control Register—The Counter Mode Control Register (CMCR) allows program selection of any of eight Counter/Timer modes of operation, for the enabling or disabling of the Prescaler, and the enabling or disabling of the $\overline{\text{IRQT}}$ interrupt line. Bits 2, 1, 0 of the CMCR selects one of the following Counter/Timer operating modes:

- Disable Counter/Timer
- One-Shot Interval Timer
- Free-Run Interval Timer
- Pulse Width Measurement
- Event Counter
- One-Shot Pulse Width Generation
- Free-Run Pulse Generation
- Retriggerable Interval Timer

Bit 7 of the CMCR determines whether the $\overline{\text{IRQT}}$ line is enabled or disabled for generating an interrupt request on the $\overline{\text{IRQ}}$ output to the processor. When bit 7 is set to a 1, $\overline{\text{IRQT}}$ is enabled so that an Underflow Flag (UF bit in the Status Register set to a 1) will cause $\overline{\text{IRQ}}$ to be asserted. When bit 7 is set to a 0, the $\overline{\text{IRQT}}$ is disabled.

Bit 4 of the CMCR enables or disables the Prescaler. A 1 in bit 4 causes the Prescaler to be enabled so that the Counter/Timer is operating in a divide-by-sixteen mode. When this bit is a 0, the Prescaler is disabled so that the Counter/Timer is operating in a normal (divide-by-one) mode.

Status Register—Bit 7 of the Status Register (SR) reports the Counter Underflow Status. This underflow (UF) bit is set to 1 when the counter decrements past \$0000. When this bit is set, the $\overline{\text{IRQ}}$ output will be asserted if the Interrupt Enable bit in the CMCR is set to a 1. The status of the Port A Interrupt Flag ($\overline{\text{IRQA}}$) and Port B Interrupt Flag ($\overline{\text{IRQB}}$) are reported in bits 6 and 5, respectively, in addition to being reported in the ISCA and ISCB registers.

INTERFACE SIGNALS

The PIAT interfaces to the R6500, R6500* or the R65C00 microprocessor family with a reset line, a $\phi/2$ clock line, a read/write line, an interrupt request line, three register select lines, two chip select lines, and an 8-bit bidirectional data bus.

The PIAT interfaces to the peripheral devices with four interrupt/control lines and two 8-bit bidirectional data buses. A Counter/Timer input/output line (CNTR) also interfaces to a peripheral device.

Figure 1 (on the front page) shows the pin assignments for these interface signals and Figure 4 shows the interface relationship of these signals as they pertain to the CPU and the peripheral devices.

CHIP SELECT ($\overline{\text{CS0}}$, $\overline{\text{CS2}}$)

The PIAT is selected when $\overline{\text{CS0}}$ is high and $\overline{\text{CS2}}$ is low. These two chip select lines are normally connected to the processor address lines either directly or through external decoder circuits. When the PIAT is selected, data will be transferred between the data lines and PIAT registers, and/or peripheral interface lines as determined by the R/W, RS0, RS1 and RS2 lines and the contents of Control Registers A and B.

Note:

An R65C24 PIAT may be installed in a circuit in place of an R65C21 PIA subject to chip select considerations. Since the R65C21 has a $\overline{\text{CS1}}$ input and the R65C24 does not have a $\overline{\text{CS1}}$ input, the PIAT will be selected in the same addresses as the PIA and maybe more depending upon external address decoding circuitry.

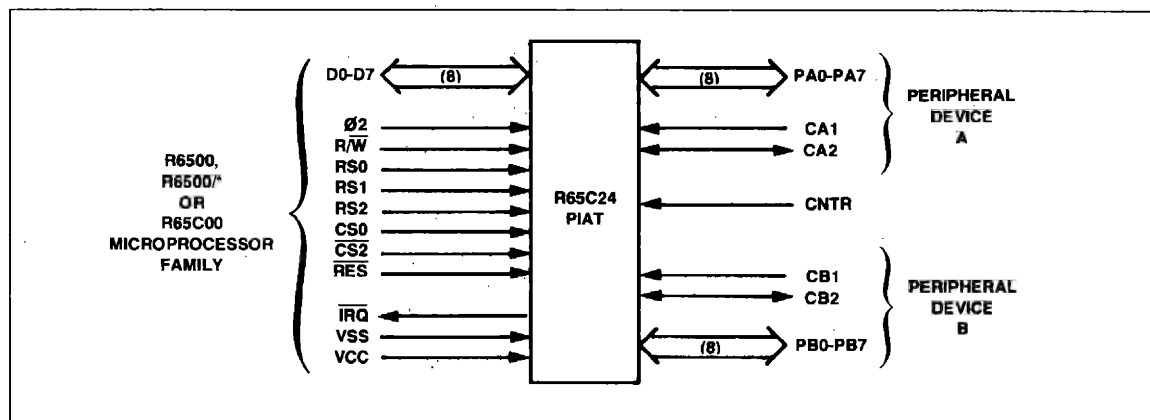


Figure 4. Interface Signals Relationship

RESET SIGNAL ($\overline{\text{RES}}$)

The Reset ($\overline{\text{RES}}$) input initializes the R65C24 PIAT. A low signal on the $\overline{\text{RES}}$ input causes all internal registers to be cleared.

CLOCK SIGNAL ($\phi 2$)

The Phase 2 Clock Signal ($\phi 2$) is the system clock that triggers all data transfers between the CPU and the PIAT. $\phi 2$ is generated by the CPU and is therefore the synchronizing signal between the CPU and the PIAT.

READ/WRITE SIGNAL ($\overline{\text{R/W}}$)

Read/Write ($\overline{\text{R/W}}$) controls the direction of data transfers between the PIAT and the data lines associated with the CPU and the peripheral devices. A high on the $\overline{\text{R/W}}$ line permits the peripheral devices to transfer data to the CPU from the PIAT. A low on the $\overline{\text{R/W}}$ line allows data to be transferred from the CPU to the peripheral devices from the PIAT.

REGISTER SELECT (RS0, RS1, RS2)

Two of the Register Select lines (RS0, RS1), in conjunction with the Control Registers (CRA, CRB) Data Direction Register access bits select various R65C24 registers to be accessed by the CPU. RS0 and RS1 are normally connected to the microprocessor (CPU) address output lines. Through control of these lines, the CPU can write directly into the Control Registers (CRA, CRB) the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore are shown separately in Table 2.

Note:

In order to address the ORA and ORB Registers in the PIAT, Register Select line RS2 *must be high*. When RS2 is low, the Counter/Timer registers are selected (as shown in Table 3).

Table 2. Peripheral Register Addressing

Register Address (Hex)	Register Select Lines			Data Direction Register Control		Register Operation	
	RS2	RS1	RS0	CRA (Bit 2)	CRB (Bit 2)	$\overline{\text{R/W}} = \text{H}$	$\overline{\text{R/W}} = \text{L}$
4	H	L	L	1	—	Read PIBA	Write ORA
4	H	L	L	0	—	Read DDRA	Write DDRA
5	H	L	H	—	—	Read CRA	Write CRA
6	H	H	L	—	1	Read PIBB	Write ORB
6	H	H	L	—	0	Read DDRB	Write DDRA
7	H	H	H	—	—	Read CRB	Write CRB

Register Select line RS2 determines whether the addressed registers are part of the Counter/Timer or the peripheral Port A and Port B sections of the PIAT. When RS2 is high, the Port A/Port B registers shown in Table 2 are selected. When the RS2 is low, the Counter/Timer registers are selected and operated upon as shown in Table 3.

Table 3. Counter/Timer Register Addressing

Register Address (Hex)	Register Select Lines			Counter/Timer Operation	
	RS2	RS1	RS0	($\overline{\text{R/W}} = \text{H}$)	($\overline{\text{R/W}} = \text{L}$)
0	L	L	L	Read Snapshot Latch (SL) SL \rightarrow D0-D7 0 \rightarrow UF	Write Upper Latch (UL) D0-D7 \rightarrow UL 0 \rightarrow UF Load and Enable Counter UL \rightarrow UC, LL \rightarrow LC
1	L	L	H	Read Upper Counter (UC) UC \rightarrow D0-D7	Write Upper Latch (UL) D0-D7 \rightarrow UL
2	L	H	L	Read Lower Counter (LC) LC \rightarrow D0-D7 UC \rightarrow SL	Write Lower Latch (LL) D0-D7 \rightarrow LL UC \rightarrow SL
3	L	H	H	Read Status Register (SR) SR \rightarrow D0-D7 0 \rightarrow UF	Write Counter Control Mode Register (CMCR) D0-D7 \rightarrow CMCR

INTERRUPT REQUEST LINE ($\overline{\text{IRQ}}$)

Three internal active low Interrupt Request lines ($\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, and $\overline{\text{IRQT}}$) act to interrupt the microprocessor through the external $\overline{\text{IRQ}}$ output. $\overline{\text{IRQ}}$ is an open drain output and is capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a wired-OR configuration. The A and B in the titles of these internal lines correspond to the peripheral port A and the peripheral port B so that each interrupt request line services one peripheral data port. The T corresponds to the Counter/Timer generated interrupt request.

$\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ Lines—These two internal Interrupt Request lines are associated with the Port A and Port B sections of the PIAT and are controlled by Control Registers CRA and CRB, and the Peripheral Control lines CA1, CA2, CB1, and CB2.

These Interrupt Request lines have three interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers (CRA, CRB). These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt

inputs (CA1, CA2, CB1, CB2). The four interrupt flags are set (enabled) by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

CRA bit 7 (IRQA1) is always set by an active transition of the CA1 interrupt input signal. However, $\overline{\text{IRQA}}$ can be disabled by setting bit 0 in CRA to a 0. Likewise, CRA bit 6 (IRQA2) can be set by an active transition of the CA2 interrupt input signal and $\overline{\text{IRQA}}$ can be disabled by setting bit 3 in CRA to a 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the read/write, proper data direction register and register select signals are provided to allow the processor to read the Peripheral A I/O port. A summary of $\overline{\text{IRQA}}$ control is shown in Table 3.

Control of $\overline{\text{IRQB}}$ is performed in exactly the same manner as that described above for $\overline{\text{IRQA}}$. Bit 7 in CRB ($\overline{\text{IRQB1}}$) is set by an active transition on CB1 and $\overline{\text{IRQB}}$ from this flag is controlled by CRB bit 0. Likewise, bit 6 ($\overline{\text{IRQB2}}$) in CRB is set by an active transition on CB2, and $\overline{\text{IRQB}}$ from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 of CRB are reset by a "Read Peripheral B Output Register" operation. A summary of $\overline{\text{IRQB}}$ control is shown in Table 4.

Table 4. $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ Control Summary

Control Register Bits	Action
CRA-7=1 and CRA-0=1	$\overline{\text{IRQA}}$ goes low (Active)
CRA-6=1 and CRA-3=1	$\overline{\text{IRQA}}$ goes low (Active)
CRB-7=1 and CRB-0=1	$\overline{\text{IRQB}}$ goes low (Active)
CRB-6=1 and CRB-3=1	$\overline{\text{IRQB}}$ goes low (Active)
<p>Note:</p> <p>The flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.</p>	

$\overline{\text{IRQT}}$ Line—The internal $\overline{\text{IRQT}}$ line is associated with the Counter/Timer and is controlled by the $\overline{\text{IRQT}}$ Enable bit in the Counter Mode Control Register and the Underflow Flag in the Status Register. A thorough discussion of the functions and operation of the $\overline{\text{IRQT}}$ line is given in the Counter/Timer Operation section of this product description.

INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 5 summarizes the operation of these control lines.

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

Note:

A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

CA2 can act as a totally independent interrupt or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupt.

In the output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a 0 and CRA, bit 3 to a 1. This pulse output can be used to control the counters, shift registers, etc. which make sequential data available on the Peripheral input lines.

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0 respectively.

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

CA2 INPUT MODE (BIT 5 = 0)

CONTROL REGISTER A (CRA)

7	6	5	4	3	2	1	0
IRQA1 FLAG	IRQA2 FLAG	CA2 INPUT MODE SELECT (=0)	IRQA2 POSITIVE TRANSITION	IRQA ENABLE FOR IRQA2	ORA SELECT	IRQA1 POSITIVE TRANSITION	IRQA ENABLE FOR IRQA1
			IRQA/IRQA2 CONTROL			IRQA/IRQA1 CONTROL	

CA2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQA1 FLAG	0	CA2 OUTPUT MODE SELECT (=1)	CA2 OUTPUT CONTROL	CA2 RESTORE CONTROL	ORA SELECT	IRQA1 POSITIVE TRANSITION	IRQA ENABLE FOR IRQA1
			CA2 CONTROL			IRQA/IRQA1 CONTROL	

CA2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7	IRQA1 FLAG
1	A transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria. This bit is cleared by a read of Output Register A or by RES.
0	No transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria.
Bit 2	OUTPUT REGISTER A SELECT
1	Select Output Register A.
0	Select Data Direction Register A.
Bit 1	IRQA1 POSITIVE TRANSITION
1	Set IRQA1 Flag (bit 7) on a positive (low-to-high) transition of CA1.
0	Set IRQA1 Flag (bit 7) on a negative (high-to-low) transition of CA1.
Bit 0	IRQA ENABLE FOR IRQA1
1	Enable assertion of IRQA when IRQA1 Flag (bit 7) is set.
0	Disable assertion of IRQA when IRQA1 Flag (bit 7) is set.

CA2 INPUT MODE (BIT 5 = 0)

Bit 6	IRQA2 FLAG
1	A transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria. This flag is cleared by a read of Output Register A or by RES.
0	No transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria.
Bit 5	CA2 MODE SELECT
0	Select CA2 Input Mode.
Bit 4	IRQA2 POSITIVE TRANSITION
1	Set IRQA2 Flag (bit 6) on a positive (low-to-high) transition of CA2.
0	Set IRQA2 Flag (bit 6) on a negative (high-to-low) transition of CA2.
Bit 3	IRQA ENABLE FOR IRQA2
1	Enable assertion of IRQA when IRQA2 Flag (bit 6) is set.
0	Disable assertion of IRQA when IRQA2 Flag (bit 6) is set.

CA2 OUTPUT MODE (BIT 5 = 1)

Bit 6	NOT USED
0	Always zero.
Bit 5	CA2 MODE SELECT
1	Select CA2 Output Mode.
Bit 4	CA2 OUTPUT CONTROL
1	CA2 goes low when a zero is written into CRA bit 3. CA2 goes high when a one is written into CRA bit 3.
0	CA2 goes low on the first negative (high-to-low) ϕ 2 clock transition following a read of Output Register A. CA2 returns high as specified by bit 3.
Bit 3	CA2 READ STROBE RESTORE CONTROL (BIT 4 = 0)
1	CA2 returns high on the next ϕ 2 clock negative transition following a read of Output Register A.
0	CA2 returns high on the next active CA1 transition following a read of Output Register A as specified by bit 1.

Figure 5. Summary of Control Lines Operation (1 of 2)

CB2 INPUT MODE (BIT 5 = 0)

CONTROL REGISTER B (CRB)

7	6	5	4	3	2	1	0
IRQB1 FLAG	IRQB2 FLAG	CB2 INPUT MODE SELECT (=0)	IRQB2 POSITIVE TRANSITION	IRQB ENABLE FOR IRQB2	ORB SELECT	IRQB1 POSITIVE TRANSITION	IRQB ENABLE FOR IRQB1
			IRQB/IRQB2 CONTROL			IRQB/IRQB1 CONTROL	

CB2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQB1 FLAG	0	CB2 OUTPUT MODE SELECT (=1)	CB2 OUTPUT CONTROL	CB2 RESTORE CONTROL	ORB SELECT	IRQB1 POSITIVE TRANSITION	IRQB ENABLE FOR IRQB1
			CB2 CONTROL			IRQB/IRQB1 CONTROL	

CB2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7	IRQB1 FLAG
1	A transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria. This bit is cleared by a read of Output Register B or by RES.
0	No transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria.
Bit 2	OUTPUT REGISTER B SELECT
1	Select Output Register B.
0	Select Data Direction Register B.
Bit 1	IRQB1 POSITIVE TRANSITION
1	Set IRQB1 Flag (bit 7) on a positive (low-to-high) transition of CB1.
0	Set IRQB1 Flag (bit 7) on a negative (high-to-low) transition of CB1.
Bit 0	IRQB ENABLE FOR IRQB1
1	Enable assertion of IRQB when IRQB1 Flag (bit 7) is set.
0	Disable assertion of IRQB when IRQB1 Flag (bit 7) is set.

CB2 INPUT MODE (BIT 5 = 0)

Bit 6	IRQB2 FLAG
1	A transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria. This flag is cleared by a read of Output Register B or by RES.
0	No transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria.
Bit 5	CB2 MODE SELECT
0	Select CB2 Input Mode.
Bit 4	IRQB2 POSITIVE TRANSITION
1	Set IRQB2 Flag (bit 6) on a positive (low-to-high) transition of CB2.
0	Set IRQB2 Flag (bit 6) on a negative (high-to-low) transition of CB2.
Bit 3	IRQB ENABLE FOR IRQB2
1	Enable assertion of IRQB when IRQB2 Flag (bit 6) is set.
0	Disable assertion of IRQB when IRQB2 Flag (bit 6) is set.

CB2 OUTPUT MODE (BIT 5 = 1)

Bit 6	NOT USED
0	Always zero.
Bit 5	CB2 MODE SELECT
1	Select CB2 Output Mode.
Bit 4	CB2 OUTPUT CONTROL
1	CB2 goes low when a zero is written into CRB bit 3. CB2 goes high when a one is written into CRB bit 3.
0	CB2 goes low on the first negative (high-to-low) ϕ_2 clock transition following a write to Output Register B. CB2 returns high as specified by bit 3.
Bit 3	CB2 WRITE STROBE RESTORE CONTROL (BIT 4 = 0)
1	CB2 returns high on the next ϕ_2 clock negative transition following a write to Output Register B.
0	CB2 returns high on the next active CB1 transition following a write to Output Register B as specified by bit 1.

Figure 5. Summary of Control Lines Operation (2 of 2)

COUNTER/TIMER REGISTERS

COUNTER MODE CONTROL REGISTER (CMCR)

The 8-bit Counter Mode Control Register (CMCR) selects the Counter/Timer mode of operation and enables or disables both the internal $\overline{\text{IRQT}}$ and the Prescaler. The format of the CMCR is:

7	6	5	4	3	2	1	0
$\overline{\text{IRQT}}$ Enabled	0	0	Prescaler Enabled	0	Counter/Timer Mode		

Bit 7 $\overline{\text{IRQT}}$ Enabled

0 $\overline{\text{IRQT}}$ Disabled

1 $\overline{\text{IRQT}}$ Enabled

Bits 6-5 Not used, don't care value during write.

Bit 4 Prescaler Enabled

0 Prescaler Disabled ($\div 1$)

1 Prescaler Enabled ($\div 16$)

Bit 3 Not used, don't care value during write.

Bits 2-0 Counter/Timer Mode

0 0 0 Mode 0—Disable Counter/Timer

0 0 1 Mode 1—One-Shot Interval Timer

0 1 0 Mode 2—Free-Run Interval Timer

0 1 1 Mode 3—Pulse Width Measurement

1 0 0 Mode 4—Event Counter

1 0 1 Mode 5—One-Shot Pulse Width Generation

1 1 0 Mode 6—Free-Run Pulse Generation

1 1 1 Mode 7—Retriggerable Interval Timer

The CMCR can be written into at any time without disabling or stopping the Counter/Timer. This allows the Counter/Timer mode of operation to be changed while it is still in operation. However, selecting Mode 0 disables the Counter/Timer and stops its operation. The Prescaler and the $\overline{\text{IRQT}}$ interrupt can also be enabled or disabled at any time. The CMCR is written to when the register address is 3 and $\overline{\text{R/W}}$ is low.

STATUS REGISTER (SR)

The 8-bit Status Register (SR) reports the status of two interrupt conditions: Counter underflow ($\overline{\text{IRQT}}$) and Port A interrupt ($\overline{\text{IRQA}}$). The format of the Status Register is:

7	6	5	4	3	2	1	0
UF ($\overline{\text{IRQT}}$) Interrupt Flag	IRQA Interrupt Flag	0	1	1	1	1	1

Bit 7 Counter Underflow (UF) Interrupt Flag

0 Counter underflow has not occurred.

1 Counter underflow has occurred.

Bit 6 IRQA Interrupt Flag

0 Port A interrupt has not occurred.

1 Port A interrupt has not occurred.

Bit 5-0 Not used, always read as shown in register figure.

The Counter underflow (UF), bit 7, is updated in the same clock cycle that an underflow condition occurs on the Counter/Timer. The $\overline{\text{IRQA}}$ interrupt flag (bit 6) is updated at the rising edge of the next $\phi 2$ clock immediately following the setting of corresponding interrupt bits ($\overline{\text{IRQA1}}$, $\overline{\text{IRQA2}}$) in the CRA register. $\overline{\text{IRQA}}$ is set whenever $\overline{\text{IRQA1}}$ or $\overline{\text{IRQA2}}$ is set. The underflow bit is cleared whenever the Status Register is read, the Snapshot Latch is read, the UL is written to at register address 0, Mode 0 is selected in the CMCR, or a $\overline{\text{RES}}$ occurs. Reading the Status Register also clears the $\overline{\text{IRQA}}$ interrupt flag. The Status Register is read when the register address is 3 and $\overline{\text{R/W}}$ is high.

LOWER LATCH (LL)

The Lower Latch (LL) holds the least significant 8-bits of the 16-bit latch value. The LL is written from the data bus (D0-D7) when the register address is 2 and $\overline{\text{R/W}}$ is low. When the LL is loaded, the contents of the UC are copied into the Snapshot Latch (SL) without affecting the counting operation of the UC.

UPPER LATCH (UL)

The Upper Latch (UL) holds the most significant 8-bits of the 16-bit latch value. The UL is written from the data bus (D0-D7) when $\overline{\text{R/W}}$ is low and the register address is either 0 or 1. The difference in the two register address functions are:

Register Address 0

1. The UL is loaded from D0-D7.
2. The contents of the Latch (UL and LL) are transferred to the Counter (UC and LC, respectively).
3. The UF bit is cleared in the SR.
4. The Counter is enabled, i.e., the count in UC and LC is decremented by one upon detection of a rising edge on either $\phi 2$ or CNTR (depending upon mode selection) as scaled by the Prescaler.

Register Address 1

1. The UL is loaded from D0-D7.
2. All other elements of the Counter/Timer are unaffected.

LOWER COUNTER (LC)

The Lower Counter (LC) holds the least significant 8-bits of the 16-bit counter.

When the LC decrements below \$00, 1 is borrowed from the UC to load \$FF into the LC.

The LC is read to the data bus (D0-D7) when the register address is 2 and $\overline{R/W}$ is high. When LC is read, the 8-bit contents of the UC is transferred to the Snapshot Latch without affecting the operation of the counter (i.e., the count-down continues without interruption).

UPPER COUNTER

The Upper Counter (UC) holds the most significant 8-bits of the 16-bit counter. The UC is read to the data bus (D0-D7) when the register address is 1 and $\overline{R/W}$ is high. When the UC is read, there is no other effect on the Counter/Timer operation. Counter underflow occurs when the LC borrows a 1 from the UC value of \$00.

Note:

When reading the UC directly, the value read can be one count too high if the LC value is just above \$0000 at the start of the read since an underflow in the LC will result in decrementing the UC by one count. The Snapshot Latch should be read to obtain the UC value corresponding to the LC value.

SNAPSHOT LATCH (SL)

The Snapshot Latch holds the value of the UC corresponding to the LC value. The SL is loaded with the value of the UC when the LL is written to, or when the LC is read. The SL is read to the data bus (D0-D7) when the register address is 0 and $\overline{R/W}$ is high, without affecting the counting operation. When the SL is read, the UF bit in the SR is cleared. Since the SL is loaded with the value of the UC whenever the LC is read, an accurate count of the total 16-bit counter can be made without the need for further calculations to account for delays between the reading of the LC and the UC.

COUNTER/TIMER OPERATION

The Counter/Timer has eight modes of operation. The Counter/Timer is always either disabled (mode 0) or operating in one of the other seven modes as selected in the Counter Mode Control Register (CMCR).

To operate the Counter/Timer, first issue Mode 0 to stop any counting in progress due to a previously selected mode, to clear the counter underflow bit in the SR and to disable the \overline{IRQ} interrupt. The order of mode selection and latch loading depends upon the desired mode. Generally, if a timer mode based on the $\phi/2$ clock rate is to be selected, first select the mode then write the timer initialization value to the latch. Write the LL first then the UL value (to register address 0). When the UL is written, the

UL and LL values are loaded into the UC and LC, respectively, and the counter is enabled. The counter then decrements one count for every positive edge (low to high) transition detected on the $\phi/2$ or CNTR input (depending on the selected mode) as scaled by the Prescaler. In most modes, each time the counter underflows below \$0000, the underflow bit is set in the SR, the counter reloads to the latch value and the down-counting continues. If the UF bit is set when the \overline{IRQ} is enabled in the CMCR, the \overline{IRQ} output will be asserted to the processor.

MODE 0—DISABLE COUNTER/TIMER

The Counter/Timer is disabled (all counting stops), the \overline{IRQ} interrupt (bit 7 in the CMCR) is disabled, and the counter underflow (bit 7 in the SR) is cleared. Mode 0 may be selected at any time by selecting Mode 0 in the CMCR or upon \overline{RES} which initializes the CMCR to \$00. Selecting Mode 0 in the CMCR does not affect any data in the LL or UL, any count in the LC or UC, or any data in the SL.

MODE 1—ONE SHOT INTERVAL TIMER

The counter counts down once from the latch value at the $\phi/2$ clock rate (as scaled by the Prescaler) and sets the UF bit in the SR upon underflow. The counter starts when data is written to the UL at register address 0, which causes the UL and LL values to be loaded into the UC and LC, respectively. When the counter decrements below \$0000, the UF bit in the SR is set. The set UF bit causes \overline{IRQ} to be asserted if the \overline{IRQ} Enable bit is set in the CMCR. Upon decrementing below \$0000, the UC and LC are automatically reset to a value of \$FFFF and the counter continues down-counting. However, the UF bit in the SR will not be set again (due to the counter again decrementing through \$0000) until the UL is again written at register address 0. The CNTR line is not used in this mode. Figure 6 shows the timing relationship for Mode 1 operation.

Typical Application: Can be used for an accurate time delay such as would be required to control the duration of time to have a thermal printer element activated.

MODE 2—FREE-RUN INTERVAL TIMER

The counter repetitively counts down at the $\phi/2$ clock rate, as scaled by the Prescaler, and sets the UF bit in the SR each time the counter underflows. The counter is initialized to the UL and LL values and starts down counting at the clock rate when the UL value is written to register address 0. Each time the counter decrements below \$0000, the UF bit in the SR is set, the counter is reloaded with the UL and LL value, and the count-down cycle continues. If the \overline{IRQ} Enable bit is set in the CMCR, \overline{IRQ} will thus be asserted upon each time-out. The CNTR line is not used in this mode. Figure 7 shows the timing relationship for Mode 2 operation.

Typical Application: Can be used for a timed interrupt structure when a hardware location needs updating at specific intervals, such as would be required to update a multiplexed display.

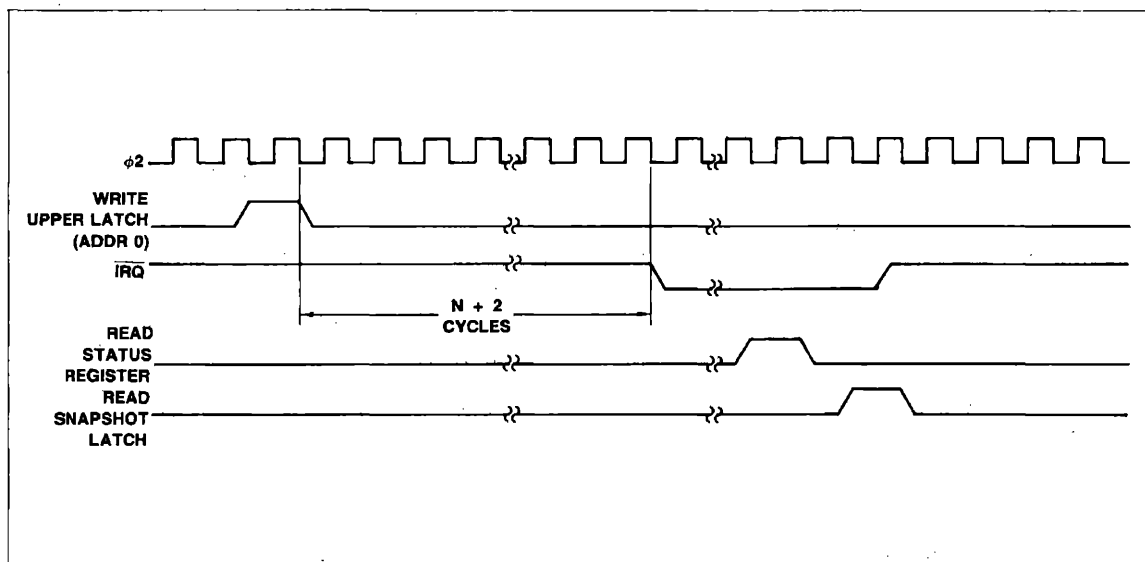


Figure 6. Mode 1—One-Shot Interval Timer Timing

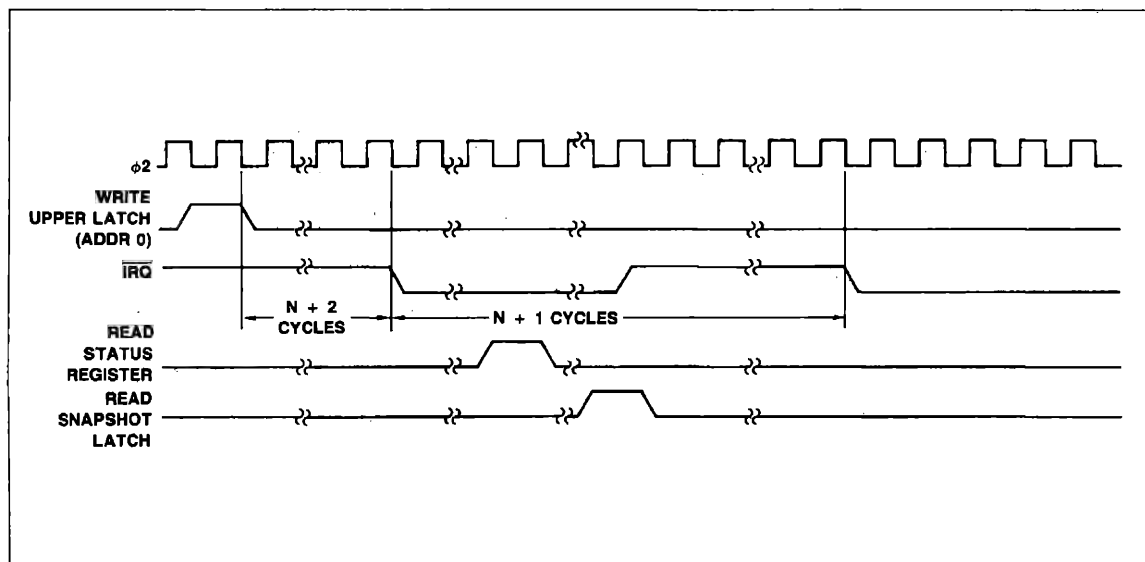


Figure 7. Mode 2—Free-Run Interval Timer Timing

MODE 3—PULSE WIDTH MEASUREMENT

The counter counts down from the latch value at the $\phi 2$ clock rate (scaled by the Prescaler) from the time the CNTR input goes low until CNTR goes high to provide a measurement of the CNTR low pulse duration. The counter is loaded with the value of the UL and LL upon writing UL to register address 0. The counter starts decrementing at the scaled $\phi 2$ clock rate when the CNTR line goes low and stops decrementing when the CNTR line returns high. If the counter decrements below \$0000 before the CNTR line goes low, the UF bit in the SR is set, the counter is reloaded with the UL and LL value, and the cycle continues down until CNTR goes high. Once the CNTR line has cycled from high to low and back to high, the Counter/Timer will ignore any additional high to low transitions on the CNTR line. To reinitiate Mode 3, it is necessary to reload the UL by writing to register address 0. Figure 8 shows the timing relationships for a Mode 3 operation.

Typical Application: Can be used to measure the duration of an event from an external device. Allows an accurate measurement of the duration of a logical low pulse on the CNTR line.

MODE 4—EVENT COUNTER

CNTR is an input and the Counter/Timer counts the number of positive transitions on CNTR. The counter is initially loaded with the UL and LL value when the UL is written to register address 0. The counter then decrements one count on the rising edge of the $\phi 2$ clock after a rising edge (low to high transition) is detected on the CNTR input (as scaled by the Prescaler). The maximum rate at which this rising edge can be detected is one-half the $\phi 2$ clock rate. When the counter decrements below \$0000, the UF bit in the SR is set, the counter is reloaded with the UL and LL value and the operation repeats. Figure 9 shows the timing relationship of a Mode 4 operation.

Typical Application: Can be used with a timed software loop to count external events (i.e., a frequency counter).

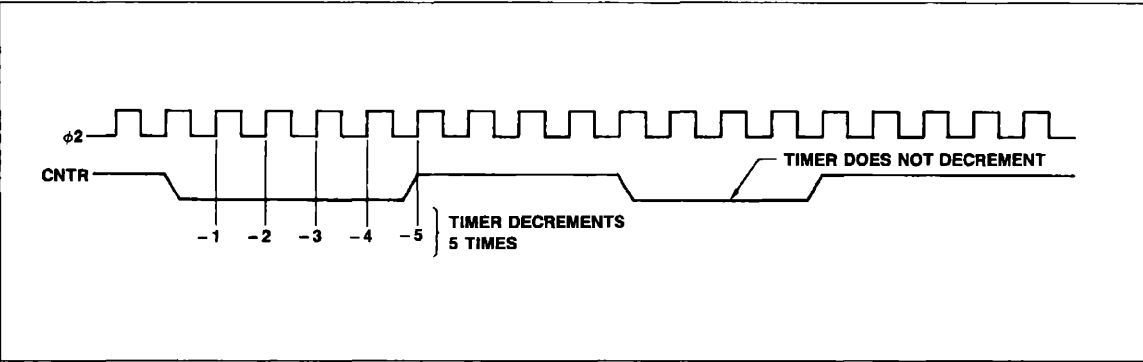


Figure 8. Mode 3—Pulse Width Measurement Timing

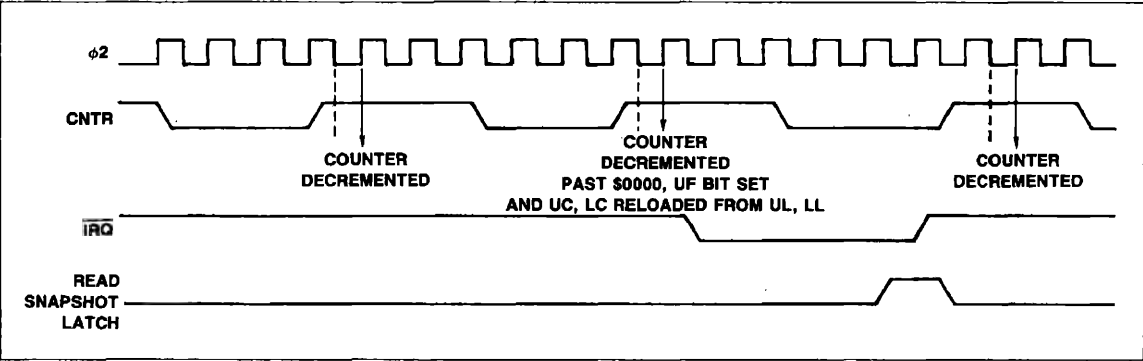


Figure 9. Mode 4—Event Counter Timing

MODE 5—ONE-SHOT PULSE WIDTH GENERATION

CNTR is an output which can be pulsed low for a programmed time interval. When this mode is selected in the CMCR, the CNTR output goes high (if the UF bit is set) or goes low (if the UF bit is cleared). The CNTR line then goes low when data is written to the UL at register address 0, which also starts the counter. The counter decrements from the UL and LL value at the $\phi 2$ clock rate as scaled by the Prescaler. When the counter decrements below \$0000, the CNTR output goes high, the UF bit is set in the SR, the counter is reloaded with \$FFFF and the count-down continues. Figure 10 shows the timing relationship of Mode 5 operation.

Note that clearing the UF bit after it is set upon the first timeout causes CNTR to go low, in which case CNTR will again go high upon the next counter timeout.

Typical Application: Can be used to hold-off (delay) an external hardware event on an asynchronous basis such as disallowing a motor startup until certain parameters are met.

MODE 6—FREE-RUN PULSE GENERATION

CNTR is an output and the Counter/Timer can be programmed to generate a symmetrical waveform, an asymmetrical waveform, or a string of varying width pulses on CNTR. The CNTR line is forced low (if high upon mode selection) or remains low

(if low upon mode selection) when data is written to the UL at register address 0 which also starts the counter. The counter decrements at the $\phi 2$ clock rate as scaled by the Prescaler. When the counter decrements below \$0000, CNTR toggles from low to high (or high to low depending upon its initial state), the counter is reloaded with the UL and LL value and the counter continues down-counting. The UF bit in the SR is set the first time the counter decrements past \$0000 and is cleared only if a new write to UL at register address 0 occurs. Figure 11 shows the timing relationship of a Mode 6 operation.

This mode can be used to generate an asymmetrical waveform by toggling the UL and LL with the CNTR high and low times. Immediately after starting the counter with the first CNTR low time, load the LL and UL (by writing to register address 1, which does not restart the counter) with the CNTR high time. When the first counter underflow occurs, the counter loads the new latch value (i.e., the CNTR high time) into the counter and continues counting. During the \overline{IRQ} interrupt processing resulting from the first counter time-out, load the LL and UL (at register address 1) with the original CNTR low time. Continue to alternate loading of the high and low time latch values during the interrupt processing for the duration of the mode.

Typical Application: Can be used to supply external circuitry with a software variable clock based upon the system $\phi 2$ clock (e.g., a tone generator for audio feedback).

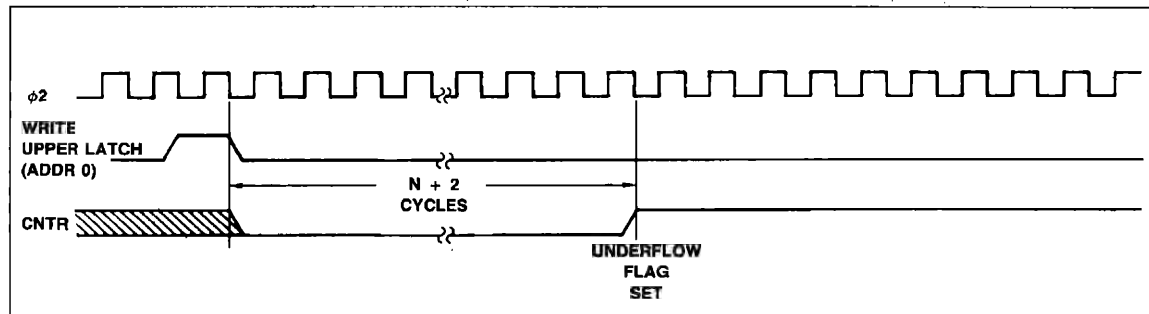


Figure 10. Mode 5—One-Shot Pulse Width Generation Timing

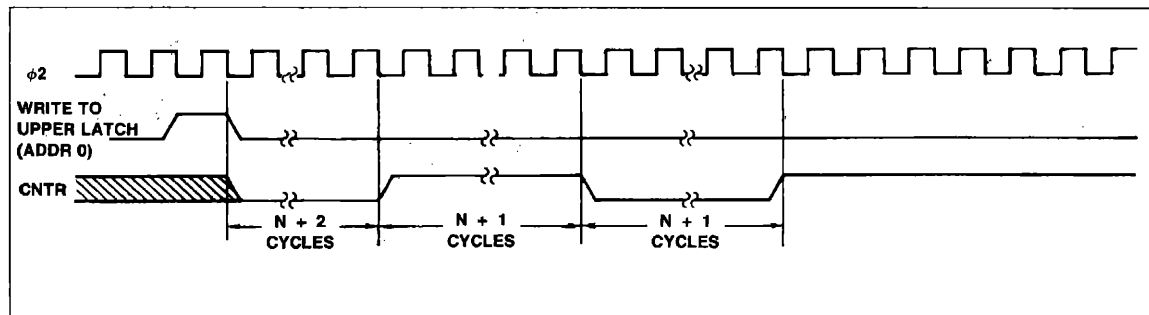


Figure 11. Mode 6—Free-Run Pulse Generation Timing

MODE 7—RETRIGGERABLE INTERVAL TIMER

The Counter/Timer operates as a timer which is retriggered, i.e., reinitialized to its starting value, upon detection of a negative transition on the CNTR input. The counter is initially loaded with the UL and LL value when the UL is written to register address 0. The counter starts decrementing at the $\phi 2$ clock rate (as scaled by the Prescaler) when a falling edge (high to low transition) is detected on CNTR. The counter is reinitialized to the UL and LL value whenever a falling edge is subsequently detected on CNTR. If the counter decrements past \$0000 before the falling edge is detected, the UF bit is set in the SR, the counter is initialized to the UL and LL value and the count-down continues.

Typical Application: Can be used to monitor signals that should be periodic and can interrupt the processor if the signal being monitored does not occur within a specified time frame; such as a synchronous motor that has fallen out of synchronization.

PRESCALER

The Counter/Timer operates in either the divide by one or divide by sixteen mode. In the divide by one mode, the counter holds from 1 to 65,535 counts. The counter capacity is therefore 1 μ s to 65,535 μ s at 1 MHz $\phi 2$ clock rate or 0.25 μ s to 16,383 μ s at a 4 MHz $\phi 2$ clock rate. Timer intervals greater than the maximum counter value can be easily measured by counting underflow flags or IRQ interrupt requests.

The divide by sixteen prescaler can be enabled to extend the timing interval by 16. This provides timing from 1048.56 ms (1 MHz) to 260.21 ms (4 MHz). The prescaler clocks the Counter/Timer at the $\phi 2$ clock rate divided by sixteen, except for Mode 4. In Mode 4, sixteen positive CNTR edges must occur to decrement the Counter/Timer by one count.

INITIALIZING THE COUNTER/TIMER

The following program segment is one suggested technique for initializing the Counter/Timer:

;Data Definition

```
SL      = $XXX0    ;Snapshot Latch
UC      = $XXX1    ;Upper Counter
LC      = $XXX2    ;Lower Counter
SR      = $XXX3    ;Status Register
ULEC    = $XXX0    ;Upper Latch and Enable Counter
UL      = $XXX1    ;Upper Latch
LL      = $XXX2    ;Lower Latch
CMCR    = $XXX3    ;Counter Mode Control Register
```

;Program

```
LDA     #$mode0    ;disable Counter/Timer
STA     CMCR       ;write to mode register
LDA     #$mode     ;select mode and Prescaler and
                    ;IRQT enable/disable
STA     CMCR       ;write to mode register
```

```
LDA     #$lovalue   ;lower latch value
STA     LL          ;write to lower latch
LDA     #$hivalue   ;upper latch value
STA     ULEC        ;write to upper latch
                    ;clear underflow flag, and enable
                    ;counter
```

The following instructions is a way to change modes while the Counter/Timer is in operation:

```
LDA     #$mode      ;select desired mode, except
                    ;mode 0
STA     CMCR        ;write to mode register
```

The change of mode operation will take effect immediately. Thus, the Free-Run Internal Timer mode (Mode 2) could be systematically stopped by changing to the One-Shot Interval Timer mode (Mode 1). The Counter/Timer will then halt operation when the underflow condition occurs. This technique can also be used to enable or disable IRQ during program execution.

READING THE COUNTER/TIMER

To service an interrupt request, the following sequence can be used:

```
BIT     $status     ;get underflow flag
BNE     error       ;check if flag is set
LDA     $LC         ;get low counter value for overflow
LDX     $SL         ;get high counter value for overflow
                    ;underflow flag is cleared
```

By reading the LC and SL, it is possible to determine the amount of time between the interrupt request and servicing the interrupt.

To read a timer value at any time, the suggested technique is as follows:

```
LDA     $LC         ;get low counter value
                    ;upper counter transferred to
                    ;snapshot
                    ;any miscellaneous code to store
                    ;value if desired
LDA     $SL         ;get high counter value
```

READ/WRITE TIMING CHARACTERISTICS OF PIAT

Figure 12 is a timing diagram for the R65C24 PIAT during a Read operation (input mode). Figure 13 is a timing diagram for the PIAT during a Write operation (output mode). Table 5 shows the characteristics of the times shown in Figures 12 and 13.

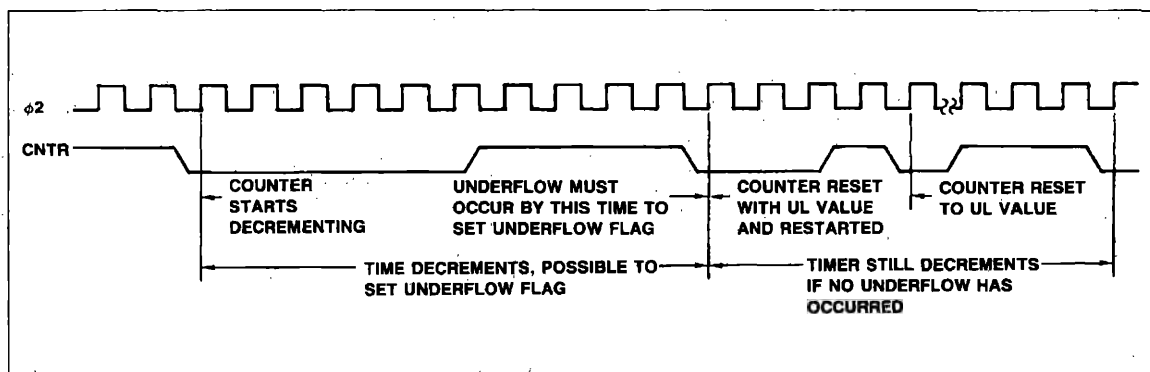


Figure 12. Mode 7—Retriggerable Interval Timer Timing

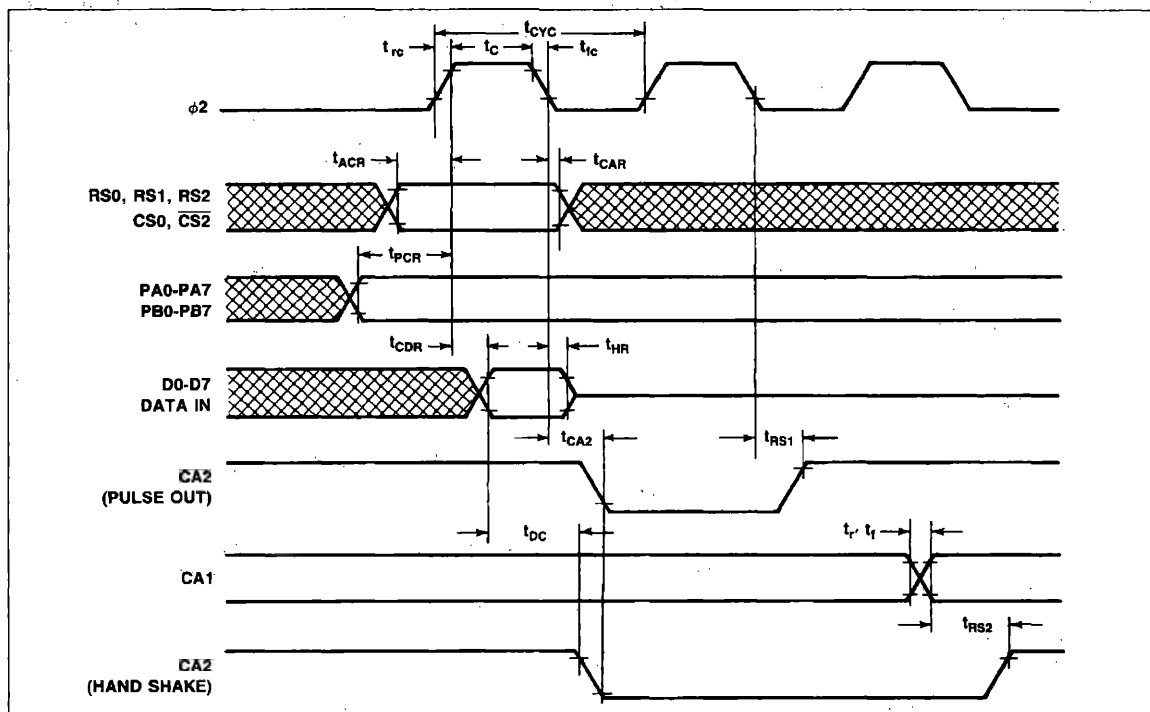


Figure 13. Read Timing Diagram

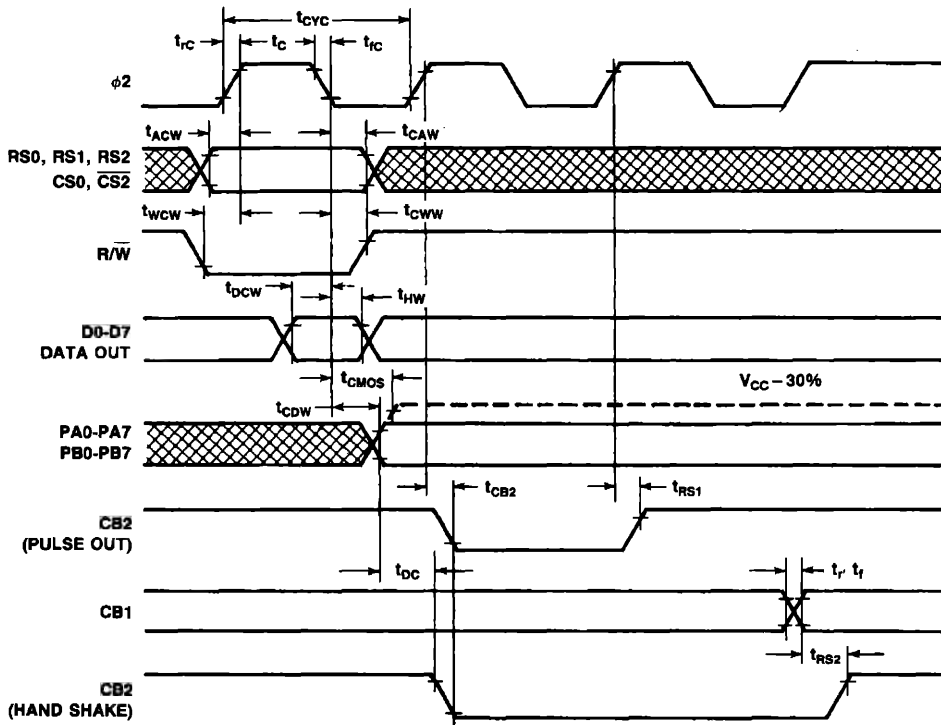


Figure 14. Write Timing Diagram

READING THE PERIPHERAL A I/O PORT

Performing a Read operation with $RS1 = 0$, $RS0 = 0$ and the Data Direction Register Access Control bit ($CRA-2$) = 1, directly transfers the data on the Peripheral A I/O lines to the data bus. In this situation, the data bus will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read by the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC

when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

READING THE PERIPHERAL B I/O PORT

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back to the processor on a Read operation.

BUS TIMING CHARACTERISTICS

Parameter	Symbol	1MHz		2MHz		3MHz		4MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$\phi 2$ Cycle	T_{CVC}	1.0	—	0.5	—	0.33	—	0.25	—	μs
$\phi 2$ Pulse Width	t_C	480	—	240	—	180	—	120	—	ns
$\phi 2$ Rise and Fall Time	t_{rC}, t_{fC}	—	25	—	15	—	12	—	10	ns

READ TIMING

Address Set-Up Time	t_{ACR}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	0	—	0	—	ns
Peripheral Data Set-Up Time	t_{PCR}	300	—	150	—	110	—	75	—	ns
Data Bus Delay Time	t_{CDR}	—	395	—	190	—	100	—	75	ns
Data Bus Hold Time	t_{HR}	20	—	20	—	20	—	20	—	ns

WRITE TIMING

Address Set-Up Time	t_{ACW}	140	—	70	—	53	—	53	—	ns
Address Hold Time	t_{CAW}	0	—	0	—	0	—	0	—	ns
R/W Set-Up Time	t_{WCW}	180	—	90	—	67	—	45	—	ns
R/W Hold Time	t_{CWW}	0	—	0	—	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	180	—	90	—	67	—	45	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	10	—	10	—	ns
Peripheral Data Delay Time	t_{CPW}	—	1.0	—	0.5	—	0.33	—	0.25	μs
Peripheral Data Delay Time to CMOS Level	t_{CMOS}	—	2.0	—	1.0	—	0.7	—	0.5	μs

PERIPHERAL INTERFACE TIMING

Parameter	Symbol	1MHz		2MHz		3MHz		4MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	ns
$\phi 2$ Low to CA2 Low Delay	t_{CA2}	—	1.0	—	0.5	—	0.33	—	0.25	μs
$\phi 2$ Low to CA2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	μs
CA1 Active to CA2 High Delay	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.5	μs
$\phi 2$ High to CB2 Low Delay	t_{CB2}	—	1.0	—	0.5	—	0.33	—	0.25	μs
Peripheral Data Valid to CB2 Low Delay	t_{DC}	0	1.5	0	0.75	0	0.5	0	0.37	μs
$\phi 2$ High to CB2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	μs
CB1 Active to CB2 High Delay	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.5	μs
CA1, CA2, CB1 and CB2 Input Rise and Fall Time	t_r, t_f	—	1.0	—	1.0	—	1.0	—	1.0	μs

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0	Vdc
Input Voltage	V _{IN}	-0.3 to V _{CC} +0.3	Vdc
Output Voltage	V _{OUT}	-0.3 to V _{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T _A	0 to +70 -40 to +85	°C
Storage Temperature	T _{STG}	-55 to +150	°C

*Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V _{CC}	5V ± 5%
Temperature Range Commercial Industrial	T _A	0° to 70°C -40° to +85°C

DC CHARACTERISTICS

V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = T_L to T_H, (unless otherwise noted)

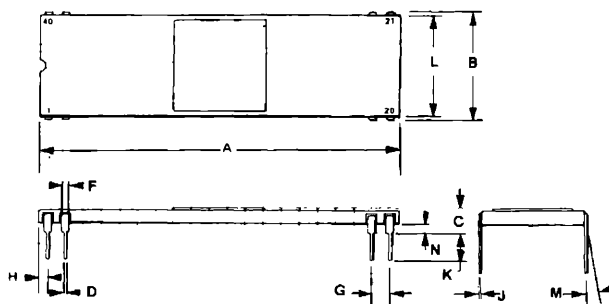
Parameter	Symbol	Min	Typ ³	Max	Unit ¹	Test Conditions
Input High Voltage	V _{IH}	+2.0	—	V _{CC}	V	
Input Low Voltage	V _{IL}	-0.3	—	+0.8	V	
Input Leakage Current: R/W, RES, RS0, RS1, RS2, CS0, CS2, CA1, CB1, φ2	I _{IN}	—	±1	±2.5	μA	V _{IN} = 0V to V _{CC} V _{CC} = 5.25V
Input Leakage Current for Three-State Off D0-D7, PB0-PB7, CB2	I _{TSI}	—	±2	±10	μA	V _{IN} = 0.4V to 2.4V V _{CC} = 5.25V
Input High Current PA0-PA7, CA2	I _{IH}	-200	-400	—	μA	V _{IH} = 2.4V
Input Low Current PA0-PA7, CA2	I _{IL}	—	-2	-3.2	mA	V _{IL} = 0.4V
Output High Voltage Logic PB0-PB7, CB2 (Darlington Drive)	V _{OH}	2.4 1.5	— —	— —	V V	V _{CC} = 4.75V I _{LOAD} = 200μA I _{LOAD} ² = -3.2 mA
Output Low Voltage PA0-PA7, CA2, PB0-PB7, CB2 D0-D7, IRQ, CNTR	V _{OL}	—	—	+0.4	V	V _{CC} = 4.75V I _{LOAD} = 3.2 mA I _{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0-PB7, CB2 (Darlington Drive)	I _{OH}	-200 -3.2	-1500 -6	— —	μA mA	V _{OH} = 2.4V V _{OH} = 1.5V
Output Low Current (Sinking) PA0-PA7, PB0-PB7, CB2, CA2 D0-D7, IRQ, CNTR	I _{OL}	3.2 1.6	— —	— —	mA mA	V _{OL} = 0.4V
Output Leakage Current (Off State): IRQ	I _{OFF}	—	1	±10	μA	V _{OH} = 2.4V V _{CC} = 5.25V
Power Dissipation	P _D	—	7	10	mW/MHz	
Input Capacitance D0-D7, PA0-PA7, PB0-PB7, CA2, CB2, CNTR R/W, RES, RS0, RS1, RS2, CS0, CS2 CA1, CB1, φ2	C _{IN}	— — —	— — —	10 7 20	pF pF pF	V _{CC} = 5.0V V _{IN} = 0V f = 2 MHz T _A = 25°C
Output Capacitance	C _{OUT}	—	—	10	pF	

Notes:

1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

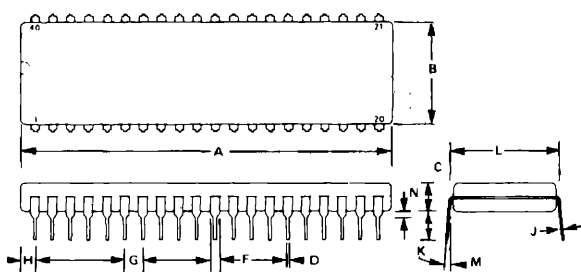
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040



R65C51 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

PRELIMINARY

DESCRIPTION

The Rockwell CMOS R65C51 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The ACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or at $1/16$ times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at $1/16$ times the external clock rate. The ACIA has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, $1\frac{1}{2}$, or 2 stop bits.

The ACIA is designed for maximum programmed control from the microprocessor (MPU), to simplify hardware implementation. Three separate registers permit the MPU to easily select the R65C51's operating modes and data checking parameters and determine operational status.

The Command Register controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{\text{RTS}}$ line, receiver interrupt control, and the state of the $\overline{\text{DTR}}$ line.

The Control Register controls the number of stop bits, word length, receiver clock source, and baud rate.

The Status Register indicates the states of the $\overline{\text{IRQ}}$, $\overline{\text{DSR}}$, and $\overline{\text{DCD}}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing, and Parity Error conditions.

The Transmitter and Receiver Data Registers are used for temporary data storage by the ACIA Transmit and Receiver circuits.

ORDERING INFORMATION

Part No.: R65C51

Temperature Range (T_L to T_H):
Blank = 0°C to $+70^\circ\text{C}$
E = -40°C to $+85^\circ\text{C}$

Frequency Range:
1 = 1 MHz
2 = 2 MHz
3 = 3 MHz
4 = 4 MHz

Package:
C = Ceramic
P = Plastic

FEATURES

- Low power CMOS N-well silicon gate technology
- Direct replacement for NMOS R6551 ACIA
- Full duplex operation with buffered receiver and transmitter
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 19,200)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Program reset
- Program-selectable serial echo mode
- Two chip selects
- 2 or 4 MHz operation
- $5.0\text{ Vdc} \pm 5\%$ supply requirements
- 28-pin plastic or ceramic DIP
- Full TTL compatibility
- Compatible with R6500, R6500/* and R65C00 micro-processors

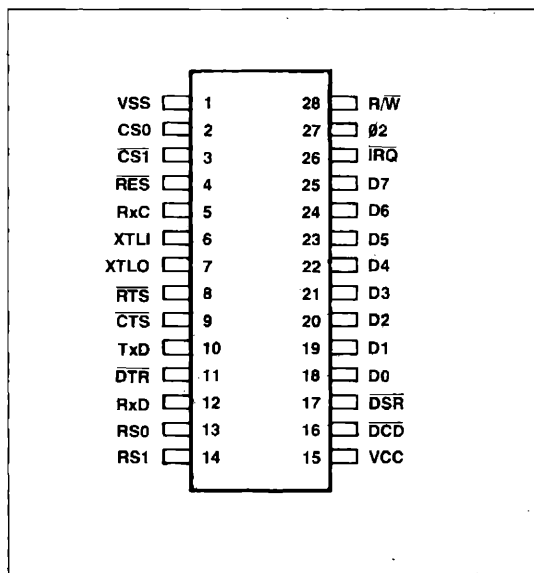


Figure 1. R65C51 ACIA Pin Configuration

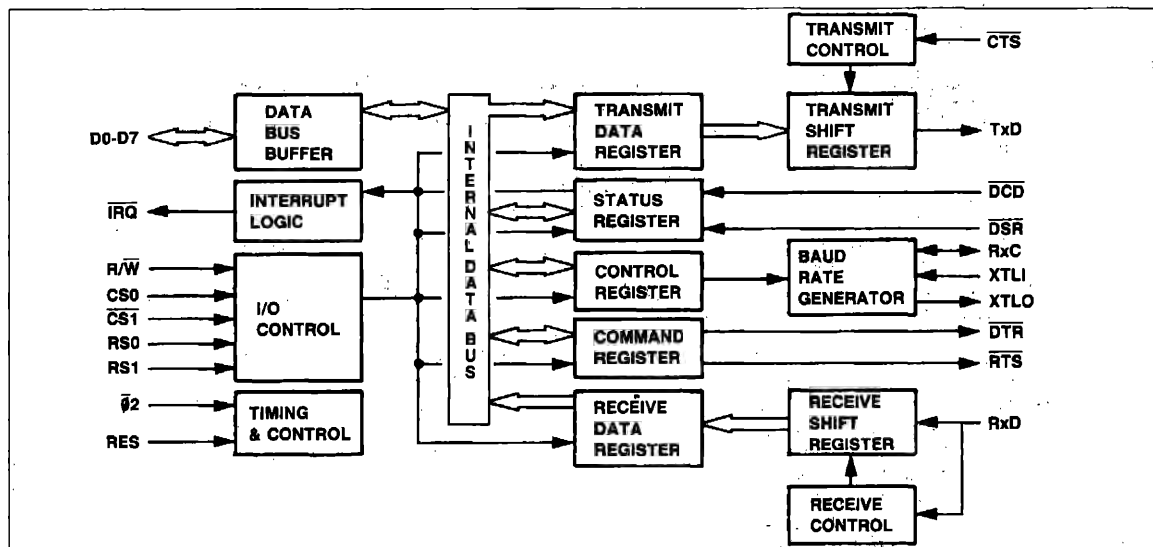


Figure 2. ACIA Internal Organization

FUNCTIONAL DESCRIPTION

A block diagram of the ACIA is presented in Figure 2 followed by a description of each functional element of the device.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the R/W line is high and the chip is selected, the Data Bus Buffer passes the data from the system data lines to the ACIA internal data bus. When the R/W line is low and the chip is selected, the Data Bus Buffer writes the data from the internal data bus to the system data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{\text{IRQ}}$ line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register, if enabled. Bits 5 and 6 correspond to the Data Carrier Detect (DCD) logic and the Data Set Ready (DSR) logic. Bits 3 and 4 correspond to the Receiver Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers in preparation for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Receiver Select (RS1, RS0) and Read/Write (R/W) lines as described later in Table 1.

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus and the registers, the Data Bus Buffer, and the microprocessor data bus, and the hardware reset features.

Timing is controlled by the system $\phi 2$ clock input. The chip will perform data transfers to or from the microcomputer data bus during the $\phi 2$ high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset ($\overline{\text{RES}}$) line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the ACIA Transmitter and Receive Circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write (R/W) line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care".

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

STATUS REGISTER

The Status Register indicates the state of interrupt conditions and other non-interrupt status lines. The interrupt conditions are the Data Set Ready, Data Carrier Detect, Transmitter Data Register Empty and Receiver Data Register Full as reported in bits 6 through 3, respectively. If any of these bits are set, the Interrupt (IRQ) indicator (bit 7) is also set. Overrun, Framing Error, and Parity Error are also reported (bits 2 through 0 respectively).

7	6	5	4	3	2	1	0
IRQ	DSR	DCD	TDRE	RDRE	OVN	FE	PE

Bit 7 Interrupt (IRQ)

- 0 No interrupt
- 1 Interrupt has occurred

Bit 6 Data Set Ready (DSR)

- 0 DSR low (ready)
- 1 DSR high (not ready)

Bit 5 Data Carrier Detect (DCD)

- 0 DCD low (detected)
- 1 DCD high (not detected)

Bit 4 Transmitter Data Register Empty

- 0 Not empty
- 1 Empty

Bit 3 Receiver Data Register Full

- 0 Not full
- 1 Full

Bit 2 Overrun*

- 0 No overrun
- 1 Overrun has occurred

Bit 1 Framing Error*

- 0 No framing error
- 1 Framing error detected

Bit 0 Parity Error*

- 0 No parity error
- 1 Parity error detected

*No interrupt occurs for these conditions

Reset Initialization

7	6	5	4	3	2	1	0	
0	—	—	1	0	0	0	0	Hardware reset
—	—	—	—	0	—	—	—	Program reset

Parity Error (Bit 0), Framing Error (Bit 1), and Overrun (2)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified. These bits are self clearing (i.e., they are automatically cleared after a read of the Receiver Data Register).

Receiver Data Register Full (Bit 3)

This bit goes to a 1 when the ACIA transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a 0 (is cleared) when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a 1 when the ACIA transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a 0 (is cleared) when the processor writes new data onto the Transmitter Data Register.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs to the ACIA. A 0 indicates a low level (true condition) and a 1 indicates a high level (false). Whenever either of these inputs change state, an immediate processor interrupt (IRQ) occurs, unless bit 1 of the Command Register (IRD) is set to a 1 to disable IRQ. When the interrupt occurs, the status bits indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until the Status Register is interrogated by the processor. At that time, another interrupt will immediately occur and the status bits reflect the new input levels. These bits are not automatically cleared (or reset) by an internal operation.

Interrupt (Bit 7)

This bit goes to a 1 whenever an interrupt condition occurs and goes to a 0 (is cleared) when the Status Register is read.

CONTROL REGISTER

The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.

7	6	5	4	3	2	1	0
SBN	WL		RCS	SBR			
	WL1	WL0		SBR3	SBR2	SBR1	SBR0

Bit 7 Stop Bit Number (SBN)

0	1 Stop bit
1	2 Stop bits
1	1½ Stop bits
	For WL = 5 and no parity
1	1 Stop bit
	For WL = 8 and parity

Bits 6-5 Word Length (WL)

6	5	No. Bits
0	0	8
0	1	7
1	0	6
1	1	5

Bit 4 Receiver Clock Source (RCS)

0	External receiver clock
1	Baud rate

Bits 3-0 Selected Baud Rate (SBR)

3	2	1	0	Baud
0	0	0	0	16x
0	0	0	1	50
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset (RES)
-	-	-	-	-	-	-	-	Program reset

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits select the Transmitter baud rate, which can be at $1/16$ an external clock rate or one of 15 other rates controlled by the internal baud rate generator.

If the Receiver clock uses the same baud rate as the transmitter, then RxC becomes an output and can be used to slave other circuits to the ACIA. Figure 3 shows the Transmitter and Receiver layout.

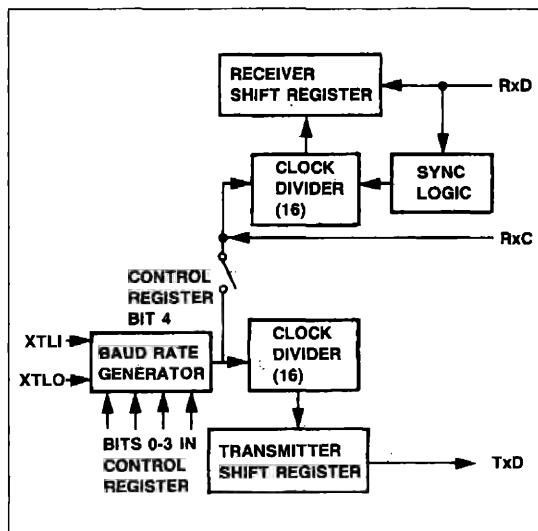


Figure 3. Transmitter/Receiver Clock Circuits

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A 0 causes the Receiver to operate at a baud rate of $1/16$ an external clock. A 1 causes the Receiver to operate at the same baud rate as is selected for the transmitter.

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits).

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A 0 always indicates one stop bit. A 1 indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, and 2 stop bits in all other configurations.

COMMAND REGISTER

The Command Register controls specific modes and functions.

7	6	5	4	3	2	1	0
PMC	PME	REM	TIC	IRD	DTR		
PNC1 PNC0			TIC1 TIC0				

Bits 7-6 Parity Mode Control (PMC)

7	6	
0	0	Odd parity transmitted/received
0	1	Even parity transmitted/received
1	0	Mark parity bit transmitted Parity check disabled
1	1	Space parity bit transmitted Parity check disabled

Bit 5 Parity Mode Enabled (PME)

0	Parity mode disabled No parity bit generated Parity check disabled
1	Parity mode enabled

Bit 4 Receiver Echo Mode (REM)

0	Receiver normal mode
1	Receiver echo mode bits 2 and 3 Must be zero for receiver echo mode, RTS will be low.

Bits 3-2 Transmitter Interrupt Control (TIC)

3	2	
0	0	\overline{RTS} = High, transmit interrupt disabled
0	1	\overline{RTS} = Low, transmit interrupt enabled
1	0	\overline{RTS} = Low, transmit interrupt disabled
1	1	\overline{RTS} = Low, transmit interrupt disabled transmit break on TxD

Bit 1 Interrupt Request Disabled (IRD)

0	\overline{IRQ} enabled
1	\overline{IRQ} disabled

Bit 0 Data Terminal Ready (DTR)

0	Data terminal not ready (DTR high)
1	Data terminal ready (DTR low)

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready (DTR) line. A 0 indicates the microcomputer system is not ready by setting the DTR line high. A 1 indicates the microcomputer system is ready by setting the DTR line low.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a 1. The Receiver interrupt is enabled when this bit is set to a 0 and Bit 0 is set to a 1.

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send (\overline{RTS}) line and the Transmitter interrupt.

Receiver Echo Mode (Bit 4)

A 1 enables the Receiver Echo Mode and a 0 enables the Receiver Echo Mode. When bit 4 is a 1 bits 2 and 3 must be 0. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by one-half bit time.

Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A 0 disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A 1 bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check).

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset (\overline{RES})
—	—	—	0	0	0	0	0	Program reset

INTERFACE SIGNALS

Figure 4 shows the ACIA interface signals associated with the microprocessor and the modem.

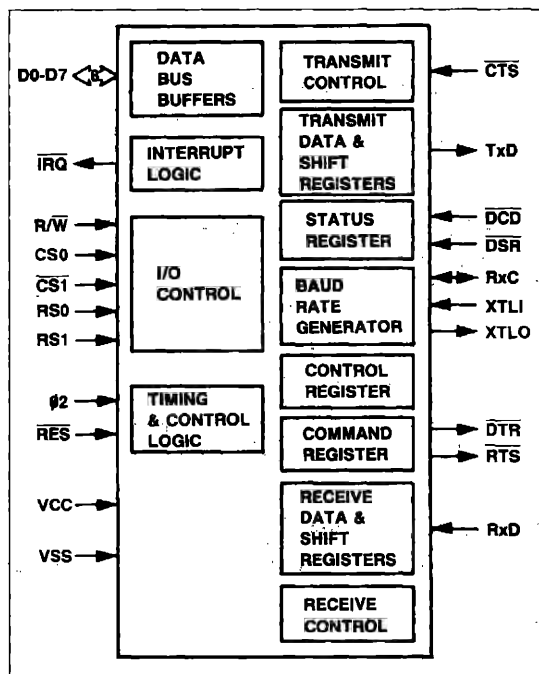


Figure 4. ACIA Interface Diagram

MICROPROCESSOR INTERFACE

Reset (\overline{RES})

During system initialization a low on the \overline{RES} input causes a hardware reset to occur. Upon reset, the Command Register and the Control Register are cleared (all bits set to 0). The Status Register is cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the \overline{DSR} and \overline{DCD} lines, and the transmitter Empty bit, which is set. \overline{RES} must be held low for one $\phi 2$ clock cycle for a reset to occur.

Input Clock ($\phi 2$)

The input clock is the system $\phi 2$ clock and clocks all data transfers between the system microprocessor and the ACIA.

Read/Write (R/\overline{W})

The R/\overline{W} input, generated by the microprocessor controls the direction of data transfers. A high on the R/\overline{W} pin allows the processor to read the data supplied by the ACIA, a low allows a write to the ACIA.

Interrupt Request (\overline{IRQ})

The \overline{IRQ} pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common \overline{IRQ} microprocessor input. Normally a high level, \overline{IRQ} goes low when an interrupt occurs.

Data Bus (D0-D7)

The eight data line (D0-D7) pins transfer data between the processor and the ACIA. These lines are bi-directional and are normally high-impedance except during Read cycles when the ACIA is selected.

Chip Selects ($CS0, \overline{CS1}$)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The ACIA is selected when $CS0$ is high and $\overline{CS1}$ is low. When the ACIA is selected, the internal registers are addressed in accordance with the register select lines ($RS0, RS1$).

Register Selects ($RS0, RS1$)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various ACIA internal registers. Table 1 shows the internal register select coding.

Table 1. ACIA Register Selection

RS1	RS0	Register Operation	
		R/W = Low	R/W = High
L	L	Write, Transmit Data Register	Read Receiver Data Register
L	H	Programmed Reset (Data is "Don't Care")	Read Status Register
H	L	Write Command Register	Read Command Register
H	H	Write Control Register	Read Control Register

Only the Command and Control registers can both be read and written. The programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command register and bit 2 in the Status Register. The Control Register is unchanged by a programmed Reset. It should be noted that the programmed Reset is slightly different from the hardware Reset (\overline{RES}); refer to the register description.

ACIA/MODEM INTERFACE

Crystal Pins (XTLI, XTLO)

These pins are normally directly connected to the external crystal (1.8432 MHz) to derive the various baud rates. Alternatively, an externally generated clock can drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

Transmit Data (TxD)

The TxD output line transfers serial nonreturn-to-zero (NRZ) data to the modem. The least significant bit (LSB) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or under control of an external clock. This selection is made by programming the Control Register.

Receive Data (Rx D)

The Rx D input line transfers serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or under the control of an externally generated receiver clock. The selection is made by programming the Control Register.

Receive Clock (Rx C)

The Rx C is a bi-directional pin which is either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

Request to Send (RTS)

The RTS output pin controls the modem from the processor. The state of the RTS pin is determined by the contents of the Command Register.

Clear to Send (CTS)

The CTS input pin controls the transmitter operation. The enable state is with CTS low. The transmitter is automatically disabled if CTS is high.

Data Terminal Ready (DTR)

This output pin indicates the status of the ACIA to the modem. A low on DTR indicates the ACIA is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

Data Set Ready (DSR)

The DSR input pin indicates to the ACIA the status of the modem. A low indicates the "ready" state and a high, "not-ready."

Data Carrier Detect (DCD)

The DCD input pin indicates to the ACIA the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

TRANSMITTER AND RECEIVER OPERATION

Continuous Data Transmit

In the normal operating mode, the interrupt request output (IRQ) signals when the ACIA is ready to accept the next data word to be transmitted. This interrupt occurs at the beginning of the Start Bit. When the processor reads the Status Register of the ACIA, the interrupt is cleared.

The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted. Figure 5 shows the continuous Data Transmit timing relationship.

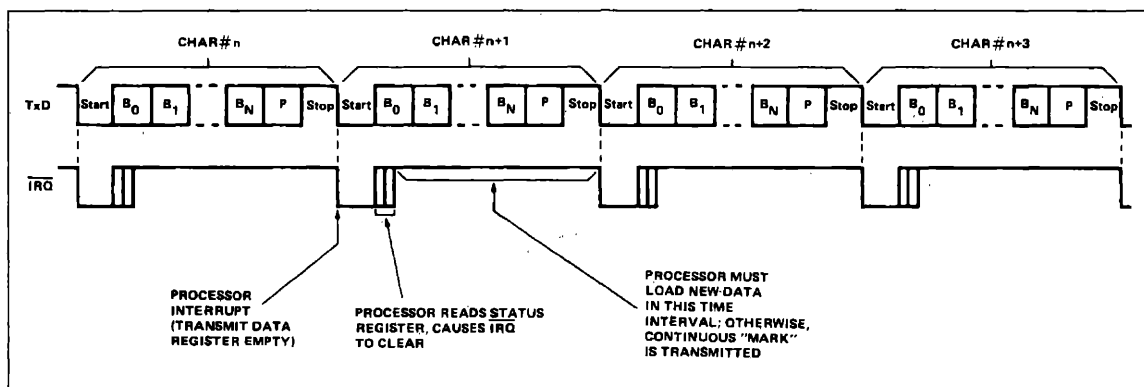


Figure 5. Continuous Data Transmit

Continuous Data Receive

Similar to the Continuous Data Transmit case, the normal operation of this mode is to assert $\overline{\text{IRQ}}$ when the ACIA has received a full data word. This occurs at about $9/16$ point through the Stop Bit. The processor must read the Status Register and

read the data word before the next interrupt, otherwise the Overrun condition occurs. Figure 6 shows the continuous Data Receive Timing Relationship.

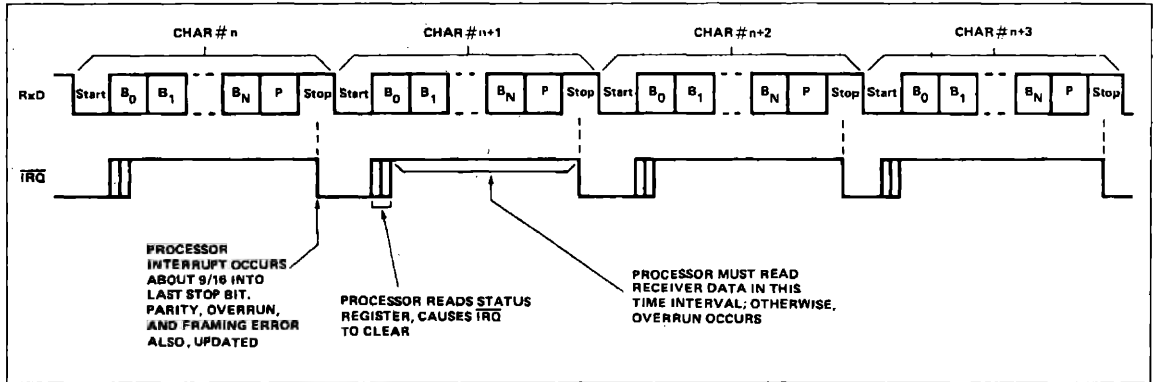


Figure 6. Continuous Data Receive

Transmit Data Register Not Loaded by Processor

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line goes to the "MARK" condition until the data is loaded. $\overline{\text{IRQ}}$ interrupts continue to occur at the same rate as previously, except no data is transmitted.

When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word. Figure 7 shows the timing relationship for this mode of operation.

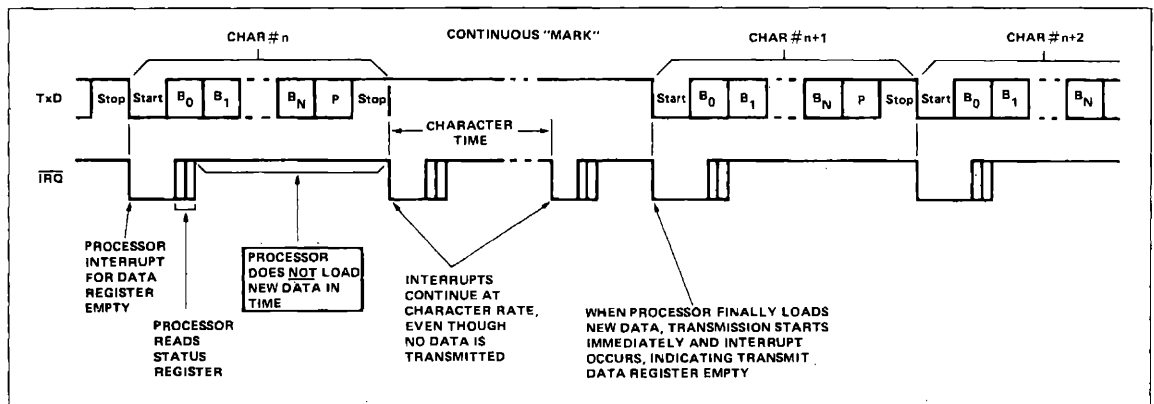


Figure 7. Transmit Data Register Not Loaded by Processor

Effect of $\overline{\text{CTS}}$ on Transmitter

$\overline{\text{CTS}}$ is the Clear-to-Send signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the Tx $\overline{\text{D}}$ line goes to the "MARK" condition after the entire last character (including parity and stop bit) have been transmitted. Bit 4 in the Status Register

indicates that the Transmitter Data Register is not empty and $\overline{\text{IRQ}}$ is not asserted. $\overline{\text{CTS}}$ is a transmit control line only, and has no effect on the ACIA Receiver Operation. Figure 8 shows the timing relationship for this mode of operation.

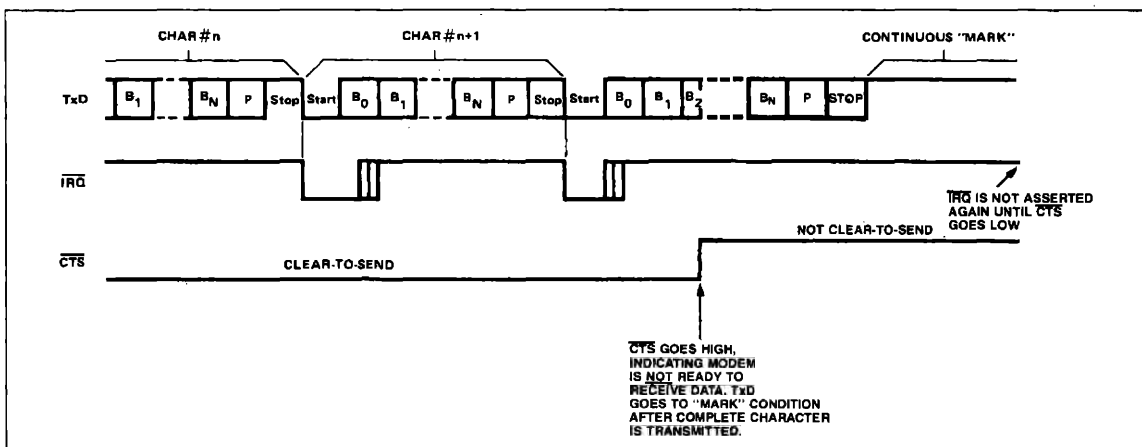


Figure 8. Effect of CTS on Transmitter

Effect of Overrun on Receiver

If the processor does not read the Receiver data Register in the allocated time, then, when the following interrupt occurs, the new data word is not transferred to the Receiver Data Register,

but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost. Figure 9 shows the timing relationship for this mode.

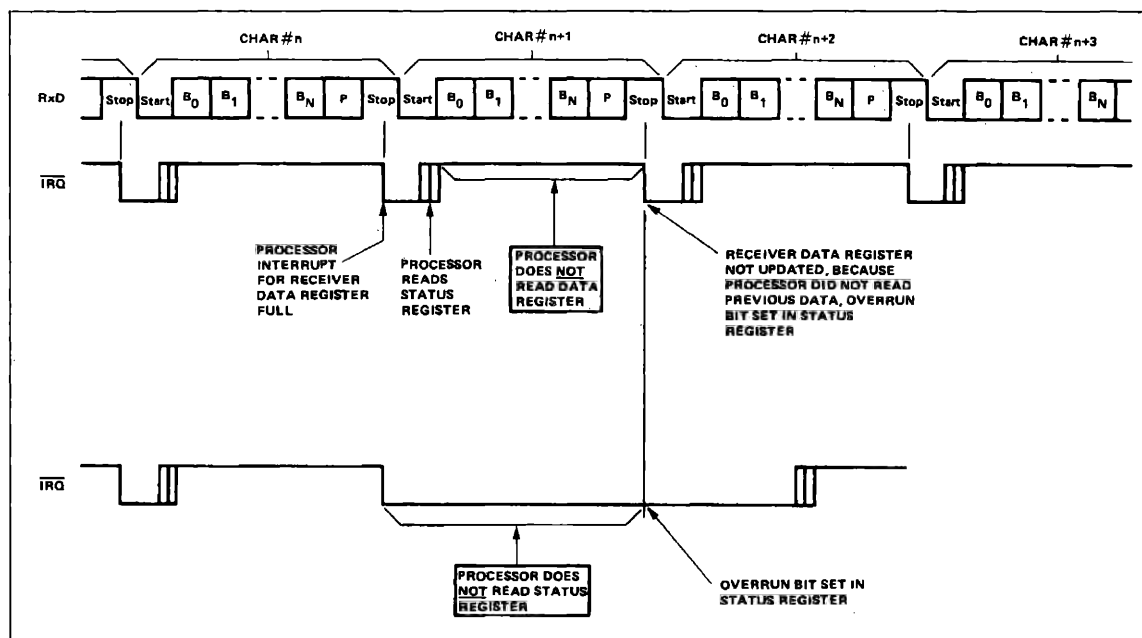


Figure 9. Effect of Overrun on Receiver

Echo Mode Timing

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by $\frac{1}{2}$ of the bit time, as shown in Figure 10.

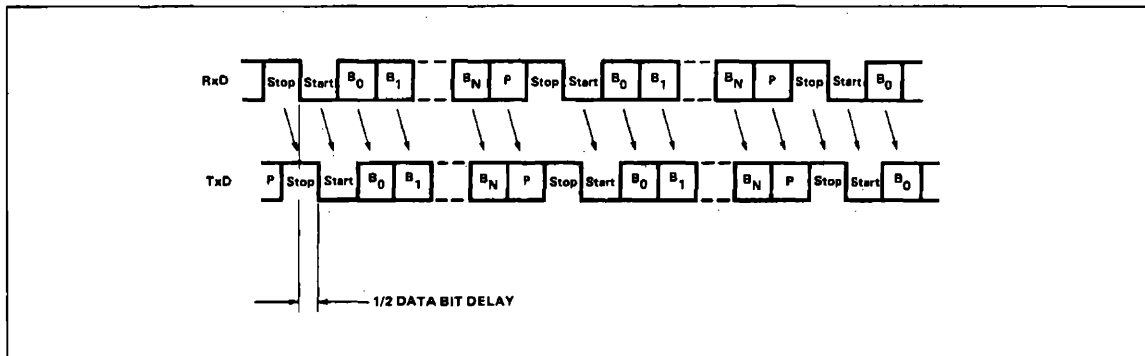


Figure 10. Echo Mode Timing

Effect of $\overline{\text{CTS}}$ on Echo Mode Operation

In Echo Mode, the Receiver operation is unaffected by $\overline{\text{CTS}}$, however, the Transmitter is affected when $\overline{\text{CTS}}$ goes high, i.e., the TxD line immediately goes to a continuous "MARK" condition. In this case, however, the Status Request indicates that

the Receiver Data Register is full in response to an $\overline{\text{IRQ}}$, so the processor has no way of knowing that the Transmitter has ceased to echo. See Figure 11 for the timing relationship of this mode.

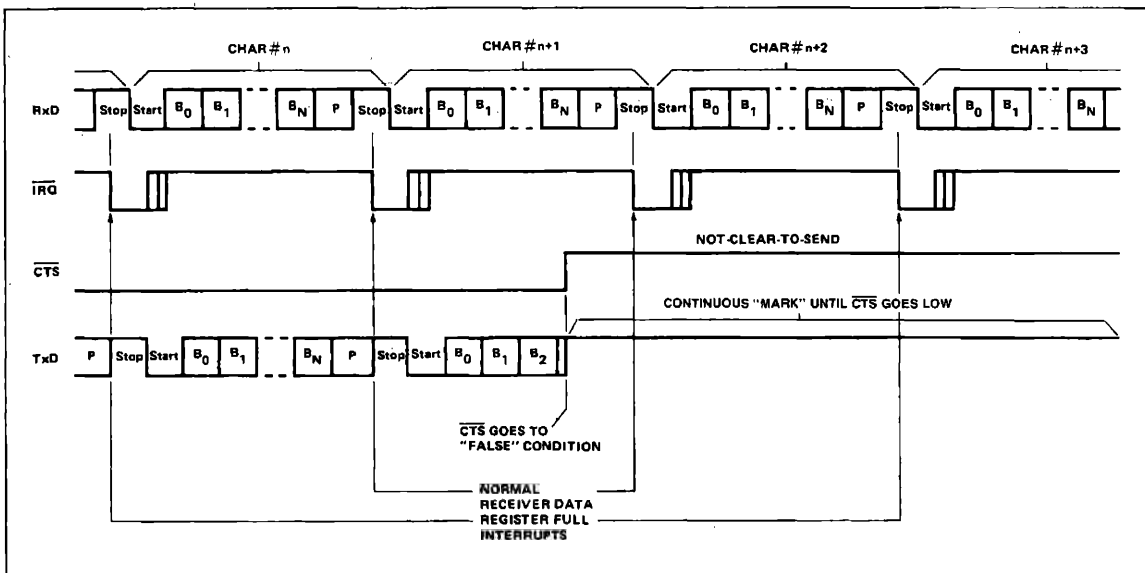


Figure 11. Effect of $\overline{\text{CTS}}$ on Echo Mode

Overrun In Echo Mode

If Overrun occurs in Echo Mode, the Receiver is affected the same way as a normal overrun in Receive Mode. For the re-transmitted data, when overrun occurs, the TxD line goes to the

"MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor. Figure 12 shows the timing relationship for this mode.

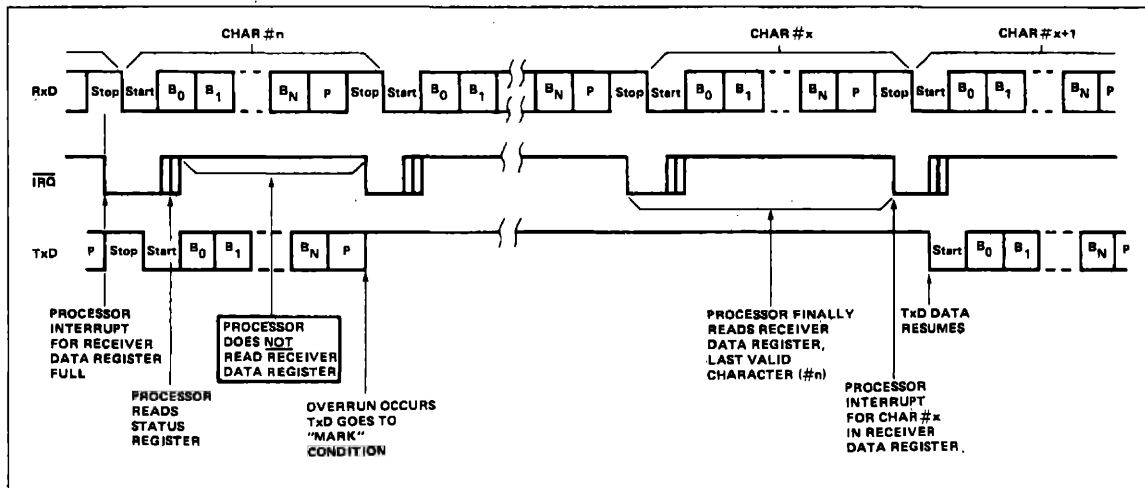


Figure 12. Overrun In Echo Mode

Framing Error

Framing Error is caused by the absence of Stop Bit(s) on received data. A Framing Error is indicated by the setting of bit 4 in the Status Register at the same time the Receiver Data Register Full bit is set, also in the Status Register. In response to IRQ, generated by RDRF, the Status Register can also be

checked for the Framing Error. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received. See Figure 13 for Framing Error timing relationship.

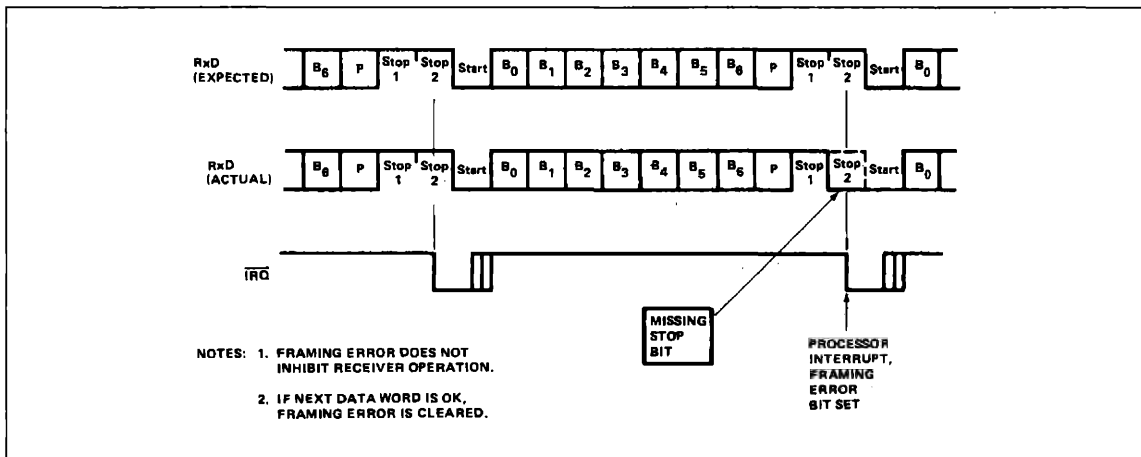


Figure 13. Framing Error

Effect of $\overline{\text{DCD}}$ on Receiver

$\overline{\text{DCD}}$ is a modem output indicating the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data some time later. The ACIA asserts $\overline{\text{IRQ}}$ whenever $\overline{\text{DCD}}$ changes state and indicates this condition via bit 5 in the Status Register.

Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register is read by the processor, the ACIA automatically checks the level of the $\overline{\text{DCD}}$ line, and if it has changed, another $\overline{\text{IRQ}}$ occurs (see Figure 14).

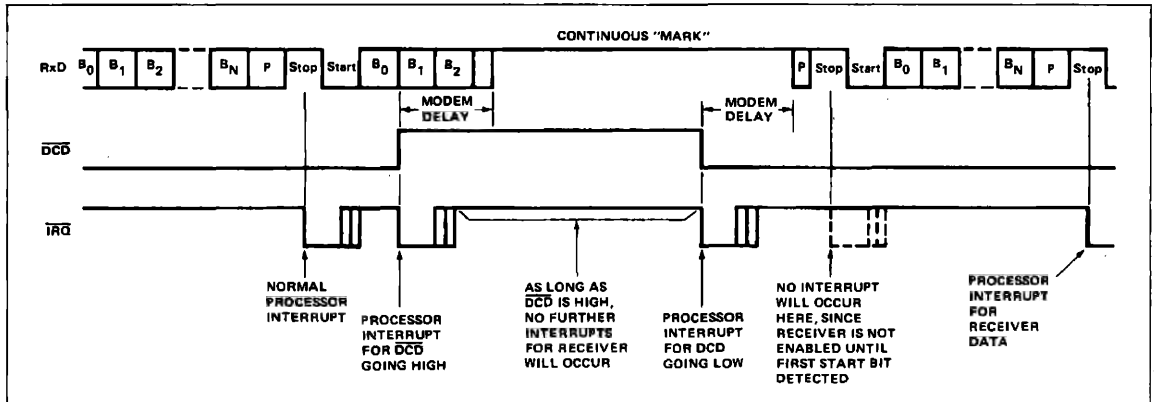


Figure 14. Effect of $\overline{\text{DCD}}$ on Receiver

Timing with 1½ Stop Bits

It is possible to select 1½ Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the $\overline{\text{IRQ}}$ asserted for Receiver Data Register Full occurs halfway through the

trailing half-Stop Bit. Figure 15 shows the timing relationship for this mode.

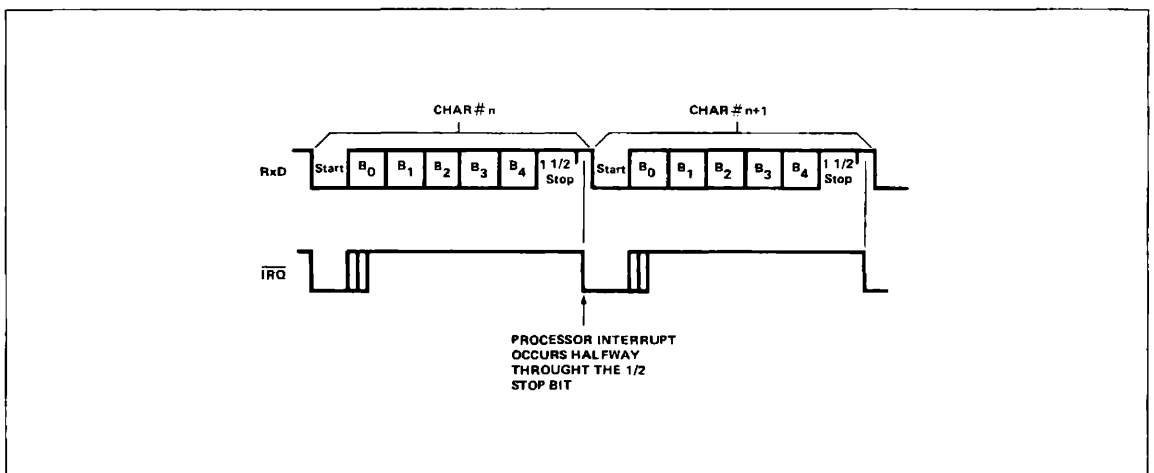


Figure 15. Timing with 1½ Stop Bits

Transmit Continuous "BREAK"

This mode is selected via the ACIA Command Register and causes the Transmitter to send continuous "BREAK" characters, beginning with the next character transmitted. At least one full "BREAK" character will be transmitted, even if the processor quickly re-programs the Command Register transmit mode. Later, when the Command Register is programmed back to normal transmit mode, an immediate Stop Bit will be generated and transmission will resume. Figure 16 shows the timing relationship for this mode.

Note

If, while operating in the Transmit Continuous "BREAK" mode, the \overline{CTS} should go to a high, the TxD will be overridden by the \overline{CTS} and will go to continuous "MARK" at the beginning of the next character transmitted after the \overline{CTS} goes high.

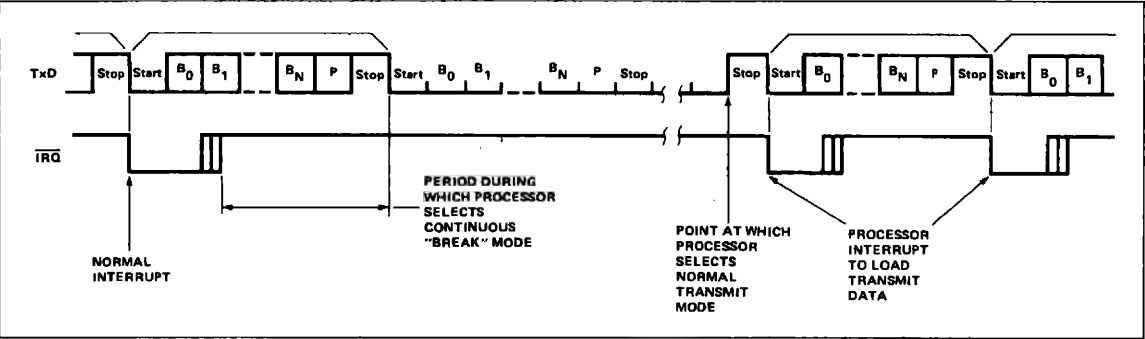


Figure 16. Transmit Continuous "BREAK"

Receive Continuous "BREAK"

In the event the modem transmits continuous "BREAK" characters, the ACIA will terminate receiving. Reception will resume only after a Stop Bit is encountered by the ACIA. Figure 17

shows the timing relationship for continuous "BREAK" characters.

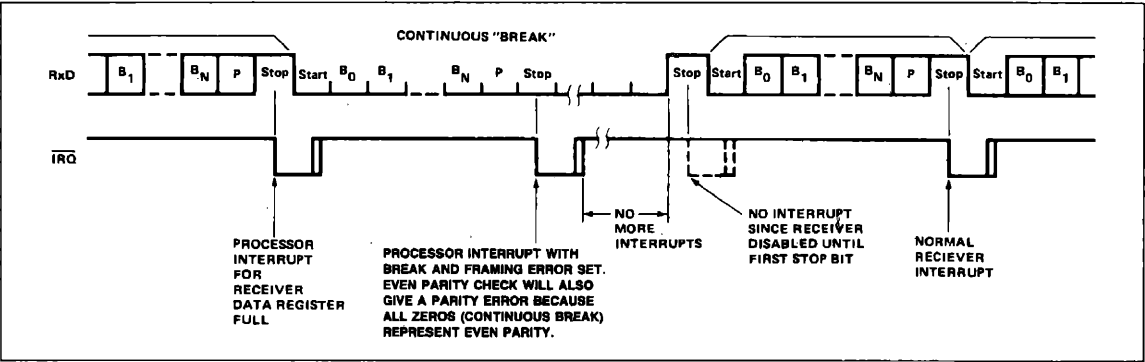


Figure 17. Receive Continuous "BREAK"

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the ACIA should be interrogated, as follows:

1. Read Status Register

This operation automatically clears Bit 7 (\overline{IRQ}). Subsequent transitions on \overline{DSR} and \overline{DCD} will cause another interrupt.

2. Check \overline{IRQ} (Bit 7) in the data read from the Status Register

If not set, the interrupt source is not the ACIA.

3. Check \overline{DCD} and \overline{DSR}

These must be compared to their previous levels, which must have been saved by the processor. If they are both 0 (modern "on-line") and they are unchanged then the remaining bits must be checked.

4. Check RDRF (Bit 3)

Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0-2) if the Receiver Data Register is full.

6. Check TDRE (Bit 4)

Check for Transmitter Data Register Empty.

7. If none of the above conditions exist, then \overline{CTS} must have gone to the false (high) state.

PROGRAM RESET OPERATION

A program reset occurs when the processor performs a write operation to the ACIA with RS0 low and RS1 high. The program reset operates somewhat different from the hardware reset (\overline{RES} pin) and is described as follows:

1. Internal registers are not completely cleared. Check register formats for the effect of a program reset on internal registers.

2. The \overline{DTR} line goes high immediately.

3. Receiver and transmitter interrupts are disabled immediately. If \overline{IRQ} is low when the reset occurs, it stays low until serviced, unless interrupt was caused by \overline{DCD} or \overline{DSR} transition.

4. \overline{DCD} and \overline{DSR} interrupts are disabled immediately. If \overline{IRQ} is low and was caused by \overline{DCD} or \overline{DSR} , then it goes high, also \overline{DCD} and \overline{DSR} status bits subsequently will follow the input lines, although no interrupt will occur.

5. Overrun cleared, if set.

MISCELLANEOUS

1. If Echo Mode is selected, \overline{RTS} goes low.

2. If Bit 0 of Command Register is 0 (disabled), then:

- a) All interrupts are disabled, including those caused by \overline{DCD} and \overline{DSR} transitions.
- b) Transmitter is disabled immediately.
- c) Receiver is disabled, but a character currently being received will be completed first.

3. Odd parity occurs when the sum of all the 1 bits in the data word (including the parity bit) is odd.

4. In the receive mode, the received parity bit does not go into the Receiver Data Register, but generates parity error or no parity error for the Status Register.

5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.

6. If the RxD line inadvertently goes low and then high right after a Stop Bit, the ACIA does not interpret this as a Start Bit, but samples the line again halfway into the bit to determine if it is a true Start Bit or a false one. For false Start Bit detection, the ACIA does not begin to receive data, instead, only a true Start Bit initiates receiver operation.

7. Precautions to consider with the crystal oscillator circuit:

- a) The external crystal should be a "series" mode crystal.
- b) The XTALI input may be used as an external clock input. The unused pin (EXTALO) must be floating and may not be used for any other function.

8. \overline{DCD} and \overline{DSR} transitions, although causing immediate processor interrupts, have no effect on transmitter operation. Data will continue to be sent, unless the processor forces transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be terminated either to GND or V_{CC} .

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the ACIA Control Register, as shown in Table 2.

Generating Other Baud Rates

By using a different crystal, other baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the ACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 6) must be the clock input and XTALO (pin 7) must be a no-connect.

Table 2. Divisor Selection

Control Register Bits	Divisor Selected For The Internal Counter	Baud Rate Generated With 1.8432 MHz Crstal	Baud Rate Generated With a Crystal of Frequency (F)
3 2 1 0			
0 0 0 0	No Divisor Selected	16 × External Clock at Pin RxC	16 × External Clock at Pin RxC
0 0 0 1	36,864	$\frac{1.8432 \times 10^6}{36,864} = 50$	$\frac{F}{36,864}$
0 0 1 0	24,576	$\frac{1.8432 \times 10^6}{24,576} = 75$	$\frac{F}{24,576}$
0 0 1 1	16,769	$\frac{1.8432 \times 10^6}{16,769} = 109.92$	$\frac{F}{16,769}$
0 1 0 0	13,704	$\frac{1.8432 \times 10^6}{13,704} = 134.51$	$\frac{F}{13,704}$
0 1 0 1	12,288	$\frac{1.8432 \times 10^6}{12,288} = 150$	$\frac{F}{12,288}$
0 1 1 0	6,144	$\frac{1.8432 \times 10^6}{6,144} = 300$	$\frac{F}{6,144}$
0 1 1 1	3,072	$\frac{1.8432 \times 10^6}{3,072} = 600$	$\frac{F}{3,072}$
1 0 0 0	1,536	$\frac{1.8432 \times 10^6}{1,536} = 1,200$	$\frac{F}{1,536}$
1 0 0 1	1,024	$\frac{1.8432 \times 10^6}{1,024} = 1,800$	$\frac{F}{1,024}$
1 0 1 0	768	$\frac{1.8432 \times 10^6}{768} = 2,400$	$\frac{F}{768}$
1 0 1 1	512	$\frac{1.8432 \times 10^6}{512} = 3,600$	$\frac{F}{512}$
1 1 0 0	384	$\frac{1.8432 \times 10^6}{384} = 4,800$	$\frac{F}{384}$
1 1 0 1	256	$\frac{1.8432 \times 10^6}{256} = 7,200$	$\frac{F}{256}$
1 1 1 0	192	$\frac{1.8432 \times 10^6}{192} = 9,600$	$\frac{F}{192}$
1 1 1 1	96	$\frac{1.8432 \times 10^6}{96} = 19,200$	$\frac{F}{96}$

DIAGNOSTIC LOOP-BACK OPERATING MODES

A simplified block diagram for a system incorporating an ACIA is shown in Figure 18.

It may be desirable to include in the system a facility for "loop-back" testing, of which there are two kinds:

1. Local Loop-Back

Loop-back from the point of view of the processor. In this case, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

2. Remote Loop-Back

Loop-back from the point of view of the Data Link and Modem. In this case, the processor, itself, is disconnected and all received data is immediately retransmitted, so the system on the other end of the Data Link may operate independent of the local system.

The ACIA does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry. Figure 19 indicates the necessary logic to be used with the ACIA. The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following:

1. Disables outputs TxD, $\overline{\text{DTR}}$, and $\overline{\text{RTS}}$ (to Modem).
2. Disables inputs RxD, $\overline{\text{DCD}}$, $\overline{\text{CTS}}$, $\overline{\text{DSR}}$ (from Modem).
3. Connects transmitter outputs to respective receiver inputs (i.e., TxD to RxD, $\overline{\text{DTR}}$ to $\overline{\text{DCD}}$, $\overline{\text{RTS}}$ to $\overline{\text{CTS}}$).

LLB may be tied to a peripheral control pin (from an R65C21 or R65C24, for example) to provide processor control of local

loop-back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

Remote loop-back does not require this circuitry, so LLB must be set low. However, the processor must select the following:

1. Control Register bit 4 must be 1, so that the transmitter clock equals the receiver clock.
2. Command Register bit 4 must be 1 to select Echo Mode.
3. Command Register bits 3 and 2 must be 1 and 0, respectively to disable $\overline{\text{IRQ}}$ interrupt to transmitter.
4. Command Register bit 1 must be 0 to disable $\overline{\text{IRQ}}$ interrupt for receiver.

In this way, the system re-transmits received data without any effect on the local system.

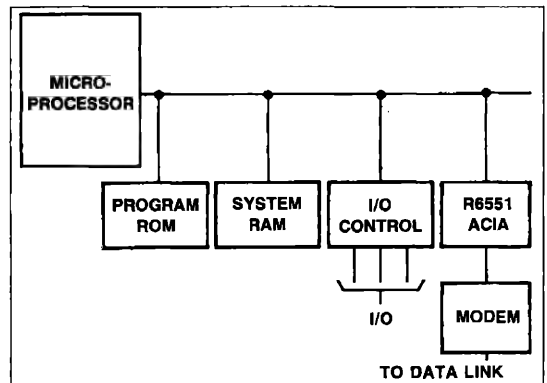


Figure 18. Simplified System Diagram

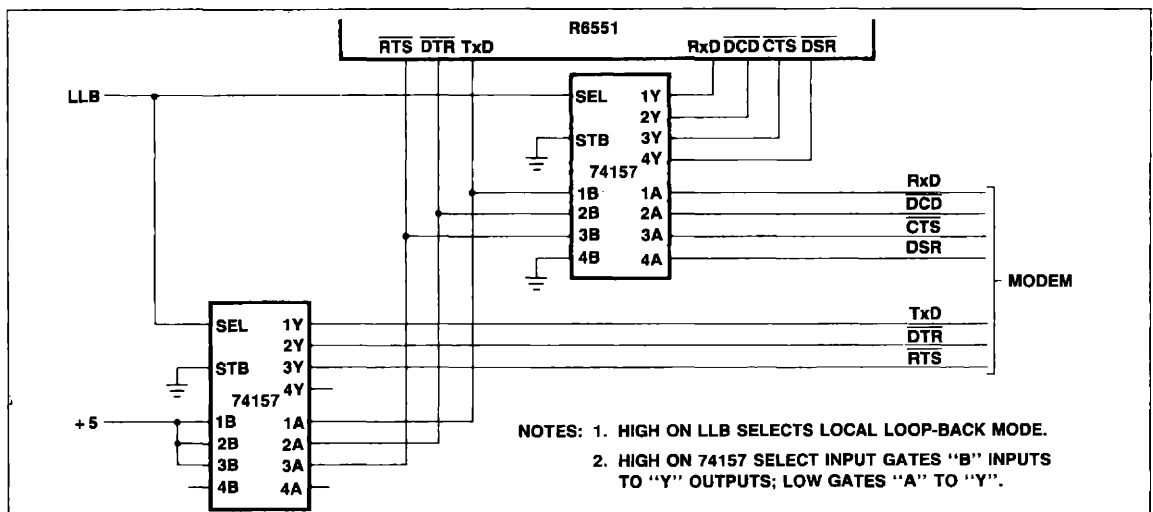


Figure 19. Loop-Back Circuit Schematic

READ TIMING DIAGRAM

Timing diagrams for transmit with external clock, receive with external clock, and $\overline{\text{IRQ}}$ generation are shown in Figures 20, 21 and 22, respectively. The corresponding timing characteristics are listed in Table 3.

Table 3. Transmit/Receive Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	—	400*	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	175	—	ns
Transmit/Receive Clock Low Time	t_{CL}	175	—	175	—	ns
XTLI to TxD Propagation Delay	t_{DD}	—	500	—	500	ns
RTS Propagation Delay	t_{DLY}	—	500	—	500	ns
$\overline{\text{IRQ}}$ Propagation Delay (Clear)	t_{IRQ}	—	500	—	500	ns

Notes:

(t_R , t_F = 10 to 30 ns)

*The baud rate with external clocking is: $\text{Baud Rate} = \frac{1}{16 \times t_{CCY}}$

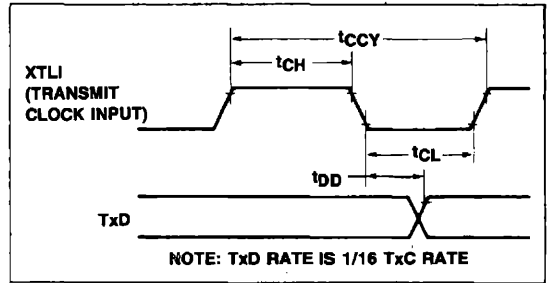


Figure 20. Transmit Timing with External Clock

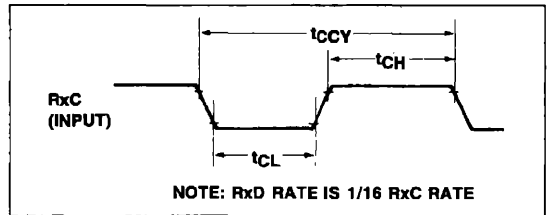


Figure 21. Receive External Clock Timing

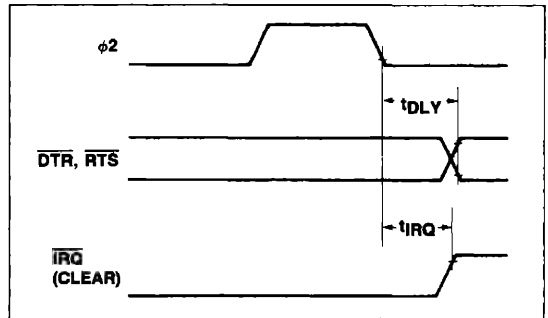


Figure 22. Interrupt and Output Timing

AC CHARACTERISTICS

Parameter	Symbol	2 MHz		4 MHz		Unit
		Min	Max	Min	Max	
$\phi 2$ Cycle Time	t_{CYC}	500	—	250	—	ns
$\phi 2$ Pulse Width	t_C	200	—	100	—	ns
Address Set-Up Time	t_{AC}	60	—	30	—	ns
Address Hold Time	t_{CAH}	0	—	0	—	ns
R/W Set-Up Time	t_{WC}	60	—	30	—	ns
R/W Hold Time	t_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	60	—	35	—	ns
Data Bus Hold Time	t_{HW}	10	—	5	—	ns
Read Access Time (Valid Data)	t_{CDR}	—	150	—	50	ns
Read Hold Time	t_{HR}	10	—	10	—	ns
Bus Active Time (Invalid Data)	t_{CDA}	20	—	10	—	ns

Notes:

1. $V_{CC} = 5.0V \pm 5\%$.
2. $T_A = T_L$ to T_H .
3. t_R and $t_F = 10$ to 30 ns.

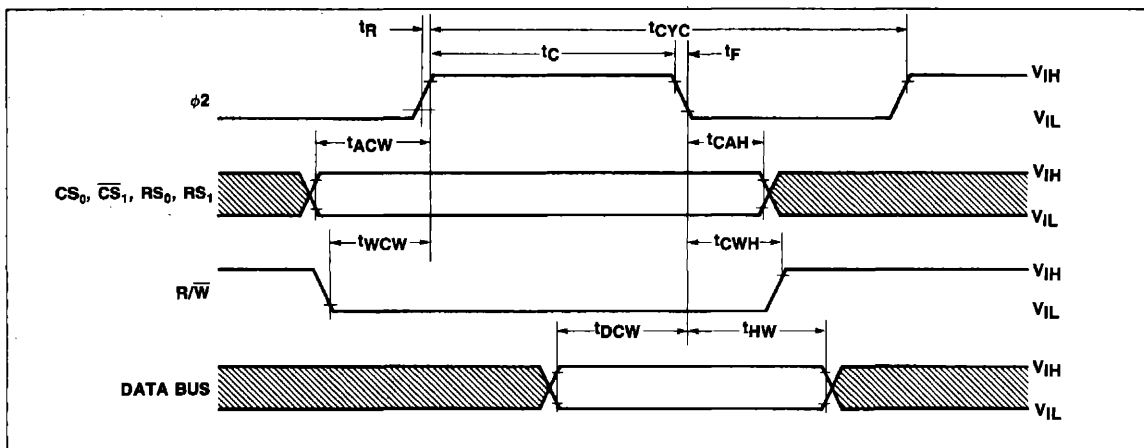


Figure 23. Write Timing Diagram

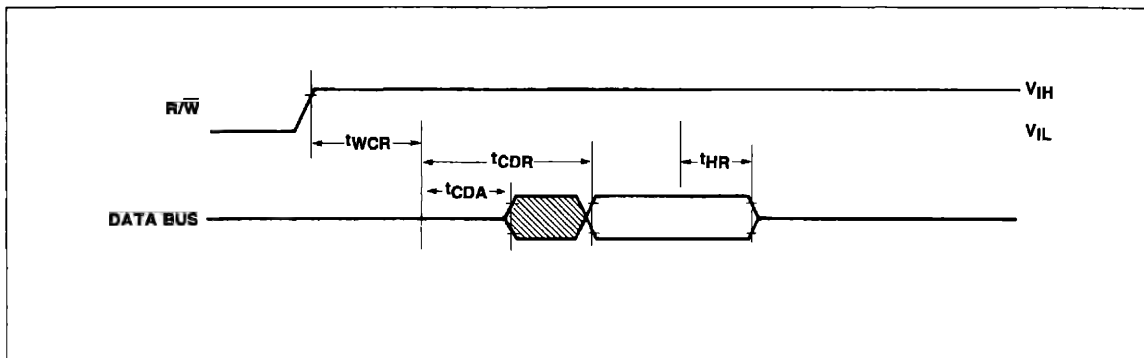


Figure 24. Read Timing Characteristics

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	Vdc
Output Voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	Vdc
Operating Temperature Commercial Industrial	T_A	0 to +70 -40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V \pm 5%
Temperature Range Commercial Industrial	T_A	0° to 70°C -40°C to +85°C

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0$, $T_A = T_L$ to T_H , unless otherwise noted)

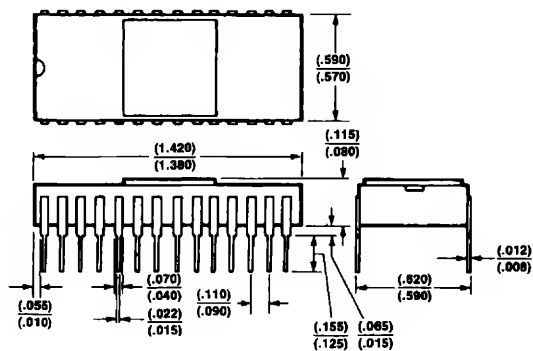
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V	
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V	
Input Leakage Current: Ø2, R/W, RES, CS0, CS1, RS1, \overline{CTS} , RxD, \overline{DCD} , DSR	I_{IN}	—	± 1	± 2.5	μA	$V_{IN} = 0V$ to V_{CC} $V_{CC} = 5.25V$
Input Leakage Current (Three State Off) D0-D7	I_{TSI}	—	± 2	± 10	μA	$V_{IN} = 0.4V$ to 2.4V $V_{CC} = 5.25V$
Output High Voltage: D0-D7, TxD, RxC, RTS, DTR	V_{OH}	2.4	—	—	V	$V_{CC} = 4.75V$ $I_{LOAD} = -100 \mu A$
Output Low Voltage: D0-D7, TxD, RxC, RTS, DTR, IRQ	V_{OL}	—	—	0.4	V	$V_{CC} = 4.75V$ $I_{LOAD} = 1.6 mA$
Output High Current (Sourcing): D0-D7, TxD, RxC, RTS, DTR	I_{OH}	-200	-400	—	μA	$V_{OH} = 2.4V$
Output Low Current (Sinking): D0-D7, TxD, RxC, RTS, DTR, IRQ	I_{OL}	1.6	—	—	mA	$V_{OL} = 0.4V$
Output Leakage Current (off state): IRQ	I_{OFF}	—	—	10	μA	$V_{OUT} = 5.0V$
Power Dissipation	P_D	—	7	10	mW/MHz	
Input Capacitance All except Ø2	C_{CLK} C_{IN}	— —	—	20 10	pF pF	$V_{CC} = 5.0V$ $V_{IN} = 0V$ $f = 2 MHz$ $T_A = 25^\circ C$
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:

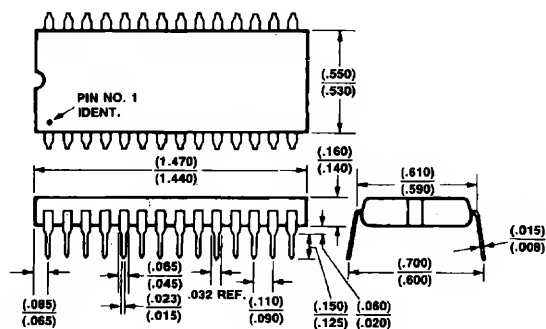
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP





R65C52 DUAL ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (DACIA)

PRELIMINARY

2

DESCRIPTION

The Rockwell CMOS R65C52 Dual Asynchronous Communications Interface Adapter (DACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The DACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 38,400 baud, or at 1/16 times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at 1/16 times the external clock rate. The DACIA is programmable for word lengths of 5, 6, 7 or 8 bits; even, odd, or no parity; and 1 or 2 stop bits.

The DACIA is designed for maximum programmed control from the microprocessor (MPU) to simplify hardware implementation. Dual sets of registers allow independent control and monitoring of each channel. The DACIA also provides a unique, programmable Automatic Address Recognition Mode for use in a multi-drop environment.

The Control Register and Status Register permit the MPU to easily select the R65C52's operating modes and determine operational status.

The Interrupt Enable Registers (IER) and Interrupt Status Registers (ISR) allow the MPU to control and monitor the interrupt capabilities of the DACIA.

The Control and Format Register (CFR) permits selection of baud rates, word lengths, parity and stop bits as well as control of DTR and RTS output signals.

The Status Register (SR) gives the MPU access to the state of the modem control lines, framing error, transmitter underrun and break conditions.

The Compare Data Registers (CDR) hold the data value to be used in the compare mode and the Transmit Break Register (TBR) commands a Transmit Break and provides for parity/address recognition, for Automatic Address Mode.

The Transmitter Data Register and Receiver Data Register are used for temporary data storage of input and output data.

FEATURES

- Low power CMOS N-well silicon gate technology
- Two independent full duplex channels with buffered receivers and transmitters.
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 38,400)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Programmable control of edge detect for DCD, DSR, DTR, RTS, and CTS
- Program-selectable serial echo mode for each channel
- Automatic Address Recognition Mode for multi-drop operation.
- Up to 4 MHz host bus operation
- 5.0 Vdc \pm 5% supply requirements
- 40-pin plastic or ceramic DIP
- Full TTL or CMOS input/output compatibility
- Compatible with R6500 and R65C00 microprocessors and R6500/* microcomputers.

ORDERING INFORMATION

Part Number:

R65C52

Temperature Range (T_L to T_H):
Blank = 0°C to +70°C
E = -40°C to +85°C

Frequency Range:
2 = 2 MHz
4 = 4 MHz

Package
C = Ceramic
P = Plastic

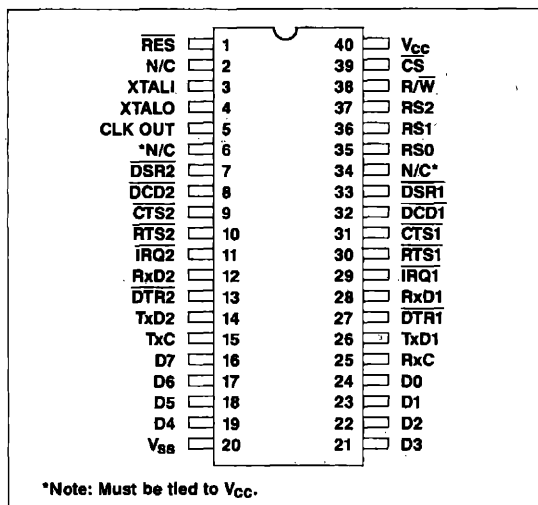


Figure 1. R65C52 Pin Configuration

INTERFACE SIGNALS

Figure 2 shows the DACIA interface signals associated with the microprocessor and the modem.

DATA BUS (D0-D7)

The D0-D7 pins are eight data lines that transfer data between the microprocessor (MPU) and the DACIA. These lines are bidirectional and are normally high-impedance except during READ cycle when the DACIA is selected.

REGISTER SELECTS (RS0, RS1, RS2)

The three register select lines are normally connected to the processor address lines to allow the MPU to select the various internal registers. Table 1 shows the internal register select coding and identifies the abbreviations (ABBR) used throughout the text for each register.

READ/WRITE (R/W)

The R/W input, generated by the microprocessor, controls the direction of data transfer. A high on the R/W line indicates a read cycle, while a low indicates a write cycle.

CHIP SELECT (CS)

The chip select input is normally connected to the processor address lines either directly or through decoders. The DACIA latches address and R/W inputs on the falling edge of CS and latches the data bus inputs on the rising edge of CS.

RESET (RES)

During system initialization a low level on the RES input causes a RESET to occur. At this time the IER's are set to \$80, the DTR and RTS lines go to the high state, the RDR register is cleared, the TBR is set to \$0F, the compare mode is disabled, and the CTS, DCD, DSR flags are cleared. No other bits are affected.

TRANSMIT DATA (TXD1, TXD2)

The TxD outputs transfer serial non-return to zero (NRZ) data to the data communications equipment (DCE). The data is transferred, LSB first, at a rate determined by the baud rate generator.

RECEIVE DATA (RXD1, RXD2)

The RxD inputs transfer serial NRZ data into the DACIA from the DCE, LSB first. The receiver baud rate is determined by the baud rate generator.

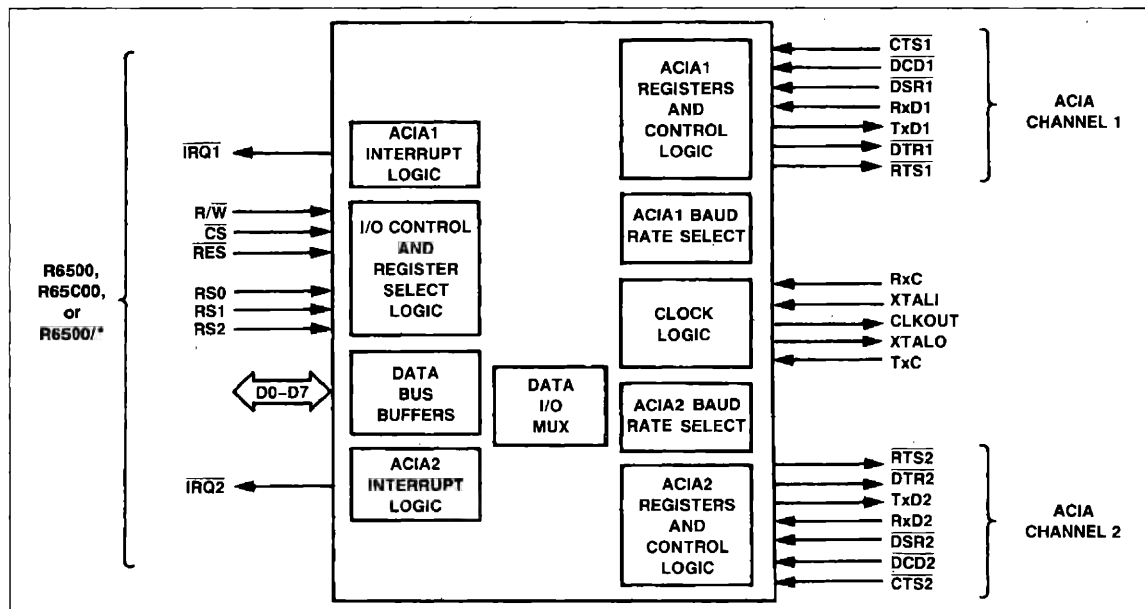


Figure 2. DACIA Interface Signals

CLEAR TO SEND ($\overline{\text{CTS1}}$, $\overline{\text{CTS2}}$)

The $\overline{\text{CTS}}$ control line inputs allow handshaking by the transmitter. When $\overline{\text{CTS}}$ is low, the data is transmitted continuously. When $\overline{\text{CTS}}$ is high, the Transmit Data Register empty bit in the ISR is not set. The word presently in the Transmit Shift Register is sent normally. Any active transition on the CTS lines sets the $\overline{\text{CTS}}$ bit in the appropriate ISR. The $\overline{\text{CTS}}$ status bit in the CSR reflects the current high or low state of $\overline{\text{CTS}}$.

DATA CARRIER DETECT ($\overline{\text{DCD1}}$, $\overline{\text{DCD2}}$)

These two lines may be used as general purpose inputs. An active transition sets the $\overline{\text{DCD}}$ bit in the ISR. The $\overline{\text{DCD}}$ bit in the CSR reflects the current state of the $\overline{\text{DCD}}$ line.

DATA SET READY ($\overline{\text{DSR1}}$, $\overline{\text{DSR2}}$)

These two lines may be used as general purpose inputs. An active transition sets the $\overline{\text{DSR}}$ bit in the ISR. The $\overline{\text{DSR}}$ bit in the CSR reflects the current state of the $\overline{\text{DSR}}$ line.

REQUEST TO SEND ($\overline{\text{RTS1}}$, $\overline{\text{RTS2}}$)

These two lines may be used as general purpose outputs. They are set high upon reset. Their state may be programmed by setting the appropriate bits in the CFR high or low. The state of the $\overline{\text{RTS}}$ line is reflected by the $\overline{\text{RTS}}$ bit in the CSR.

DATA TERMINAL READY ($\overline{\text{DTR1}}$, $\overline{\text{DTR2}}$)

These two lines may be used as general purpose outputs. They are set high upon reset. Their state may be programmed by setting the appropriate bits in the CFR high or low. The state of the $\overline{\text{DTR}}$ line is reflected by the $\overline{\text{DTR}}$ bit in the CSR.

INTERRUPT REQUEST ($\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$)

The $\overline{\text{IRQ}}$ lines are open-drain outputs from the interrupt control logic. $\overline{\text{IRQ1}}$ is associated with ACIA1 and $\overline{\text{IRQ2}}$ is associated with ACIA2. These lines are normally high but go low when one of the flags in the ISR is set, provided that its corresponding enable bit is set in the IER.

Table 1. DACIA Register Selection

HEX ADDR	REGISTER SELECT LINES			CONTROL AND FORMAT REGISTER BITS		REG ADDR	REGISTER ACCESS	
	RS2	RS1	RS0	CFR-7	CFR-6		WRITE	READ
00	L	L	L	—	—	IER1 ISR1	INTERRUPT ENABLE REGISTER 1	INTERRUPT STATUS REGISTER 1
01	L	L	H	0	—	CFR1 SR1	CONTROL REGISTER 1	STATUS REGISTER 1
				1	—	DFR1	FORMAT REGISTER 1	INVALID
02	L	H	L	—	0	CDR1	COMPARE DATA REGISTER 1	INVALID
				—	1	TBR1	TRANSMIT BREAK REGISTER 1	INVALID
03	L	H	H	—	—	TDR1 RDR1	TRANSMIT DATA REGISTER 1	RECEIVE DATA REGISTER 1
04	H	L	L	—	—	IER2 ISR2	INTERRUPT ENABLE REGISTER 2	INTERRUPT STATUS REGISTER 2
05	H	L	H	0	—	CFR2 SR2	CONTROL REGISTER 2	STATUS REGISTER 2
				1	—	CFR2	FORMAT REGISTER 2	INVALID
06	H	H	L	—	0	CDR2	COMPARE DATA REGISTER 2	INVALID
				—	1	TBR2	TRANSMIT BREAK REGISTER 2	INVALID
07	H	H	H	—	—	TDR2 RDR2	TRANSMIT DATA REGISTER 2	RECEIVE DATA REGISTER 2

FUNCTIONAL DESCRIPTION

Figure 3 is a block diagram of the DACIA which consists of two asynchronous communications interface adapters with common microprocessor interface control logic and data bus buffers. The individual functional elements of the DACIA are described in the following paragraphs.

INTERRUPT LOGIC

The interrupt logic causes the $\overline{\text{IRQ}}$ lines ($\overline{\text{IRQ1}}$ or $\overline{\text{IRQ2}}$) to go low when conditions are met that require the attention of the MPU. There are two registers (the Interrupt Enable Register and the Interrupt Status Register) involved in the control of interrupts in the DACIA. Corresponding bits in both registers must be set to cause an $\overline{\text{IRQ}}$.

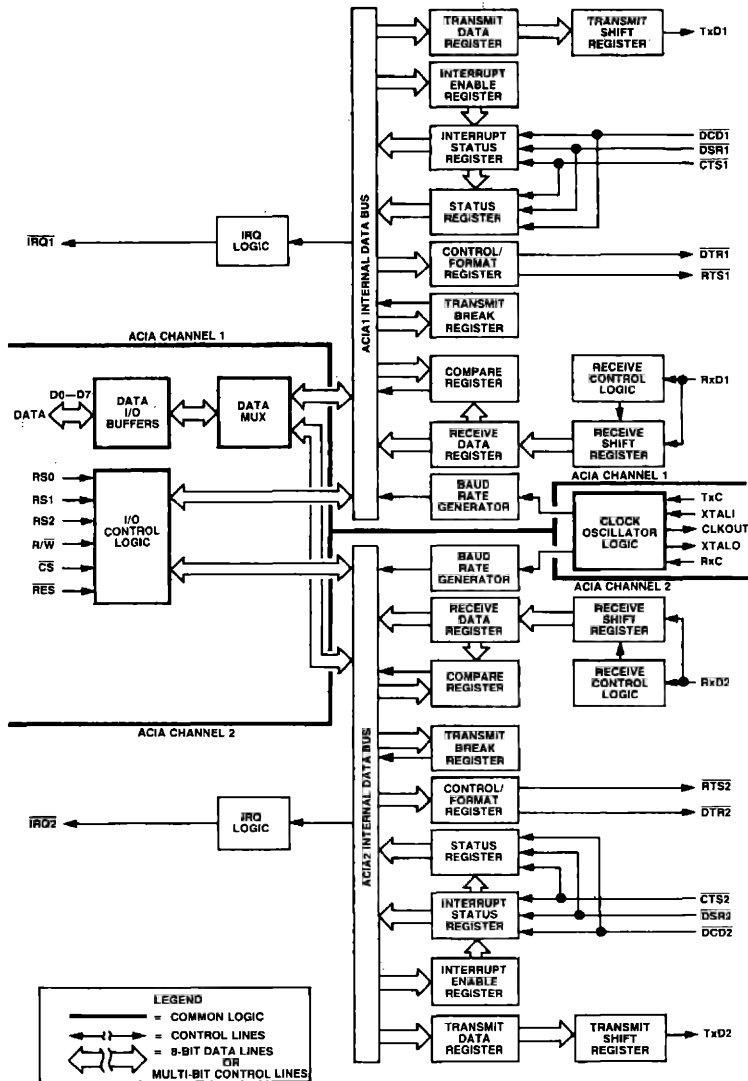


Figure 3. DACIA Block Diagram

DATA BUS BUFFER

The Data Bus Buffer is a bidirectional interface between the system data lines and the internal data bus. When R/\overline{W} is high and \overline{CS} is low, the Data Bus Buffer passes data from the internal data bus to the system data lines. When R/\overline{W} is low and \overline{CS} is low, data is brought into the DACIA from the system data bus. Table 2 summarizes the Data Bus Buffer states.

Table 2. Data Bus Buffer Summary

Control Signals		Data Bus Buffer State
R/\overline{W}	\overline{CS}	
L	L	Write Mode — Tri-State
H	L	Read Mode — Output Data

TRANSMIT AND RECEIVE DATA REGISTERS

These registers are used as temporary data storage for the DACIA Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.
- Write-only register.

The Receive Data Register is characterized in a similar fashion as follows:

- Bit 0 is the leading bit received.
- Unused data bits are the high order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped off after being used for external parity checking. Parity and all unused high-order bits are "0".
- Read-only register

Figure 4 shows an example of a Parity Mode single transmitted or received data word. In this example, the data word is formatted with 8 data bits, parity, and two stop bits. Figure 4 also shows a single character transmitted or received in Address/Data Mode. In this example, the address or data word is 8 bits, there is no

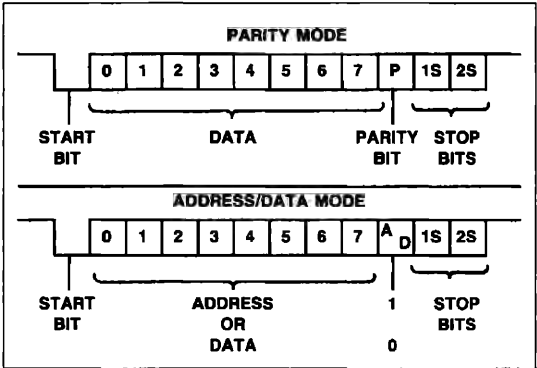


Figure 4. Typical Character

parity bit, and there are two stop bits. The 10th bit (normal parity bit) is an address/data indicator. A 1 means the 8 bits are an address and a 0 means the 8 bits are data.

CLOCK CIRCUIT

The internal clock oscillator supplies the time base for the baud rate generator. The oscillator can be driven by a crystal or an external clock, or it can be disabled, in which case the time base for the baud rate is generated by the Receiver External Clock (RxC) and Transmitter External Clock (TxC) input pins. Figure 5 shows the three possible clock configurations.

Crystal (XTALI, XTALO)

These pins are normally connected to an external 3.6864 MHz crystal used as the time base for the baud rate generator. As an alternative, the XTALI pin may be driven with an externally generated clock in which case the XTALO pin must float.

Receiver Clock (RxC)

This pin is the Receiver 16x clock input when the baud rate generator is programmed for external clock. Figure 15 shows timing considerations for RxC.

Transmitter Clock (TxC)

This pin is the transmitter 16x clock input when the baud rate generator is programmed for external clock. Figure 16 shows timing considerations for TxC.

Note

When RxC and TxC are used for external clock input, XTALI must be tied to ground (Vss) and XTALO must be left open (floating).

Clock Out (CLK OUT)

This output is a buffered output from the 3.6864 MHz crystal oscillator. It may be used to drive the XTALI input of another DACIA. This allows multiple DACIA chips to be used in a system with only one crystal needed. CLK OUT is in phase with XTALI.

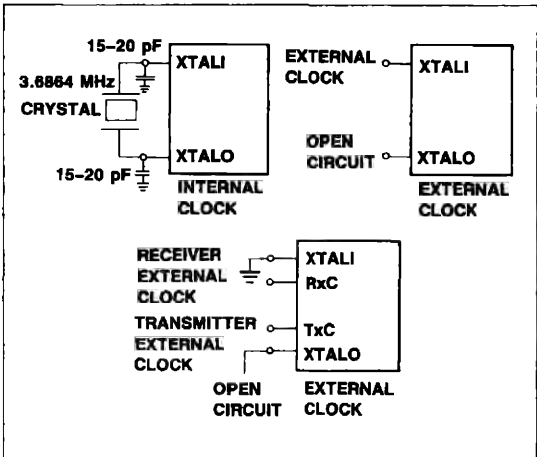


Figure 5. DACIA Clock Generation

CONTROL AND FORMAT REGISTER (CFR)

The Control and Format Register (CFR) is a dual-function, write-only register which allows control of word length, baud rate, control line outputs, parity, echo mode, and compare/TBR access. When the CFR is written to with bit 7 = 0, the CFR functions as a Control Register. When the CFR is written to with bit 7 = 1, the CFR operates as a Format Register.

Control Register (CFR Addressed with Bit 7 = 0)

7	6	5	4	3	2	1	0
0	TBR/CDR	NO. STOP BITS	ECHO	BAUD RATE SELECTION			

Bit 7 **Control or Format Register**
0 Control Register

Bit 6 **TBR/CDR**
1 Access the Transmit Break Register (TBR)
0 Access the Compare Data Register (CDR)

Bit 5 **Number of Stop Bits**
1 Two stop bits
0 One stop bit

Bit 4 **Echo Selection (ECHO)**
1 Echo activated
0 Echo deactivated

Bits 3-0				Baud Rate Selection
3	2	1	0	Baud Rate
0	0	0	0	50
0	0	0	1	109.2
0	0	1	0	134.58
0	0	1	1	150
0	1	0	0	300
0	1	0	1	600
0	1	1	0	1200
0	1	1	1	1800
1	0	0	0	2400
1	0	0	1	3600
1	0	1	0	4800
1	0	1	1	7200
1	1	0	0	9600
1	1	0	1	19200
1	1	1	0	38400
1	1	1	1	External Tx/C and Rx/C Clocks

Format Register (CFR Addressed with Bit 7 = 1)

7	6	5	4	3	2	1	0
1	NUMBER OF DATA BITS		PARITY SELECTION	PARITY ENABLE	DTR CONTROL	RTS CONTROL	

Bit 7 **Control or Format Register**
1 Format Register

Bits 6-5 **Number of Data Bits Per Channel**
No. Bits
6 5
0 0 5
0 1 6
1 0 7
1 1 8

Bits 4-3 **Parity Mode Selection**
Selects
4 3
0 0 Odd Parity
0 1 Even Parity
1 0 Mark Parity
1 1 Space Parity

Bit 2 **Parity Enable**
1 Parity as specified by bits 4-3
0 No Parity

Bit 1 **DTR Control**
1 DTR high
0 DTR low

Bit 0 **RTS Control**
1 RTS high
0 RTS low

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) is a write-only register that allows each of the possible IRQ sources to be enabled, or disabled, individually without affecting any of the other interrupt enable bits in the register. IRQ sources are enabled by writing to the IER with bit 7 set to a 1 and every bit set to a 1 that corresponds to the IRQ source to be enabled. IRQ sources are disabled by writing to the IER with bit 7 set to a 0 and every bit set to a 1 that corresponds to the IRQ source to be disabled. Any bit (except bit 7) to which a 0 is written is unaffected and remains in its original state. As an example, writing \$7F to the IER will disable all IRQ source bits, but writing \$FF to the IER will enable all IRQ source bits. A hardware reset (\overline{RES}) clears all IRQ source bits to the 0 state. Bit assignments for the IER are as follows:

7	6	5	4	3	2	1	0
CLEAR/ SET BITS	TDR EMPTY IE	CTS IE	DCD IE	DSR IE	PARITY ERROR IE	FRM OVR BRK IE	RDR FULL IE

INTERRUPT STATUS REGISTER (ISR)

The Interrupt Status Register (ISR) is a read-only register that identifies the current status condition for each DACIA internal IRQ source. Bits 6 through 0 of the ISR are set to a 1 whenever the corresponding IRQ source condition has occurred in the DACIA. Bit 7 identifies if any of the IRQ source status bits have been set in the ISR.

7	6	5	4	3	2	1	0
ANY BIT SET	TDR EMPTY	CTS TRANS	DCD TRANS	DSR TRANS	PARITY ERROR	FRM OVR BRK	RDR FULL

Bit 7 Any Bit Set

- 1 Any bit (6 through 0) has been set to a 1
- 0 No bits have been set to a 1

Bit 6 Transmit Data Register Empty (TDR EMPTY)

- 1 Transmit Data Register has been transferred to the shift register
- 0 New data has been written to the Transmit Data Register

Bit 5 Transition On $\overline{\text{CTS}}$ Line ($\overline{\text{CTS}}$ TRANS)

- 1 A positive or negative transition has occurred on $\overline{\text{CTS}}$
- 0 No transition has occurred on $\overline{\text{CTS}}$, or ISR has been Read

Bit 4 Transition On $\overline{\text{DCD}}$ Line ($\overline{\text{DCD}}$ TRANS)

- 1 A positive or negative transition has occurred on $\overline{\text{DCD}}$
- 0 No transition has occurred on $\overline{\text{DCD}}$, or ISR has been Read

Bit 3 Transition On $\overline{\text{DSR}}$ Line ($\overline{\text{DSR}}$ TRANS)

- 1 A positive or negative transition has occurred on $\overline{\text{DSR}}$
- 0 No transition has occurred on $\overline{\text{DSR}}$, or ISR has been Read

Bit 2 Parity Error

- 1 A parity error has occurred in received data
- 0 No parity error has occurred, or the Receive Data Register (RDR) has been Read

Bit 1 Frame Error, Overrun or Break (FRM OVR BRK)

- 1 A framing error, receive overrun, or receive break has occurred
- 0 No error, overrun, break has occurred or RDR has been Read

Bit 0 Receive Data Register Full (RDR FULL)

- 1 Shift register data has been transferred to Receive Data Register
- 0 Receive Data Register has been Read

CONTROL STATUS REGISTER (CSR)

The Control Status Register (CSR) is a read-only register that provides I/O status and error condition information. The CSR is normally read after an IRQ has occurred to determine the exact cause of the interrupt condition.

7	6	5	4	3	2	1	0
FRAMING ERROR	TRANS UNDR	CTS STATUS	DCD STATUS	DSR STATUS	REC BREAK	DTR STATUS	RTS STATUS

Bit 7 Framing Error

- 1 A framing error occurred in receive data
- 0 No framing error occurred, or the RDR was Read

Bit 6 Transmitter Underrun (TRANS UNDR)

- 1 Transmit shift register is empty and TDRE bits in IER and ISR are set
- 0 A write to the TDR has occurred

Bit 5 $\overline{\text{CTS}}$ Status

- 1 A low-to-high transition occurred on $\overline{\text{CTS}}$ line
- 0 A high-to-low transition occurred on $\overline{\text{CTS}}$ line

Bit 4 $\overline{\text{DCD}}$ Status

- 1 A low-to-high transition occurred on $\overline{\text{DCD}}$ line
- 0 A high-to-low transition occurred on $\overline{\text{DCD}}$ line

Bit 3 $\overline{\text{DSR}}$ Status

- 1 A low-to-high transition occurred on $\overline{\text{DSR}}$ line
- 0 A high-to-low transition occurred on $\overline{\text{DSR}}$ line

Bit 2 REC Break

- 1 A Receive Break has occurred
- 0 No Receive Break occurred, or RDR, was read

Bit 1 $\overline{\text{DTR}}$ Status

- 1 A low-to-high transition occurred on $\overline{\text{DTR}}$ line
- 0 A high-to-low transition occurred on $\overline{\text{DTR}}$ line

Bit 0 $\overline{\text{RTS}}$ Status

- 1 A low-to-high transition occurred on $\overline{\text{RTS}}$ line
- 0 A high-to-low transition occurred on $\overline{\text{RTS}}$ line

TRANSMIT BREAK REGISTER (TBR)

The DACIA has two Transmit Break Registers which are write-only registers. Only two bits of these registers are used; one during the Receive mode to command a Transmit Break and the other to provide for Parity/Address recognition. Writing a 1 to bit 1 of the TBR causes a continuous Break to be transmitted by the ACIA associated with the register. Writing a 0 to this bit allows normal transmission to resume. Writing a 1 to bit 0 of the TBR commands the value of the Parity bit to be sent to the Parity Error bit (bit 2 of the ISR). Writing a 0 to this bit allows normal Parity Error recognition to be in force. When an RES is received by the DACIA, both of these bits are reset to 0. The bits format for the TBR are as follows:

7	6	5	4	3	2	1	0
NOT USED						TRANS BRK	PAR/ ADDR

Bits 7-2 Not used (don't care)

Bit 1 Transmit Break (TRANS BRK)

- 1 Transmit continuous Break until disabled
- 0 Resume normal transmission

Bit 0 Parity/Address Recognition (PAR ADDR)

- 1 Send value of parity to ISR bit 2
- 0 Return to normal Parity Error recognition mode

COMPARE DATA REGISTER

The Compare Data Register (CDR) is a write-only register which can be accessed when CFR bit 6 = 0. By writing a value into the CDR, the DACIA is put in the compare mode. In this mode, setting of the RDRF bit is inhibited until a character is received which matches the value in the CDR. The next character is then received and the RDRF bit is set. The receiver will now operate normally until the CDR is again loaded.

SUMMARY OF REGISTERS

Table 3 shows the control and status registers associated with the DACIA in a single summary table. Each of the ACIA's has its own set of these seven registers.

OPERATION

The following paragraphs describe ten modes (or conditions) of operation of the DACIA. The modes described are:

- Continuous Data Transmit
- Continuous Data Receive
- Transmit Underrun Condition
- Effects of CTS on Transmitter
- Effects of Overrun on Receiver
- Echo Mode Timing
- Framing Error
- Transmit Break Character
- Receive Break Character
- Automatic Address Recognition

Table 3. Control and Status Registers Format Summary

REGISTER BIT NUMBERS								REGISTER	RES
7	6	5	4	3	2	1	0	INTERRUPT ENABLE REGISTERS	\$80
CLEAR/SET BITS	TDR EMPTY IE	CTS IE	DCD IE	DSR IE	PARITY ERROR IE	FRM OVR BRK IE	RDR FULL IE	INTERRUPT STATUS REGISTERS	—
ANY BIT SET	TDR EMPTY	CTS TRANS	DCD TRANS	DSR TRANS	PARITY ERROR	FRM OVR BRK	RDR FULL	STATUS REGISTERS	—
FRAMING ERROR	TRANS UNDR	CTS STATUS	DCD STATUS	DSR STATUS	REC BREAK	DTR STATUS	RTS STATUS	CONTROL REGISTERS AND FORMAT REGISTERS	—
0	TBR/ CDR	NO. STOP BITS	ECHO	BAUD RATE SELECTION					
1	NUMBER OF DATA BITS		PARITY SELECTION		PARITY ENABLE	DTR CONTROL	RTS CONTROL		
NOT USED						TRANS BRK	PAR/ ADDR	TRANSMIT BREAK REGISTERS	\$0F
COMPARE BITS (ADDRESS RECOGNITION)								COMPARE DATA REGISTERS	—

CONTINUOUS DATA TRANSMIT

In the normal operating mode, the TDRE bit in the ISR signals the MPU that the DACIA is ready to accept the next data word. An IRQ occurs if the corresponding TDRE IRQ enable bit is set in the IER. The TDRE bit is set at the beginning of the start bit.

When the MPU writes a word to the TDR the TDRE bit is cleared. In order to maintain continuous transmission the TDR must be loaded before the stop bit(s) are ended. Figure 6 shows the relationship between IRQ and TxD for the Continuous Data Transmit mode.

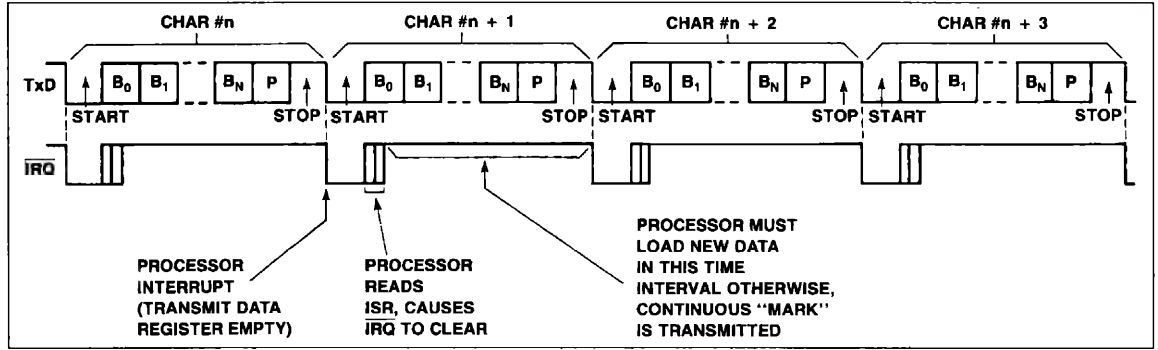


Figure 6. Continuous Data Transmit

CONTINUOUS DATA RECEIVE

Similar to the continuous data transmit mode, the normal receive mode sets the RDRF bit in the ISR when the DACIA has received a full data word. This occurs at about the 9/16 point through the

stop bit. The processor must read the RDR before the next stop bit, or an overrun error occurs. Figure 7 shows the relationship between IRQ and RxD for the continuous Data Receive mode.

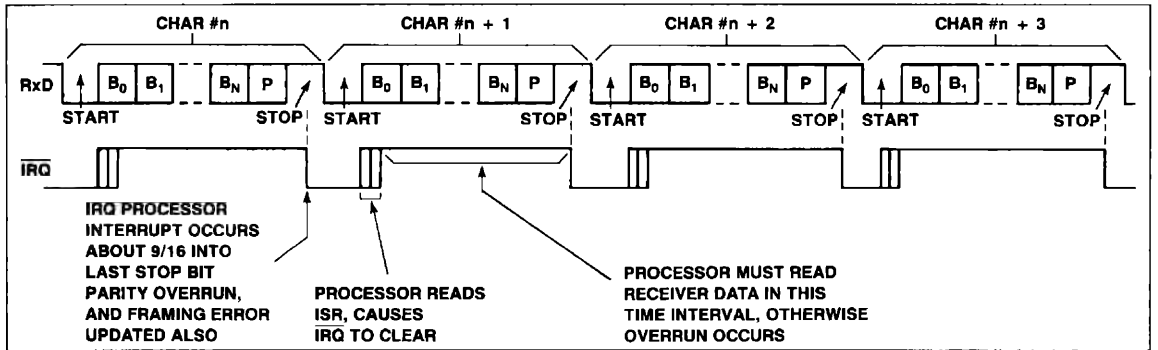


Figure 7. Continuous Data Receive

TRANSMIT UNDERRUN CONDITION

If the MPU is unable to load the TDR before the last stop bit is sent, the TxD line goes to the MARK condition and the underrun

flag is set. This condition persists until the TDR is loaded with a new word. Figure 8 shows the relation between $\overline{\text{IRQ}}$ and TxD for the Transmit Underrun Condition.

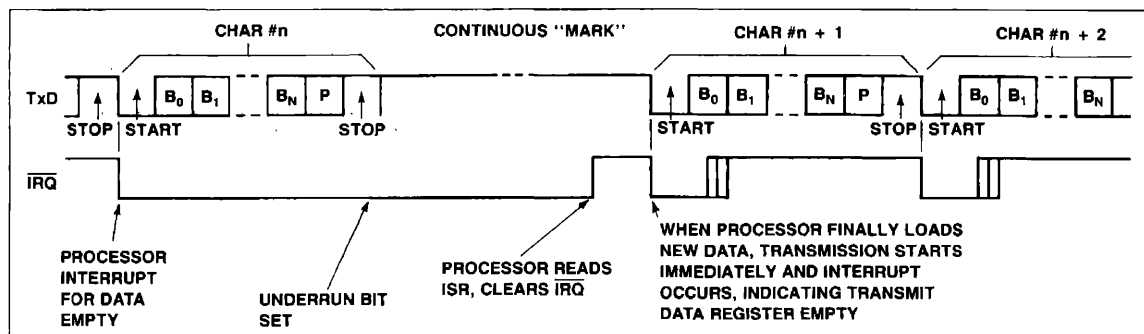


Figure 8. Transmit Underrun Condition Relationship

EFFECTS OF $\overline{\text{CTS}}$ ON TRANSMITTER

The $\overline{\text{CTS}}$ control line controls the transmission of data or the handshaking of data to a "busy" device (such as a printer). When the $\overline{\text{CTS}}$ line is low, the transmitter operates normally. Any transition on this line sets the $\overline{\text{CTS}}$ bit in the ISR. A high condition inhibits the TDRE bit in the ISR from becoming set. The word currently

in the shift register continues to be sent but any word in the TDR is held until $\overline{\text{CTS}}$ goes low. At the high-to-low transition the $\overline{\text{CTS}}$ bit in the ISR is again set. Figure 9 shows the relationship of $\overline{\text{IRQ}}$, TxD, and $\overline{\text{CTS}}$ for the effects of $\overline{\text{CTS}}$ on the transmitter.

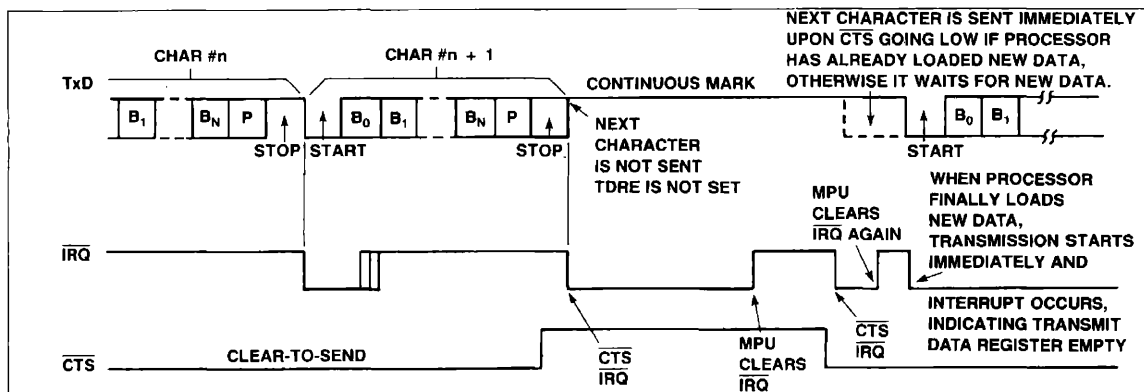


Figure 9. Effects of $\overline{\text{CTS}}$ on Transmitter

EFFECTS OF OVERRUN ON RECEIVER

If the processor does not read the RDR before the stop bit of the next word, an overrun error occurs, the overrun bit is set in the ISR, and the new data word is not transferred to the RDR. The RDR contains the last word not read by the MPU and all follow-

ing data is lost. The receiver will return to normal operation when the RDR is read. Figure 10 shows the relation of $\overline{\text{IRQ}}$ and $\text{Rx}\overline{\text{D}}$ for the effects of overrun on the receiver.

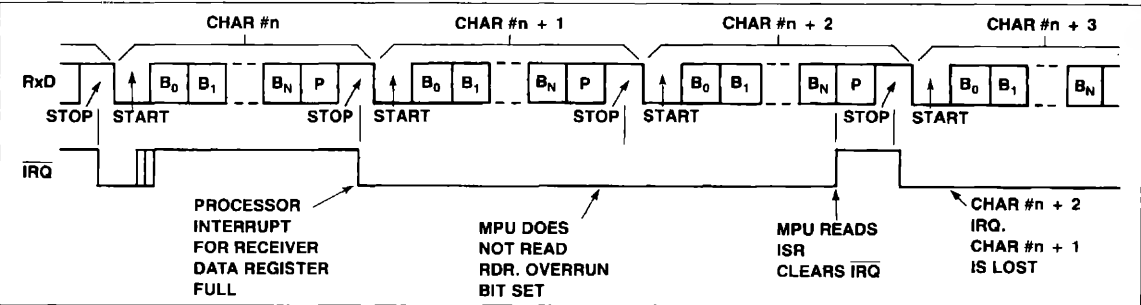


Figure 10. Effects of Overrun on Receiver

ECHO MODE TIMING

In the Echo Mode, the Tx̄D line re-transmits the data received on the Rx̄D line, delayed by 1/2 of a bit time. An internal underflow mode must occur before Echo Mode will start transmitting. In normal transmit mode if TDRE occurs (indicating end of data) an

underflow flag would be set and continuous Mark transmitted. If Echo is initiated, the underflow flag will not be set at end of data and continuous Mark will not be transmitted. Figure 11 shows the relationship of Rx̄D and Tx̄D for Echo Mode.

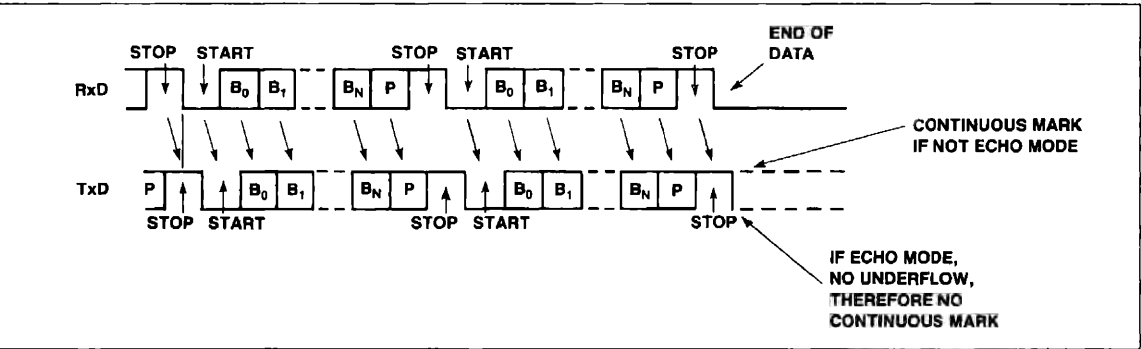
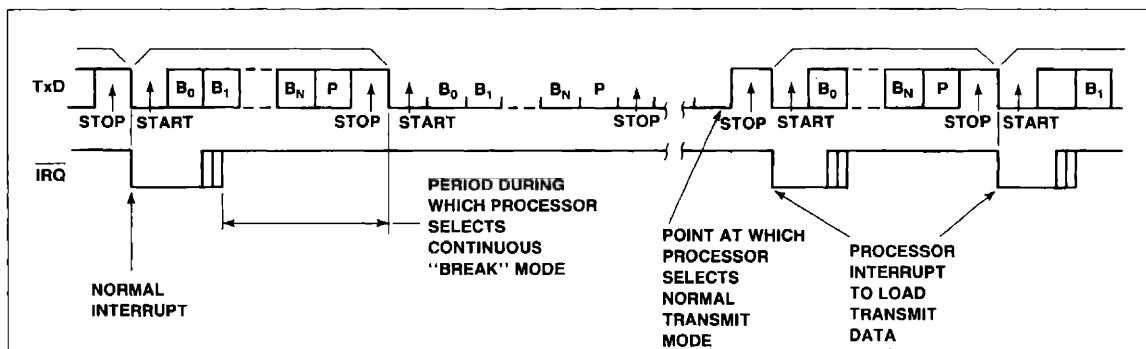
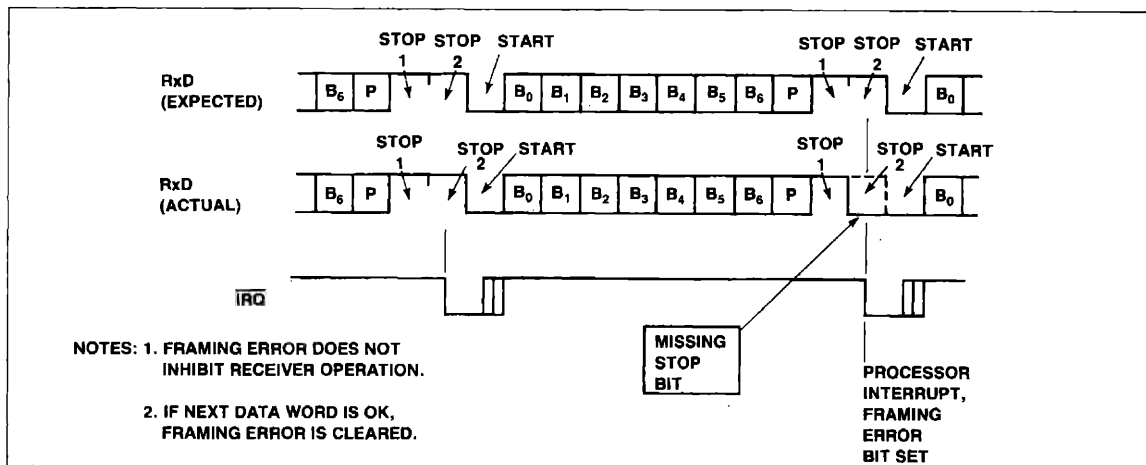


Figure 11. Echo Mode Timing



RECEIVE BREAK CHARACTER

In the event that a Break character is received by the receiver, the Break bit is set. The receiver does not set the RDRF bit and remains in this state until a stop bit is received. At this time the

next character is to be received normally. Figure 14 shows the relationship of IRQ and RxD for a Receive Break Character.

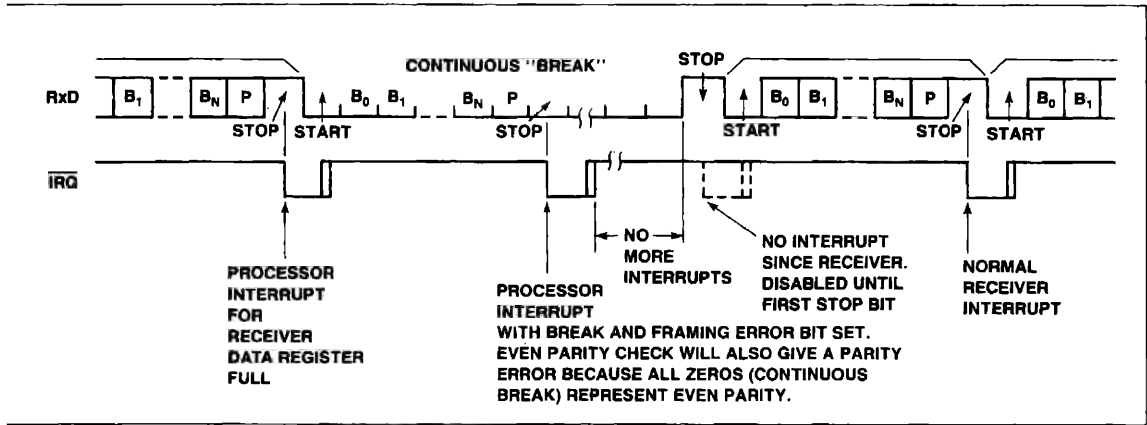


Figure 14. Receive Break Character

AUTOMATIC ADDRESS RECOGNITION

The DACIA offers a unique solution to the standard problem associated with multi-drop environment UARTs and communication interface controllers. In the standard configuration used by other devices, the slave CPU must be constantly interrupted to analyze incoming characters on the communications net to determine if an address word is present and if so, does that address match the address assigned to the slave UART. This CPU interrupt scheme can become intolerable in very large multi-drop networks because every slave on the communications net must "wake-up" its CPU for every character sent down the network by the master. The end result is that the CPUs on the communications net are constantly being interrupted for the mundane task of address recognition.

To avoid this constant CPU interrupt problem, the DACIA has been designed to do address comparison and recognition internally without the need for CPU intervention. Therefore, the slave CPU is not interrupted until the DACIA has determined that the character sent over the communications net by the master was an address and the address matched the address stored in the DACIA Compare Register. At this point the DACIA interrupts the CPU, goes out of Compare Mode, and receives the string of characters being transmitted by the master, (i.e., the data characters). When all data has been received by the slave, its CPU must again write the slave address into the DACIA Compare Register which automatically puts it back into the Compare Mode, waiting for another address character.

GENERATION OF NON-STANDARD BAUD RATES

These can be determined by:

Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the CFR Control Register, as shown in Table 4.

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the DACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 3) must be the clock input and XTALO (pin 4) must be a nonconnect.

Generating Other Baud Rates

By using a different crystal, other baud rates may be generated.

Table 4. Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 3.6864 MHz Crystal	Baud Rate Generated With a Crystal of Frequency (f)
3	2	1	0			
0	0	0	0	73,728	$(3.6864 \times 10^6)/73,728 = 50$	$f/73,728$
0	0	0	1	33,538	$(3.6864 \times 10^6)/33,538 = 109.92$	$f/33,538$
0	0	1	0	27,408	$(3.6864 \times 10^6)/27,408 = 134.58$	$f/27,408$
0	0	1	1	24,576	$(3.6864 \times 10^6)/24,576 = 150$	$f/24,576$
0	1	0	0	12,288	$(3.6864 \times 10^6)/12,288 = 300$	$f/12,288$
0	1	0	1	8,144	$(3.6864 \times 10^6)/8,144 = 600$	$f/6,144$
0	1	1	0	3,072	$(3.6864 \times 10^6)/3,072 = 1,200$	$f/3,072$
0	1	1	1	2,048	$(3.6864 \times 10^6)/2,048 = 1,800$	$f/2,048$
1	0	0	0	1,536	$(3.6864 \times 10^6)/1,536 = 2,400$	$f/1,536$
1	0	0	1	1,024	$(3.6864 \times 10^6)/1,024 = 3,600$	$f/1,024$
1	0	1	0	768	$(3.6864 \times 10^6)/768 = 4,800$	$f/768$
1	0	1	1	512	$(3.6864 \times 10^6)/512 = 7,200$	$f/512$
1	1	0	0	384	$(3.6864 \times 10^6)/384 = 9,600$	$f/384$
1	1	0	1	192	$(3.6864 \times 10^6)/192 = 19,200$	$f/192$
1	1	1	0	96	$(3.6864 \times 10^6)/96 = 38,400$	$f/96$
1	1	1	1	16	$TxC/16 = \text{Baud Rate or } RxC/16 = \text{Baud Rate}$	

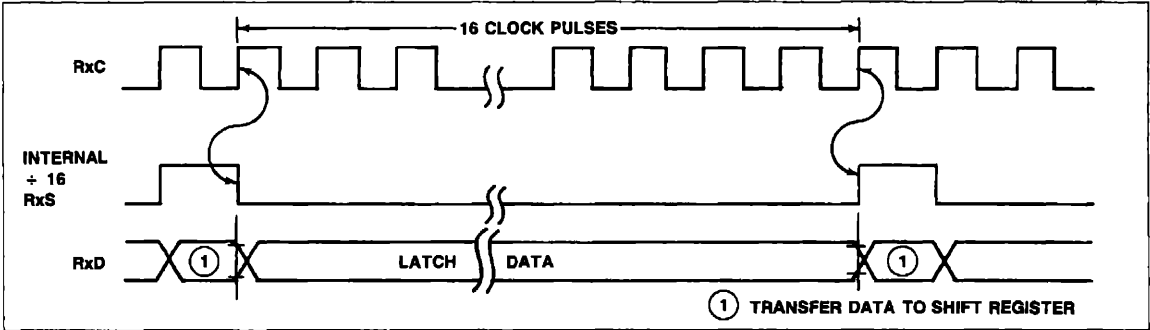


Figure 15. DACIA External Clock Timing — Receive Data

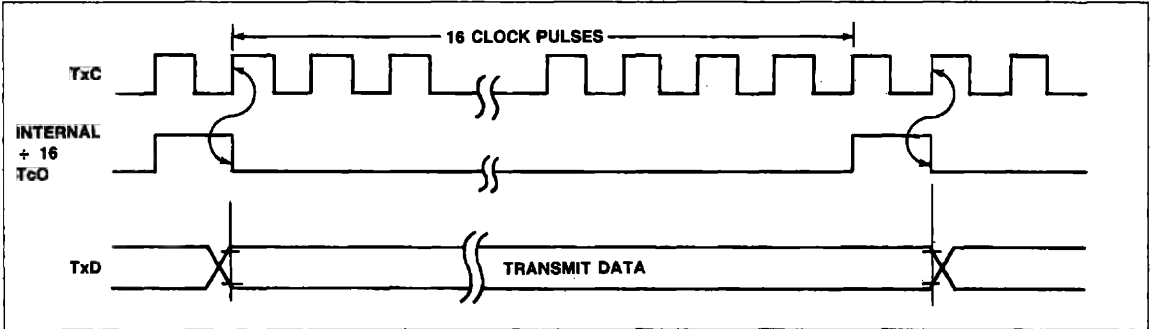


Figure 16. DACIA External Clock Timing — Transmit Data

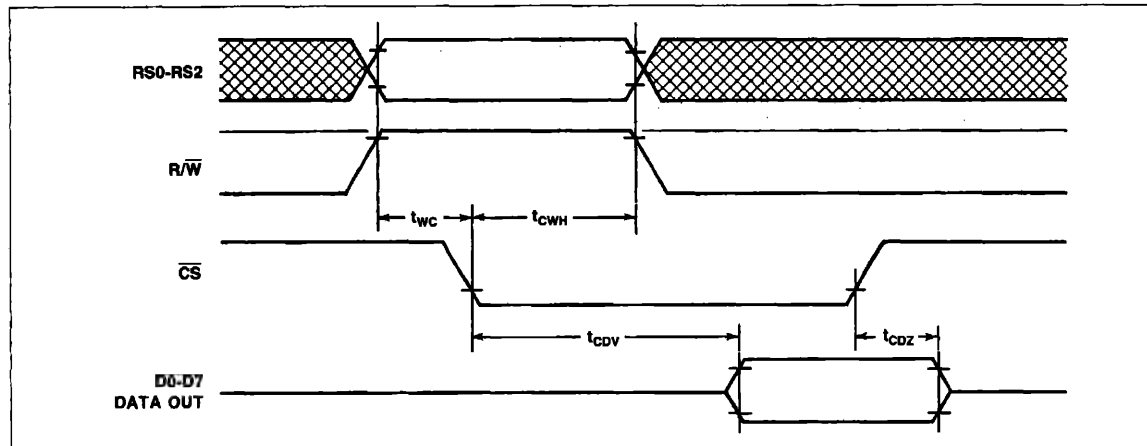
AC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_A = T_L to T_H)

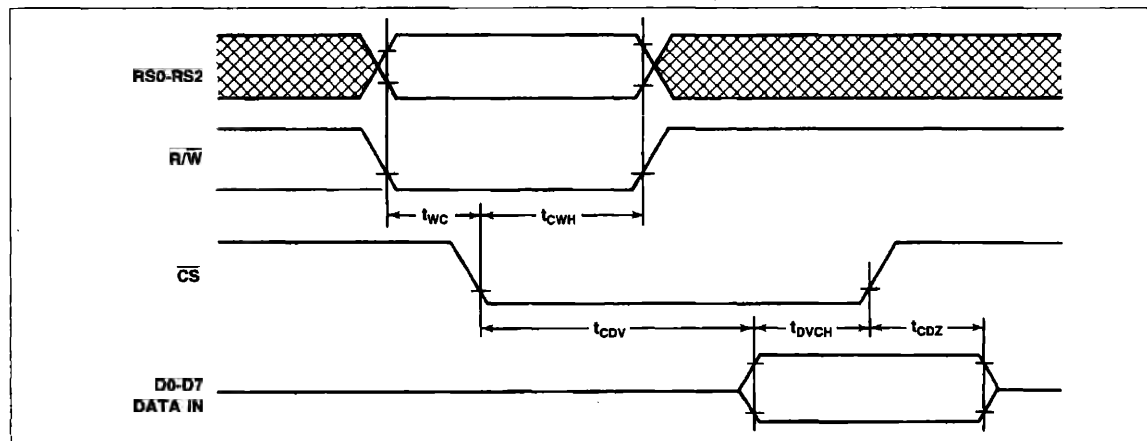
READ/WRITE TIMING

Characteristic	Symbol	2 MHz		4 MHz		Unit
		Min	Max	Min	Max	
R/ \overline{W} , RS0-RS2 Valid to \overline{CS} Low (Setup Time)	t _{wc}	0	—	0	—	ns
\overline{CS} Low to R/ \overline{W} , RS0-RS2 (Hold Time)	t _{cwh}	65	—	65	—	ns
\overline{CS} Low to Data Valid	t _{cdv}	—	100	—	100	ns
\overline{CS} High to Data Invalid (Hold Time)	t _{cdz}	—	10	—	10	ns
Data Valid to \overline{CS} High	t _{dvch}	20	—	20	—	ns

Note:
1. All times are in nanoseconds.



DACIA Read Cycle Waveforms



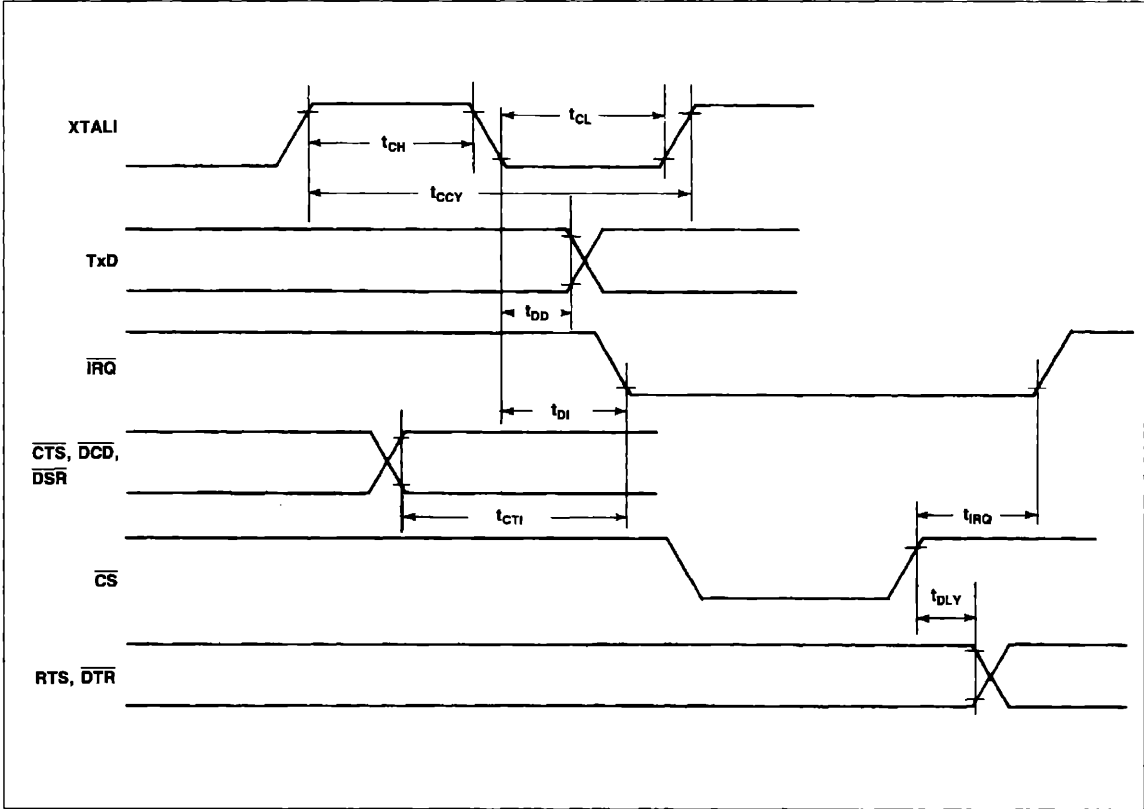
DACIA Write Cycle Waveforms

TRANSMIT/RECEIVE TIMING

Characteristic	Symbol	Min	Max	Unit
Transmit/Receive Clock Rate	t_{CCY}	250	—	ns
Transmit/Receive Clock High Time	t_{CH}	100	—	ns
Transmit/Receive Clock Low Time	t_{CL}	100	—	ns
XTALI to TxD Propagation Delay	t_{DD}	—	250	ns
XTALI to \overline{IRQ} Propagation Delay	t_{DI}	—	250	ns
\overline{CTS} , \overline{DCD} , \overline{DSR} to \overline{IRQ}	t_{CTI}	—	150	ns
\overline{IRQ} Propagation Delay (Clear)	t_{IRQ}	—	150	ns
RTS, \overline{DTR} Propagation Delay	t_{DLY}	—	150	ns

Note:
1. All times are in nanoseconds.

2



DACIA Transmit/Receive Timing

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	Vdc
Output Voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	Vdc
Operating Temperature Commercial Industrial	T_A	0 to +70 -40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V \pm 5%
Temperature Range Commercial Industrial	T_A	0° to 70°C -40°C to +85°C

DC CHARACTERISTICS

($V_{CC} = 5.0\text{ V} \pm 5\%$, $V_{SS} = 0\text{V}$, $T_A = T_L$ to T_H , unless otherwise noted)

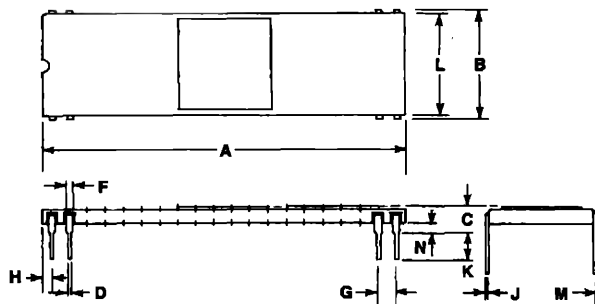
Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTALI and XTALO XTALI and XTALO	V_{IH}	+2.0 +2.4	— —	$V_{CC} + 0.3$ $V_{CC} + 0.3$	V	
Input Low Voltage Except XTALI and XTALO XTALI and XTALO	V_{IL}	-0.3 -0.3	— —	+0.8 +0.4	V	
Input Leakage Current R/W, RES, RS0, RS1, RS2, RxD, CTS, DCD, DSR, RxC, TxC, CS	I_{IN}	—	10	50	μA	$V_{IN} = 0\text{V to } V_{CC}$ $V_{CC} = 5.25\text{V}$
Input Leakage Current for Three-State Off D0-D7	I_{TSI}	—	± 2	10	μA	$V_{IN} = 0.4\text{V to } 2.4\text{V}$ $V_{CC} = 5.25\text{V}$
Output High Voltage D0-D7, TxD, CLK OUT, RTS, DTR	V_{OH}	+2.4 1.5	— —	— —	V	$V_{CC} = 4.75\text{V}$ $I_{LOAD} = -100\text{ }\mu\text{A}$
Output Low Voltage D0-D7, TxD, CLK OUT, RTS, DTR	V_{OL}	—	—	+0.4	V	$V_{CC} = 4.75\text{V}$ $I_{LOAD} = 1.6\text{ mA}$
Output Leakage Current (Off State) IRQ	I_{OFF}	—	± 2	± 10	μA	$V_{CC} = 5.25\text{V}$ $V_{OUT} = 0\text{ to } 2.4\text{V}$
Power Dissipation	P_D	—	—	10	mW/MHz	
Input Capacitance Except XTALI and XTALO XTALI and XTALO	C_{IN}	— —	— —	5 10	pF pF	$V_{CC} = 5.0\text{V}$ $V_{IN} = 0\text{V}$ $f = 2\text{ MHz}$ $T_A = 25^\circ\text{C}$
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:

1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.

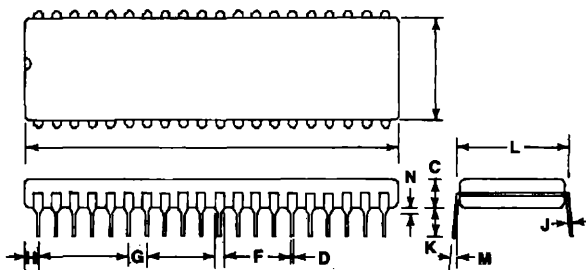
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.88	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
E	0.76	1.40	0.030	0.055
F	2.54 BSC		0.100 BSC	
G	0.76	1.78	0.030	0.070
H	0.20	0.33	0.008	0.013
J	2.54	4.19	0.100	0.165
K	14.60	15.37	0.575	0.605
L	0°	10°	0°	10°
M	0.51	1.52	0.020	0.060

48-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
E	1.02	1.52	0.040	0.060
F	2.54 BSC		0.100 BSC	
G	1.65	2.16	0.065	0.085
H	0.20	0.30	0.008	0.012
J	3.05	3.56	0.120	0.140
K	15.24 BSC		0.600 BSC	
L	7°	10°	7°	10°
M	0.51	1.02	0.020	0.040



R6265 MICRO FLOPPY DISK CONTROLLER (MFDC)

PRELIMINARY

DESCRIPTION

The R6265 Micro Floppy Disk Controller (MFDC) interfaces up to four Sony microfloppy and floppy disk drives to an 8-bit or 16-bit microprocessor-based system including Z-80, 8080A, 8085A, 8086, and 8088. The MFDC simplifies the system design by minimizing both the number of external hardware components and software steps needed to implement the floppy disk drive (FDD) interface. Control signals supplied by the MFDC reduce the number of components required in external phase locked loop and write precompensation circuitry. Memory-mapped registers containing commands, status and data simplify the software interface. Built-in functions reduce the software overhead needed to control the FDD interface. The MFDC provides full compatibility with the single- and double-density formats recommended by Sony Corporation as well as the ability to read the IBM 3740 single-density (FM) and IBM System 34 double-density (MFM) formats.

The MFDC interfaces directly to the synchronous microprocessor bus and operates with 8-bit byte length data transferred on the bus in either DMA or non-DMA mode. In DMA mode, the CPU need only load the command into the MFDC and all data transfers occur under DMA control. The R6265 is directly compatible with the Z8410/ μ PD8257 Direct Memory Access Controller (DMAC). In non-DMA mode, the MFDC generates an interrupt to the CPU indicating that a byte of data is available.

Controller commands, command or device status, and data are transferred between the MFDC and the CPU via six internal registers. The Main Status Register (MSR) stores the MFDC status information while four additional status registers provide result information to the CPU following each controller command. The Data Register (DR) stores actual disk data, parameters, controller commands and FDD status information for use by the CPU.

The R6265 executes 15 separate multi-byte commands:

Read Data	Specify
Write Data	Format a Track
Read Deleted Data	Scan Equal
Write Deleted Data	Scan High or Equal
Read a Track	Scan Low or Equal
Read ID	Sense Interrupt Status
Seek	Sense Drive Status
Recalibrate (Restore to Track 0)	

FEATURES

- Address mark detection circuitry
- Software control of
 - Track stepping rate
 - Head load time
 - Head unload time
- Compatible with Sony recommended format in both single- and double-density recording formats
- Reads standard IBM formats
- Reads and writes in same format as NEC μ PD7265 for Sony microfloppy and floppy disk drives
- Programmable data record lengths: 128, 256, 512 or 1024 bytes/sector
- Multi-sector and multi-track transfer capability
- Controls up to four floppy disk drives
- Data scan capability—will scan a single sector or an entire track of data fields, comparing on a byte-by-byte basis, data in the processor's memory with data read from the disk
- Data transfers in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Directly compatible with an 8-bit or 16-bit synchronous microprocessor bus including Z-80/8080A/8085A, 8086, and 8088
- Alternative to NEC μ PD7265
- Pin, software, and electrically compatible with the R6265
- Single phase 8 MHz Clock
- Single +5 Volt Power Supply

ORDERING INFORMATION

Part Number	CLK Frequency	Temperature Range
R6265	8 MHz	0°C to 70°C
Package:		
C = Ceramic		
P = Plastic		

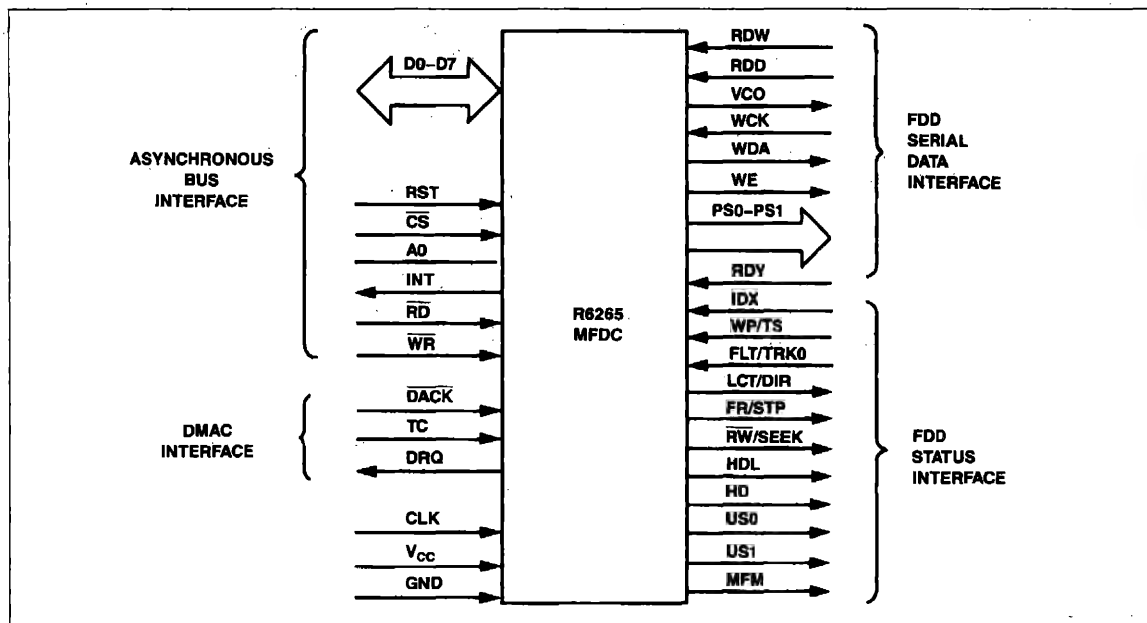


Figure 1. MFDC Input and Output Signals

PIN DESCRIPTION

Throughout this document signals are presented using the terms active and inactive, or asserted and negated, independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar.

BUS INTERFACE

D0-D7—Data Lines. The bidirectional data lines transfer data between the MFDC and the 8-bit data bus.

CLK—CLOCK. The clock is a TTL compatible 8 MHz square wave signal.

RST—RESET. This active high input places the MFDC in the idle state and resets the output lines to the floppy disk drive (FDD) to the low state.

CS—Chip Select. The MFDC is selected when the $\overline{\text{CS}}$ input is low.

A0—Data/Status Register Select. This input selects the Data or Status Register for reading from or writing to. When $\text{A0} = \text{high}$, the Data Register is selected and the state of RD or WR determines whether it is a read ($\text{RD} = \text{low}$) or a write ($\text{WR} = \text{low}$) operation. When $\text{A0} = \text{low}$, the Status Register is selected. This register may only be read ($\text{RD} = \text{low}$); the state $\text{WR} = \text{low}$ is invalid when the Status Register is selected.

INT—Interrupt Request. This active high output is the interrupt request generated by the MFDC to the CPU. INT is asserted upon completion of some MFDC commands and before a data byte is transferred between the MFDC and the data bus (in the Non-DMA mode).

RD—Read. This active low input defines the data bus transfer as a read cycle. When low, the data transfer is from the MFDC to the data bus.

WR—Write. This active low input defines the data bus transfer as a write cycle. When low, the data transfer is from the data bus to the MFDC.

DIRECT MEMORY ACCESS CONTROLLER (DMAC) INTERFACE

DACK—DMA Acknowledge. The DMA transfer acknowledge signal is a TTL compatible input generated by the DMA controller (DMAC) controlling the MFDC. The DMA cycle is active when DACK is low and the MFDC is performing a DMA transfer.

DRQ—Data DMA Request. The transfer request signal is a TTL compatible output generated by the MFDC to request a data transfer operation under control of the DMAC (in the DMA mode). The request is active when $\text{DRQ} = \text{high}$. The signal is reset inactive when DMA Acknowledge ($\overline{\text{DACK}}$) is asserted (low).

TC—Terminal Count. This input signal is issued to the MFDC when the DMA transfer for a channel is complete. The signal is active high concurrent with the **DACK** input when the DMA operation is complete as a result of that transfer.

FDD SERIAL DATA INTERFACE

RDD—Read Data. Read Data input from the floppy disk drive (FDD) containing clock and data bits.

RDW—Read Data Window. Data Window input generated by the Phase Locked Loop (PLL) and used to sample data from the FDD.

VCO—Variable Frequency Oscillator Sync. This output signal inhibits the VCO in the PLL circuit when low and enables the VCO in the PLL circuit when high. This inhibits RDD and RDW from being generated until valid data is detected from the FDD.

WCK—Write Clock. This input clock determines the Write Data rate to the FDD. The data rate is 500 KHz in the FM mode (MFM = low) and 1 MHz in the MFM mode (MFM = high). The pulse width is 250 ns (typical) in both modes.

WDA—Write Data. Serial write data output to the FDD containing both clock and data bits.

WE—Write Enable. This output signal enables the Write Data into the FDD when high.

PS0-PS1—Preshift. These outputs are encoded to convey write compensation status during the MFM mode to determine early, late or normal times as follows:

Write Precompensation Status	Preshift Outputs	
	PS0	PS1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1
0 = Low, 1 = High		

FDD STATUS INTERFACE

RDY—Ready. An active high input signal indicates the FDD is ready to send data to, or receive data from, the MFDC.

IDX—Index. An active high input signal from the FDD indicates the index hole is under the index sensor. Index is used to synchronize MFDC timing.

RW/SEEK—Read Write/Seek. Mode selection signal to the FDD which controls the multiplexer from the multiplexed signals. When **RW/SEEK** is low, the Read/Write mode is commanded; when **RW/SEEK** is high, the Seek mode is commanded.

RW/SEEK	Mode	Active FDD Interface Signals
Low	Read/Write	WP, FLT, LCT, FR
High	Seek	TS, TRK0, DIR, STP

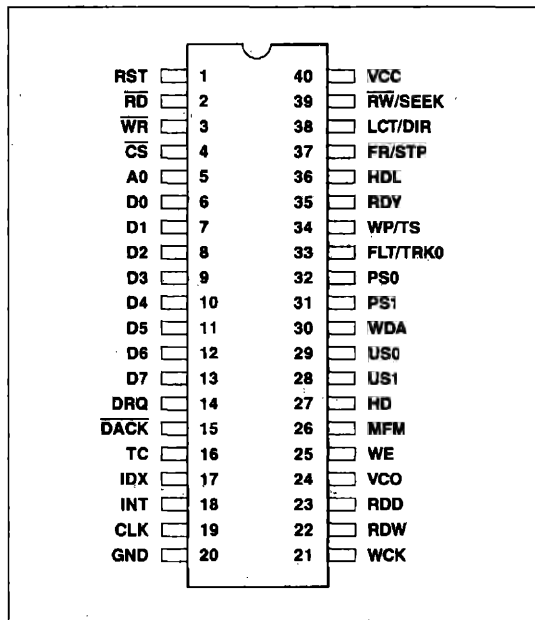
WP/TS—Write Protect/Two Side. An active high multiplexed input signal from the FDD. In the Read/Write mode, **WP/TS** high indicates the media is write-protected. In the Seek mode, **WP/TS** high indicates the media is two-sided.

FLT/TRK0—Fault/Track Zero. An active high multiplexed input from the FDD. In the Read/Write mode (**RW/SEEK** = low), **FLT/TRK0** high indicates an FDD fault. In the Seek mode, **FLT/TRK0** high indicates that the read/write head is positioned over track zero.

LCT/DIR—Low Current/Direction. A multiplexed output to the FDD. In the Read/Write mode, **LCT/DIR** is low when the read/write head is to be positioned over the inner tracks and the **LCT/DIR** is high when the head is to be positioned over the outer tracks. In the Seek mode, **LCT/DIR** controls the head direction. When **LCT/DIR** is high, the head steps to the outside of the disk; when **LCT/DIR** is low, the head steps to the inside of the disk.

FR/STP—Fault Reset/Step. A multiplexed output to the FDD. In the Read/Write mode, **FR/STP** high resets the fault indicator in the FDD. An **FR** pulse is issued at the beginning of each read or write command prior to issuing **HDL**. In the Seek mode, **FR/STP** provides the step pulses to move the read/write head to another track in the direction indicated by the **LCT/DIR** signal.

HDL—Head Load. An active high output to notify the FDD that the read/write head should be loaded (placed in contact with the media). A low level indicates the head should be unloaded.



R6265 MFDC Pin Diagram

HD—Head Select. An output to the FDD to select the proper read/write head. Head One is selected when HD = high and Head Zero is selected when HD = low.

US0-US1—Unit Select. Output signals for floppy disk drive selection as follows:

Unit Select		Floppy Disk Drive Select
US0	US1	
0	0	0
0	1	1
1	0	2
1	1	3

0 = Low, 1 = High

MFM—MFM Mode. Output signal to the FDD to indicate MFM or FM mode. Selects the MFM mode when MFM = high and the FM mode when MFM = low.

VCC—Power. +5V dc.

GND—Ground (V_{SS}).

MFDC REGISTERS

The MFDC contains six registers which may be accessed by the processor or DMA controller via the system (i.e., micro-processor) bus: a Main Status Register, a Data Register, and four Result Status Registers. The 8-bit Main Status Register (MSR) contains the status information of the MFDC, and may be accessed at any time. The 8-bit Data Register, consisting of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, parameters and FDD status information. Bytes of data are read out of, or written into, the Data Register in order to initiate a command or to obtain the results of a command execution.

The read-only Main Status Register facilitates the transfer of data between the system and the MFDC. The other Status Registers (ST0, ST1, ST2 and ST3) are only available during the result phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

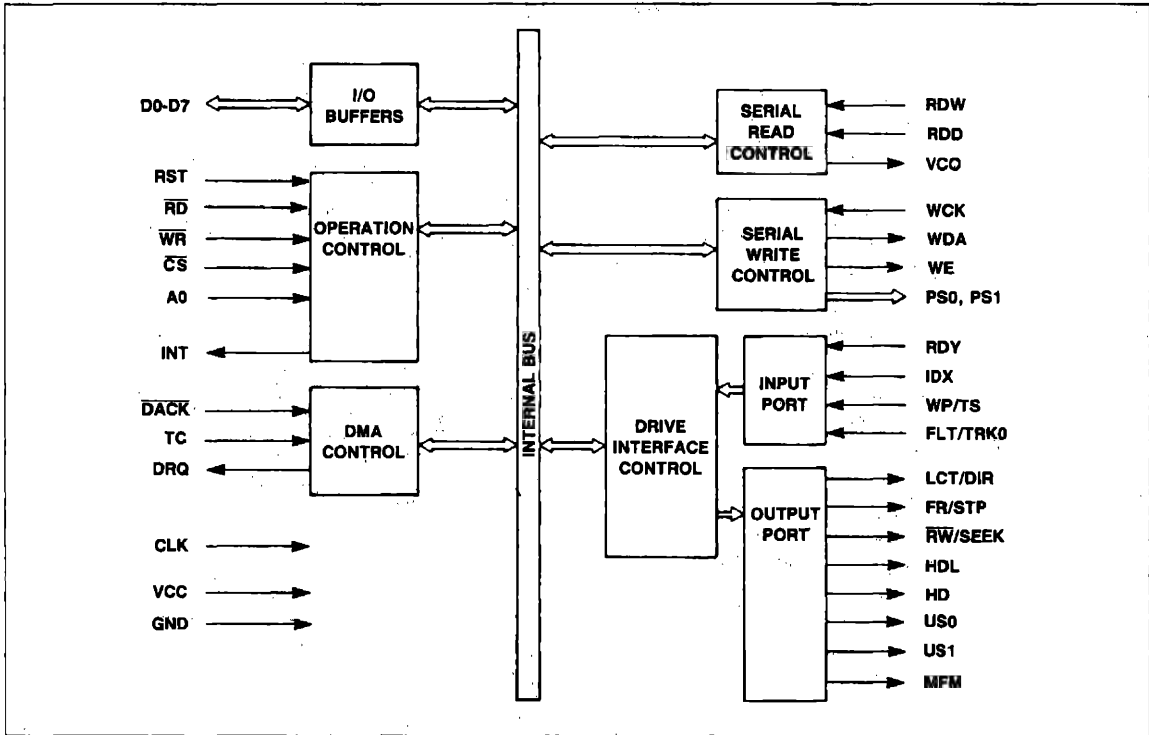


Figure 2. R6265 MFDC Block Diagram

The relationship between the status/data registers and the \overline{WR} , \overline{RD} and $A0$ signals is shown below.

A0	RD	WR	Function
0	0	0	Illegal
0	0	1	Read Main Status Register
0	1	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

0 = Low, 1 = High

Table 1 shows each of the status registers used by the MFDC and each bit assignment within the individual registers. Table 2 defines the symbols used throughout the command definitions. Each register bit symbol is defined in the register descriptions that follow Table 2.

REGISTER DEFINITIONS

Main Status Register (MSR)

7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B

The Main Status Register (MSR) contains the status information of the MFDC, and must be read by the processor before each byte is written to, or read from, the Data Register during the command or result phase. MSR reads are not required during the execution phase. The Data Input/Output (DIO) and Request for Master (RQM) bits in the MSR indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last \overline{RD} or \overline{WR} during command or result phases and the DIO and RQM getting set or reset is 12 μ s. For this reason, every time the MSR is read the processor should wait 12 μ s. The maximum time from the trailing edge of the last \overline{RD} in the result phase to when bit 4 (MFDC Busy) goes low is also 12 μ s.

The DIO and RQM timing chart is shown in Figure 3.

MSR

- 7 **RQM** —Request for Master.
 0 Data Register is not ready.
 1 Data Register is ready.

MSR

- 6 **DIO** —Data Input/Output.
 0 Data transfer is from system to the Data Register.
 1 Data transfer is from Data Register to the system.

MSR

- 5 **EXM** —Execution Mode. (Non-DMA mode only).
 0 Execution phase ended, result phase begun.
 1 Execution phase started.

MSR

- 4 **CB** —Controller (MFDC) Busy.
 0 MFDC is not busy, will accept a command.
 1 MFDC is busy, will not accept a command.

MSR

- 3 **D3B** —Floppy Disk Drive (FDD) 3 Busy.
 0 FDD 3 is not busy, MFDC will accept read or write command.
 1 FDD 3 is busy, MFDC will not accept read or write command.

MSR

- 2 **D2B** —FDD 2 Busy.
 0 FDD 2 is not busy, MFDC will accept read or write command.
 1 FDD 2 is busy, MFDC will not accept read or write command.

MSR

- 1 **D1B** —FDD 1 Busy.
 0 FDD 1 is not busy, MFDC will accept read or write command.
 1 FDD 1 is busy, MFDC will not accept read or write command.

MSR

- 0 **D0B** —FDD 0 Busy.
 0 FDD 0 is not busy, MFDC will accept read or write command.
 1 FDD 0 is busy, MFDC will not accept read or write command.

Status Register 0 (ST0)

7	6	5	4	3	2	1	0
IC		SE	EC	NR	HD	US	
						US1	US0

The Status Register 0 (ST0) as well as the other status registers (ST1-ST3), are available only during the result phase, and may be read only after completing a command. The particular command executed determines which status registers are used and may be read.

ST0

- 7 6 **IC** —Interrupt Code.
 0 0 Normal Termination (NT). Command was properly executed and completed.
 0 1 Abnormal Termination (AT). Command execution was started, but was not successfully completed.
 1 0 Invalid Command (IC). Received command was invalid.
 1 1 Abnormal Termination (AT). The Ready (RDY) signal from the FDD changed state during command execution.

ST0

- 5 **SE** —Seek End.
 0 Seek command is not completed.
 1 Seek command completed by MFDC.

ST0

- 4 **EC** —Equipment Check.
 0 No error.
 1 Either a fault signal is received from the FDD or the track 0 signal failed to occur after 256 step pulses (Recalibrate Command).

Table 1. MFDC Status Register Bit Assignments

Bit Number							
7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B
IC		SE	EC	NR	HD	US	
EN	0	DE	OR	0	ND	NW	MA
0	CM	DD	WT	SH	SN	BT	MD
FLT	WP	RDY	TRK0	TS	HD	US1	US0

Main Status Register (MSR)

Status Register 0 (ST0)

Status Register 1 (ST1)

Status Register 2 (ST2)

Status Register 3 (ST3)

2

Table 2. Command Symbol Description

Symbol	Name	Description
A0	Address Line A0	Controls selection of Main Status Register (A0 = low) or Data Register (A0 = high).
D	Data	The data pattern which is going to be written into a sector.
D0-D7	Data Bus	8-bit data bus, where D0 is the least significant data line and D7 is the most significant data line.
DTL	Data Length	When N is defined as 00, DTL is the number of data bytes to read from or write into the sector.
EOT	End of Track	The final sector number on a track. During read or write operation, the DDFDC stops data transfer after reading from or writing to the sector equal to EOT.
GPL	Gap Length	The length of Gap 3. During read/write commands this value determines the number of bytes that the VCO will stay low after two CRC bytes. During the Format a Track command it determines the size of Gap 3.
H	Head Address	Head number 0 or 1, as specified in ID field.
HD (H)	Head	A selected head number 0 or 1 which controls the polarity of pin 27. (H = HD in all command words).
HLT	Head Load Time	The head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	The head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	When MF = 0, FM mode is selected; and when MF = 1, MFM mode is selected.
MT	Multi-Track	When MT = 1, a multi-track operation is to be performed. After finishing a read/write operation on side 0, the DDFDC will automatically start searching for sector 1 on side 1.
N	Bytes/Sector	The number of data bytes written in a sector.
ND	Non-DMA Mode	When ND = 1, operation is in the Non-DMA mode; when ND = 0, operation is in the DMA mode.
NTN	New Track Number	A new track number, which will be reached as a result of the Seek command. Desired head position.
PTN	Present Track Number	The track number at the completion of Sense Interrupt Status command. Present head position.
R	Record (Sector)	The sector number to be read or written.
R/W	Read/Write	Either read (R) or write (W) signal.
ST	Sectors/Track	The number of sectors per track.
SK	Skip	Skip Deleted Data Address Mark.
SRT	Step Rate Time	The stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (F = 1 ms, E = 2 ms, etc.).
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0 = low). ST0-ST3 may be read only after a command has been executed and contain information relevant to that particular command.
STP	Sector Test Process	During a Scan command, if STP = 01, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA controller); and if STP = 02, then alternate sectors are read and compared.
T	Track Number	The current/selected track number of the medium (0-255).
US0,US1	Unit Select	A selected drive number (0-3).

ST0

- 3 NR —Not Ready.**
 0 FDD is ready.
 1 FDD is not ready at issue of read or write command. If a read or write command is issued to side 1 of a single-sided drive, this bit is also set.

ST0

- 2 HD —Head Address. (At Interrupt).**
 0 Head Select 0.
 1 Head Select 1.

ST0

- 1 0 US —Unit Select. (At Interrupt).**
 0 0 FDD 0 selected.
 0 1 FDD 1 selected.
 1 0 FDD 2 selected.
 1 1 FDD 3 selected.

Status Register 1 (ST1)

7	6	5	4	3	2	1	0
EN	0	DE	OR	0	ND	NW	MA

ST1

- 7 EN —End of Track.**
 0 No error.
 1 MFDC attempted to access a sector beyond the last sector of a track.

ST1

- 6 —Not Used. Always Zero.**

ST1

- 5 DE —Data Error.**
 0 No error.
 1 MFDC detected a CRC error in ID field or the Data field.

ST1

- 4 OR —Over Run.**
 0 No error.
 1 MFDC was not serviced by the system during data transfers, within a predetermined time interval.

ST1

- 3 —Not Used. Always Zero.**

ST1

- 2 ND —No Data.**
 0 No error.
 1 3 possible errors.
 1. MFDC cannot find sector specified in ID Register during execution of Read Data, Write Deleted Data or Scan commands.
 2. MFDC cannot read ID field without an error during Read ID command.
 3. MFDC cannot find starting sector during execution of Read a Track command.

ST1

- 1 NW —Not Writable.**
 0 No error.
 1 MFDC detected a write protect signal from FDD during execution of Write Data, Write Deleted Data or Format a Track commands.

ST1

- 0 MA —Missing Address Mark.**
 0 No error.
 1 2 possible errors.
 1. MFDC cannot detect the ID Address Mark after encountering the index hole twice.
 2. MFDC cannot detect the Data Address Mark or Deleted Data Address Mark. The MD (Missing Address Mark in Data field) of Status Register 2 is also set.

Status Register 2 (ST2)

7	6	5	4	3	2	1	0
0	CM	DD	WT	SH	SN	BT	MD

ST2

- 7 —Not Used. Always Zero.**

ST2

- 6 CM —Control Mark.**
 0 No error.
 1 MFDC encountered a sector which contained a Deleted Data Address Mark during execution of a Read Data, Read a Track, or Scan command, or which contained a Data Address Mark during execution of a Read Deleted Data command.

ST2

- 5 DD —Data Error in Data Field.**
 0 No error.
 1 MFDC detected a CRC error in the Data field.

ST2

- 4 WT —Wrong Track.**
 0 No error.
 1 Contents of T on the disk is different from that stored in IDR. Bit is related to ND (Bit 2) of Status Register 1.

ST2

- 3 SH —Scan Equal Hit.**
 0 No "equal" condition during a scan command.
 1 "Equal" condition satisfied during a scan command.

ST2

- 2 SN —Scan Not Satisfied.**
 0 No error.
 1 MFDC cannot find a sector on the track which meets the scan command condition.

ST2

- 1 BT —Bad Track.**
 0 No error.
 1 Contents of T on the disk is different from that stored in the IDR and T = FF. Bit is related to ND (Bit 2) of Status Register 1.

ST2

- 0 MD —Missing Address Mark in Data Field.**
 0 No error.
 1 MFDC cannot find a Data Address Mark or Deleted Data Address Mark during a data read from the disk.

Status Register 3 (ST3)

7	6	5	4	3	2	1	0
FLT	WP	RDY	TRK0	TS	HD	US1	US0

Status Register 3 (ST3) holds the results of the Sense Drive Status command.

ST3

- 7 FLT —Fault.**
 0 Fault (FLT) signal from the FDD is low.
 1 Fault (FLT) signal from the FDD is high.

ST3

- 6 WP —Write Protect.**
 0 Write Protect (WP) signal from the FDD is low.
 1 Write Protect (WP) signal from the FDD is high.

ST3

- 5 RDY —Ready.**
 0 Ready (RDY) signal from the RDD is low.
 1 Ready (RDY) signal from the FDD is high.

ST3

- 4 TRK0 —Track 0.**
 0 Track 0 (TRK0) signal from the FDD is low.
 1 Track 0 (TRK0) signal is from the FDD is high.

ST3

- 3 TS —Two Side.**
 0 Two Side (TS) signal from the FDD is low.
 1 Two Side (TS) signal from the FDD is high.

ST3

- 2 HD —Head Select.**
 0 Head Select (HD) signal to the FDD is low.
 1 Head Select (HD) signal to the FDD is high.

ST3

- 1 US1 —Unit Select 1.**
 0 Unit Select 1 (US1) signal to the FDD is low.
 1 Unit Select 1 (US1) signal to the FDD is high.

ST3

- 0 US0 —Unit Select 0.**
 0 Unit Select 0 (US0) signal to the FDD is low.
 1 Unit Select 0 (US1) signal to the FDD is high.

COMMAND SEQUENCE

The MFDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer of data from the system. After command execution, the result of the command may be a multi-byte transfer of data back to the system. Because of this multi-byte transfer of information between the MFDC and the system, each command consists of three phases:

Command Phase—The MFDC receives all information required to perform a particular operation from the system.

Execution Phase—The MFDC performs the instructed operation.

Result Phase—After completion of the operation, status and other housekeeping information are made available to the system.

The bytes of data sent to the MFDC to form a command, and read out of the MFDC in the result phase, must occur in the order shown for each command sequence. That is, the command code byte must be sent first followed by the other bytes in the specified sequence. All command bytes must be written and all result bytes must be read in each phase. After the last byte of data in the command phase is received by the MFDC, the execution phase starts. Similarly, when the last byte of data is read out in the result phase, the command is ended and the MFDC is ready to accept a new command. A command can be terminated by asserting the Terminal Count (TC) signal to the MFDC. This ensures that the processor can always get the MFDC's attention even if the command in process hangs up in an abnormal manner.

COMMAND DESCRIPTION

READ DATA

A command set of nine bytes places the MFDC into the Read Data mode. After the Read Data command has been received the MFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID Address Marks and ID fields from the disk. When the current sector number (R) stored in the ID Register (IDR) matches the sector number read from the disk, the MFDC transfers data from the disk Data field to the data bus.

After completion of the read operation from the current sector, the MFDC increments the Sector Number (R) by one, and the data from the next sector is read and output to the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Command terminates after reading the last data byte from sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The Read Data command can also be terminated by a high Terminal Count (TC) signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of TC, the MFDC stops outputting data to the data bus, but continues to read data from the current sector, checks CRC (Cyclic Redundancy Count) bytes, and then at the end of that sector terminates the Read Data command and sets bits 7 and 6 in ST0

to 0. The amount of data which can be handled with a single command to the MFDC depends upon MT (Multi-Track), MF (MFM/FM), and N (Number of Bytes/Sector) values. Table 3 shows the transfer capacity.

The multi-track function (MT) allows the MFDC to read data from both sides of the disk. For a particular track, data is transferred starting at sector 1, side 0 and completed at sector L, side 1 (sector L = last sector on the side). This function pertains to only one track (the same track) on each side of the disk.

When N = 0 in command byte 6 (FM mode), the Data Length (DTL) in command byte 9 defines the data length that the MFDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond the DTL is not sent to the data bus. The MFDC reads (internally) the complete sector, performs the CRC check, and depending upon the manner of command termination, may perform a multi-sector Read operation. When N is non-zero (MFM mode), DTL has no meaning and should be set to FF.

At the completion of the Read Data command, the head is not unloaded until the Head Unload Time (HUT) interval defined in the Specify command has elapsed. The head settling time may be avoided between subsequent reads if the processor issues another command before the head unloads. This time savings is considerable when disk contents are copied from one drive to another.

If the MFDC detects the Index Hole twice in succession without finding the right sector (indicated in R), then the MFDC sets the No Data (ND) flag in Status Register 1 (ST1) to a 1, sets Status Register 0 (ST0) bits 7 and 6 to 0 and 1, respectively, and terminates the Read Data command.

After reading the ID and Data fields in each sector, the MFDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the MFDC sets the Data Error (DE) flag in ST1 to a 1, sets the Data Error in Data Field (DD) flag in ST2 to a 1. If a CRC error occurs in the Data field, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the MFDC reads a Deleted Data Address Mark from the disk, and the Skip Deleted Data Address Mark bit in the first command byte is not set (SK = 0), then the MFDC reads all the data in the sector, sets the Control Mark (CM) flag in ST2 to a 1, and terminates the command. If SK = 1, the MFDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers from the MFDC to the system, the MFDC must be serviced by the system within 27 μ s in the FM mode, and within 13 μ s in the MFM mode, otherwise the MFDC sets the Over Run (OR) flag in ST1 to a 1, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the processor terminates a read (or write) operation in the MFDC, then the ID information in the result phase is dependent upon the state of the MT bit in the first command byte and the End of Track (EOT) byte. Table 4 shows the values for Track Number (T), Head Number (H), Sector Number (R), and Number of Data Bytes/Sector (N), when the processor terminates the command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	0	1	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Table 3. MFDC Transfer Capacity

Multi-Track (MT)	MFM/FM (MF)	Bytes/Sector (N)	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read* from Disk
0	0	00	(128) (16) = 2,048	16 at Side 0
0	1	01	(256) (16) = 4,096	or 16 at Side 1
1	0	00	(128) (32) = 4,096	16 at Side 1
1	1	01	(256) (32) = 8,192	
0	0	01	(256) (9) = 2,304	9 at Side 0
0	1	02	(512) (9) = 4,608	or 9 at Side 1
1	0	01	(256) (18) = 4,608	9 at Side 1
1	1	02	(512) (18) = 9,216	
0	0	02	(512) (5) = 2,560	5 at Side 0
0	1	03	(1024) (5) = 5,120	or 5 at Side 1
1	0	02	(512) (10) = 5,120	8 at Side 1
1	1	03	(1024) (10) = 10,240	

*Note: Typical values are for Sony recommended format.

Table 4. MFDC Command Termination Values

Command Phase ID		Final Sector Transferred to/from Data Bus	Result Phase ID			
Multi-Track (MT)	Head Number (HD)		Track Number (T)	Head Number (H)	Sector Number (R)	No. of Data Bytes (N)
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	T + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	LSB	01	NC

Notes:
 1. NC (No Change): The same value as the one at the beginning of command execution.
 2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DATA

A command set of nine bytes places the MFDC in the Write Data mode. After the Write Data command has been received the MFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID fields from the disk. When the four bytes (T, H, R, N) loaded during the command match the four bytes of the ID field from the disk, the MFDC transfers data from the data bus to the disk Data field.

After writing data into the current sector, the MFDC increments the sector number (R) by one, and writes into the Data field in the next sector. The MFDC continues this multi-sector write operation until the last byte is written to sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The command can also be terminated by a high on Terminal Count (TC). If TC is sent to the MFDC while writing into the current sector, then the remainder of the Data field is filled with 00 (zeros). In this case, ST0 bits 7 and 6 are set to 0 and the command is terminated.

The MFDC reads the ID field of each sector and checks the CRC bytes. If the MFDC detects a read error (incorrect CRC) in one

of the ID fields, it terminates the Write Data command, sets the DE flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

The Write Data command operates in much the same manner as the Read Data command. Refer to the Read Data command for the handling of the following items:

- Transfer Capacity
- End of Track (EN) flag
- No Data (ND) flag
- Head Unload Time (HUT) interval
- ID information when the processor terminates command (see Table 4)
- Definition of Data Length (DTL) when N = 0 and when N ≠ 0

In the Write Data mode, data transfers from the data bus to the MFDC must occur within 27 μs in the FM mode, and within 13 μs in the MFM mode. If the time interval between data transfers is longer than this, then the MFDC terminates the Write Data command, sets the Over Run (OR) flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	0	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DELETED DATA

The Write Deleted Data command is the same as the Write Data command except a Deleted Data Address Mark is written at the beginning of the Data field instead of the normal Data Address Mark.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ DELETED DATA

The Read Deleted Data command is the same as the Read Data command except that if SK = 0 when the MFDC detects a **Data Address Mark** at the beginning of a Data field, it reads all the data in the sector and sets the CM flag in ST2 to a 1, and then terminates the command. If SK = 1, then the MFDC skips the sector with the **Data Address Mark** and reads the next sector.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	1	1	0	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ A TRACK

The Read a Track command is similar to the Read Data command except that this is a continuous read operation where all Data fields from each of the sectors on a track are read and transferred to the data bus. Immediately after encountering the Index Hole, the MFDC starts reading the Data fields as continuous blocks of data. This command terminates when the number of sectors read is equal to EOT. Multi-track operations are not allowed with this command.

If the MFDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The MFDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag in ST1 to a 1 if there is no match.

If the MFDC does not find an ID Address Mark on the disk after it encounters the Index Hole for the second time it terminates the command, sets the Missing Address Mark (MA) flag in ST1 to a 1, and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	SK	0	0	0	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ ID

The two-byte Read ID command returns the present position of the read/write head. The MFDC obtains the value from the first ID field it is able to read, sets bits 7 and 6 in ST0 to 0 and terminates the command.

If no proper ID Address Mark is found on the disk before the Index Hole is encountered for the second time then the Missing Address Mark (MA) flag in ST1 is set to a 1, and if no data is found then the ND flag in ST1 is also set a 1. Bits 7 and 6 in ST0 are set to 0 and 1, respectively and the command is terminated.

During this command there is no data transfer between MFDC and the data bus except during the result phase.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	0	1	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

FORMAT A TRACK

The six-byte Format a Track command formats an entire track. After the Index Hole is detected, data is written on the disk: Gaps, Address Marks, ID fields and Data fields; all are recorded per the format recommended by Sony Corporation. The particular format written is also controlled by the values of Number of Bytes/ Sector (N), Sectors/Track (ST), Gap Length (GPL) and Data Pattern (D) which are supplied by the processor during the command phase. The Data field is filled with the data pattern stored in D.

The ID field for each sector is supplied by the processor in response to four data requests per sector issued by the MFDC. The type of data request depends upon the Non-DMA flag (ND) in the Specify command. In the DMA mode (ND = 0), the MFDC asserts the DMA Request (DRQ) output four times per sector. In the Non-DMA mode (ND = 1), the MFDC asserts Interrupt Request (INT) output four times per sector.

The processor must write one data byte in response to each request, sending (in the consecutive order) the Track Number (T), Head Number (H), Sector Number (R) and Number of Bytes/ Sector (N). This allows the disk to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for T, H, R, and N to the MFDC for each sector on the track. For sequential formatting R is incremented by one after each sector is formatted, thus, R contains the total numbers of sectors formatted when it is read during the result phase. This incrementing and formatting continues for the whole track until the MFDC, upon encountering the Index Hole for the second time, terminates the command and sets bits 7 and 6 in ST0 to 0.

If the Fault (FLT) signal is high from the FDD at the end of a write operation, the MFDC sets the Equipment Check (EC) flag in ST0 to a 1, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command. Also, a low (RDY) signal at the beginning of a command execution phase causes bits 7 and 6 of ST0 to be set to 0 and 1, respectively.

Table 5 shows the relationship between N, ST, and GPL for various disk and sector sizes.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Number of Bytes per Sector (N)							
	4	Sectors per Track (ST)							
	5	Gap Length (GPL)							
	6	Data Pattern (D)							

Table 5. Micro Floppy Disk Sector Size Relationship

Format	Mode	Sector Size Bytes/Sector	No. of Data Bytes/Sector (N)	No. of Sectors/Tracks (ST) ¹	Gap Length (GPL) ¹ Format Command
Sony (Read and Write)	FM	128	00	10	1B
		256	01	09	2A
		512	02	05	3A
	MFM ²	256	01	10	36
		512	02	09	54
		1024	03	05	74
IBM (Read Only)	FM	128	00	0F	1B
		128	00	09	2A
		256	01	04	3A
	MFM ²	256	01	0F	36
		512	02	09	54
		1024	03	04	74

Notes:

1. Values of ST and GPL are hexadecimal.
2. In MFM mode the MFDC cannot perform a read/write/format operation with 128 bytes/sector (N = 00).

Result Phase

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)*
	5	Head Number (H)*
	6	Sector Number (R)*
	7	Number of Data Bytes per Sector (N)*

*The ID information has no meaning in this command.

If conditions for scan are met, the MFDC sets the Scan Hit (SH) flag in ST2 to a 1, and terminates the command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the track (EOT), then the MFDC sets the Scan Not Satisfied (SN) flag in ST2 to a 1, and terminates the command. The receipt of TC from the processor or DMA controller during the scan operation will cause the MFDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6 shows the status of bits SH and SN under various conditions of scan.

If SK = 0 and the MFDC encounters a Deleted Data Address Mark on one of the sectors, it regards that sector as the last sector of the track, sets the Control Mark (CM) bit in ST2 to a 1 and terminates the command. If SK = 1, the MFDC skips the sector with the Deleted Data Address Mark, sets the CM flag to a 1 in order to show that a Deleted Sector has been encountered, and reads the next sector.

SCAN COMMANDS

The scan commands compare data read from the disk to data supplied from the data bus. The MFDC compares the data, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{BUS}$, $D_{FDD} \leq D_{BUS}$, or $D_{FDD} \geq D_{BUS}$ (D = the data pattern in hexadecimal). A magnitude comparison is performed (FF = largest number, 00 = smallest number). The hexadecimal byte of FF either from the bus or from FDD can be used as a mask byte because it always meets the condition of the compare. After a whole sector of data is compared, if the conditions are not met, the sector number is incremented ($R + STP \rightarrow R$), and the scan operation is continued. The scan operation continues until one of the following events occur: the conditions for scan are met (equal, low or equal, or high or equal), the last sector on the track is reached (EOT), or TC is received.

When either the STP sectors are read (contiguous sectors = 01, or alternate sectors = 02) or MT (Multi-Track) is set, the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and the scan command starts reading at sector 21. Sectors 21, 23, and 25 are read, then the next sector (26) is skipped and the Index Hole is encountered before the EOT value of 26 can be read. This results in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the scan command would be completed in a normal manner.

Table 6. Scan Status Codes

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{BUS}$
	1	0	$D_{FDD} \neq D_{BUS}$
Scan Low or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} < D_{BUS}$
	1	0	$D_{FDD} > D_{BUS}$
Scan High or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} > D_{BUS}$
	1	0	$D_{FDD} < D_{BUS}$

During a scan command data is supplied from the data bus for comparison against the data read from the disk. In order to avoid having the Over Run (OR) flag set in ST1, data must be available from the data bus in less than 27 μ s (FM mode) or 13 μ s (MFM mode). If an OR occurs, the MFDC terminates the command and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

The following tables specify the command bytes and describe the result bytes for the three scan commands.

SCAN EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	0	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R		
	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN LOW OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R		
	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN HIGH OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SEEK

The three-byte Seek command steps the FDD read/write head from track to track. The MFDC has two independent Present Track Registers for each drive. They are cleared only by the Recalibrate command. The MFDC compares the Present Track Number (PTN) which is the current head position with the New Track Number (NTN), and if there is a difference, performs the following operation:

If $PTN < NTN$: Sets the direction output (LCT/DIR) high and issues step pulses (FR/STP) to the FDD to cause the read/write head to step in.

If $PTN > NTN$: Sets the direction output (LCT/DIR) low and issues step pulses to the FDD to cause the read/write head step out.

The rate at which step pulses are issued is controlled by the Step Rate Time (SRT) in the Specify command. After each step pulse is issued, NTN is compared against PTN. When $NTN = PTN$, then the Seek End (SE) flag in ST0 is set to a 1, bits 7 and 6 in ST0 are set to 0, and the command is terminated. At this point MFDC asserts INT.

The FDD Busy flag (bit 0-3) in the Main Status Register (MSR) corresponding to the FDD performing the Seek operation is set to a 1.

After command termination, all FDD Busy bits set are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the MFDC sets the Controller Busy (CB) flag in the MSR to 1; but during the execution phase the CB flag is set to 0 to indicate MFDC non-busy. While the MFDC is in the non-busy state, another Seek command may be issued, and in this manner parallel seek operations may be performed on all drives at once.

No command other than Seek will be accepted while the MFDC is sending step pulses to any FDD. If a different command type is attempted, the MFDC will set bits 7 and 6 in ST0 to a 1 and 0, respectively, to indicate an invalid command.

If the FDD is in a not ready state at the beginning of the command execution phase or during the Seek operation, then the MFDC sets the Not Ready (NR) flag in ST0 to a 1, sets ST0 bits 7 and 6 to 0 and 1, respectively, and terminates the command.

If the time to write the three bytes of the Seek command exceeds 150 μ s, the time between the first two step pulses may be shorter than the Step Rate Time (SRT) defined by the Specify command by as much as 1 ms.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	1	1	1
	2	X	X	X	X	X	0	US1	US0
	3	New Track Number (NTN)							

Result Phase: None.

RECALIBRATE

This two-byte command retracts the FDD read/write head to the Track 0 position. The MFDC clears the contents of the PTN counters, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal (TRK0) is low, the direction signal (LCT/DIR) output remains low and step pulses are issued on FR/STP. When TRK0 goes high the MFDC sets the Seek End (SE) flag in ST0 to a 1 and terminates the command. If the TRK0 is still low after 256 step pulses have been issued, the MFDC sets Seek End (SE) and Equipment Check (EC) flags in ST0 to 1s, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the RDY signal, as described in the Seek command, also applies to the Recalibrate command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	1	1
	2	X	X	X	X	X	0	US1	US0

Result Phase: None.

SENSE INTERRUPT STATUS

Interrupt Request (INT) is asserted by the MFDC when any of the following conditions occur:

1. Upon entering the result phase of:
 - a. Read Data command
 - b. Read a Track command
 - c. Read ID command
 - d. Read Deleted Data command
 - e. Write Data command
 - f. Format a Track command
 - g. Write Deleted Data command
 - h. Scan commands
2. Ready (RDY) line from the FDD changes state
3. Seek or Recalibrate command termination
4. During execution phase in the Non-DMA mode

INT caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in Non-DMA mode, bit 5 in the MSR is set to 1. Upon entering result phase this bit is set to 0. Reasons 1 and 4 do not require the Sense Interrupt Status command. The interrupt is cleared by reading or writing data to MFDC. Interrupts caused by reasons 2 and 3 are identified with the aid of the Sense Interrupt Status command. This command resets INT and sets/resets bits 5, 6, and 7 of ST0 to identify the cause of the interrupt. Table 7 defines the seek and interrupt codes.

Neither the Seek or Recalibrate command has a result phase. Therefore, it is mandatory to use the Sense Interrupt Status command after these commands to effectively terminate them and to verify where the head is positioned by checking the Present Track Number (PTN).

Issuing a Sense Interrupt Status command without an interrupt pending is treated as an invalid command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	0	0	0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Present Track Number (PTN)

SPECIFY

The three-byte Specify command sets the initial values for each of the three internal timers. The Head Unload Time (HUT) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (1 = 16 ms, 2 = 32 ms, ... F = 240 ms).

The Step Rate Time (SRT) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, ... 0 = 16 ms.)

The Head Load Time (HLT) defines the time between the Head Load (HDL) signal going high and the start of the read/write operation. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms, ... 7F = 254 ms).

The time intervals are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock. If the clock is reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of two.

The choice of DMA or Non-DMA operation is made by the Non-DMA mode (ND) bit. When this bit = 1 the Non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	0	1	1
	2	SRT				HUT			
	3	HLT							ND

SRT — Step Rate Time
 HUT — Head Unload Time
 HLT — Head Load Time
 ND — Non-DMA mode

Result Phase: None.

Table 7. ST0 Seek and Interrupt Code Definition for Sense Interrupt Status

Status Register 0 (ST0) Bits			Cause
Interrupt Code (IC)		Seek End (SE)	
7	6	5	
1	1	0	RDY line changed state, either polarity
0	0	1	Normal termination of Seek or Recalibrate command
0	1	1	Abnormal termination of Seek or Recalibrate command

SENSE DRIVE STATUS

This two-byte command obtains and reports the status of the FDDs. Status Register 3 (ST3) is returned in the result phase and contains the drive status.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	0	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 3 (ST3)
---	---	-------------------------

INVALID COMMAND

If an invalid command (i.e., a command not previously defined) is received by the MFDC, then the MFDC terminates the command after setting bits 7 and 6 of ST0 to 1 and 0, respectively. The MFDC does not generate an interrupt during this condition. Bits 6 and 7 (DIO and RQM) in the MSR are both set to a 1 indicating to the processor that the MFDC is in the result phase and that ST0 must be read. A hex 80 in ST0 indicates that an invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt, otherwise the MFDC considers the next command to be an invalid command.

In some applications the user may wish to use this command as a No-Op command, to place the MFDC in a standby or no operation state.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	Invalid Codes							

Result Phase:

R	1	Status Register 0 (ST0) = 80
---	---	------------------------------

PROCESSOR INTERFACE

During the command or result phases, the Main Status Register (MSR) must be read by the processor before each byte of information is transferred to, or from, the MFDC Data Register. After each byte of data is written to, or read from, the Data Register, the processor should wait 12 μ s before reading the MSR. Bits 6 and 7 in the MSR must be a 0 and 1, respectively, before each command byte can be written to the MFDC. During the result phase, bits 6 and 7 of the MSR must both be 1s prior to reading each byte from the Data Register onto the data bus. Note that this status reading of bits 6 and 7 of the MSR before each byte transfer to and from the MFDC is required in only the command and result phases and not during the execution phase.

During the result phase all bytes shown in the result phase must be read by the processor. The Read Data command, for example, has seven bytes of data in the result phase. All seven

bytes must be read to successfully complete the Read Data command. The MFDC will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

INTERRUPT REQUEST MODE

During the execution phase, the MSR need not be read. The receipt of each data byte from the FDD is indicated by INT high on pin 18. When the MFDC is in Non-DMA mode, INT is asserted during the execution phase. When the MFDC is in the DMA mode, INT is asserted at the result phase. The INT signal is reset by a read (RD low) or write (WR low) of data to the MFDC. A further explanation of the INT signal is described in the Sense Interrupt Status command on page 16. If the system cannot handle interrupts fast enough (within 13 μ s for MFM mode or 27 μ s for FM mode), it should poll bit 7 (RQM) in the MSR. In this case, RQM in the MSR functions as an Interrupt Request (INT). If the RQM bit is not set, the Over Run (OR) flag in ST1 will be set to a 1 and bits 7 and 6 of ST0 will be set to a 0 and 1, respectively.

DMA MODE

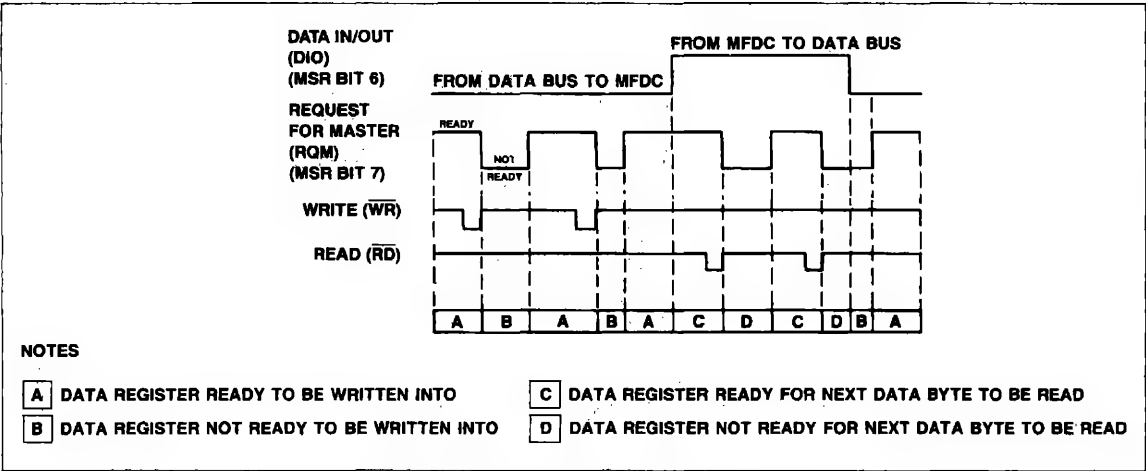
When the MFDC is in the DMA mode (ND = 0 in the third command byte of the Specify command), DRQ (DMA Request) is asserted during the execution phase (rather than INT) to request the transfer of a data byte between the data bus and the MFDC.

During a read command, the MFDC asserts DRQ as each byte of data is available to be read. The DMA controller responds to this request with DACK low (DMA Acknowledge) and RD low (read). When DACK goes low the DMA Request is reset (DRQ low). After the execution phase has been completed (TC high or the EOT sector is read), INT is asserted to indicate the beginning of the result phase. When the first byte of data is read during the result phase, INT is reset low.

During a write command, the MFDC asserts DRQ as each byte of data is required. The DMA controller responds to this request with DACK low (DMA Acknowledge) and WR low (write). When DACK goes low the DMA Request is reset (DRQ low). After the execution phase has been completed (TC high or the EOT sector is written), INT is asserted. This signals the beginning of the result phase. When the first byte of data is read during the result phase, the INT is reset low.

FDD POLLING

After the Specify command has been received by the MFDC, the Unit Select lines (US0 and US1) begin the polling mode. Between commands (and between step pulses in the Seek Command) the MFDC polls all the FDD's looking for a change in the RDY line from any of the drives. If the RDY line changes state (usually due to the door opening or closing) then the MFDC asserts INT. When Status Register 0 (ST0) is read (after Sense Interrupt Status command is issued), Not Ready (NR = 1) will be indicated. The polling of the RDY line by the MFDC occurs continuously between commands, thus notifying the processor which drives are on- or off-line. Each drive is polled every 1.024 ms except during read/write commands.



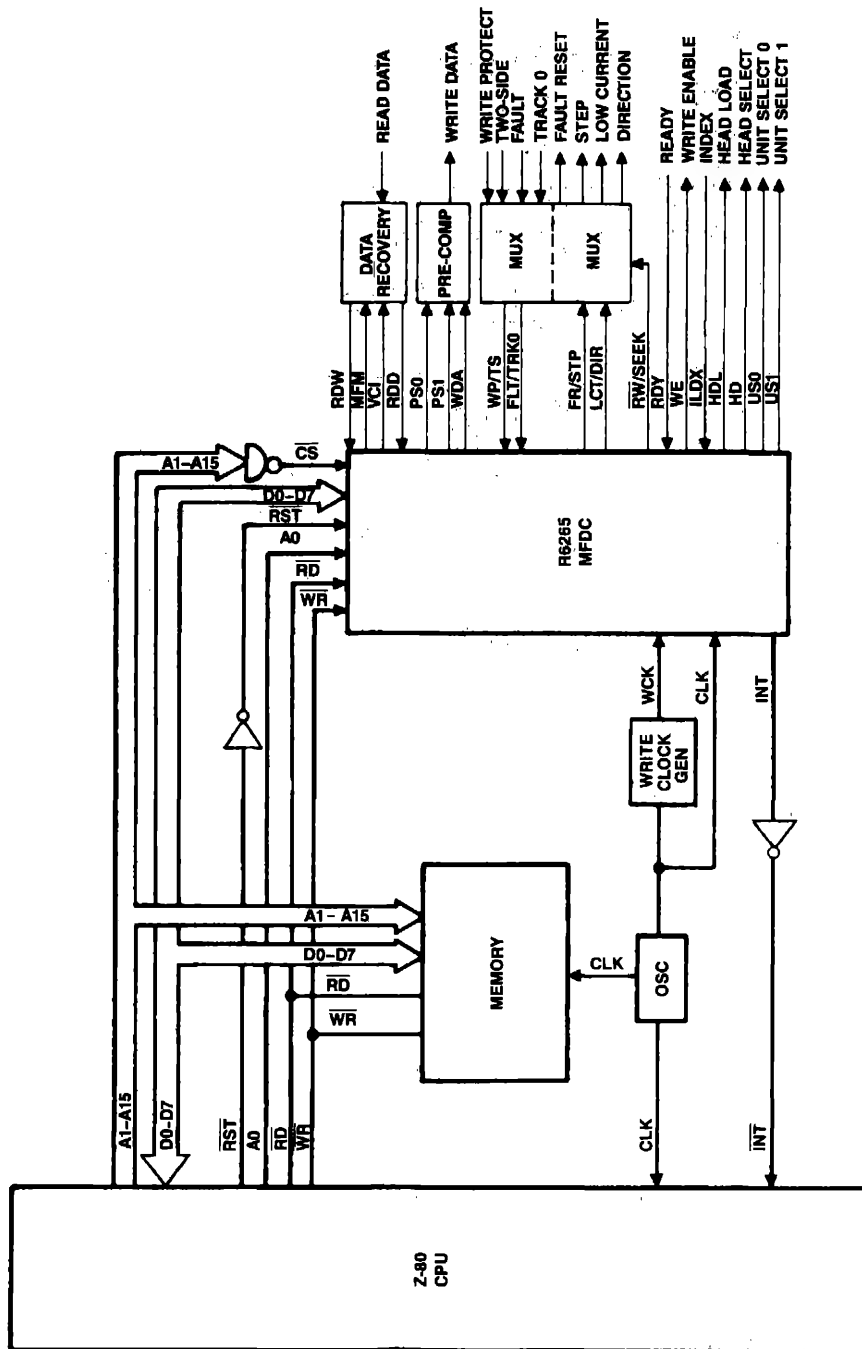


Figure 4. R6265 MFDC Interface to Z-80

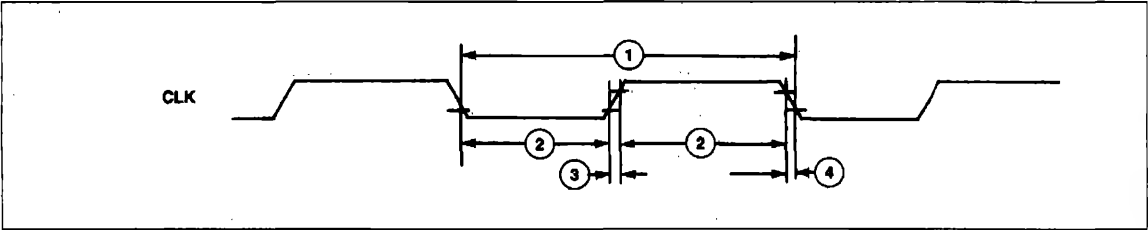


Figure 5. Clock Timing

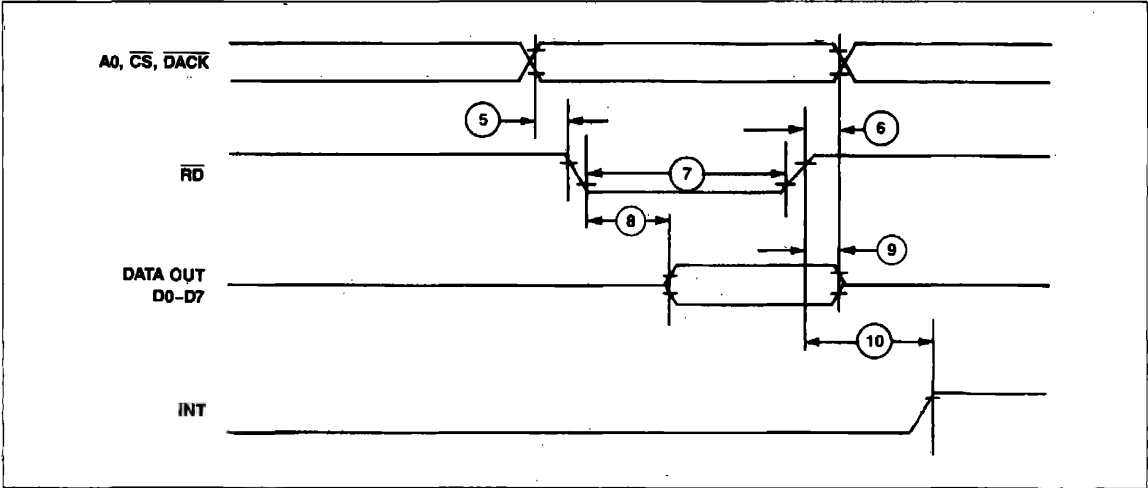


Figure 6. Read Cycle Timing

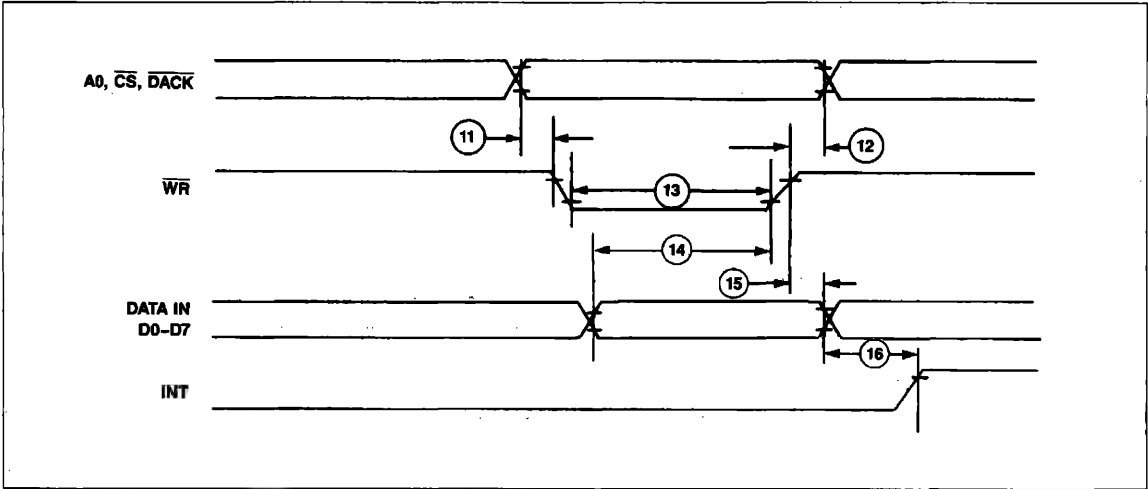


Figure 7. Write Cycle Timing

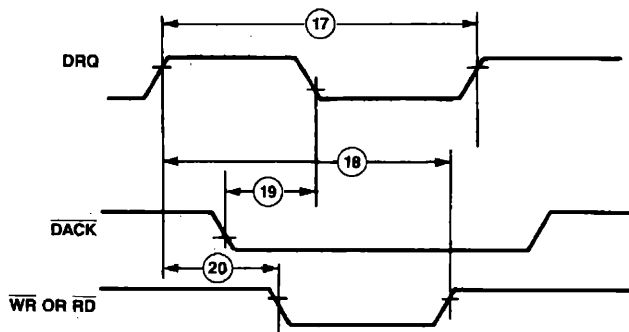


Figure 8. DMA Operation Timing

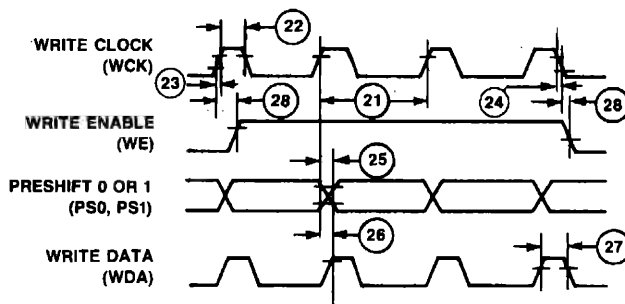
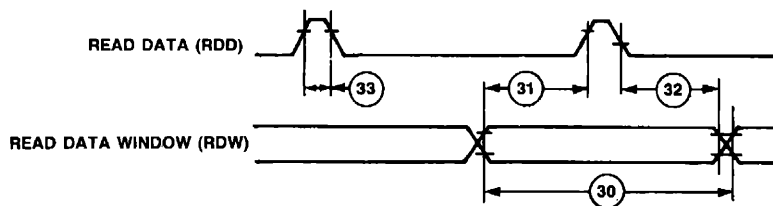


Figure 9. FDD Write Operation Timing



NOTE:
EITHER POLARITY DATA WINDOW IS VALID

Figure 10. FDD Read Operation Timing

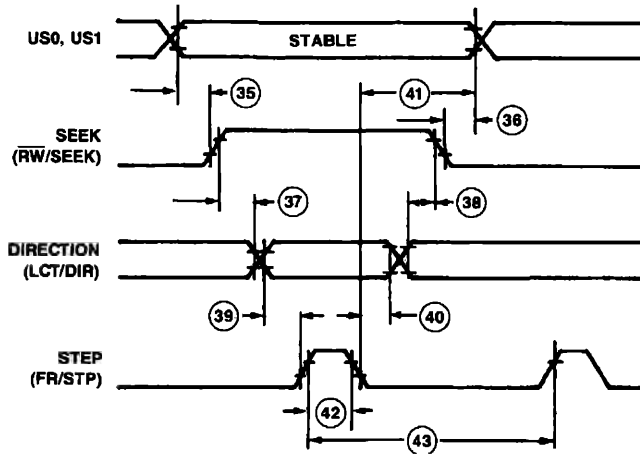


Figure 11. Seek Operation Timing

FAULT RESET
(FR)

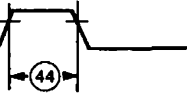


Figure 12. Fault Reset Timing

INDEX
(IDX)

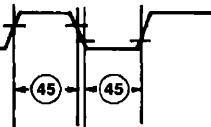


Figure 13. Index Timing

TERMINAL COUNT
(TC)

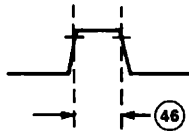


Figure 14. Terminal Count Timing

RESET
(RST)

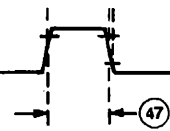
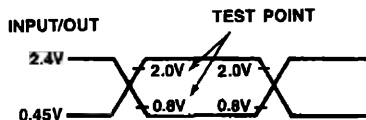
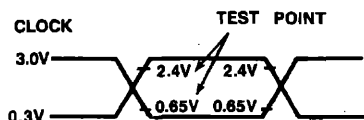


Figure 15. Reset Timing



INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".



CLOCKS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.3V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.4V FOR A LOGIC "1" AND 0.65V FOR A LOGIC "0".

Figure 16. AC Timing Measurement Conditions

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Ref. Fig.	No.	Characteristic	Symbol	Alt. Sym.	Min.	Typ.	Max.	Unit	Test Conditions
5	1	Clock Period	t _{CY}	φ _{CY}	120	125	500	ns	CLK = 8 MHz
	2	Clock High, Low Width	t _{CA}	φ ₀	40	62.5	—	ns	
	3	Clock Rise Time	t _{CLCH}	φ _r	—	—	20	ns	
	4	Clock Fall Time	t _{CHCL}	φ _f	—	—	20	ns	
6	5	A0, CS, DACK Valid to RD Low (Setup)	t _{SLRL}	t _{AR}	0	—	—	ns	C _L = 100 pF
	6	RD High to A0, CS, DACK Invalid (Hold)	t _{RHSH}	t _{RA}	0	—	—	ns	
	7	RD Low Width	t _{RLRH}	t _{RR}	250	—	—	ns	
	8	RD Low to Data Valid (Access)	t _{RLDV}	t _{RD}	—	—	200	ns	
	9	RD High to Output High Z	t _{RHDZ}	t _{DF}	20	—	100	ns	
	10	RD High to INT High	t _{RHHI}	t _{RI}	—	—	500	ns	
	11	A0, CS, DACK Valid to WR Low (Setup)	t _{SLWL}	t _{AW}	0	—	—	ns	
	12	WR High to A0, CS, DACK Invalid (Hold)	t _{WHSH}	t _{WA}	0	—	—	ns	
7	13	WR Low Width	t _{WLWH}	t _{WW}	250	—	—	ns	CLK = 8 MHz
	14	Data Valid to WR High (Setup)	t _{DVWH}	t _{DW}	150	—	—	ns	
	15	WR High to Data Invalid (Hold)	t _{WHDX}	t _{WD}	5	—	—	ns	
	16	WR High to INT High	t _{WHIH}	t _{WI}	—	—	500	ns	
8	17	DRQ Cycle Time	t _{QCY}	t _{MCY}	13	—	—	μs	CLK = 8 MHz
	18	DRQ High to RD, WR High (Response)	t _{QHSH}	t _{MRW}	—	—	12	μs	
	19	DACK Low to DRQ Low (Delay)	t _{ALQL}	t _{AM}	—	—	200	ns	
	20	DRQ High to RD Low (Delay)	t _{QHRL}	t _{MR}	800	—	—	ns	
9		DRQ High to WR Low (Delay)	t _{QHWL}	t _{MW}	250	—	—	ns	CLK = 8 MHz
	21	WCK Cycle Time	t _{KCY}	t _{CY}	—	note 1	—	μs	
	22	WCK High Width	t _{KHKL}	t ₀	80	250	350	ns	
	23	WCK Rise Time	t _{KLKH}	t _r	—	—	20	ns	
	24	WCK Fall Time	t _{KHKL}	t _f	—	—	20	ns	
	25	WCK High to PS0, PS1 Valid (Delay)	t _{KHPV}	t _{CP}	20	—	100	ns	
	26	PS0, PS1 Valid to WDA High (Delay)	t _{PVDH}	t _{CD}	20	—	100	ns	
	27	WDA High Width	t _{DHDL}	t _{WDD}	t _{WCH} - 50	—	—	ns	
10	28	WE High to WCK High or WE Low to WCK Low	t _{EKKH}	t _{WE}	20	—	100	ns	CLK = 8 MHz
	30	RDW Cycle Time	t _{WCY}	t _{WCY}	—	note 2	—	μs	
	31	RDW Valid to RDD High (Setup)	t _{WVRH}	t _{WRD}	15	—	—	ns	
	32	RDD Low to RDW Invalid (Hold)	t _{RLWI}	t _{RDW}	15	—	—	ns	
11	33	RDD High Width	t _{RHRL}	t _{RDD}	40	—	—	ns	CLK = 8 MHz
	35	US0, US1 Valid to SEEK High (Setup)	t _{UVSH}	t _{US}	12	—	—	μs	
	36	SEEK Low to US0, US1 Invalid (Hold)	t _{SLUI}	t _{SU}	15	—	—	μs	
	37	SEEK High to DIR Valid (Setup)	t _{SHDV}	t _{SD}	7	—	—	μs	
	38	DIR Invalid to SEEK Low (Hold)	t _{DXSL}	t _{DS}	30	—	—	μs	
	39	DIR Valid to STP High (Setup)	t _{DVTH}	t _{DST}	1	—	—	μs	
	40	STP Low to DIR Invalid (Hold)	t _{TLDX}	t _{STD}	24	—	—	μs	
	41	STP Low to US0, US1 Invalid (Hold)	t _{TLUX}	t _{STU}	5	—	—	μs	
12	42	STP High Width	t _{THTL}	t _{STP}	6	7	—	μs	CLK = 8 MHz
	43	STP Cycle Time	t _{TCY}	t _{SC}	33 ³	—	note 3	μs	
	44	FR High Width	t _{FHFL}	t _{FR}	8	—	10	μs	
	45	IDX High Width	t _{HIIL}	t _{IDX}	10	—	—	t _{CY}	
13	46	TC High Width	t _{HTL}	t _{TC}	1	—	—	t _{CY}	CLK = 8 MHz
	47	RST High Width	t _{RHRL}	t _{AST}	14	—	—	t _{CY}	

Notes:

1.	MFM	Mini	Standard
	0	4 μs	2 μs
	1	2 μs	1 μs

2. For MFM = 0: Typ. = 2 μs

For MFM = 1: Typ. = 1 μs

3. t_{SC} = 33 μs min. is for different drive units. In the case of the same unit, t_{SC} can range from 1 ms to 16 ms with 8 MHz clock period.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Output Voltage	V_{OUT}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	C°
Storage Temperature Range	T_{STG}	-55 to +150	C°

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Range
V_{CC} Power Supply	5.0V \pm 5%
Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

($V_{CC} = 5.0$ Vdc \pm 5%, $V_{SS} = 0$ Vdc, $T_A = 0^\circ\text{C}$ to 70°C , unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Low Voltage Logic CLK and WCK	V_{IL}	-0.5 -0.5	0.8 0.65	V	
Input High Voltage Logic CLK and WCK	V_{IH}	2.0 2.4	$V_{CC} + 0.5$ $V_{CC} + 0.5$	V	
Output Low Voltage	V_{OL}		0.45	V	$V_{CC} = 4.75\text{V}$, $I_{OL} = 2.0$ mA
Output High Voltage	V_{OH}	2.4	V_{CC}	V	$V_{CC} = 4.75\text{V}$, $I_{OH} = -200$ μA
V_{CC} Supply Current	I_{CC}		150	mA	$V_{CC} = 4.75\text{V}$
Input Load Current All Inputs	I_{IL}		10 -10	μA μA	$V_{IN} = V_{CC}$ $V_{IN} = 0\text{V}$
High Level Output Leakage Current	I_{LOH}		10	μA	$V_{CC} = 0\text{V}$ to 5.25V, $V_{SS} = 0\text{V}$ $V_{OUT} = V_{CC}$
Low Level Output Leakage Current	I_{LOL}		-10	μA	$V_{CC} = 0\text{V}$ to 5.25V, $V_{SS} = 0\text{V}$ $V_{OUT} = +0.45\text{V}$
Internal Power Dissipation	P_{INT}	—	1.0	W	$T_A = 25^\circ\text{C}$

CAPACITANCE

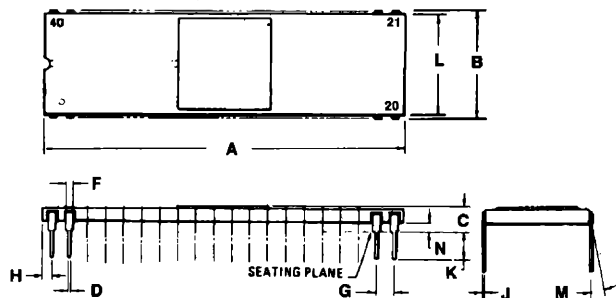
($T_A = 25^\circ\text{C}$; $f_c = 1$ MHz; $V_{CC} = 0\text{V}$)

Parameter	Symbol	Max Limit	Unit
Clock Input	$C_{IN(0)}$	20	pF
Input	C_{IN}	10	pF
Output	C_{OUT}	20	pF

Note: All pins except pin under test tied to ground.

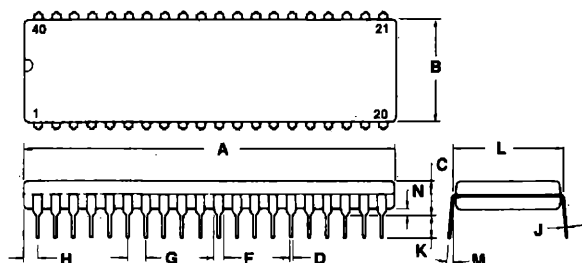
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	-0.53	0.015	0.021
F	0.78	1.40	0.030	0.055
G	2.54	BSC	0.100	BSC
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.38	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24	BSC	0.600	BSC
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040



R6765 DOUBLE-DENSITY FLOPPY DISK CONTROLLER (DDFDC)

2

PRELIMINARY

DESCRIPTION

The R6765 Double-Density Floppy Disk Controller (DDFDC) interfaces up to four floppy disk drives to an 8-bit or 16-bit microprocessor-based system including Z-80, 8080A, 8085A, 8086, and 8088. The DDFDC simplifies the system design by minimizing both the number of external hardware components and software steps needed to implement the floppy disk drive (FDD) interface. Control signals supplied by the DDFDC reduce the number of components required in external phase locked loop and write precompensation circuitry. Memory-mapped registers containing commands, status and data simplify the software interface. Built-in functions reduce the software overhead needed to control the FDD interface. The DDFDC supports both the IBM 3740 Single-Density (FM) and IBM System 34 Double-Density (MFM) formats.

The DDFDC interfaces directly to the synchronous microprocessor bus and operates with 8-bit byte length data transferred on the bus in either DMA or non-DMA mode. In DMA mode, the CPU need only load the command into the DDFDC and all data transfers occur under DMA control. The R6765 is directly compatible with the Z8410/ μ PD8257 Direct Memory Access Controller (DMAC). In non-DMA mode, the DDFDC generates an interrupt to the CPU indicating that a byte of data is available.

Controller commands, command or device status, and data are transferred between the DDFDC and the CPU via six internal registers. The Main Status Register (MSR) stores the DDFDC status information while four additional status registers provide result information to the CPU following each controller command. The Data Register (DR) stores actual disk data, parameters, controller commands and FDD status information for use by the CPU.

The R6765 executes 15 separate multi-byte commands:

Read Data	Specify
Write Data	Format a Track
Read Deleted Data	Scan Equal
Write Deleted Data	Scan High or Equal
Read a Track	Scan Low or Equal
Read ID	Sense Interrupt Status
Seek	Sense Drive Status
Recalibrate (Restore to Track 0)	

FEATURES

- Address mark detection circuitry
- Software control of
 - Track stepping rate
 - Head load time
 - Head unload time
- IBM compatible in both single- and double-density recording formats
- Programmable data record lengths: 128, 256, 512, 1024, 2048, 4096 or 8192 bytes/sector
- Multi-sector and multi-track transfer capability
- Controls up to four floppy disk drives
- Data scan capability—will scan a single sector or an entire track of data fields, comparing on a byte-by-byte basis data in the processor's memory with data read from the disk
- Data transfers in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Directly compatible with an 8-bit or 16-bit synchronous microprocessor bus including Z-80/8080A/8085A, 8086, and 8088
- Replacement for NEC μ PD765A and Intel 8272
- Single phase 4 or 8 MHz Clock
- Single +5 Volt Power Supply

ORDERING INFORMATION

Part Number	Temperature Range
R6765	0°C to 70°C
CLK Frequency: 5 = 4 MHz Blank = 8 MHz	
Package: P = Plastic C = Ceramic	

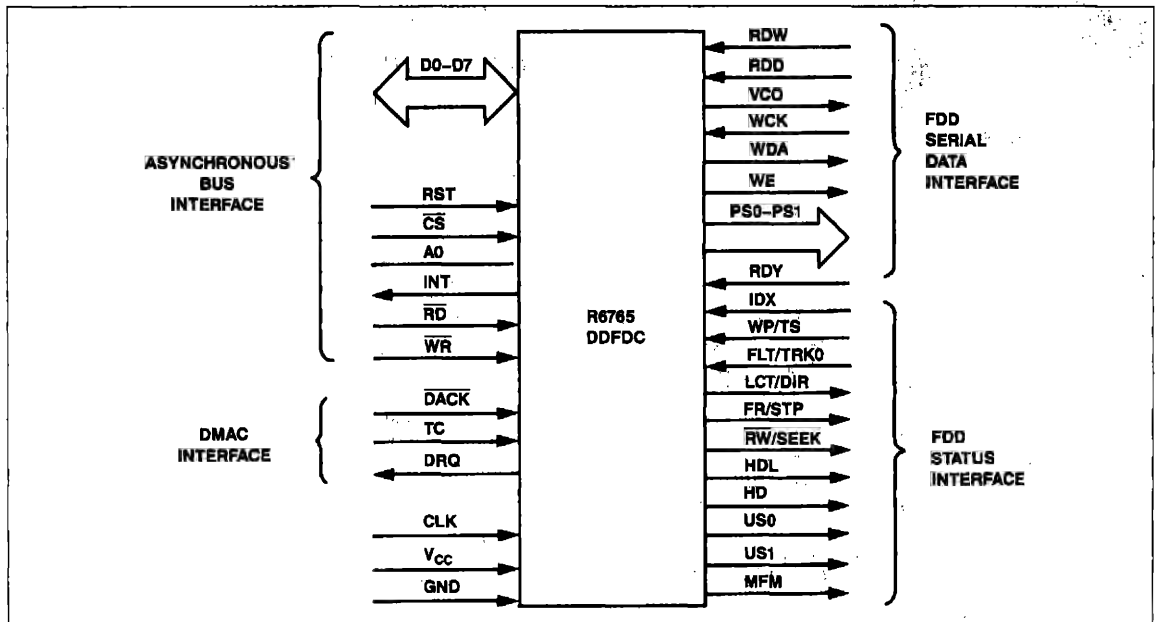


Figure 1. DDFDC Input and Output Signals

PIN DESCRIPTION

Throughout this document signals are presented using the terms active and inactive, or asserted and negated, independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar.

BUS INTERFACE

D0-D7—Data Lines. The bidirectional data lines transfer data between the DDFDC and the 8-bit data bus.

CLK—CLOCK. The clock is a TTL compatible 4 or 8 MHz square wave signal.

RST—RESET. This active high input places the DDFDC in the idle state and resets the output lines to the floppy disk drive (FDD) to the low state.

CS—Chip Select. The DDFDC is selected when the \overline{CS} input is low.

A0—Data/Status Register Select. This input selects the Data or Status Register for reading from or writing to. When $A0 = \text{high}$, the Data Register is selected and the state of \overline{RD} or \overline{WR} determines whether it is a read ($\overline{RD} = \text{low}$) or a write ($\overline{WR} = \text{low}$) operation. When $A0 = \text{low}$, the Status Register is selected. This register may only be read ($\overline{RD} = \text{low}$); the state $\overline{WR} = \text{low}$ is invalid when the Status Register is selected.

INT—Interrupt Request. This active high output is the interrupt request generated by the DDFDC to the CPU. INT is asserted upon completion of some DDFDC commands and before a data byte is transferred between the DDFDC and the data bus (in the Non-DMA mode).

\overline{RD} —Read. This active low input defines the data bus transfer as a read cycle. When low, the data transfer is from the DDFDC to the data bus.

\overline{WR} —Write. This active low input defines the data bus transfer as a write cycle. When low, the data transfer is from the data bus to the DDFDC.

DIRECT MEMORY ACCESS CONTROLLER (DMAC) INTERFACE

DACK—DMA Acknowledge. The DMA transfer acknowledge signal is a TTL compatible input generated by the DMA controller (DMAC) controlling the DDFDC. The DMA cycle is active when DACK is low and the DDFDC is performing a DMA transfer.

DRQ—Data DMA Request. The transfer request signal is a TTL compatible output generated by the DDFDC to request a data transfer operation under control of the DMAC (in the DMA mode). The request is active when $\overline{DRQ} = \text{high}$. The signal is reset inactive when DMA Acknowledge (\overline{DACK}) is asserted (low).

TC—Terminal Count. This input signal is issued to the DDFDC when the DMA transfer for a channel is complete. The signal is active high concurrent with the **DACK** input when the DMA operation is complete as a result of that transfer.

FDD SERIAL DATA INTERFACE

RDD—Read Data. Read Data input from the floppy disk drive (FDD) containing clock and data bits.

RDW—Read Data Window. Data Window input generated by the Phase Locked Loop (PLL) and used to sample data from the FDD.

VCO—Variable Frequency Oscillator Sync. This output signal inhibits the VCO in the PLL circuit when low and enables the VCO in the PLL circuit when high. This inhibits RDD and RDW from being generated until valid data is detected from the FDD.

WCK—Write Clock. This input clock determines the Write Data rate to the FDD. The data rate is 500 KHz in the FM mode (MFM = low) and 1 MHz in the MFM mode (MFM = high). The pulse width is 250 ns (typical) in both modes.

WDA—Write Data. Serial write data output to the FDD containing both clock and data bits.

WE—Write Enable. This output signal enables the Write Data into the FDD when high.

PS0-PS1—Preshift. These outputs are encoded to convey write compensation status during the MFM mode to determine early, late or normal times as follows:

Write Precompensation Status	Preshift Outputs	
	PS0	PS1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

0 = Low, 1 = High

FDD STATUS INTERFACE

RDY—Ready. An active high input signal indicates the FDD is ready to send data to, or receive data from, the DDFDC.

IDX—Index. An active high input signal from the FDD indicates the index hole is under the index sensor. Index is used to synchronize DDFDC timing.

RW/SEEK—Read Write/Seek. Mode selection signal to the FDD which controls the multiplexer from the multiplexed signals. When **RW/SEEK** is low, the Read/Write mode is commanded; when **RW/SEEK** is high, the Seek mode is commanded.

RW/SEEK	Mode	Active FDD Interface Signals
Low	Read/Write	WP, FLT, LCT, FR
High	Seek	TS, TRK0, DIR, STP

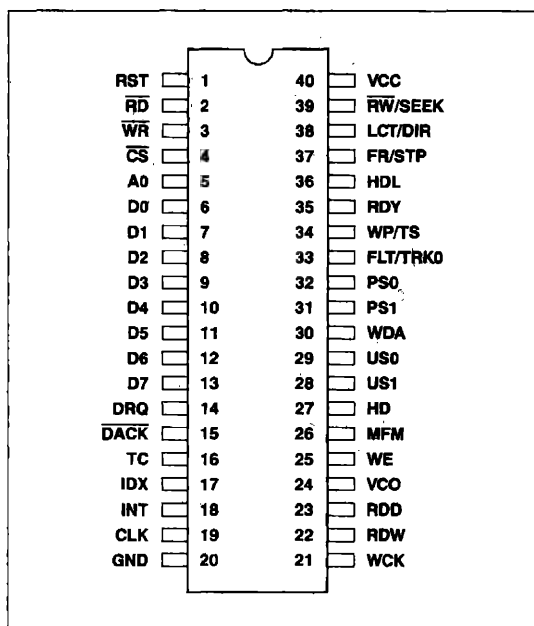
WP/TS—Write Protect/Two Side. An active high multiplexed input signal from the FDD. In the Read/Write mode, **WP/TS** high indicates the media is write-protected. In the Seek mode, **WP/TS** high indicates the media is two-sided.

FLT/TRK0—Fault/Track Zero. An active high multiplexed input from the FDD. In the Read/Write mode (**RW/SEEK** = low), **FLT/TRK0** high indicates an FDD fault. In the Seek mode, **FLT/TRK0** high indicates that the read/write head is positioned over track zero.

LCT/DIR—Low Current/Direction. A multiplexed output to the FDD. In the Read/Write mode, **LCT/DIR** is low when the read/write head is to be positioned over the inner tracks and the **LCT/DIR** is high when the head is to be positioned over the outer tracks. In the Seek mode, **LCT/DIR** controls the head direction. When **LCT/DIR** is high, the head steps to the outside of the disk; when **LCT/DIR** is low, the head steps to the inside of the disk.

FR/STP—Fault Reset/Step. A multiplexed output to the FDD. In the Read/Write mode, **FR/STP** high resets the fault indicator in the FDD. An **FR** pulse is issued at the beginning of each read or write command prior to issuing **HDL**. In the Seek mode, **FR/STP** provides the step pulses to move the read/write head to another track in the direction indicated by the **LCT/DIR** signal.

HDL—Head Load. An active high output to notify the FDD that the read/write head should be loaded (placed in contact with the media). A low level indicates the head should be unloaded.



R6765 DDFDC Pin Diagram

HD—Head Select. An output to the FDD to select the proper read/write head. Head One is selected when HD = high and Head Zero is selected when HD = low.

US0-US1—Unit Select. Output signals for floppy disk drive selection as follows:

Unit Select		Floppy Disk Drive Select
US0	US1	
0	0	0
0	1	1
1	0	2
1	1	3
0 = Low, 1 = High		

MFM—MFM Mode. Output signal to the FDD to indicate MFM or FM mode. Selects the MFM mode when MFM = high and the FM mode when MFM = low.

VCC—Power. +5V dc.

GND—Ground (V_{ss}).

DDFDC REGISTERS

The DDFDC contains six registers which may be accessed by the processor or DMA controller via the system (i.e., micro-processor) bus: a Main Status Register, a Data Register; and four Result Status Registers. The 8-bit Main Status Register (MSR) contains the status information of the DDFDC, and may be accessed at any time. The 8-bit Data Register, consisting of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, parameters and FDD status information. Bytes of data are read out of, or written into, the Data Register in order to initiate a command or to obtain the results of a command execution.

The read-only Main Status Register facilitates the transfer of data between the system and the DDFDC. The other Status Registers (ST0, ST1, ST2 and ST3) are only available during the result phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

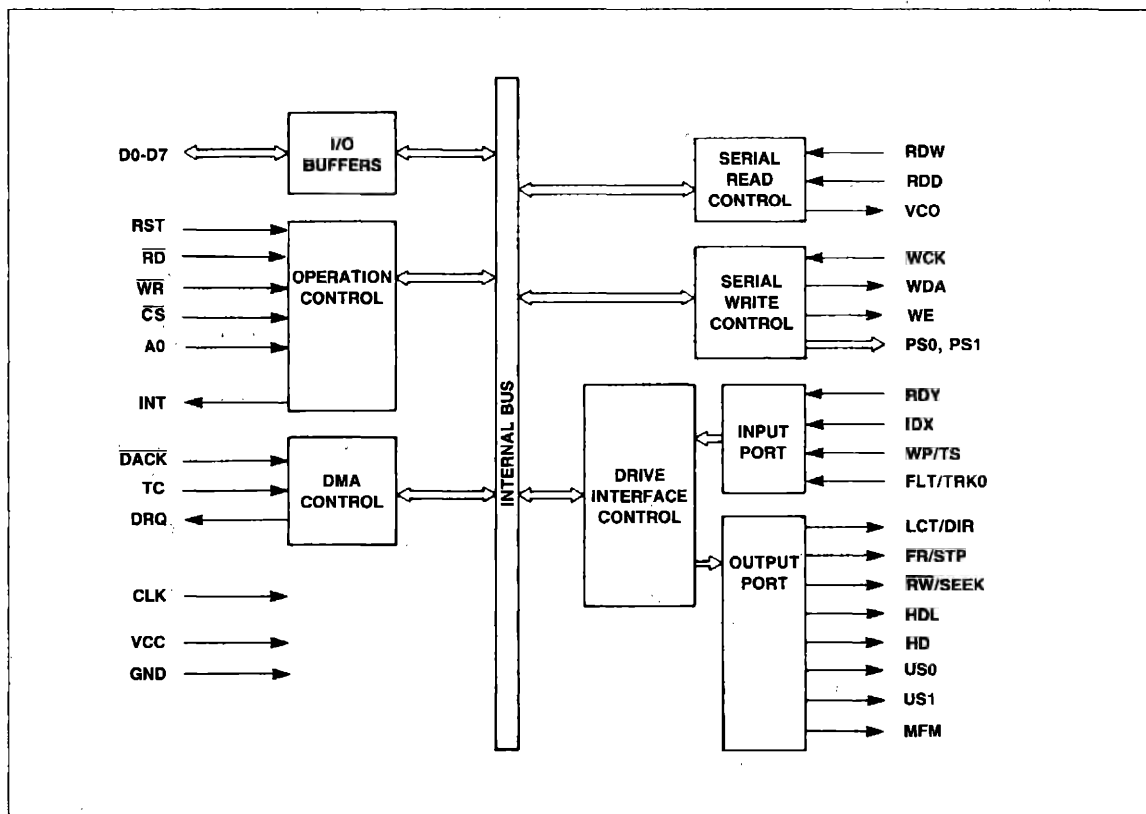


Figure 2. DDFDC Block Diagram

The relationship between the status/data registers and the \overline{WR} , \overline{RD} and A0 signals is shown below.

A0	\overline{RD}	\overline{WR}	Function
0	0	0	Illegal
0	0	1	Read Main Status Register
0	1	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

0 = Low, 1 = High

Table 1 shows each of the status registers used by the DDFDC and each bit assignment within the individual registers. Table 2 defines the symbols used throughout the command definitions. Each register bit symbol is defined in the register descriptions that follow Table 2.

REGISTER DEFINITIONS

Main Status Register (MSR)

7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B

The Main Status Register (MSR) contains the status information of the DDFDC, and must be read by the processor before each byte is written to, or read from, the Data Register during the command or result phase. MSR reads are not required during the execution phase. The Data Input/Output (DIO) and Request for Master (RQM) bits in the MSR indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last \overline{RD} or \overline{WR} during command or result phases and the DIO and RQM getting set or reset is 12 μ s. For this reason, every time the MSR is read the processor should wait 12 μ s. The maximum time from the trailing edge of the last \overline{RD} in the result phase to when bit 4 (DDFDC Busy) goes low is also 12 μ s.

The DIO and RQM timing chart is shown in Figure 3.

MSR

- 7 RQM —Request for Master.**
 0 Data Register is not ready.
 1 Data Register is ready.

MSR

- 6 DIO —Data Input/Output.**
 0 Data transfer is from system to the Data Register.
 1 Data transfer is from Data Register to the system.

MSR

- 5 EXM —Execution Mode. (Non-DMA mode only).**
 0 Execution phase ended, result phase begun.
 1 Execution phase started.

MSR

- 4 CB —Controller (DDFDC) Busy.**
 0 DDFDC is not busy, will accept a command.
 1 DDFDC is busy, will not accept a command.

MSR

- 3 D3B —Floppy Disk Drive (FDD) 3 Busy.**
 0 FDD 3 is not busy, DDFDC will accept read or write command.
 1 FDD 3 is busy, DDFDC will not accept read or write command.

MSR

- 2 D2B —FDD 2 Busy.**
 0 FDD 2 is not busy, DDFDC will accept read or write command.
 1 FDD 2 is busy, DDFDC will not accept read or write command.

MSR

- 1 D1B —FDD 1 Busy.**
 0 FDD 1 is not busy, DDFDC will accept read or write command.
 1 FDD 1 is busy, DDFDC will not accept read or write command.

MSR

- 0 D0B —FDD 0 Busy.**
 0 FDD 0 is not busy, DDFDC will accept read or write command.
 1 FDD 0 is busy, DDFDC will not accept read or write command.

Status Register 0 (ST0)

7	6	5	4	3	2	1	0
IC		SE	EC	NR	HD	US	
						US1	US0

The Status Register 0 (ST0) as well as the other status registers (ST1-ST3), are available only during the result phase, and may be read only after completing a command. The particular command executed determines which status registers are used and may be read.

ST0

- 7 6 IC —Interrupt Code.**
 0 0 Normal Termination (NT). Command was properly executed and completed.
 0 1 Abnormal Termination (AT). Command execution was started, but was not successfully completed.
 1 0 Invalid Command (IC). Received command was invalid.
 1 1 Abnormal Termination (AT). The Ready (RDY) signal from the FDD changed state during command execution.

ST0

- 5 SE —Seek End.**
 0 Seek command is not completed.
 1 Seek command completed by DDFDC.

ST0

- 4 EC —Equipment Check.**
 0 No error.
 1 Either a fault signal is received from the FDD or the track 0 signal failed to occur after 256 step pulses (Recalibrate command).

Table 1. DDFDC Status Register Bit Assignments

Main Status Register (MSR)

Status Register 0 (ST0)

Status Register 1 (ST1)

Status Register 2 (ST2)

Status Register 3 (ST3)

Bit Number							
7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B
IC		SE	EC	NR	HD	US	
EN	0	DE	OR	0	ND	NW	MA
0	CM	DD	WT	SH	SN	BT	MD
FLT	WP	RDY	TRK0	TS	HD	US1	US0

Table 2. Command Symbol Description

Symbol	Name	Description
A0	Address Line A0	Controls selection of Main Status Register (A0 = low) or Data Register (A0 = high).
D	Data	The data pattern which is going to be written into a sector.
D0-D7	Data Bus	8-bit data bus, where D0 is the least significant data line and D7 is the most significant data line.
DTL	Data Length	When N is defined as 00, DTL is the number of data bytes to read from or write into the sector.
EOT	End of Track	The final sector number on a track. During read or write operation, the DDFDC stops data transfer after reading from or writing to the sector equal to EOT.
GPL	Gap Length	The length of Gap 3. During read/write commands this value determines the number of bytes that the VCO will stay low after two CRC bytes. During the Format a Track command it determines the size of Gap 3.
H	Head Address	Head number 0 or 1, as specified in ID field.
HD (H)	Head	A selected head number 0 or 1 which controls the polarity of pin 27. (H = HD in all command words).
HLT	Head Load Time	The head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	The head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	When MF = 0, FM mode is selected; and when MF = 1, MFM mode is selected.
MT	Multi-Track	When MT = 1, a multi-track operation is to be performed. After finishing a read/write operation on side 0, the DDFDC will automatically start searching for sector 1 on side 1.
N	Bytes/Sector	The number of data bytes written in a sector.
ND	Non-DMA Mode	When ND = 1, operation is in the Non-DMA mode; when ND = 0, operation is in the DMA mode.
NTN	New Track Number	A new track number, which will be reached as a result of the Seek command. Desired head position.
PTN	Present Track Number	The track number at the completion of Sense Interrupt Status command. Present head position.
R	Record (Sector)	The sector number to be read or written.
R/W	Read/Write	Either read (R) or write (W) signal.
ST	Sectors/Track	The number of sectors per track.
SK	Skip	Skip Deleted Data Address Mark.
SRT	Step Rate Time	The stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0 = low). ST0-ST3 may be read only after a command has been executed and contain information relevant to that particular command.
STP	Sector Test Process	During a Scan command, if STP = 01, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA controller); and if STP = 02, then alternate sectors are read and compared.
T	Track Number	The current/selected track number of the medium (0-255).
US0,US1	Unit Select	A selected drive number (0-3).

ST0

- 3 NR —Not Ready.**
 0 FDD is ready.
 1 FDD is not ready at issue of read or write command. If a read or write command is issued to side 1 of a single-sided drive, this bit is also set.

ST0

- 2 HD —Head Address. (At Interrupt).**
 0 Head Select 0.
 1 Head Select 1.

ST0

- 1 0 US —Unit Select. (At Interrupt).**
 0 0 FDD 0 selected.
 0 1 FDD 1 selected.
 1 0 FDD 2 selected.
 1 1 FDD 3 selected.

Status Register 1 (ST1)

7	6	5	4	3	2	1	0
EN	0	DE	OR	0	ND	NW	MA

ST1

- 7 EN —End of Track.**
 0 No error.
 1 DDFDC attempted to access a sector beyond the last sector of a track.

ST1

- 6 —Not Used. Always Zero.**

ST1

- 5 DE —Data Error.**
 0 No error.
 1 DDFDC detected a CRC error in ID field or the Data field.

ST1

- 4 OR —Over Run.**
 0 No error.
 1 DDFDC was not serviced by the system during data transfers, within a predetermined time interval.

ST1

- 3 —Not Used. Always Zero.**

ST1

- 2 ND —No Data.**
 0 No error.
 1 3 possible errors.
 1. DDFDC cannot find sector specified in ID Register during execution of Read Data, Write Deleted Data or Scan commands.
 2. DDFDC cannot read ID field without an error during Read ID command.
 3. DDFDC cannot find starting sector during execution of Read a Track command.

ST1

- 1 NW —Not Writable.**
 0 No error.
 1 DDFDC detected a write protect signal from FDD during execution of Write Data, Write Deleted Data or Format a Track commands.

ST1

- 0 MA —Missing Address Mark.**
 0 No error.
 1 2 possible errors.
 1. DDFDC cannot detect the ID Address Mark after encountering the index hole twice.
 2. DDFDC cannot detect the Data Address Mark or Deleted Data Address Mark. The MD (Missing Address Mark in Data field) of Status Register 2 is also set.

Status Register 2 (ST2)

7	6	5	4	3	2	1	0
0	CM	DD	WT	SH	SN	BT	MD

ST2

- 7 —Not Used. Always Zero.**

ST2

- 6 CM —Control Mark.**
 0 No error.
 1 DDFDC encountered a sector which contained a Deleted Data Address Mark during execution of a Read Data, Read a Track, or Scan command, or which contained a Data Address Mark during execution of a Read Deleted Data command.

ST2

- 5 DD —Data Error in Data Field.**
 0 No error.
 1 DDFDC detected a CRC error in the Data field.

ST2

- 4 WT —Wrong Track.**
 0 No error.
 1 Contents of T on the disk is different from that stored in IDR. Bit is related to ND (Bit 2) of Status Register 1.

ST2

- 3 SH —Scan Equal Hit.**
 0 No "equal" condition during a scan command.
 1 "Equal" condition satisfied during a scan command.

ST2

- 2 SN —Scan Not Satisfied.**
 0 No error.
 1 DDFDC cannot find a sector on the track which meets the scan command condition.

ST2

- 1 BT —Bad Track.**
 0 No error.
 1 Contents of T on the disk is different from that stored in the IDR and T = FF. Bit is related to ND (Bit 2) of Status Register 1.

ST2

- 0 MD —Missing Address Mark in Data Field.**
 0 No error.
 1 DDFDC cannot find a Data Address Mark or Deleted Data Address Mark during a data read from the disk.

Status Register 3 (ST3)

7	6	5	4	3	2	1	0
FLT	WP	RDY	TRK0	TS	HD	US1	US0

Status Register 3 (ST3) holds the results of the Sense Drive Status command.

ST3

- 7 FLT —Fault.**
 0 Fault (FLT) signal from the FDD is low.
 1 Fault (FLT) signal from the FDD is high.

ST3

- 6 WP —Write Protect.**
 0 Write Protect (WP) signal from the FDD is low.
 1 Write Protect (WP) signal from the FDD is high.

ST3

- 5 RDY —Ready.**
 0 Ready (RDY) signal from the FDD is low.
 1 Ready (RDY) signal from the FDD is high.

ST3

- 4 TRK0 —Track 0.**
 0 Track 0 (TRK0) signal from the FDD is low.
 1 Track 0 (TRK0) signal is from the FDD is high.

ST3

- 3 TS —Two Side.**
 0 Two Side (TS) signal from the FDD is low.
 1 Two Side (TS) signal from the FDD is high.

ST3

- 2 HD —Head Select.**
 0 Head Select (HD) signal to the FDD is low.
 1 Head Select (HD) signal to the FDD is high.

ST3

- 1 US1 —Unit Select 1.**
 0 Unit Select 1 (US1) signal to the FDD is low.
 1 Unit Select 1 (US1) signal to the FDD is high.

ST3

- 0 US0 —Unit Select 0.**
 0 Unit Select 0 (US0) signal to the FDD is low.
 1 Unit Select 0 (US1) signal to the FDD is high.

COMMAND SEQUENCE

The DDFDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer of data from the system. After command execution, the result of the command may be a multi-byte transfer of data back to the system. Because of this multi-byte transfer of information between the DDFDC and the system, each command consists of three phases:

Command Phase—The DDFDC receives all information required to perform a particular operation from the system.

Execution Phase—The DDFDC performs the instructed operation.

Result Phase—After completion of the operation, status and other housekeeping information are made available to the system.

The bytes of data sent to the DDFDC to form a command, and read out of the DDFDC in the result phase, must occur in the order shown for each command sequence. That is, the command code byte must be sent first followed by the other bytes in the specified sequence. All command bytes must be written and all result bytes must be read in each phase. After the last byte of data in the command phase is received by the DDFDC, the execution phase starts. Similarly, when the last byte of data is read out in the result phase, the command is ended and the DDFDC is ready to accept a new command. A command can be terminated by asserting the Terminal Count (TC) signal to the DDFDC. This ensures that the processor can always get the DDFDC's attention even if the command in process hangs up in an abnormal manner.

COMMAND DESCRIPTION**READ DATA**

A command set of nine bytes places the DDFDC into the Read Data mode. After the Read Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID Address Marks and ID fields from the disk. When the current sector number (R) stored in the ID Register (IDR) matches the sector number read from the disk, the DDFDC transfers data from the disk Data field to the data bus.

After completion of the read operation from the current sector, the DDFDC increments the Sector Number (R) by one, and the data from the next sector is read and output to the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Command terminates after reading the last data byte from sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The Read Data command can also be terminated by a high Terminal Count (TC) signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of TC, the DDFDC stops outputting data to the data bus, but continues to read data from the current sector, checks CRC (Cyclic Redundancy Count) bytes, and then at the end of that sector terminates the Read Data command and sets bits 7 and 6 in ST0

to 0. The amount of data which can be handled with a single command to the DDFDC depends upon MT (Multi-Track), MF (MFM/FM), and N (Number of Bytes/Sector) values. Table 3 shows the transfer capacity.

The multi-track function (MT) allows the DDFDC to read data from both sides of the disk. For a particular track, data is transferred starting at sector 1, side 0 and completed at sector L, side 1 (sector L = last sector on the side). This function pertains to only one track (the same track) on each side of the disk.

When N = 0 in command byte 6 (FM mode), the Data Length (DTL) in command byte 9 defines the data length that the DDFDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond the DTL is not sent to the data bus. The DDFDC reads (internally) the complete sector, performs the CRC check, and depending upon the manner of command termination, may perform a multi-sector Read operation. When N is non-zero (MFM mode), DTL has no meaning and should be set to FF.

At the completion of the Read Data command, the head is not unloaded until the Head Unload Time (HUT) interval defined in the Specify command has elapsed. The head settling time may be avoided between subsequent reads if the processor issues another command before the head unloads. This time savings is considerable when disk contents are copied from one drive to another.

If the DDFDC detects the Index Hole twice in succession without finding the right sector (indicated in R), then the DDFDC sets the No Data (ND) flag in Status Register 1 (ST1) to a 1, sets Status Register 0 (ST0) bits 7 and 6 to 0 and 1, respectively, and terminates the Read Data command.

After reading the ID and Data fields in each sector, the DDFDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the DDFDC sets the Data Error (DE) flag in ST1 to a 1, sets the Data Error in Data Field (DD) flag in ST2 to a 1 if a CRC error occurs in the Data field, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the DDFDC reads a **Deleted Data Address Mark** from the disk, and the Skip Deleted Data Address Mark bit in the first command byte is not set (SK = 0), then the DDFDC reads all the data in the sector, sets the Control Mark (CM) flag in ST2 to a 1, and terminates the command. If SK = 1, the DDFDC skips the sector with the **Deleted Data Address Mark** and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers from the DDFDC to the system, the DDFDC must be serviced by the system within 27 μ s in the FM mode, and within 13 μ s in the MFM mode, otherwise the DDFDC sets the Over Run (OR) flag in ST1 to a 1, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the processor terminates a read (or write) operation in the DDFDC, then the ID information in the result phase is dependent upon the state of the MT bit in the first command byte and the End of Track (EOT) byte. Table 4 shows the values for Track Number (T), Head Number (H), Sector Number (R), and Number of Data Bytes/Sector (N), when the processor terminates the command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	0	1	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Table 3. DDFDC Transfer Capacity

Multi-Track (MT)	MFM/FM (MF)	Bytes/Sector (N)	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Disk
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 4. DDFDC Command Termination Values

Command Phase ID		Final Sector Transferred to/from Data Bus	Result Phase ID			
Multi-Track (MT)	Head Number (HD)		Track Number (T)	Head Number (H)	Sector Number (R)	No. of Data Bytes (N)
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	T + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	LSB	01	NC

Notes:
 1. NC (No Change): The same value as the one at the beginning of command execution.
 2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DATA

A command set of nine bytes places the DDFDC in the Write Data mode. After the Write Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID fields from the disk. When the four bytes (T, H, R, N) loaded during the command match the four bytes of the ID field from the disk, the DDFDC transfers data from the data bus to the disk Data field.

After writing data into the current sector, the DDFDC increments the sector number (R) by one, and writes into the Data field in the next sector. The DDFDC continues this multi-sector write operation until the last byte is written to sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The command can also be terminated by a high on Terminal Count (TC). If TC is sent to the DDFDC while writing into the current sector, then the remainder of the Data field is filled with 00 (zeros). In this case, ST0 bits 7 and 6 are set to 0 and the command is terminated.

The DDFDC reads the ID field of each sector and checks the CRC bytes. If the DDFDC detects a read error (incorrect CRC)

in one of the ID fields, it terminates the Write Data command, sets the DE flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

The Write Data command operates in much the same manner as the Read Data command. Refer to the Read Data command for the handling of the following items:

- Transfer Capacity
- End of Track (EN) flag
- No Data (ND) flag
- Head Unload Time (HUT) interval
- ID information when the processor terminates command (see Table 4)
- Definition of Data Length (DTL) when N = 0 and when N ≠ 0

In the Write Data mode, data transfers from the data bus to the DDFDC must occur within 27 μs in the FM mode, and within 13 μs in the MFM mode. If the time interval between data transfers is longer than this, then the DDFDC terminates the Write Data command, sets the Over Run (OR) flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	0	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DELETED DATA

The Write Deleted Data command is the same as the Write Data command except a Deleted Data Address Mark is written at the beginning of the Data field instead of the normal Data Address Mark.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ DELETED DATA

The Read Deleted Data command is the same as the Read Data command except that if SK = 0 when the DDFDC detects a **Data Address Mark** at the beginning of a Data field, it reads all the data in the sector and sets the CM flag in ST2 to a 1, and then terminates the command. If SK = 1, then the DDFDC skips the sector with the **Data Address Mark** and reads the next sector.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	1	1	0	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ A TRACK

The Read a Track command is similar to the Read Data command except that this is a continuous read operation where all Data fields from each of the sectors on a track are read and transferred to the data bus. Immediately after encountering the Index Hole, the DDFDC starts reading the Data fields as continuous blocks of data. This command terminates when the number of sectors read is equal to EOT. Multi-track operations are not allowed with this command.

If the DDFDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The DDFDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag in ST1 to a 1 if there is no match.

If the DDFDC does not find an ID Address Mark on the disk after it encounters the Index Hole for the second time it terminates the command, sets the Missing Address Mark (MA) flag in ST1 to a 1, and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	SK	0	0	0	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ ID

The two-byte Read ID command returns the present position of the read/write head. The DDFDC obtains the value from the first ID field it is able to read, sets bits 7 and 6 in ST0 to 0 and terminates the command.

If no proper ID Address Mark is found on the disk before the Index Hole is encountered for the second time then the Missing Address Mark (MA) flag in ST1 is set to a 1, and if no data is found then the ND flag in ST1 is also set to a 1. Bits 7 and 6 in ST0 are set to 0 and 1, respectively and the command is terminated.

During this command there is no data transfer between DDFDC and the data bus except during the result phase.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	0	1	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

FORMAT A TRACK

The six-byte Format a Track command formats an entire track. After the Index Hole is detected, data is written on the disk: Gaps, Address Marks, ID fields and Data fields; all are recorded in either the double-density IBM System 34 format (MF = 1) or the single-density IBM 3740 format (MF = 0). The particular format written is also controlled by the values of Number of Bytes/Sector (N), Sectors/Track (ST), Gap Length (GPL) and Data Pattern (D) which are supplied by the processor during the command phase. The Data field is filled with the data pattern stored in D.

The ID field for each sector is supplied by the processor in response to four data requests per sector issued by the DDFDC. The type of data request depends upon the Non-DMA flag (ND) in the Specify command. In the DMA mode (ND = 0), the DDFDC asserts the DMA Request (DRQ) output four times per sector. In the Non-DMA mode (ND = 1), the DDFDC asserts Interrupt Request (INT) output four times per sector.

The processor must write one data byte in response to each request, sending (in the consecutive order) the Track Number (T), Head Number (H), Sector Number (R) and Number of Bytes/Sector (N). This allows the disk to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for T, H, R, and N to the DDFDC for each sector on the track. For sequential formatting R is incremented by one after each sector is formatted, thus, R contains the total numbers of sectors formatted when it is read during the result phase. This incrementing and formatting continues for the whole track until the DDFDC, upon encountering the Index Hole for the second time, terminates the command and sets bits 7 and 6 in ST0 to 0.

If the Fault (FLT) signal is high from the FDD at the end of a write operation, the DDFDC sets the Equipment Check (EC) flag in ST0 to a 1, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command. Also, a low (RDY) signal at the beginning of a command execution phase causes bits 7 and 6 of ST0 to be set to 0 and 1, respectively.

Table 5 shows the relationship between N, ST, and GPL for various disk and sector sizes.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Number of Bytes per Sector (N)							
	4	Sectors per Track (ST)							
	5	Gap Length (GPL)							
	6	Data Pattern (D)							

Table 5. Standard Floppy Disk Sector Size Relationship

Disk Size	Mode	Sector Size Bytes/Sector	No. of Data Bytes/Sector (N)	No. of Sectors/Tracks (ST)	Gap Length (GPL) ⁴		Remarks
					Read/Write Command ¹	Format Command ²	
8"	FM	128	00	1A	07	1B	IBM Disk 1
		256	01	0F	0E	2A	IBM Disk 2
		512	02	08	1B	3A	
		1024	03	04	47	8A	
		2048	04	02	C8	FF	
		4096	05	01	C8	FF	
	MFM ³	256	01	1A	0E	36	IBM Disk 2D
		512	02	0F	1B	54	
		1024	03	08	35	74	IBM Disk 2D
		2048	04	04	99	FF	
		4096	05	02	C8	FF	
		8192	06	01	C8	FF	
5¼"	FM	128	00	12	07	09	
		128	00	10	10	19	
		256	01	08	18	30	
		512	02	04	46	87	
		1024	03	02	C8	FF	
		2048	04	01	C8	FF	
	MFM ³	256	01	12	0A	0C	
		256	01	10	20	32	
		512	02	08	2A	50	
		1024	03	04	80	F0	
		2048	04	02	C8	FF	
		4096	05	01	C8	FF	

Notes:

1. Suggested values of GPL in Read or Write commands to avoid overlapping between Data field and ID field of contiguous sections.
2. Suggested values of GPL in Format a Track command.
3. In MFM mode the DDFDC cannot perform a read/write/format operation with 128 bytes/sector (N = 00).
4. Values of ST and GPL are in hexadecimal.

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)*
	5	Head Number (H)*
	6	Sector Number (R)*
	7	Number of Data Bytes per Sector (N)*

* The ID information has no meaning in this command.

the sector number is incremented ($R + STP - R$), and the scan operation is continued. The scan operation continues until one of the following events occur: the conditions for scan are met (equal, low or equal, or high or equal), the last sector on the track is reached (EOT), or TC is received.

If conditions for scan are met, the DDFDC sets the Scan Hit (SH) flag in ST2 to a 1, and terminates the command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the track (EOT), then the DDFDC sets the Scan Not Satisfied (SN) flag in ST2 to a 1, and terminates the command. The receipt of TC from the processor or DMA controller during the scan operation will cause the DDFDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6 shows the status of bits SH and SN under various conditions of scan.

If SK = 0 and the DDFDC encounters a Deleted Data Address Mark on one of the sectors, it regards that sector as the last sector of the track, sets the Control Mark (CM) bit in ST2 to a 1 and terminates the command. If SK = 1, the DDFDC skips the sector with the Deleted Data Address Mark, sets the CM flag to a 1 in order to show that a Deleted Sector has been encountered, and reads the next sector.

SCAN COMMANDS

The scan commands compare data read from the disk to data supplied from the data bus. The DDFDC compares the data, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{BUS}$, $D_{FDD} \leq D_{BUS}$, or $D_{FDD} \geq D_{BUS}$ (D = the data pattern in hexadecimal). A magnitude comparison is performed (FF = largest number, 00 = smallest number). The hexadecimal byte of FF either from the bus or from FDD can be used as a mask byte because it always meets the condition of the compare. After a whole sector of data is compared, if the conditions are not met,

Table 6. Scan Status Codes

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{BUS}$
	1	0	$D_{FDD} \neq D_{BUS}$
Scan Low or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} < D_{BUS}$
	1	0	$D_{FDD} > D_{BUS}$
Scan High or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} > D_{BUS}$
	1	0	$D_{FDD} < D_{BUS}$

When either the STP sectors are read (contiguous sectors = 01, or alternate sectors = 02) or MT (Multi-Track) is set, the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and the scan command starts reading at sector 21. Sectors 21, 23, and 25 are read, then the next sector (26) is skipped and the Index Hole is encountered before the EOT value of 26 can be read. This results in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the scan command would be completed in a normal manner.

During a scan command data is supplied from the data bus for comparison against the data read from the disk. In order to avoid having the Over Run (OR) flag set in ST1, data must be available from the data bus in less than 27 μ s (FM mode) or 13 μ s (MFM mode). If an OR occurs, the DDFDC terminates the command and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

The following tables specify the command bytes and describe the result bytes for the three scan commands.

SCAN EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	0	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN LOW OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN HIGH OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SEEK

The three-byte Seek command steps the FDD read/write head from track to track. The DDFDC has two independent Present Track Registers for each drive. They are cleared only by the Recalibrate command. The DDFDC compares the Present Track Number (PTN) which is the current head position with the New Track Number (NTN), and if there is a difference, performs the following operation:

If $PTN < NTN$: Sets the direction output (LCT/DIR) high and issues step pulses (FR/STP) to the FDD to cause the read/write head to step in.

If $PTN > NTN$: Sets the direction output (LCT/DIR) low and issues step pulses to the FDD to cause the read/write head to step out.

The rate at which step pulses are issued is controlled by the Step Rate Time (SRT) in the Specify command. After each step pulse is issued, NTN is compared against PTN. When $NTN = PTN$, then the Seek End (SE) flag in ST0 is set to a 1, bits 7 and 6 in ST0 are set to 0, and the command is terminated. At this point DDFDC asserts INT.

The FDD Busy flag (bit 0-3) in the Main Status Register (MSR) corresponding to the FDD performing the Seek operation is set to a 1.

After command termination, all FDD Busy bits set are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the DDFDC sets the Controller Busy (CB) flag in the MSR to 1; but during the execution phase the CB flag is set to 0 to indicate DDFDC non-busy. While the DDFDC is in the non-busy state, another Seek command may be issued, and in this manner parallel seek operations may be performed on all drives at once.

No command other than Seek will be accepted while the DDFDC is sending step pulses to any FDD. If a different command type is attempted, the DDFDC will set bits 7 and 6 in ST0 to a 1 and 0, respectively, to indicate an invalid command.

If the FDD is in a not ready state at the beginning of the command execution phase or during the seek operation, then the DDFDC sets the Not Ready (NR) flag in ST0 to a 1, sets ST0 bits 7 and 6 to 0 and 1, respectively, and terminates the command.

If the time to write the three bytes of the Seek command exceeds 150 μ s, the time between the first two step pulses may be shorter than the Step Rate Time (SRT) defined by the Specify command by as much as 1 ms.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	1	1	1
	2	X	X	X	X	X	0	US1	US0
	3	New Track Number (NTN)							

Result Phase: None.

RECALIBRATE

This two-byte command retracts the FDD read/write head to the Track 0 position. The DDFDC clears the contents of the PTN counters, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal (TRK0) is low, the direction signal (LCT/DIR) output remains low and step pulses are issued on FR/STP. When TRK0 goes high the DDFDC sets the Seek End (SE) flag in ST0 to a 1 and terminates the command. If the TRK0 is still low after 256 step pulses have been issued, the DDFDC sets Seek End (SE) and Equipment Check (EC) flags in ST0 to 1s, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the RDY signal, as described in the Seek command, also applies to the Recalibrate command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	1	1
	2	X	X	X	X	X	0	US1	US0

Result Phase: None.

SENSE INTERRUPT STATUS

Interrupt Request (INT) is asserted by the DDFDC when any of the following conditions occur:

- Upon entering the result phase of:
 - Read Data command
 - Read a Track command
 - Read ID command
 - Read Deleted Data command
 - Write Data command
 - Format a Track command
 - Write Deleted Data command
 - Scan commands
- Ready (RDY) line from the FDD changes state
- Seek or Recalibrate command termination
- During execution phase in the Non-DMA mode

INT caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in Non-DMA mode, bit 5 in the MSR is set to 1. Upon entering result phase this bit is set to 0. Reasons 1 and 4 do not require the Sense Interrupt Status command. The interrupt is cleared by reading or writing data to DDFDC. Interrupts caused by reasons 2 and 3 are identified with the aid of the Sense Interrupt Status command. This command resets INT and sets/resets bits 5, 6, and 7 of ST0 to identify the cause of the interrupt. Table 7 defines the seek and interrupt codes.

Neither the Seek or Recalibrate command has a result phase. Therefore, it is mandatory to use the Sense Interrupt Status command after these commands to effectively terminate them and to verify where the head is positioned by checking the Present Track Number (PTN).

Issuing a Sense Interrupt Status command without an interrupt pending is treated as an invalid command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	0	0	0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Present Track Number (PTN)

SPECIFY

The three-byte Specify command sets the initial values for each of the three internal timers. The Head Unload Time (HUT) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (1 = 16 ms, 2 = 32 ms, ... F = 240 ms).

The Step Rate Time (SRT) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, ... 0 = 16 ms.)

The Head Load Time (HLT) defines the time between the Head Load (HDL) signal going high and the start of the read/write operation. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms, ... 7F = 254 ms).

The time intervals are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock. If the clock is reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of two.

The choice of DMA or Non-DMA operation is made by the Non-DMA mode (ND) bit. When this bit = 1 the Non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	0	1	1
	2	SRT				HUT			
	3	HLT							ND

SRT — Step Rate Time
 HUT — Head Unload Time
 HLT — Head Load Time
 ND — Non-DMA mode

Result Phase: None.

Table 7. ST0 Seek and Interrupt Code Definition for Sense Interrupt Status

Status Register 0 (ST0) Bits			
Interrupt Code (IC)		Seek End (SE)	Cause
7	6	5	
1	1	0	RDY line changed state, either polarity
0	0	1	Normal termination of Seek or Recalibrate command
0	1	1	Abnormal termination of Seek or Recalibrate command

SENSE DRIVE STATUS

This two-byte command obtains and reports the status of the FDDs. Status Register 3 (ST3) is returned in the result phase and contains the drive status.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	0	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 3 (ST3)
---	---	-------------------------

INVALID COMMAND

If an invalid command (i.e., a command not previously defined) is received by the DDFDC, then the DDFDC terminates the command after setting bits 7 and 6 of ST0 to 1 and 0, respectively. The DDFDC does not generate an interrupt during this condition. Bits 6 and 7 (DIO and RQM) in the MSR are both set to a 1 indicating to the processor that the DDFDC is in the result phase and that ST0 must be read. A hex 80 in ST0 indicates that an invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt, otherwise the DDFDC considers the next command to be an invalid command.

In some applications the user may wish to use this command as a No-Op command, to place the DDFDC in a standby or no operation state.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	Invalid Codes							

Result Phase:

R	1	Status Register 0 (ST0) = 80
---	---	------------------------------

PROCESSOR INTERFACE

During the command or result phases, the Main Status Register (MSR) must be read by the processor before each byte of information is transferred to, or from, the DDFDC Data Register. After each byte of data is written to, or read from, the Data Register, the processor should wait 12 μ s before reading the MSR. Bits 6 and 7 in the MSR must be a 0 and 1, respectively, before each command byte can be written to the DDFDC. During the result phase, bits 6 and 7 of the MSR must both be 1s prior to reading each byte from the Data Register onto the data bus. Note that this status reading of bits 6 and 7 of the MSR before each byte transfer to and from the DDFDC is required in only the command and result phases and not during the execution phase.

During the result phase all bytes shown in the result phase must be read by the processor. The Read Data command, for example, has seven bytes of data in the result phase. All seven bytes must be read to successfully complete the Read Data command. The DDFDC will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

INTERRUPT REQUEST MODE

During the execution phase, the MSR need not be read. The receipt of each data byte from the FDD is indicated by INT high on pin 18. When the DDFDC is in Non-DMA mode, INT is asserted during the execution phase. When the DDFDC is in the DMA mode, INT is asserted at the result phase. The INT signal is reset by a read (RD low) or write (WR low) of data to the DDFDC. A further explanation of the INT signal is described in the Sense Interrupt Status command on page 16. If the system cannot handle interrupts fast enough (within 13 μ s for MFM mode or 27 μ s for FM mode), it should poll bit 7 (RQM) in the MSR. In this case, RQM in the MSR functions as an Interrupt Request (INT). If the RQM bit is not set, the Over Run (OR) flag in ST1 will be set to a 1 and bits 7 and 6 of ST0 will be set to a 0 and 1, respectively.

DMA MODE

When the DDFDC is in the DMA mode (ND = 0 in the third command byte of the Specify command), DRQ (DMA Request) is asserted during the execution phase (rather than INT) to request the transfer of a data byte between the data bus and the DDFDC.

During a read command, the DDFDC asserts DRQ as each byte of data is available to be read. The DMA controller responds to this request with DACK low (DMA Acknowledge) and RD low (read). When DACK goes low the DMA Request is reset (DRQ low). After the execution phase has been completed (TC high or the EOT sector is read), INT is asserted to indicate the beginning of the result phase. When the first byte of data is read during the result phase, INT is reset low.

During a write command, the DDFDC asserts DRQ as each byte of data is required. The DMA controller responds to this request with DACK (DMA Acknowledge) and WR low (write). When DACK goes low the DMA Request is reset (DRQ low). After the execution phase has been completed (TC high or the EOT sector is written), INT is asserted. This signals the beginning of the result phase. When the first byte of data is read during the result phase, the INT is reset low.

FDD POLLING

After the Specify command has been received by the DDFDC, the Unit Select lines (US0 and US1) begin the polling mode. Between commands (and between step pulses in the Seek Command) the DDFDC polls all the FDD's looking for a change in the RDY line from any of the drives. If the RDY line changes state (usually due to the door opening or closing) then the DDFDC asserts INT. When Status Register 0 (ST0) is read (after Sense Interrupt Status command is issued), Not Ready (NR = 1) will be indicated. The polling of the RDY line by the DDFDC occurs continuously between commands, thus notifying the processor which drives are on- or off-line. Each drive is polled every 1.024 ms except during read/write commands.

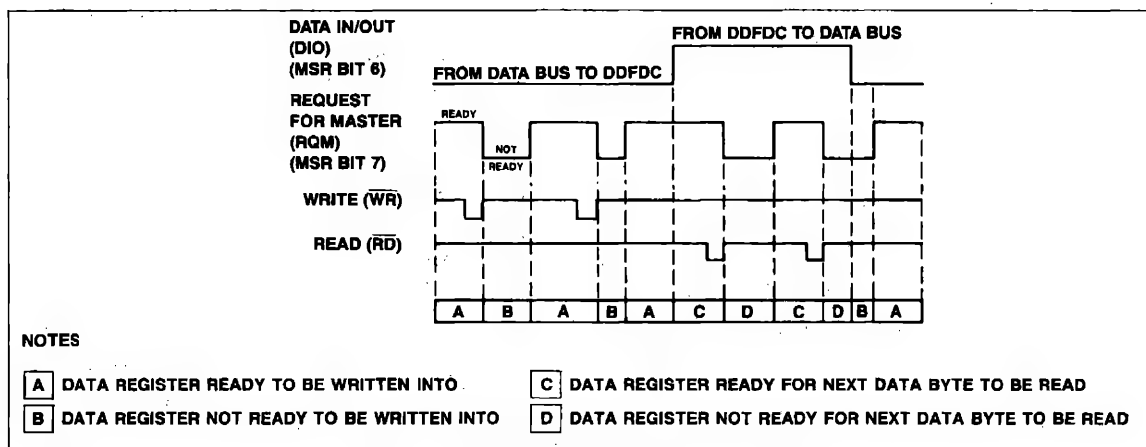


Figure 3. DDFDC and System Data Transfer Timing

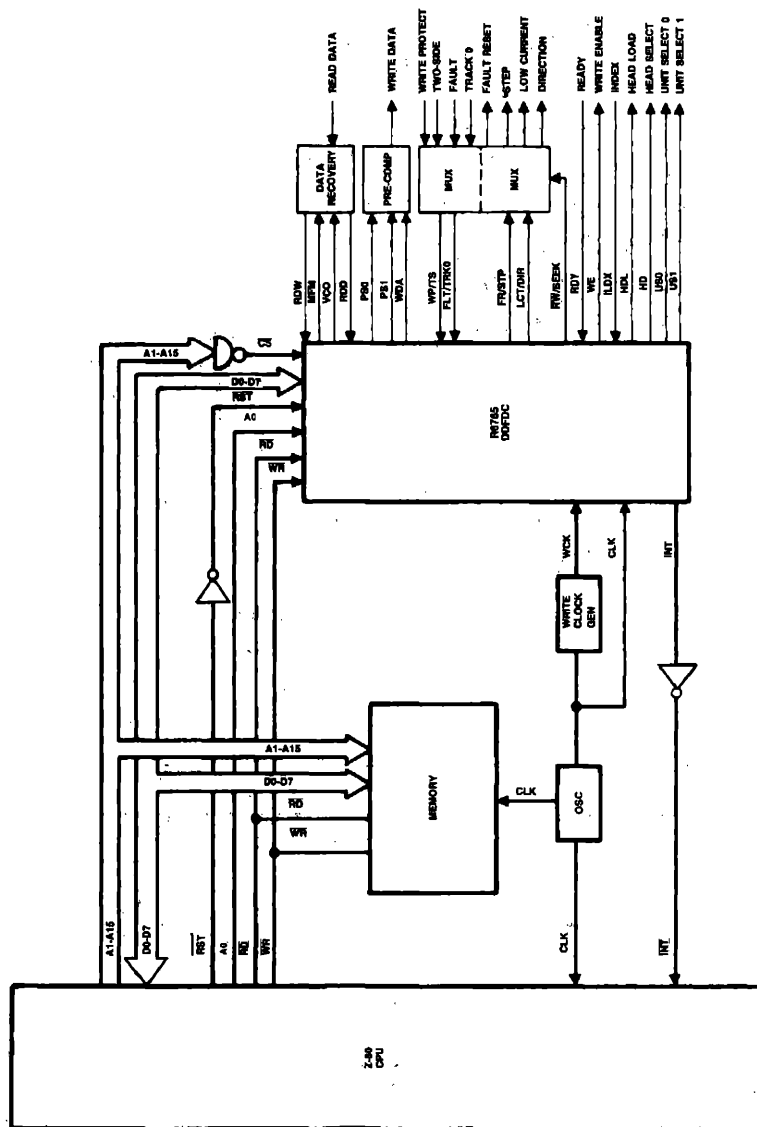


Figure 4. R6765 DDFDC Interface to Z-80

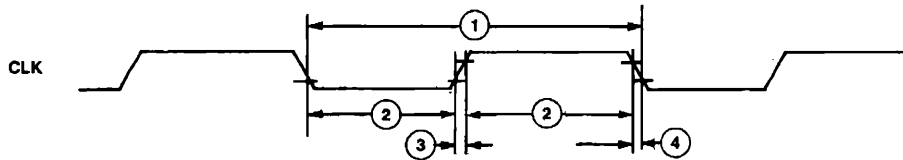


Figure 5. Clock Timing

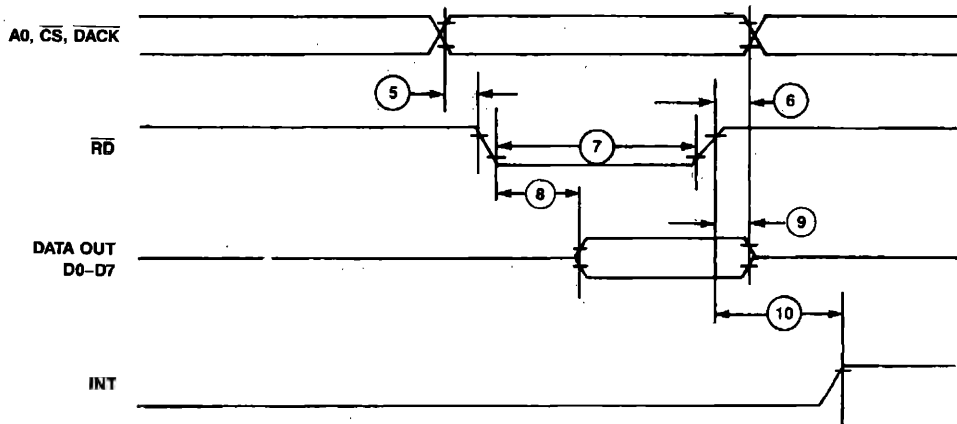


Figure 6. Read Cycle Timing

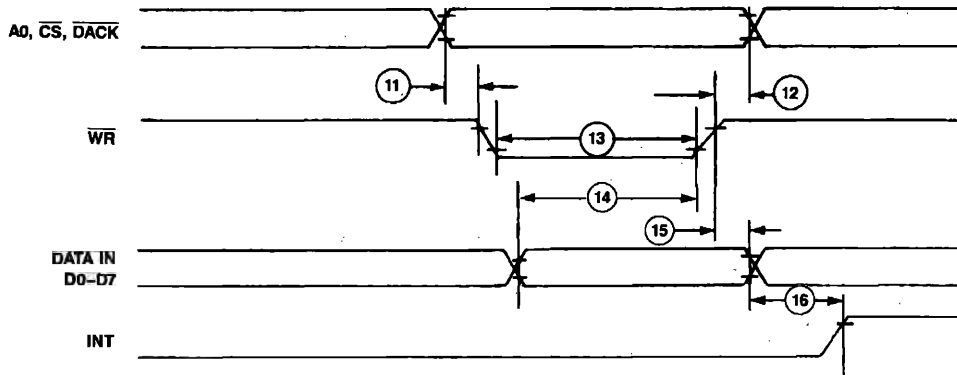


Figure 7. Write Cycle Timing

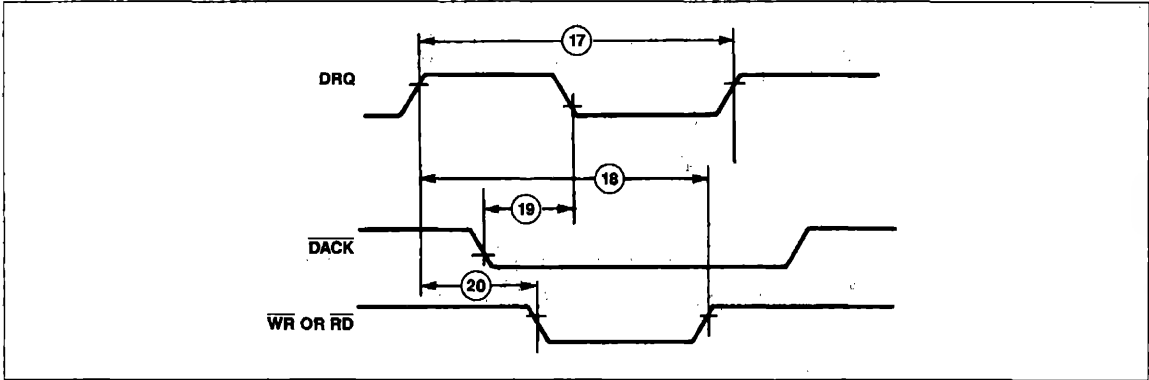


Figure 8. DMA Operation Timing

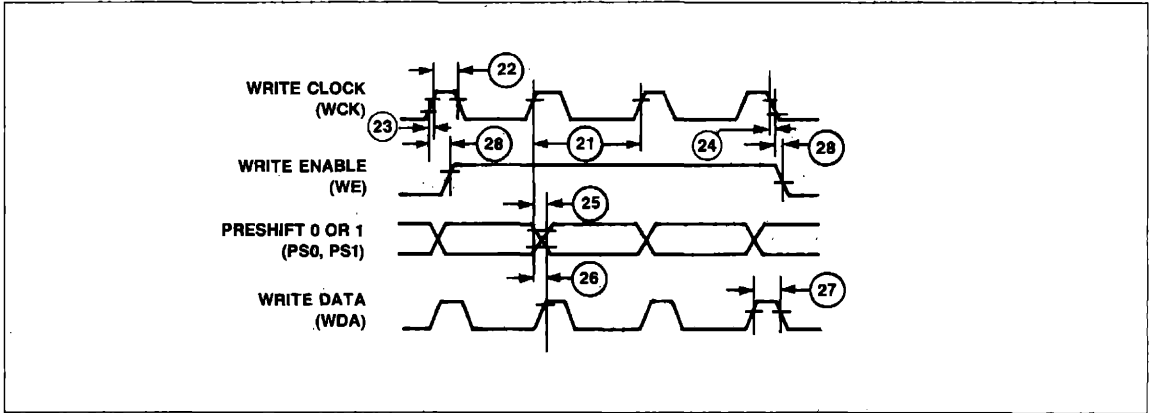


Figure 9. FDD Write Operation Timing

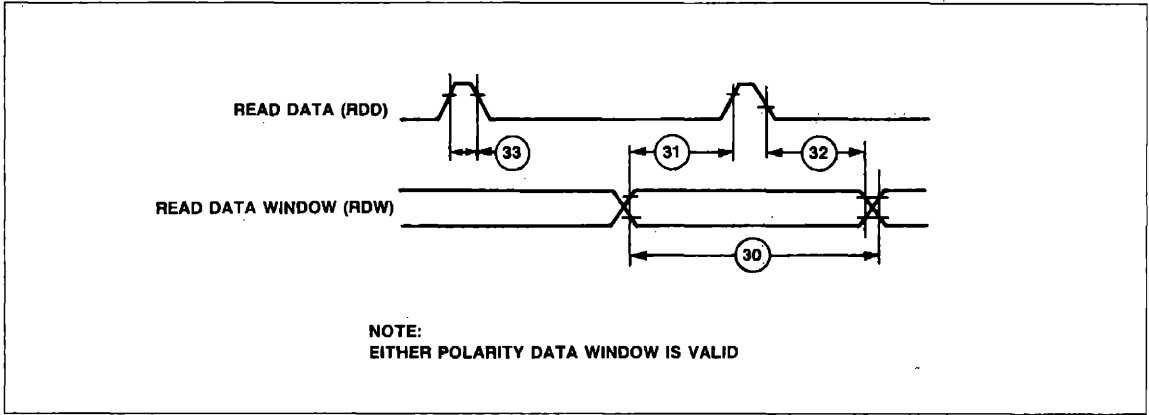


Figure 10. FDD Read Operation Timing

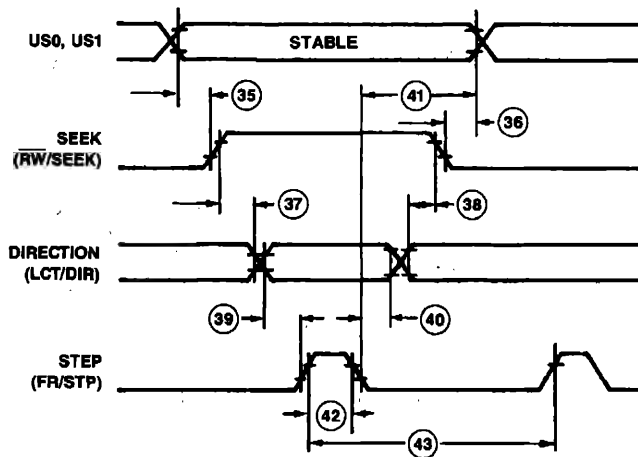


Figure 11. Seek Operation Timing

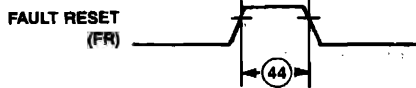


Figure 12. Fault Reset Timing

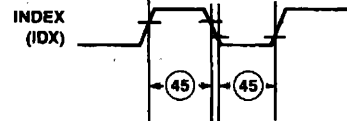


Figure 13. Index Timing

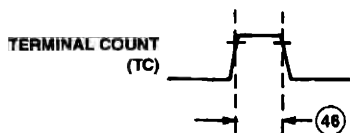
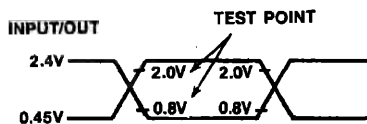


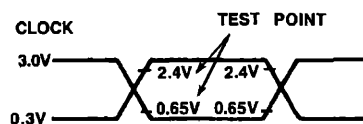
Figure 14. Terminal Count Timing



Figure 15. Reset Timing



INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."



CLOCKS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.3V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.4V FOR A LOGIC "1" AND 0.65V FOR A LOGIC "0."

Figure 16. AC Timing Measurement Conditions

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Ref. Fig.	No.	Characteristic	Symbol	Alt. Sym.	Min.	Typ.	Max.	Unit	Test Conditions
5	1	Clock Period	t _{CY}	φ _{CY}	240 120	250 125	500	ns	CLK = 4 MHz
	2	Clock High, Low Width	t _{CA}	φ ₀	80 40	125 62.5	—	ns	CLK = 8 MHz
	3	Clock Rise Time	t _{CLCH}	φ _r	—	—	20	ns	CLK = 8 MHz
	4	Clock Fall Time	t _{CHCL}	φ _f	—	—	20	ns	CLK = 8 MHz
6	5	A0, CS, DACK Valid to RD Low (Setup)	t _{SLRL}	t _{AR}	0	—	—	ns	C _L = 100 pF
	6	RD High to A0, CS, DACK Invalid (Hold)	t _{RHSH}	t _{RA}	0	—	—	ns	
	7	RD Low Width	t _{RLRH}	t _{RR}	250	—	—	ns	
	8	RD Low to Data Valid (Access)	t _{RLDV}	t _{RD}	—	—	200	ns	
	9	RD High to Output High Z	t _{RHDZ}	t _{DF}	20	—	100	ns	
	10	RD High to INT High	t _{RHIH}	t _{RI}	—	—	500	ns	
	11	A0, CS, DACK Valid to WR Low (Setup)	t _{SLWL}	t _{AW}	0	—	—	ns	
7	12	WR High to A0, CS, DACK Invalid (Hold)	t _{WHSH}	t _{WA}	0	—	—	ns	CLK = 8 MHz
	13	WR Low Width	t _{WLWH}	t _{WW}	250	—	—	ns	
	14	Data Valid to WR High (Setup)	t _{DVWH}	t _{DW}	150	—	—	ns	
8	15	WR High to Data Invalid (Hold)	t _{WHDX}	t _{WD}	5	—	—	ns	CLK = 8 MHz
	16	WR High to INT High	t _{WHIH}	t _{WI}	—	—	500	ns	
	17	DRQ Cycle Time	t _{QCY}	t _{MCY}	13	—	—	μs	
9	18	DRQ High to RD, WR High (Response)	t _{QHSH}	t _{MRW}	—	—	12	μs	CLK = 8 MHz
	19	DACK Low to DRQ Low (Delay)	t _{ALQL}	t _{AM}	—	—	200	ns	
	20	DRQ High to RD Low (Delay)	t _{QHRL}	t _{MR}	800	—	—	ns	
10	21	WCK Cycle Time	t _{KCY}	t _{CY}	—	note 1	—	μs	CLK = 8 MHz
	22	WCK High Width	t _{KHKL}	t ₀	80	250	350	ns	
	23	WCK Rise Time	t _{KLKH}	t _r	—	—	20	ns	
	24	WCK Fall Time	t _{KHKL}	t _f	—	—	20	ns	
	25	WCK High to PS0, PS1 Valid (Delay)	t _{KHPV}	t _{CP}	20	—	100	ns	
	26	PS0, PS1 Valid to WDA High (Delay)	t _{PVDH}	t _{CD}	20	—	100	ns	
	27	WDA High Width	t _{DHDL}	t _{WDD}	t _{WCH} - 50	—	—	ns	
11	28	WE High to WCK High or WE Low to WCK Low	t _{EHKH}	t _{WE}	20	—	100	ns	CLK = 8 MHz
	30	RDW Cycle Time	t _{WCY}	t _{WCY}	—	note 2	—	μs	
	31	RDW Valid to RDD High (Setup)	t _{WVRH}	t _{WRD}	15	—	—	ns	
	32	RDD Low to RDW Invalid (Hold)	t _{RLWL}	t _{RDW}	15	—	—	ns	
12	33	RDD High Width	t _{RHRL}	t _{RDD}	40	—	—	ns	CLK = 8 MHz
	35	US0, US1 Valid to SEEK High (Setup)	t _{UVSH}	t _{US}	12	—	—	μs	
	36	SEEK Low to US0, US1 Invalid (Hold)	t _{SLUI}	t _{SU}	15	—	—	μs	
	37	SEEK High to DIR Valid (Setup)	t _{SHDV}	t _{SD}	7	—	—	μs	
	38	DIR Invalid to SEEK Low (Hold)	t _{OXSL}	t _{DS}	30	—	—	μs	
	39	DIR Valid to STP High (Setup)	t _{DVTH}	t _{DST}	1	—	—	μs	
	40	STP Low to DIR Invalid (Hold)	t _{TLDX}	t _{STD}	24	—	—	μs	
13	41	STP Low to US0, US1 Invalid (Hold)	t _{TLUX}	t _{STU}	5	—	—	μs	CLK = 8 MHz
	42	STP High Width	t _{HTHL}	t _{STP}	6	7	—	μs	
	43	STP Cycle Time	t _{TCY}	t _{SC}	33 ³	—	note 3	μs	
14	44	FR High Width	t _{FHFL}	t _{FR}	8	—	10	μs	
15	45	IDX High Width	t _{HIL}	t _{IDX}	10	—	—	t _{CY}	
16	46	TC High Width	t _{HTHL}	t _{TC}	1	—	—	t _{CY}	
17	47	RST High Width	t _{RHRL}	t _{RST}	14	—	—	t _{CY}	

Notes:

1. MFM Mini Standard

0 4 μs 2 μs

1 2 μs 1 μs

2. For MFM = 0: Typ. = 2 μs

For MFM = 1: Typ. = 1 μs

3. t_{SC} = 33 μs min. is for different drive units. In the case of the same unit, t_{SC} can range from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Output Voltage	V_{OUT}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	C°
Storage Temperature Range	T_{STG}	-55 to +150	C°

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Range
V_{CC} Power Supply	5.0V \pm 5%
Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

($V_{CC} = 5.0$ Vdc \pm 5%, $V_{SS} = 0$ Vdc, $T_A = 0^\circ\text{C}$ to 70°C , unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Low Voltage Logic CLK and WCK	V_{IL}	-0.5 -0.5	0.8 0.65	V	
Input High Voltage Logic CLK and WCK	V_{IH}	2.0 2.4	$V_{CC} + 0.5$ $V_{CC} + 0.5$	V	
Output Low Voltage	V_{OL}		0.45	V	$V_{CC} = 4.75\text{V}$, $I_{OL} = 2.0$ mA
Output High Voltage	V_{OH}	2.4	V_{CC}	V	$V_{CC} = 4.75\text{V}$, $I_{OH} = -200$ μA
V_{CC} Supply Current	I_{CC}		150	mA	$V_{CC} = 4.75\text{V}$
Input Load Current All Inputs	I_{IL}		10 -10	μA μA	$V_{IN} = V_{CC}$ $V_{IN} = 0\text{V}$
High Level Output Leakage Current	I_{LOH}		10	μA	$V_{CC} = 0\text{V}$ to 5.25V , $V_{SS} = 0\text{V}$ $V_{OUT} = V_{CC}$
Low Level Output Leakage Current	I_{LOL}		-10	μA	$V_{CC} = 0\text{V}$ to 5.25V , $V_{SS} = 0\text{V}$ $V_{OUT} = +0.45\text{V}$
Internal Power Dissipation	P_{INT}	—	1.0	W	$T_A = 25^\circ\text{C}$

CAPACITANCE

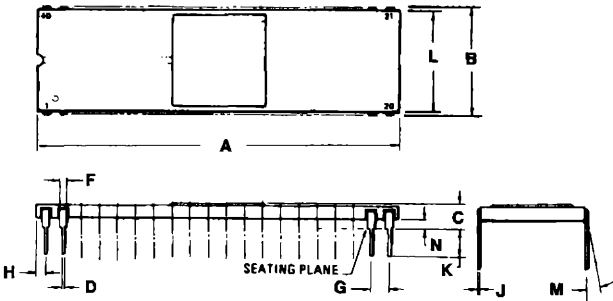
($T_A = 25^\circ\text{C}$; $f_c = 1$ MHz; $V_{CC} = 0\text{V}$)

Parameter	Symbol	Max Limit	Unit
Clock Input	$C_{IN(K)}$	20	pF
Input	C_{IN}	10	pF
Output	C_{OUT}	20	pF

Note: All pins except pin under test tied to ground.

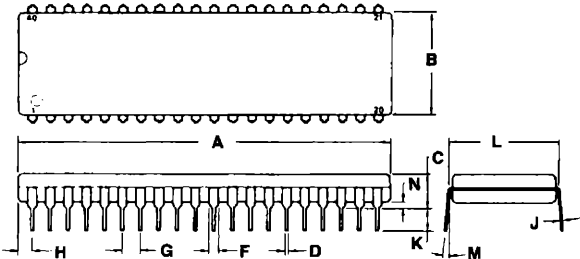
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	-0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54	BSC	0.100	BSC
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24	BSC	0.600	BSC
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

SECTION 3

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R6500/* SINGLE-CHIP MICROCOMPUTER FAMILY

Higher Performance, Broader Applications, Software Compatibility

The R6500/* single-chip microcomputers are completely software compatible with the 8-bit multi-chip family. They let you move easily from a multi-chip to a single-chip system solution when the application warrants it. They also function as intelligent peripheral controllers. The family continues to expand to include dual processors and CMOS versions. The R6500/* devices have faster execution speeds for most applications, based on our competitors own figures, even though some others use higher frequency crystals.

Features include 1.5 to 3K bytes of ROM, 64 to 192 bytes of RAM, 23 to 56 I/O ports, multiple use counter/timers, serial communication channels, new bit manipulation instructions, expansion bus, multiple bus interfaces, directly executable RAM with low power standby, multiple interrupts, all from a single 5V power supply.

Three intelligent peripheral controllers offer design effective upgrading potentials for existing 6800, 8080, Z80 and 6500 systems. They're also available in ROM-less

versions, for large memory system applications and for developing and simulating products in prototype, with external memory.

And, two versions even have all system software on chip, including an operating system and high level FORTH language. It's an extremely versatile single-chipper.

Three different sets of development ROM permit systems from 16 to 40 I/O and 8K to 48K of application program memory.

As the highest performance single-chip family, the R6500/* devices are in use now in applications such as printers, telephone answering equipment, fixed disk drives, stereos, industrial controllers, telecom, cash registers, sewing machines, test equipment and more.

Check for yourself and see how a Rockwell R6500/* can solve your system problem. There are no higher performing 8-bit single chippers, regardless of clock speeds.

ROCKWELL NMOS MICROCOMPUTERS—THE TOP PERFORMERS IN INDUSTRY

Features/Models	R6500/1	R6500/11	R6500/12	R6501Q/111Q	R6500/41	R6500/42	R6541Q
• ROM (x8)	2048	3072	3072	—	1536	1536	256
• RAM (x8)	64	192	192	192	64	64	64
• I/O Lines	32	32	56	32	23	47	23
• Serial Comm.	—	USART	USART	USART	—	—	—
• 16-Bit Counters	ONE	TWO	TWO	TWO	ONE	ONE	ONE
• Host/Slave Bus	—	—	—	—	80/65	80/65	80/65
• Expansion Bus	—	16K	16K	65K	4K	4K	8K/4K
• Interrupts							
— External	4	6	6	6	4	4	5
— Internal	1	4	4	4	1	1	1
— Host	—	—	—	—	2	2	2
• Standby RAM (mW)	35	12	12	12	—	—	—
• Package	40 DIP	40 DIP	64 QUIP	64 QUIP	40 DIP	64 QUIP	64 QUIP
Alternatives for	8048/49	8051		8031	8041		



R65C00/21 DUAL CMOS MICROCOMPUTER AND R65C29 DUAL CMOS MICROPROCESSOR

PRELIMINARY INTRODUCTION

FEATURES

- Two enhanced CMOS R6502 CPU's in one device
 - Common memory and I/O
 - Shared data and subroutines
 - Independent CPU registers and interrupt vectors
 - Independent reset operation and programs
 - R6502 software and timing compatible
- 10 new instructions for faster and smaller programs
 - Unsigned Multiply (MUL)
 - Set and Reset Memory Bit (SMB and RMB)
 - Branch on Bit Set and Reset (BBS and BBR)
 - Unconditional Branch (BRA)
 - Push and Pull Index Registers (PHX, PHY; PLX; PLY)
- Microcomputer/microprocessor/peripheral controller operation
 - Stand-alone microcomputer
 - 2048 × 8 mask programmable ROM
 - 128 × 8 random access memory (RAM)
 - Enhanced microprocessor
 - Built-in RAM, ROM and I/O with expandability
 - 8-, 12- or 16-bit extension address bus
 - Programmable peripheral controller
 - Host data bus interface (Z80/8080 or 6500/6800 option)
 - Self-contained or expandable
- 16-bit Counter/Timer A with eight modes, and prescaler
 - Timer Off
 - Free-Run Event Counter
 - Free-Run Pulse Width Measurement
 - One-Shot Retriggerable Timer
 - One-Shot Interval Timer
 - Free-Run Interval Timer
 - One-Shot Pulse Generator
 - Free-Run Pulse Generator
- 16-bit Counter/Timer B with four modes
 - Free-Run Interval Timer
 - Free-Run Pulse Generator
 - Event Counter
 - Pulse Width Measurement
- Up to 52 general purpose input/output lines
 - Five bidirectional 8-bit ports (PA, PB, PC, PD and PF)
 - One 8-bit output port (PE)
 - One 4-bit input port (PG)
 - Multi-purpose operation for selected ports

- Nine interrupts
 - Positive and negative edge detect
 - Low level detect (external IRQ)
 - Counter/Timer A and B underflow
 - Inter-processor communication
 - Host computer data transfer
 - Non-maskable
 - Reset
- Flexible system operation
 - Memory mapped I/O for easy programming
 - Page zero location for memory efficient access
- Low power at normal frequency (40 mw at 2 MHz)
- Reduced power at low frequency (2.0 mw at 2 MHz/128)
- System clock rates from 10 KHz to 4 MHz
- 5V ± 10% power supply
- 64-pin QUP

SUMMARY

The Rockwell R65C00/21 is a complete, high performance 8-bit, CMOS dual microcomputer in a single chip and is compatible with all R6500 microprocessors except that it has additional instructions including a 10-clock time multiply.

The R65C00/21 consists of two enhanced instruction set 6502 CPU's in one device. The device also has 2048 bytes of Read-Only Memory (ROM), 128 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry consists of two multimode programmable 16-bit counter/timers and 52 general purpose input/output lines. Some of these input/output lines may be used as address, data and control lines for expanded systems or as data and control lines when the R65C00/21 is used as a programmable peripheral controller.

The two CPU's in the R65C00/21 are functionally independent. Each has its own set of registers, its own reset and interrupt vectors and operates under control of its own program. The two CPU's do, however, share the same memory and system I/O resources. This allows direct communication between the two CPU's and allows sharing of subroutines and common data areas where desired. Programming and system design for applications which require simultaneous control of two or more independent asynchronous processes is thus simplified because one CPU may control one process while the other controls

another one. Consequently, complex programming usually needed to interleave the control functions or to implement an interrupt driven system, is not required.

In a multiple computer approach, both processors may need the same subroutines so that some portions of memory must be duplicated in both systems. The dual CPU's share the same program memory, therefore only one set of subroutines is required and both CPU's may even be using them at the same time without interference.

In addition to the dual CPU's, the R65C00/21 also has the innovative architecture and the demonstrated high performance of the well established R6502 CPU, flexible input/output which provides improvements over the R6522 Versatile Interface Adapter (VIA) device, and production efficient on-chip ROM and RAM. These features make the R65C00/21 a leading candidate for most imbedded microcomputer applications.

A system using the R65C00/21 Dual CMOS Microcomputer will be simpler in design, use less program memory, require fewer components, reduce circuit board sizes, simplify test requirements, and minimize field maintenance—all contributing to lower production and support costs. In addition, simpler designs shorten development effort and time—leading to reduced development costs and faster product to market.

The R65C29 Dual CMOS Microprocessor, a ROM-less version of the R65C00/21 with permanently extended data and address bus, is also available. The R65C29 is ideal for dual CPU applications requiring changeable ROM and/or extended RAM, ROM or I/O, and can also be used for R65C00/21 prototype circuit development. The R65C00/21 can also operate in an emulation mode, like the R65C29, with its internal ROM disabled.

DEVELOPMENT SYSTEM SUPPORT

Prototype circuit and software development support are available using the Rockwell Design Center (RDC) and R65C00/21 Personality Module. Program development and debugging aids such as text editing, symbolic assembly with conditionals and macros at the absolute and relocatable/linking level, and single/multiple step execution with instruction/data tracing are provided. Real-time in-circuit emulation in the target environment is also supported.

NOTE

All descriptions of R65C00/21 operation in this document also apply to the R65C29 except for internal ROM, and as otherwise noted.

ORDERING INFORMATION

The R65C00/21 Dual CMOS Microcomputer can be ordered in volume quantities with the following speed capability and mask option indicated in the R65C00/21 ROM Code Order Form (Document Order No. 2134)

- 1, 2, 3, or 4 MHz system clock (Ø2)
- Crystal/master clock or slaved clock input mask option

The R65C29 Dual CMOS Microprocessor has the following characteristics:

- Crystal/master clock input
- 8-bit data bus and 16-bit address bus extension
- No internal ROM

INTERFACE

The interfaces for the R65C00/21 and R65C29 are illustrated in Figure 1.

The pin assignments for the R65C00/21 and the R65C29 are shown in Figure 2. The R65C29 pin assignments are the same as the R65C00/21 except that bus expansion functions are permanently assigned instead of general purpose ports D and E.

The interface signals for the R65C00/21 and R65C29 are described in Table 2. The descriptions of the selectable, bus expansion pins (16-bit address mode) for the R65C00/21 apply to permanent bus expansion pins for the R65C29.

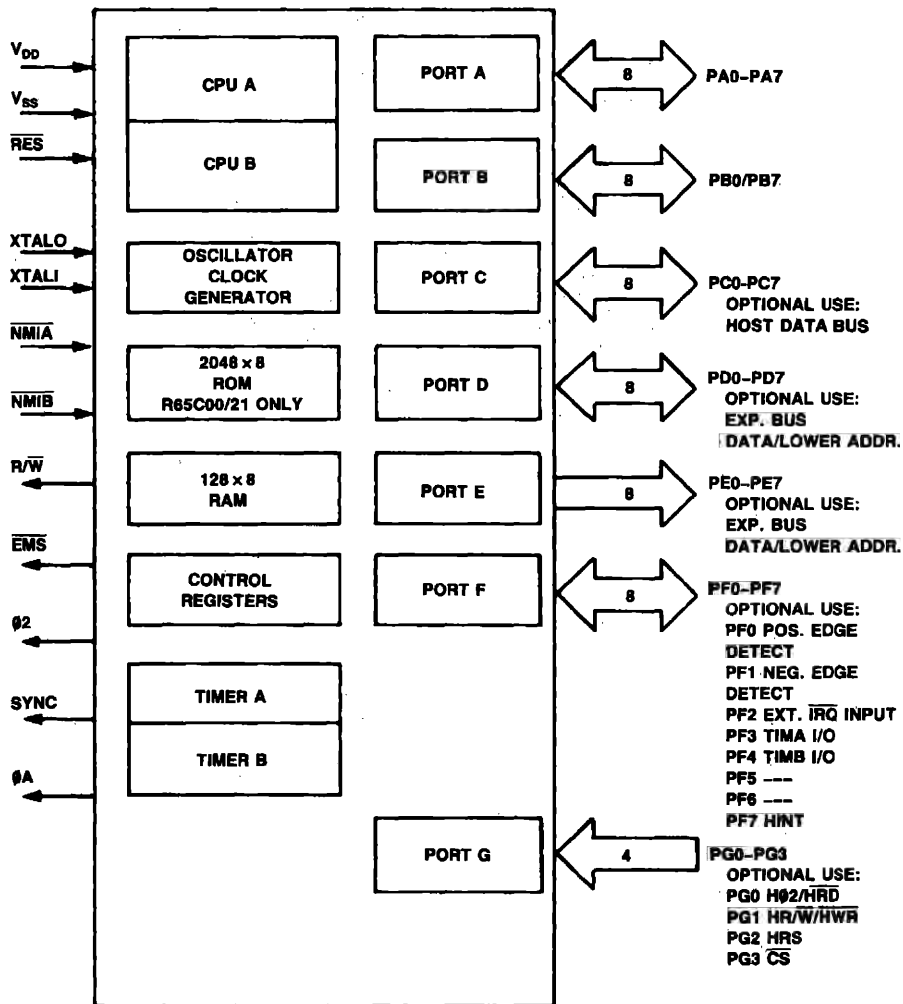


Figure 1. R65C00/21 and R65C29 Interface Diagram

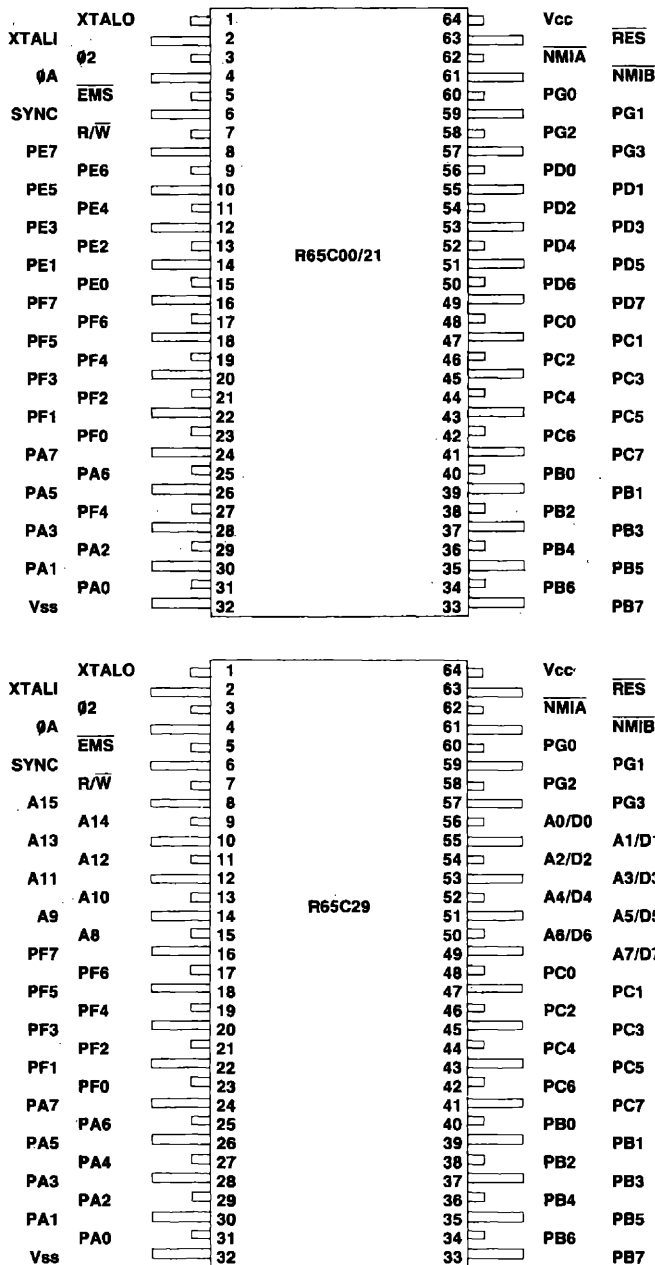


Figure 2. R65C00/21 and R65C29 Pin Assignments

Table 1. R65C00/21 Pin Descriptions

Signal Name	Pin No.	I/O	Description
PA0-PA7	31-24	I/O	Port A. General purpose 8-bit I/O Port A.
PB0-PB7	40-33	I/O	Port B. General purpose 8-bit I/O Port B.
PC0-PC7	48-41	I/O	Port C. General purpose 8-bit I/O Port C. Host Data Bus in Host Mode.
PD0-PD7	56-49	I/O	Port D. General purpose 8-bit I/O Port D. Multiplexed lower address (A0 to A7) and Data Bus (D0-D7) when Bus Extension Mode is selected.
PE0-PE7	15-8	O	Port E. General purpose 8-bit output Port E. Upper address (A8 to A11 or A8 to A15) when Bus Expansion Mode is selected.
PF0-PF7	23-16	I/O	Port F. General purpose 8-bit I/O Port F. Under software control, each line has alternate functions as follows:
PF0NEG (PF0)	23	I	PF0 Positive Edge Detect. Maskable CPU interrupt on PF0 Positive Transition.
PF1POS (PF)	22	I	PF1 Negative Edge Detect. Maskable CPU interrupt on PF1 Negative Transition.
PF2LOW (PF2)	21	I	PF2 Low Level Detect. Maskable CPU interrupt on PF2 Low (external IRQ).
TIMA (PF3)	20	I/O	Timer A External Input/Output.
TIMB (PF4)	19	I/O	Timer B External Input/Output.
HINT (PF7)	16	O	Host Interrupt. Active-low maskable interrupt request to Host.
PG0-PG3	60-57	I	Port G. General purpose 4-bit Input Port G. Under software control, Port G serves as the Host Control Bus as follows:
H ϕ 2/ $\overline{\text{HRD}}$ (PG0)	60	I	Host Bus Clock/Read Strobe Input. ϕ 2 for 6500/6800 bus; Read Strobe for Z80/8080 bus.
HR/ $\overline{\text{W}}$ / $\overline{\text{HWR}}$ (PG1)	59	I	Host Bus Read-Write/Write Strobe Input. R/ $\overline{\text{W}}$ for 6500/6800 bus; Write Strobe for Z80/8080 bus.
HRS (PG2)	58	I	Host Bus Register Select Input. Low selects Data Buffer; high selects Status Flags.
$\overline{\text{CS}}$ (PG3)	57	I	Host Bus Active-Low Chip Select Input. Low selects Host Bus operation depending on HRS and HR/ $\overline{\text{W}}$ / $\overline{\text{HWR}}$ coding and Host Control and Status Register contents; high disables Host Bus interface.
$\overline{\text{RES}}$	63	I	Reset. Active-low Reset input initializes R65C00/21 to initial conditions—resets all registers and I/O lines.
NMIA	62	I	CPU A Non-Maskable Interrupt. Non-maskable negative edge sensitive interrupt input to CPU A.
NMIB	61	I	CPU B Non-Maskable Interrupt. Non-maskable negative edge sensitive interrupt input to CPU B.
$\overline{\text{EMS}}$	5	O	External Memory Strobe. Active-low.
ϕ 2	3	O	System Phase 2 Clock Output. Maskable as system clock input for slave operation.
R/ $\overline{\text{W}}$	7	O	Read/Write. Read/write control output. High during read, low during write.
SYNC	6	O	Sync. Instruction sync output. High When Op Code fetched
ϕ A	4	O	Phase A. Phase A clock output. High during CPU A bus cycle, low during CPU B bus cycle.
XTALO	1	O	Crystal/Master Clock Return. Output connection to crystal (or no connection if external master clock connected to XTALI). Input frequency is two times system clock (ϕ 2) rate.
XTALI	2	I	Crystal/Master Clock Input. Input connection from crystal (or external master clock).
VCC	64		Power. 5.0 Vdc.
VSS	32		GND. Signal and power ground.

FUNCTIONAL DESCRIPTION

The R65C00/21 consists of two central processor units (CPU's), a 2048 × 8 read-only memory (ROM), a 128 × 8 random access memory (RAM), five 8-bit parallel I/O ports, one 8-bit output port, one 4-bit input port, two 16-bit counter/timer systems, a variety of I/O control registers, and an independent interrupt control system for each CPU. All of the ROM, RAM, I/O, internal buses, and the arithmetic logic unit (ALU) are shared by the two CPU's. A memory map of the system is shown in Figure 3. An overall block diagram of the R65C00/21 is shown in Figure 4.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

INTERNAL MEMORY

INTERNAL READ-ONLY-MEMORY (ROM)

The ROM in the R65C00/21 consists of 2048 (2K) bytes of mask programmable memory with an address space from F800 to FFFF. ROM locations FFF2 through FFFF are assigned to interrupt and reset vectors for the two CPU's.

INTERNAL RANDOM ACCESS MEMORY (RAM)

The internal RAM consists of 128 bytes of read/write memory with assigned page zero addresses of 0080 through 00FF.

EXTERNAL MEMORY

External memory can be addressed by selecting the Bus Expansion Mode in the Bus Control Register. Address space from 0200 through EFFF may be accessed for either RAM, ROM, or I/O purposes as the particular application requires it. In addition, there are 32 bytes from 0020 through 003F which may be used for I/O expansion and 256 bytes from 0100 through 01FF which may be external RAM.

CPU LOGIC

Each CPU in the R65C00/21 is effectively a standard R6502 CPU with 10 extra instructions utilizing 40 operation codes which are unused in the R6502. Therefore, each CPU has an 8-bit accumulator, two 8-bit index registers (X and Y), an 8-bit Stack Register, a 16-bit Program Counter, independent interrupt circuitry, and an instruction register with state counter. The internal buses, memory, instruction decoding circuitry, and ALU are shared by the two CPU's on alternate clock cycles.

ACCUMULATORS

The accumulator in each CPU is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. Additionally, the accumulator contains one of the two data words used in these operations.

INDEX REGISTERS

Each CPU has two index registers, X and Y. Each index register may be used as a modifier to a base address supplied as a part of the instruction being processed. The resulting effective address is usually the sum of the base address plus the contents of the indicated index register. The index registers are used in a number of the addressing modes including zero page indexed, absolute indexed, post-indexed indirect and pre-indexed indirect. Each index register also has a family of instructions which allow loading, storing, incrementing, decrementing, and comparing the contents of the register. These are discussed thoroughly in the R6500 Programming Manual (Order No. 202).

ADDRESS (HEX)

0000 001F 0020 003F 0040 007F 0080	I/O AND CONTROL REGISTERS EXTERNAL I/O EXPANSION ² NOT ACCESSIBLE INTERNAL RAM (128 BYTES) ¹ (SHARED WITH 0180-01FF)
00FF 0100 017F 0180	EXTERNAL RAM EXPANSION ² INTERNAL RAM (128 BYTES) ¹ (SHARED WITH 0080-00FF)
01FF 0200	EXTERNAL MEMORY AND I/O EXPANSION ²
EFFE F000 F7FF F800	NOT ACCESSIBLE INTERNAL ROM (2048 BYTES)
FFF1 FFF2 FFF3	NMIB VECTOR
FFF4 FFF5	RESB VECTOR
FFF6 FFF7	IRQB VECTOR
FFF8 FFF9	NOT USED
FFFA FFFB	NMIA VECTOR
FFFC FFFD	RESA VECTOR
FFFE FFFF	IRQA VECTOR

Notes:

- When bit 4 of the Bus Control Register (BCR) is a 0 (default value), the 128 bytes of internal RAM are redundantly mapped into both page zero and page one and are addressable as either 0080-00FF or 0180-01FF. When BCR bit 4 is a 1, all of page one RAM (256 bytes) is mapped externally (0100-01FF) and the 128 bytes of internal RAM are dedicated to page zero (0080-00FF).
- Accessible in bus expansion mode.

Figure 3. R65C00/21 Memory Map

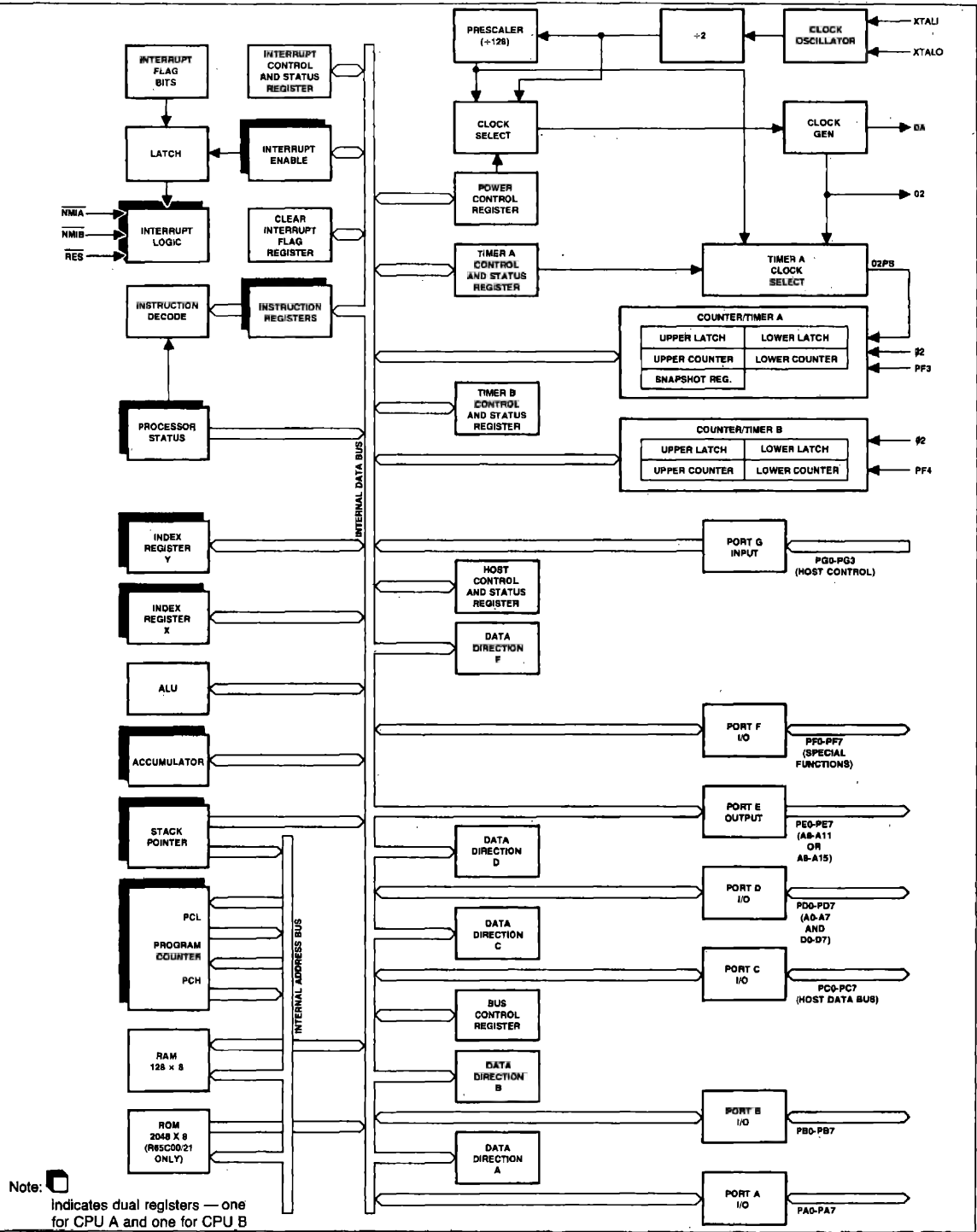


Figure 4. R65C00/21 and R65C29 Block Diagram

STACK POINTERS

Each CPU in the R65C00/21 has its own independent 8-bit Stack Register located in RAM on page zero/one and is pointed to by a Stack Pointer. Each Stack Register is automatically incremented and decremented under control of the appropriate CPU to perform proper stack manipulations in response to user instructions, an IRQ interrupt or an external NMI interrupt of the appropriate CPU. The Stack Pointers must be initialized by the user program.

These stacks allow simple implementation of multiple level independent interrupts in each CPU, subroutine nesting, and simplification of many types of data manipulation without the programmer continually being aware of specific memory addresses. The JSR, BRK, RTI, RTS, PHA, PLA, PHP, PLP, PHX, PLX, PHY and PLY instructions all make use of the stack and the appropriate CPU's Stack Pointer.

Each stack may be visualized as a deck of cards which may only be accessed from the bottom of the deck. The value to be stored is written on a card and then that card is placed on the bottom of the deck (pushed onto the stack). When the data are to be read, the bottom card is removed from the deck and the value on it transferred to the appropriate register (pulled from the stack to the specific register). Each time data are to be used as an address, the value is stored in the addressed memory cell, and the Stack Pointer is decremented by 1. When the data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1 and the resulting value can be used to address the data. The data are read from the addressed memory cell and then transferred to the appropriate register in the CPU.

Each CPU must have an independent starting location for its stack. It is the programmer's responsibility to see that the RAM utilized for each CPU stack does not conflict. It is recommended that the CPU requiring less depth in its stack be assigned the OXFF location and the other stack be started a safe distance below it. The two stacks are physically located either on page zero (although addressed as page one) for single-chip operation, or externally on page one when extended addressing is selected. (See Note 1 in Figure 3). The default areas for the stacks are on page zero. In either case, both stacks are on the same page.

ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations for both CPU's take place in a shared ALU. Incrementing and decrementing of the index registers and memory also take place here. The ALU stores data for only one cycle. Consequently, data placed on the inputs at the beginning of a cycle are processed and gated to one of the registers, or to memory, during the next cycle.

Each bit of the ALU has two inputs. These inputs may be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, etc.) using the data on the two inputs.

PROGRAM COUNTERS

The 16-bit program counters for each CPU provide addresses that step each processor through sequential instructions in a stored program. The program counter for each CPU is initially set to the value stored as the reset vector in CPU A (RESA at

FFF4) and in CPU B (RESB at FFF4) when power is applied to the R65C00/21. Each time a processor fetches an instruction from memory, the lower (least significant) byte of its program counter (PCL) is placed on the low-order eight bits of the address bus and the higher (most significant) byte of the program counter (PCH) is placed on the high-order eight bits of the address bus. The counter is incremented each time an instruction or operand is fetched from memory.

The contents of the program counter are replaced with a new value when a JMP, JSR, RTS, RTI, BRK, or any of the branch instructions are executed. Also, the program counter value is replaced when an external non-maskable interrupt NMIA or NMIB, an internal interrupt request, an external interrupt request via PF2 (see Port F description) or reset (RES) occurs.

INSTRUCTION REGISTERS AND INSTRUCTION DECODE

Instructions selected by the program counter are fetched from ROM or RAM (or Port D if in Expanded Bus Mode) and gated onto the internal data bus. These instructions are latched into the proper instruction register and then decoded using common decoding circuits for both CPU's. Timing, status bits, and interrupt controls are interpreted together with the instruction code to generate control signals for the various registers in the appropriate CPU.

INTERRUPT LOGIC

Each CPU has its own logic which controls the sequencing of three types of interrupts: RES, NMI, and IRQ. The same RESET (RES) pin is used for both CPU's; consequently, reset occurs on both CPU's at the same time. A different reset vector (RESA and RESB) exists for each CPU to allow initialization of the separate and independent programs.

Separate pins are used for the two processors' non-maskable interrupts (NMIA and NMIB). Each processor has its own NMI vector; CPU A uses NMIA Vector at FFFA and CPU B uses NMIB Vector at FFF2.

Three different types of external interrupt conditions can be detected by connecting the external signal to one of three Port F input pins. A positive-going edge, a negative-going edge, and an external interrupt request (IRQ), i.e., a low level, can be detected on PF0, PF1 and PF2, respectively. Internally, IRQ conditions can be generated by time-out of either of the two 16-bit counter/timers, upon interprocessor-communication request by the other CPU, or by the Host Interface Port.

In each case, the interrupt condition is reported as an interrupt flag in a control/status register associated with the functional area. Each CPU can either enable or disable IRQ generation by setting or resetting a corresponding interrupt enable bit in the same or associated control/status register.

Furthermore, each CPU can control whether or not its processing is interrupted when an interrupt request (IRQ) is generated. Each CPU has its own Processor Status Register (PSRA and PSRB) with the capability of disabling IRQ interrupts when its own "I flag" bit is a 1.

NEW AND MODIFIED INSTRUCTIONS

In addition to the standard R6502 instruction set, ten new instructions have been added and minor timing and other changes have been made to a few other instructions. All of these additions and changes are discussed in this section. Refer to the Instruction Set Op Code Matrix for the operation codes and addressing modes of all instructions. The times indicated for each instruction are given in terms of CPU clock-times.

UNSIGNED MULTIPLY (MUL)

The 10 clock-time hardware multiply instruction multiplies the 8-bit contents of the Y register by the 8-bit contents of the A register to give a 16-bit product. At the completion of the multiply operation, the most significant half of the product resides in the A register and the least significant half in the Y register. This operation uses unsigned numbers only. This instruction uses the implied addressing mode and, consequently, requires one byte for the op code.

SET MEMORY BIT (SMB m, ADDRESS.)

This instruction uses zero page addressing only and requires five cycle times. It sets the designated bit in the addressed memory cell or I/O port to a 1. The first byte of the two-byte instruction identifies the operation and the bit to be set while the second byte designates the address of the word in which the bit is to be set. Eight op codes are used for the eight bit locations in a byte.

RESET MEMORY BIT (RMB m, ADDRESS.)

This instruction operates in the same way as the SMB instruction except that the bit is set to 0.

BRANCH ON BIT SET RELATIVE (BBS m, ADDRESS, DESTINATION)

This instruction tests one of eight bits designated by a three-bit immediate field within the first byte of the instruction. The second byte designates the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction specifies the 8-bit relative address to which the

instruction branches if the bit tested is a 1. If the bit tested is not set to a 1, the next sequential instruction is executed. This instruction requires five cycles if the branch is not executed, six cycles if the branch executes to the same page, or seven cycles if it branches to a different page.

BRANCH ON BIT RESET RELATIVE (BBR m, ADDRESS, DESTINATION)

This instruction is similar to the BBS instruction except that the branch takes place if the bit tested is a 0.

INDEX REGISTER STACK OPERATIONS (PHX, PLX, PHY, AND PLY)

These instructions are similar to the PHA and PLA instructions in the conventional R6502 except that they push or pull the X or Y registers to and from the stack, respectively. The push instructions require three instruction cycles and the pull instructions require four cycles.

UNCONDITIONAL BRANCH (BRA)

This unconditional branch is a branch always instruction. It operates similar to the conditional branches of the R6502 except that the relative branch always occurs. It executes in three cycles if the branch is to the same page or four cycles if it is not. Two bytes are required, one for the op code and the other for the relative address.

INSTRUCTION DIFFERENCES FROM R6502

Decimal add and decimal subtract instructions on the R65C00/21 require one cycle time longer than their binary equivalents. The add and subtract times are the same for both decimal and binary operation on the R6502.

The decimal mode flag (D) in the processor status registers default to binary (D=0) operation when the R65C00/21 is RESET, whereas this bit is uninitialized on the R6502.

The indirect jump instruction increments the page address when the indirect pointer crosses a page boundary, whereas on the R6502 it does not.

PROCESSOR STATUS REGISTERS

Each CPU has its own 8-bit Processor Status Register. Each register contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the appropriate CPU. The R65C00/21 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

CARRY BIT (C)

The carry bit (C) can be considered the ninth bit of an arithmetic operation. It is set to a 1 if a carry from the eighth bit has occurred, or it is cleared to 0 if no carry has occurred, as a result of arithmetic or shift operations.

The carry bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instructions, respectively. Other operations which affect the carry bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

ZERO BIT (Z)

The zero bit (Z) is set to a 1 by the CPU during any data movements, or calculations, which sets all eight bits of the result to zero for that CPU. This bit is cleared to a 0 when all eight bits of a data movement, or calculation, operations are not all zero for that CPU. The R6500 instruction set contains no instruction to specifically set or clear the Z flag bit. The Z flag bit is, however, affected by the following instructions: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LSR, ORA, PLA, PLP, PLX, PLY, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

INTERRUPT DISABLE BIT (I)

The interrupt disable bit (I) controls the servicing of an interrupt request (IRQ). If the I bit is set to a 0 in the Processor Status Register of one, or both, of the CPU's, the IRQ signal will be serviced by that particular CPU. If the bit is set to a 1 for one or both of the CPU's, the IRQ signal will be ignored by that CPU. Each CPU will set its interrupt disable bit to a 1 if a RES, an IRQ, or its non-maskable interrupt (NMI) signal is detected. Interrupting one processor does not affect the other one unless it is programmed to respond to the same interrupt.

The I bit is cleared for each CPU when that CPU executes a Clear Interrupt Disable (CLI) instruction and is set under software control by a Set Interrupt Disable (SEI) instruction. This bit is also set by the Break (BRK) instruction. The Return From Interrupt (RTI) and Pull Processor Status (PLP) instructions also affect the I bit by setting it to the value which was stored on the stack.

DECIMAL MODE BIT (D)

The decimal mode bit (D) controls the arithmetic mode of its CPU. When this bit is set to a 1, the adder operates as a decimal adder for the Add with Carry (ADC) and the Subtract With Carry (SBC) instructions. These instructions, in the decimal mode, require one additional CPU cycle time compared with binary mode or the decimal mode in the conventional R6500. (In the conventional R6500, the decimal and binary arithmetic operations are the same speed.) When the bit is a 0, the arithmetic is performed in straight binary. The decimal mode is controlled only by the programmer for each of the CPU's. The Set Decimal Mode (SED) instruction causes decimal arithmetic to be performed and the Clear Decimal Mode (CLD) instruction causes binary arithmetic to be performed by that CPU. The PLP and RTI instructions also affect the decimal mode bit.

The D bit for each CPU is automatically set to the zero state (binary mode) when the R65C00/21 is reset by RES.

BREAK BIT (B)

The break bit (B) determines the type of condition which caused the IRQ service routine to be entered. If the IRQ service routine was entered because a BRK instruction was executed by its CPU, the B bit is set to a 1. If the service routine was entered because of an IRQ signal being generated, the B is set to a 0. There are no instructions which directly set or clear this bit.

OVERFLOW BIT (V)

The overflow bit (V) indicates that the result of a signed binary addition or subtraction operation is a value which cannot be contained in seven bits (outside the range of -128 to +127). This indicator only has meaning when signed arithmetic is performed. In this case, the arithmetic operations are being performed on the sign and seven magnitude bits for one byte, or the most significant byte of a longer signed number. When the ADC or SBC instruction is executed, the overflow bit is set to a 1 if the polarity of the sign bit is changed because the result exceeds +127 or -128 in absolute magnitude. Otherwise, the V bit is cleared to a 0. The V bit may be cleared by the programmer by executing a Clear Overflow (CLV) instruction in the appropriate CPU.

The overflow bit is also affected by the BIT instruction. The BIT instruction samples specific bits in memory or I/O interrupt status words. Most of the I/O devices used in the R6500 family and most of the interrupt flags in the R65C00/21 have interrupt flags in the upper two bits of the register. The BIT command copies these two most significant bits of the addressed word into the N and V flags. The V flag is set to the same state as bit 6 of the addressed words and the N flag copies bit 7.

The instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

NEGATIVE BIT (N)

The negative bit (N) indicates that the sign bit (bit 7) in the resulting value of a data movement or arithmetic operation is a 1. If the value represents a signed number, the most significant bit being a 1 indicates a negative number. If the sign bit is a 0, the result is interpreted as a positive value. The BIT instruction copies the most significant bit of the addressed memory cell or I/O register into the N flag bit.

There are no instructions that set or clear the N bit directly since the N bit represents only the status of a result. The instructions which produce a result that affects the state of the N bit are AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, PLX, PLY, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

Processor Status Registers (PSRA and PSRB)

7	6	5	4	3	2	1	0
NEG (N)	OVFL (V)	NOT USED	BRK (B)	DEC (D)	IRQ ENBL (I)	ZERO (Z)	CARRY (C)

Bit 7 Negative (N)¹
 1 Negative Value
 0 Positive Value

Bit 6 Overflow (O)¹
 1 Overflow Set
 0 Overflow Clear

Bit 5 Not Used (Don't care value)

Bit 4 Break Command (B)¹
 1 Break Command
 0 Non-break Command

Bit 3 Decimal Mode (D)³
 1 Decimal Mode
 0 Binary Mode

Bit 2 Interrupt Enable (I)²
 1 IRQ Interrupt Disable
 0 IRQ Interrupt Enable

Bit 1 Zero (Z)¹
 1 Zero Result
 0 Non-Zero Result

Bit 0 Carry (C)¹
 1 Carry Set
 0 Carry Clear

Notes:

1. Not initialized by $\overline{\text{RES}}$.
2. Set logic 1 by $\overline{\text{RES}}$.
3. Cleared to logic 0 by $\overline{\text{RES}}$.
4. There are two Processor Status Registers, one for each CPU.

INPUT/OUTPUT AND CONTROL/STATUS REGISTERS

REGISTER ADDRESSES

Table 2 shows the input/output, control/status and timer/counter registers which are addressed on page zero from locations 00 through 1D. Some of the registers combine other functions when they are read or written. The table lists both the primary and secondary types of functions. Table 3 summarizes the register formats.

All control/status registers and data direction registers are cleared to zero by a \overline{RES} . Thus, the zero state of each bit defines the default operating modes. Each register is associated with a functional area in the microcomputer, e.g., parallel input/output, timer/counter, bus control, etc. The detail operation of each register is defined in the appropriate sections.

Thirteen registers are used for input/output functions and nine registers used for timer/counter functions. The use of these registers is discussed in later sections.

Seven control/status registers control and monitor the basic operation of the R65C00/21. The registers and their primary functions are as follows:

BCR	Bus Control Register—defines expansion bus modes
HCSR	Host Control and Status Register—defines host bus and interrupts
ICSR	Interrupt Control and Status Register—enables and reports interrupt conditions
CIFR	Clear Interrupt Flags Register
PCR	Power Control Register—selects low power mode
TACSR	Timer A Control and Status Register—controls and monitors Timer A operation
TBCSR	Timer B Control and Status Register—controls and monitors Timer B operation

Table 2. I/O, Control/Status and Timer Registers

Address	Read	Write	Register Name/Notes
00	PA Data	PA Data	Port A Data I/O
01	PB Data	PB Data	Port B Data I/O
02	PC Data, 0→IBF ³	PC Data, 1→OBE, 0→RSO ³	Port C Data I/O
03	PC Data, 0→IBF ³	PC Data, 1→OBE, 1→RSO ³	Port C Data I/O
04	PD Data ¹	PD Data ¹	Port D Data I/O
05	—	PE Data ¹	Port E Data Output Only
06	PF Data	PF Data	Port F Data I/O
07	PG Data	—	Port G Data Input Only
08	—	PA Direction	Port A Direction
09	—	PB Direction	Port B Direction
0A	—	PC Direction	Port C Direction
0B	—	PC Direction	Port C Direction
0C	—	PD Direction ¹	Port D Direction
0D	—	—	—
0E	—	PF Direction	Port F Direction
0F	—	—	—
10	BCR	BCR	Bus Control Register
11	HCSR	HCSR	Host Control and Status Register
12	ICSR	ICSR	Interrupt Control and Status Register
13	—	CIFR	Clear Interrupt Flags Register
14	—	IPCIR	Inter-Processor Communication Interrupt Register
15	PCR	PCR	Power Control Register
16	TACSR	TACSR	Timer A Control and Status Register
17	LCA, UCA→SLA	LLA	Timer A Lower Counter (LCA)/Lower Latch (LLA)
18	SLA	ULA	Timer A Snapshot Latch (SLA)/Upper Latch (ULA)
19	SLA, 0→UFA ²	ULA, ULA→UCA, LLA→LCA, 0→UFA ²	Timer A Snapshot Latch (SLA)/Upper Latch, Download and Start Timer
1A	TBCSR	TBCSR	Timer B Control and Status Register
1B	LCB	LLB	Timer B Lower Counter (LCB)/Lower Latch (LLB)
1C	UCB	ULB	Timer B Upper Counter (UCB)/Upper Latch (ULB)
1D	UCB, 0→UFB ²	ULB, ULB→UCB, LLB→LCB, 0→UFB ²	Timer B Upper Counter (UCB)/Upper Latch (ULB), Download and Start Timer
1E	—	—	—
1F	—	—	—

Notes:

1. Addressed externally when in expanded bus mode.

2. Counter/Timer underflow flags:

UFA = Timer A Underflow Flag bit in TACSR

UFB = Timer B Underflow Flag bit in TBCSR

3. R65C00/21 to/from Host data transfer bits in HCSR:

IBF = Input Buffer Full flag bit

OBE = Output Buffer Empty flag bit

RSI = Register Select Input bit

RSO = Register Select Output bit

4. — = Not used—indeterminate data when read

Table 3. Control/Status Registers Formats Summary

Address (Hex)	Bit Number								
	7	6	5	4	3	2	1	0	
10	CPU A ACTIVE	NOT USED		PAGE ONE EXT	PORT A NIBBLE MODE		BUS EXTENSION MODE		BUS CONTROL REGISTER (BCR)
11	O/P BUFF FULL INT FLAG (OBF)	I/P BUFF FULL INT FLAG (IBF)	I/O REG SEL (RSI) (RSO)	NOT USED	I/OA INT ENBL I/OB INT ENBL	HOST INT ENBL	HOST BUS ENBL	HOST BUS TYPE	HOST CONTROL AND STATUS REGISTER (HCSR)
12	IPCA INT FLAG	PF2 LOW INT FLAG	PF1 NEG EDGE INT FLAG	PF0 POS EDGE INT FLAG	IPCA INT ENBL	PF2A INT ENBL	PF1A INT ENBL	PF0A INT ENBL	INTERRUPT CONTROL AND STATUS REGISTER (ICSR)
	IPCB INT FLAG				IPCB INT ENBL	IPCB INT ENBL	PF1B INT ENBL	PF0B INT ENBL	
13	CLR IPCA INT FLAG CLR IPCB INT FLAG	NOT USED	CLR PF1 NEG INT FLAG	CLR PF0 POS INT FLAG	NOT USED				CLEAR INTERRUPT FLAGS REGISTER (CIFR)
14	WRITE ONLY REGISTER—NO SPECIFIC BIT (IPCIR)								INTER- PROCESSOR COMMUNICATION INTERRUPT REGISTER (IPCIR)
15	NOT USED						LOW PWR CPU B (LPB)	LOW PWR CPU A (LPA)	POWER CONTROL REGISTER (PCR)
16	TMR A UNFL FLAG (UFA)	PF3 LEVEL IND	NOT USED	TMR A INT ENBL	TMR A CLK PRESC SEL	TIMER A MODE SELECT			TIMER A CONTROL AND STATUS REGISTER (TACSR)
1A	TMR B UNFL FLAG (UFB)	PF4 LEVEL IND	NOT USED	TMR B INT ENBL	NOT USED		TIMER B MODE SELECT		TIMER B CONTROL AND STATUS REGISTER (TBCSR)
Note: All control and status registers are cleared to zero by \overline{RES}									

Note: All control and status registers are cleared to zero by \overline{RES}

INTERRUPT CONTROL AND STATUS

Unlike other R6500 family devices, the R65C00/21 does not concentrate the interrupt flags into a single register. The R65C00/21, in general, places the interrupt flags in registers which also have to do with the control of the particular function which can cause the interrupt.

Interrupt enable control is located in the following registers:

HCSR Host Control and Status Register
ICSR Interrupt Control and Status Register

TACSR Timer A Control and Status Register
TBCSR Timer B Control and Status Register

Portions of each of these registers relating to interrupt enables are duplicated for each of the two CPU's. However, only one memory address has been allocated so that each CPU uses the same address to select its own interrupt enables. The specific details of the usage of the interrupt control bits are discussed in the corresponding functional area.

CLOCK CIRCUITS

CLOCK OSCILLATOR

The internal clock oscillator generates the system clock ($\phi 2$) which clocks all R65C00/21 operations. The system clock frequency ranges from 10 KHz to 4 MHz (the upper limit determined by the R65C00/21 part number) which is one-half the external crystal (or master clock) frequency. Each CPU in turn operates at one-half the system clock frequency (alternate cycles). All operations to memory or I/O take place at the system clock frequency. Since each CPU shares the common segments of the system on alternate system clock cycles, all internal operations occur at the system clock rate but, for CPU timing purposes, a CPU cycle rate of half the system rate is used. Thus with a 4 MHz crystal frequency, the system clock rate is 2 MHz and each CPU operates at an effective 1 MHz rate. Every two system clock periods sees one cycle devoted to CPU A and one cycle devoted to CPU B.

The $\phi 2$ clock is normally routed externally to clock external memory operations in the extended bus mode. A mask option allows the $\phi 2$ clock to be configured as an input so the R65C00/21 can operate in a slaved clock mode. In this case, the crystal input (XTALI) is grounded and crystal output (XTALO) is left open as shown in Figure 5.

LOW POWER OPERATION

The divide-by-128 clock prescaler operates in one of three ways (see Figure 6). One is the prescaler switched completely out which gives a system clock rate ($\phi 2$) at one-half of the crystal frequency. Another way is to select the low power operation for both CPUs which switches in the clock prescaler. The clock prescaler divides the system clock frequency by 128 to generate the prescaled system clock rate ($\phi 2PS$). This reduces the device power requirements and also reduces the counting rate of both counter/timers by a factor of 128. The third operating mode for the prescaler is to use it for prescaling Timer A only. This mode is discussed under the Counter/Timer Operation.

POWER CONTROL REGISTER (PCR)

Two bits in the Power Control Register (PCR) determine operation of the clock prescaler. Each CPU can set its own power control bit and read both of them. When both power control bits are a 1, the system switches to the low power operation at a clock rate of $\phi 2/128$ ($\phi 2PS$). The system reverts to normal power and speed when either power control bit is a 0 or when an enabled interrupt occurs. In the latter case, the system continues to operate at the low rate until the current instruction is completed, then it switches to the normal rate. The Power Control Register is shown in Figure 7.

NOTE

An enabled interrupt automatically clears the PCR bit for the affected CPU. It must be set again by software to resume low power mode.

Power Control Register (PCR)

7	6	5	4	3	2	1	0
NOT USED						LOW PWR CPU B (LPB)	LOW PWR CPU A (LPA)

Bits 7-2 Not Used (Don't care)

Bit 1	Low Power Mode Select for CPU B (LPB)
1	Low power mode requested by CPU B
0	Normal power mode requested by CPU B
Bit 0	Low Power Mode Select for CPU A (LPA)
1	Low power mode requested by CPU A
0	Normal power mode requested by CPU A

Notes:

- Both CPU's can read both bits.
- Each CPU can only write its power control bit.
- Both bits must be set to enable low power mode.

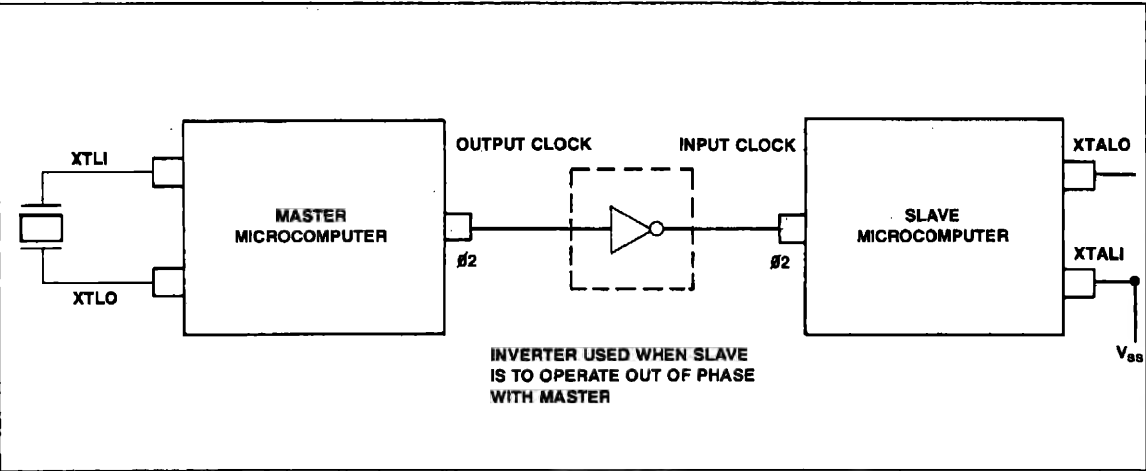


Figure 5. Master/Slave Clock Connection

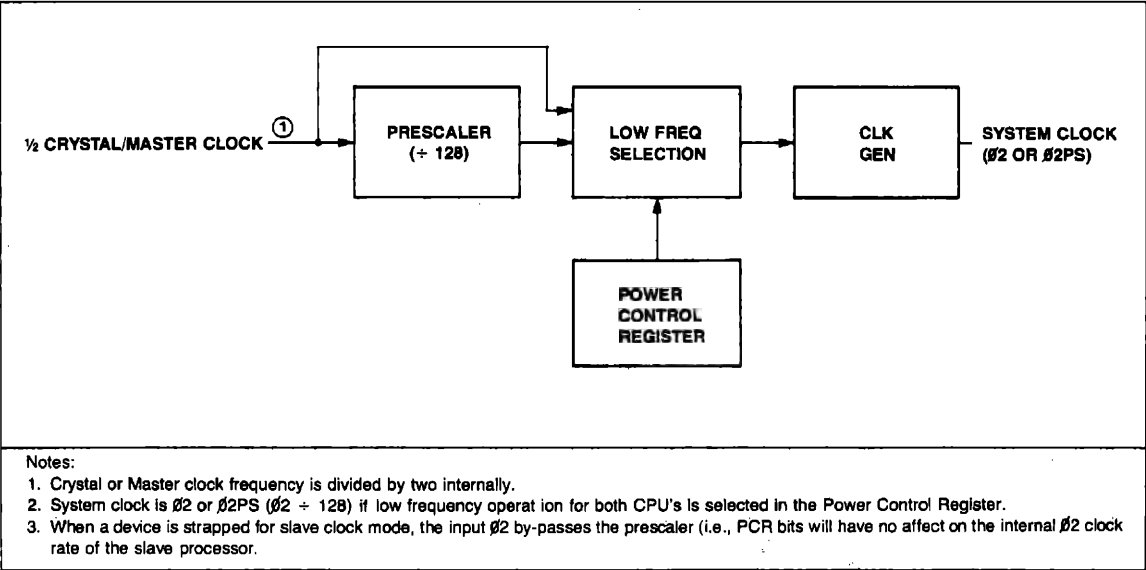


Figure 6. System Clock Operation

PARALLEL INPUT/OUTPUT PORTS

The R65C00/21 parallel input/output interface consists of five 8-bit, bidirection input/output ports, one 8-bit output only port, and one 4-bit input only port.

BIDIRECTIONAL PORTS A, B, C, D AND F

The five 8-bit bidirectional ports (Ports A, B, C, D and F) each have an associated data direction register which configures individual data ports for either input or output. Port E is output only and port G is input only, therefore, no data direction registers are required for these two ports.

OUTPUT MODE

If the data direction register for a particular bit position in a bidirectional port is a 1, that bit is defined as an output pin. The information written into each bit position of the data word is loaded into a latch. The information will remain in that latch until new data is transmitted to the data word or the power is shut off. The output latches are individually connected to output drivers for each bit position for which a corresponding bit in the data direction register is a 1. The output drivers are double-ended, push-pull type. The drivers force the output pins high ($\geq 2.4V$) if the output data bit is a 1, or low ($\geq 0.4V$) if the output data bit is a 0. The output drivers are TTL compatible.

INPUT MODE

If the data direction register for a particular bit position in a bidirectional port is 0, that bit position is defined as an input pin. When the input/output port is read via an LDA, LDX, LDY, ADC, SBC, ORA, AND, EOR, or a BIT instruction, all of the information on that port's pins are read into the corresponding register and processed as directed by the instruction. Since the input signal lines are at a "float" state, the logic level on them will be read as either a 1 or a 0 for that pin position. A low ($\geq 0.8V$) input causes a logic 0 to be read and a high ($\geq 2.0V$) input causes a logic 1 to be read. The output values can also be read (if the direction bit = 1) since the outputs are also on the pins. The input receivers are TTL compatible, are not latched, and are sampled near the end of each clock cycle $\phi/2$ and gated onto the internal bus when selected.

PORT A NIBBLE ADDRESSING

Whenever a port is shared as an output, care must be exercised that one CPU does not destroy the other CPU's output data. In general, this can be avoided by allocating complete output ports to each CPU so that there is no possibility of conflict. However, there may be some situations where at least one port must be shared for outputs to get the proper mix for the required application. Port A is slightly different from the other bidirectional ports to allow port A to be safely shared as an output port by both CPUs.

Port A is divided into two 4-bit "nibble ports". Each half (nibble) of Port A may be independently addressed by each CPU as defined by two bits in the Bus Control Register (BCR2 and BCR3) as described in Bus Extension and Host Interface section. Depending upon the control bits, either CPU may be

assigned to write to both halves, write to neither half (only read—the other CPU writes to the whole register), write to top half, or write to bottom half. When a mode has been selected for writing to only one-half of the port, the other half is unaffected.

ALTERNATIVE MODES OF OPERATION

Bidirectional Ports C, D, and F all have alternative modes of operation which may be selected in lieu of the bidirectional port capabilities.

Port C is a data bus for a host computer when the R65C00/21 is being used as a programmable peripheral device. This is discussed in more detail under Bus Extension and Host Interface.

Port D is a multiplexed data bus (D0 through D7) and address bus (A0 through A7) when the R65C00/21 is used as a microcomputer with external memory and I/O devices. This is also detailed under Bus Extension and Host Interface.

Port F also has the capability of operating in conjunction with other segments of the R65C00/21 architecture as described below.

PORT F CONTROL AND STATUS

The Interrupt Control and Status Register (ICSR) and the Clear Interrupt Flags Register (CIFR) control and monitor the operation of the Port F external interrupts (bits 2, 1, 0) as well as inter-processor communication interrupts.

When the PF0 edge-sensitive circuit detects a positive transition, bit 4 of the ICSR is set to a 1. An internal interrupt request (IRQ) is generated to a CPU whenever this bit is set and the corresponding PF0 Interrupt Enable Flag (ICSR bit 0) is set to a 1 for that CPU. Similarly, a negative going transition on PF1 sets the edge detect flag in ICSR bit 5. ICSR bit 1 is the corresponding PF1 Interrupt Enable bit. As in all cases of the interrupt enable bits, each CPU has its own set, addressed at the same location, but held separately.

Port F signal PF2 has an external interrupt request (\overline{IRQ}) capability. When this signal goes low, bit 6 of the Interrupt Control and Status Register is set and remains set as long as the signal is low. If the corresponding PF2 Interrupt Enable bit (bit 2) in its segment of the Interrupt Control and Status Register is a 1 while the PF2 Low Interrupt bit (bit 6) is a 1, an interrupt request is generated.

Each CPU may thus control the external interrupt independently of the internal interrupts. If the I flag in the Processor Status Register of a particular CPU is a 1, no \overline{IRQ} 's will be honored. If the I flag is a 0 and that CPU's interrupt enable in bit 2 of the Interrupt Control and Status Register is a 0, only internal interrupts will interrupt that CPU. If bit 2 is a 1, any \overline{IRQ} will be honored.

The Port F signals PF3 and PF4 can be used as external interfaces for Counter/Timers A and B, respectively (refer to the Counter/Timers description). Finally, PF7 can be used as an active-low interrupt to a host processor. The operation of the R65C00/21 with a host processor is discussed under Bus Extension mode.

The Inter-Processor Communication Interrupt (IPCA and IPCB) bit in the ICSR allows each CPU to interrupt the other CPU if all of the other normal IRQ conditions are correct. CPU A sets the IPCB Interrupt Flag in CPU B's Interrupt Control and Status Register and CPU B sets the IPCA Interrupt Flag in CPU A by any write to location 0014, the Inter-Processor communications Interrupt Register. This is not an actual register, but writing any value here sets the other CPU IPCI flag. This inter-processor communications is illustrated in Figure 7.

Interrupt Control And Status Register (ICSR)

7	6	5	4	3	2	1	0
IPCA INT FLAG	PF2 LOW INT FLAG	PF1 NEG EDGE INT FLAG	PF0 POS EDGE INT FLAG	IPCA INT ENBL	PF2A INT ENBL	PF1A INT ENBL	PF0A INT ENBL
IPCB INT FLAG				IPCB INT ENBL	PF2B INT ENBL	PF1B INT ENBL	PF0B INT ENBL

Bit 7 Inter-Processor Communication (IPC) Interrupt Flag (A or B)

- 1 An inter-processor interrupt is requested by the other CPU
- 0 No internal interrupt is requested

Bit 6 PF2 Low Interrupt Flag (A and B)

- 1 PF2 is low
- 0 PF2 is high

Bit 5 PF1 Negative Edge Detect Interrupt Flag

- 1 A positive-to-negative transition on PF1 occurred
- 0 No positive-to-negative transition on PF1 occurred

Bit 4 PF0 Positive Edge Detect Interrupt Flag

- 1 A positive-to-negative transition on PF0 occurred
- 0 No positive-to-negative transition on PF0 occurred

Bit 3 Inter-Processor Communication Interrupt Enable (A or B)

- 1 Enables inter-processor communication interrupt (bit 7)
- 0 Disables inter-processor communication interrupt (bit 7)

Bit 2 PF2 Interrupt Enable (A or B)

- 1 Enables PF2 interrupt (bit 6)
- 0 Disables PF2 interrupt (bit 6)

Bit 1 PF1 Interrupt Enable (A or B)

- 1 Enables PF1 interrupt (bit 5)
- 0 Disables PF1 interrupt (bit 5)

Bit 0 PF0 Interrupt Enable (A or B)

- 1 Enables PF0 interrupt (bit 4)
- 0 Disables PF0 interrupt (bit 4)

CLEAR INTERRUPT FLAGS REGISTER (CIFR)

The Clear Interrupt Flags Register (CIFR) is similar to the ICSR in that only one address is used but the bit pattern operates only on the status bits for its own processor. Thus only CPU A may clear IPCA but either may clear the edge detection flag bits. Bit 6 will only be cleared when the signal on PF2 goes high. Actually, the Clear Interrupt Flags Register is not a register at all, but addressing a bit pattern to this location performs the function. Any bit to which a zero is written will clear the corresponding interrupt flag. A read of this word returns logic one's so that the new Reset Memory Bit instructions may be used to clear these flags.

Clear Interrupt Flags Register (CIFR)

7	6	5	4	3	2	1	0
CLR IPCA INT FLAG	NOT USED	CLR PF1 NEG INT FLAG	CLR PF0 POS INT FLAG	NOT USED			
CLR IPCB INT FLAG							

Bit 7 Clear Inter-Processing Communication Interrupt Flag

- 1 Has no effect on the IPC Flag
- 0 Clears the IPC Interrupt Flag (specific CPU, A or B)

Bit 6 Not Used

Bit 5 Clear PF1 Interrupt Flag

- 1 Has no effect on the PF1 Interrupt Flag
- 0 Clears the PF1 Interrupt Flag (either CPU)

Bit 4 Clear PF0 Interrupt Flag

- 1 Has no effect on the PF0 Interrupt Flag
- 0 Clears the PF0 Interrupt Flag (either CPU)

Bit 3-0 Not Used

OUTPUT ONLY PORT E

The output characteristics of Port E are identical to that of the bidirectional ports. The main difference is that there is no data direction register and also no capability of reading the information being output. Attempting to read Port E loads indeterminate data onto the internal bus.

Port E is a dual function port which, in addition to being an output port, can also serve as address bits A15 through A8 when the R65C00/21 is addressing external memory and I/O devices. This is discussed in more detail under Bus Extension and Host Interface.

INPUT ONLY PORT G

The input characteristics of the 4-bit Port G are the same as a bidirectional port in an input mode. The difference is that only four bits are input into the least significant bits of the data register and the most significant bits are loaded as zeros.

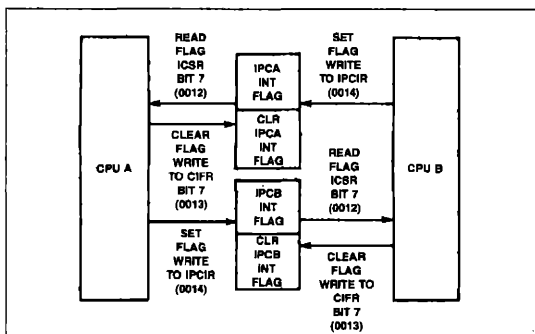


Figure 7. Inter Processor Communication

COUNTER/TIMERS

There are two separate 16-bit counter/timer systems in the R65C00/21: Counter/Timer A and Counter/Timer B. The block diagram of the counter/timers (also referred to as the timers, the counters, Timer A, or Timer B) is shown in Figure 8. Timer A has eight operating modes and five registers while Timer B has four operating modes and four registers. Both counter/timers have a 16-bit counter comprised of two 8-bit segments: Lower

Counter (LCA and LCB, where A and B refer to Counter/Timer A and B) and Upper Counter (UCA and UCB). Both counter/timers also have a 16-bit latch section consisting of two 8-bit segments: Lower Latch (LLA and LLB) and Upper Latch (ULA and ULB). In addition, only Timer A has an 8-bit Snapshot Latch (SLA) register.

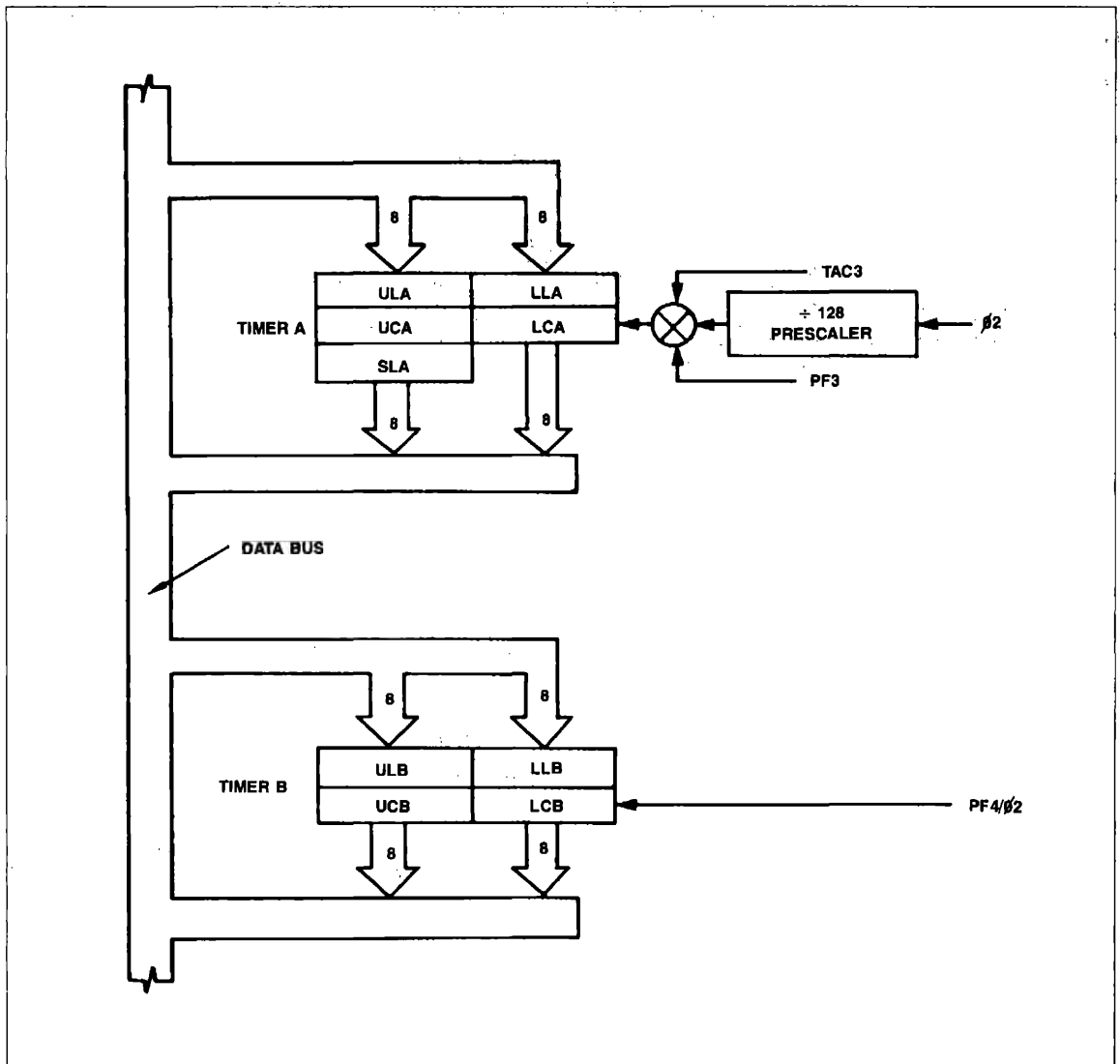


Figure 8. Counter/Timer Block Diagram

Data are written to the latches which act as holding registers for loading or reloading the initial counter/timer values upon mode initiation or counter/timer restart.

Both timers count down from the pre-set latch value and set an appropriate underflow flag when the counter counts through zero. The counter actually never counts below zero. At the time the counter would go negative, the contents of the latches replace the count value with no time delay.

Each counter/timer has three addresses for accessing the five (Counter/Timer A) or four (Counter/Timer B) 8-bit registers in its system. Consequently, the R/W line also aids in addressing the registers. Reading or writing to specific registers may also have other effects such as clearing an interrupt flag or transferring latch data to the counter. Consult the input/output and control register memory map in Table 2 for the effects of reading or writing to specific registers in the two counter/timer systems.

Each counter/timer has operating modes which are clocked either at the system clock rate ($\phi 2$) or an external event clock rate. In addition, Timer A can operate with a prescaled $\phi 2/128$ clock rate.

COUNTER/TIMER A (TA)

Counter/Timer A, with its four additional modes and Snapshot Latch, is generally more flexible than Counter/Timer B.

The Snapshot Latch (SLA) solves a problem which sometimes occurs when a timer is read. The problem is that between the time when the low byte of the 16-bit counter is read and the time when the high byte is read it is possible for the high byte to have been decremented. The resulting 16-bit value would, in this case be incorrect. In many modes of timer, the values are not actually read but the zero count transition is important. These types of applications do not require the use of the Snapshot Latch register. If the timer count value is to be used directly from a running timer, however, the Timer A Snapshot Latch should be used.

Timer A overcomes the problem stated above by sampling the value of the upper counter byte into the Snapshot Latch every time the lower counter byte is read. The value of the Upper Counter can be obtained by first reading the Lower Counter at address 0017, then reading the Snapshot Latch at address 0018 or 0019. Note that reading address 0019 also resets the Timer A Underflow (UFA) flag.

A second architectural difference between the two timers is that Timer A can have its clock input scaled down by a factor of 128 during normal power operation. This allows Timer A to measure longer periods of time internally while the microcomputer is operating at the $\phi 2$ system clock rate. With a 4 MHz system clock, more than two second time intervals (up to 2.097 seconds) can be measured directly without any software intervention. Without the prescaler, 16.384 ms is the longest time interval at 4 MHz.

Timer A Mode Control

The operation of Timer A is controlled and monitored by the Timer A Control and Status Register (TACRS).

Bits 0-2 select the Timer A mode of operation.

Bit 3, when set to a 1, causes the clock prescaler to be switched into the circuit so that the timer may count longer intervals in modes which allow it.

Timer A Interrupt Enable, TACSR bit 4, if set to a 1 by a CPU, enables generation of an internal $\overline{\text{IRQ}}$ to that CPU when the UFA flag is set.

Bit 6 copies bit 3 of Port F (PF3) as this bit has several different uses with Timer A. However, when Timer A is not using this bit it may be used as any other input or output bit. In any event, bit 3 of the Port F Data Direction Register must be set appropriately, for either input or output, whether or not it is used with Timer A.

Bit 7 is the UFA bit which indicates that Timer A has counted down through zero. This may be detected by reading the bit or may be used to cause an $\overline{\text{IRQ}}$ interrupt if bit 4 of the TACSR is set to a 1. The UFA flag is reset to a 0 by reading SLA or writing ULA at address 0019.

Timer A Control And Status Register (TACSR)

7	6	5	4	3	2	1	0
TMR A UNFL FLAG (UFA)	PF3 LEVEL IND	NOT USED	TMR A INT ENBL	TMR A CLK PRESC SEL	TIMER A MODE SELECT		

Bit 7 Timer A Underflow Flag (UFA)

1 Underflow condition occurred
0 No underflow

Bit 6 Port F Bit 3 (PF3) Level

1 PF3 High
0 PF3 Low

Bit 5 Not Used (Don't care)

Bit 4 Timer A Interrupt Enable

1 Enable Timer A Interrupt
0 Disable Timer A Interrupt

Bit 3 Timer A Clock Prescaler Enable¹

1 Enable Clock Prescaler ($\phi 2/128$)
0 Disable Clock Prescaler ($\phi 2$)

Bits 2 to 0 Timer A Mode Select (TAMS)

2	1	0	
0	0	0	Timer A Off
0	0	1	Free-Run Event Counter Mode ¹
0	1	0	Free-Run Pulse Width Measurement Mode ¹
0	1	1	Retriggerable One-Shot Timer Mode ¹
1	0	0	One-Shot Interval Timer Mode
1	0	1	Free-Run Interval Timer Mode
1	1	0	One-Shot Pulse Generation Mode
1	1	1	Free-Run Pulse Generation Mode

Note:

1. Prescaler must be disabled (bit 3=0) for Free-Run Event Counter Mode, Free-Run Pulse Width Measurement Mode, and Retriggerable One-Shot Timer Mode. These three modes do not allow prescaling.

Timer A Operating Modes

The Timer A mode of operation is selected by setting bits 0-2 of the Timer A Control and Status Register (TACSR) to the appropriate code.

Timer A Off, Mode 0

Timer A is turned off in this mode. The Timer A Underflow Flag (UFA) stays at its current state. The counter holds its current value and may be read. Writing to the registers performs the usual functions associated with that address but the counter remains stopped. This is the default condition.

Timer A Free-Run Event Counter, Mode 1

The Timer A Upper Counter (UCA) and Lower Counter (LCA) is loaded with the Timer A Upper Latch (ULA) and Lower Latch (LLA) value when the data is written to the Timer A Upper Latch at address 0019. Timer A then decrements by 1 at each negative transition of the signal on input Port PF3. (The Port F data direction register must have a 0 in bit 3.) The Timer A Underflow Flag (UFA) is set to 1 when the counter decrements below zero. At this same time, the latch value is reloaded into UCA and LCA. The maximum rate of the signal on PF3 which may be detected is one-half of the $\phi 2$ system clock rate.

Timer A Free-Run Pulse Width Measurement, Mode 2

Writing to ULA at 0019 transfers the 16-bit latch to the counter which operates as a timer in this mode. The initial value in the timer is decremented at the $\phi 2$ rate when the PF3 signal is low. Otherwise, the counter holds its value. Counting stops when the PF3 signal goes high and will resume if the signal goes low again. If the counter counts below zero, the counter initial value is reloaded from the latches and the UFA flag is set.

Timer A One-Shot Retriggerable Timer, Mode 3

This mode is similar to Mode 4 except that the timer restarts each time PF3 goes through a high-to-low transition and counts down until the counter goes through zero. A second difference is that the clock prescaler may not be used with this mode. The data direction register bit 3 (PF3) must be zero to select input.

Timer A One-Shot Interval Timer, Mode 4

Writing to ULA at 0019 transfers the initial value from the latches and starts the timer. The timer counts at either the $\phi 2$, or scaled $\phi 2$ ($\phi 2/128$), rate. When the counter counts through zero, the latch value is transferred to the counter, the UFA flag is set and the counter stops counting.

Timer A Free-Run Interval Timer, Mode 5

Writing ULA at 0019 transfers the 16-bit latch value to the timer and starts it running. The counter counts down at either the $\phi 2$, or the scaled $\phi 2$ ($\phi 2/128$), rate. When the counter counts through zero the UFA flag is set, the value in the latches is transferred to the counter, and the counter continues to count down.

Timer A One-Shot Pulse Generation, Mode 6

The PF3 data direction register bit must be set to a 1 before starting this mode to initially force a high output. Writing ULA at 0019 starts the timer and clears the PF3 data output bit to a 0 causing a low output. The PF3 output remains low until the timer counts through zero. At this time, the PF3 output goes high until the mode is restarted or a new mode is selected. The UFA flag is also set at this time and the counter is stopped. The timer counts at either the $\phi 2$, or the scaled $\phi 2$ ($\phi 2/128$), rate.

Timer A Free-Run Pulse Generation, Mode 7

The data direction register for PF3 must be set to a 1 to select the PF3 output before starting this mode. Writing to ULA at 0019 sets PF3 to 0 forcing a low output and starts the timer. Each time the timer counts through zero, the PF3 output changes state to generate a square wave at a rate dependent upon the latch value. The timer counts at either $\phi 2$, or the scaled $\phi 2$ ($\phi 2/128$), rate. Each time the counter counts through zero, the latch contents are automatically transferred to the timer registers and the UFA flag is set.

COUNTER/TIMER B (TB)

Timer B is a simpler timer than Timer A but it still retains great flexibility. Unlike Timer A, there is no "off" mode (the default mode is the Free-Run Interval Timer Mode) and there is no separate selectable clock prescaler. All counting (except for counting external events) is done either at the $\phi 2$ clock rate or $\phi 2/128$ rate (when low power mode is selected). Another difference is that Timer B does not have the snapshot latch register for freezing the upper timer byte for reading. However, in its normal modes the counter counts through zero to set the Underflow Flag B (UFB) so that a snapshot latch register is not required.

Timer B Mode Control

The operation of Timer B is controlled and monitored by the Timer B Control and Status Register (TBCSR).

Bits 0-1 select the Timer B operating mode.

Timer B Interrupt Enable, bit 4, when set to a 1 by a CPU, enables generation of an internal interrupt request (IRQ) to that CPU when the UFB flag is set.

Bit 6 of the TBCSR copies bit 4 of Port F (PF4) as this bit has several different uses with Timer B. However, when Timer B is not using this bit it may be used as any other input or output bit. In any event, bit 4 of the Port F Data Direction Register must be set appropriately for either input or output whether or not it is used with Timer B.

Bit 7 in the TBCSR is the UFB bit which indicates that Timer B has counted down through zero. This may be detected by reading the bit or may be used to cause an IRQ interrupt if bit 4 of the TBCSR is set to a 1. The UFB bit is reset by either reading UCB or writing to ULB at address 001D.

Timer B Control and Status Register (TBCSR)

7	6	5	4	3	2	1	0
TMR B UNFL FLAG (UFB)	PF4 LEVEL IND	NOT USED	TMR B INT ENBL	NOT USED		TIMER B MODE SELECT	

<u>Bit 7</u>	Timer B Underflow Flag (UFB)
1	Underflow condition occurred
0	No underflow
<u>Bit 6</u>	Port F Bit 4 (PF4) Level Indicator
1	PF4 High
0	PF4 Low
<u>Bit 5</u>	Not Used (Don't care)
<u>Bit 4</u>	Timer B Interrupt Enable
1	Enable Timer B Interrupt
0	Disable Timer B Interrupt
<u>Bits 3-2</u>	Not Used (Don't care)
<u>Bits 1-0</u>	Timer B Mode Select (TMS)
1 0	
0 0	Free-Run Interval Timer Mode
0 1	Free-Run Pulse Generator Mode
1 0	Event Counter Mode
1 1	Pulse Width Measurement Mode

Timer B Operating Modes

The Timer B operating mode is selected by setting bits 0 and 1 in the TBCSR to the appropriate code.

Timer B Free-Run Interval Timer, Mode 0

Writing to Timer B Upper Latch (ULB) at 001D transfers the 16-bit latch value to the timer and starts it running. The counter counts down at the $\phi/2$ rate. When the counter counts through

zero, the Timer B Underflow Flag (UFB) is set to a 1, the value in the latches is transferred to the counter and the counter continues to count down.

Timer B Free-Run Pulse Generation, Mode 1

The data direction register for PF4 must be set to a 1 to select PF4 output before starting this mode. Writing to ULB at 001D sets PF4 to 0 to force the PF4 output low and starts the timer. Each time the timer counts through zero, the PF4 output changes state to generate a square wave at a rate dependent upon the initial value loaded into the latches. The timer counts at the $\phi/2$ rate. Each time the counter counts through zero, the latch values are automatically transferred to the timer registers and the UFB flag is set to a 1.

Timer B Event Counter, Mode 2

The data direction register bit for PF4 must be set to a 0 to select PF4 input prior to selecting this mode. The counter is loaded with the latch value when the ULB data is written to address 001D. Timer B then decrements by 1 at each negative transition on input Port PF4. The Timer B Underflow Flag (UFB) is set to a 1; when Counter B counts through zero. At this same time, the latch value is reloaded into Timer B. The maximum rate of the signal on PF4 which may be detected is one-half of the $\phi/2$ clock rate.

Timer B Pulse Width Measurement, Mode 3

Writing to ULB at 001D transfers the 16-bit latch value to the counter. The initial value in the timer is decremented at the $\phi/2$ rate when the PF4 signal is low. Each time the PF4 signal goes high, the counter stops and then continues when the signal is low again. If the counter counts through zero, the UFB flag is set to 1 and the latch value transfers to reinitialize the counter and the countdown continues as long as PF4 is low.

BUS EXTENSION

In addition to its application as a single-chip microcomputer, the bus extension mode allows the R65C00/21 to operate as a microprocessor with external memory and I/O.

BUS EXTENSION MODE

When the R65C00/21 is used as a single-chip microcomputer, all of the output ports may be used as input or output ports. However, to use the R65C00/21 with external ROM, RAM, or I/O, a number of the ports act as extensions of the internal address and data buses. Specifically, Port D becomes dedicated as a multiplexed 8-bit data and address bus. Port D provides both the data bus (D0 through D7) and the low bits of the address (A0 through A7) on pins PD0 through PD7. When a bus extension mode is selected, the Port D Data Direction Register must be cleared to zero (its default condition) to configure Port D as all inputs. The R65C00/21 then controls Port D as an extension of the internal bus structure and provides an active-low External Memory Select (EMS) strobe signal at the time the address bits are available. The EMS signal is present even when Port D is being used as a normal input/output register.

The R65C00/21 has the option of using 8-, 12- or 16-bit address bus extensions. Selection of the bus extension mode is controlled by bits 0 and 1 of the Bus Control Register (BCR). When the 8-bit mode is selected, only the Port D multiplexed address/data bus function is required. However, if either the 12- or 16-bit address bus extension is selected, either one half or all of output Port E also becomes dedicated to the bus extension function. If a 16-bit bus extension is selected, then all of Port E becomes the upper address bits A8 through A15 on pins PE0 through PE7, respectively. If the 12-bit bus extension is selected, then the address lines A8 through A11 appear on PE0 through PE3. In this case, PE4 through PE7 have their usual output function.

Since Port D is multiplexed, it is necessary that external latches be supplied to hold the lower eight bits of the address bus. The EMS output is low when the address is being supplied from Port D. All of the other necessary control bus signals are also provided; these include $\phi 2$ and R/W. The SYNC and ϕA signals are also brought out for use by development systems and bus analyzers for system debugging.

In a one-chip configuration, the 128 bytes of internal page one RAM (address 0180 through 01FF), is logically combined with page (0080-00FF). However, when an extended bus is used, the stack page may be addressed in its normal range in external memory (0100-01FF). When bit 4 of the Bus Control Register is a 0, page one is internal and shared with page zero; when it is a 1, page one is external allowing full 256 bytes available to the two stacks.

Figure 9 is an overall block diagram of a system using the R65C00/21 in the bus extension mode.

The CPU A Active signal (bit 7 of the BCR) is high when CPU A is controlling the system bus, and low when CPU B is active. This bit copies the state of the ϕA output signal. Consequently, the bit may be sampled in common subroutines to determine the calling CPU, or for bank selection purposes. Thus, CPU A and CPU B may have some external memory or I/O dedicated to their exclusive use. Each may separately address as much as 59.5K bytes of external memory map, or external memory may be shared.

Bus Control Register (BCR)

7	6	5	4	3	2	1	0
CPU A ACTIVE	NOT USED		PAGE ONE EXT	PORT A NIBBLE MODE		BUS EXTENSION MODE	

Bit 7

1 CPU A Active
0 CPU B Active

Bits 6-5

Not Used (Don't Care)

Bit 4

1 Page One External/Internal Mapping
0 Page One Internal

Bits 3-2

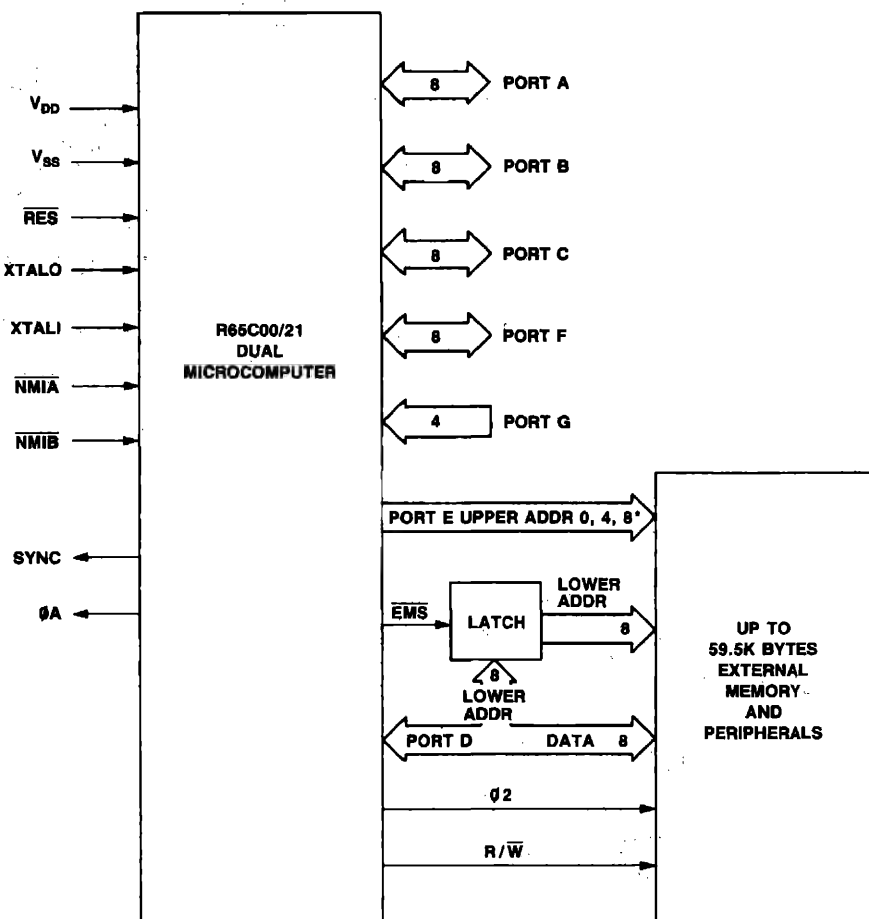
3 2
0 0 CPU A writes to both halves (PA0-PA7).
0 1 CPU A writes to upper half (PA4-PA7); CPU B writes to lower half (PA0-PA3).
1 0 CPU A writes to lower half (PA0-PA3); CPU B writes to upper half (PA4-PA7).
1 1 CPU B writes to both halves (PA0-PA7).

Bits 1-0

1 0
0 0 Bus Extension Mode not selected.
0 1 8-bit Address Extension Mode. Range equals 256.
1 0 12-bit Address Extension Mode. Range equals 4096.
1 1 16-bit Address Extension Mode. Range equals 65,536.

Note:

*Either CPU may read the full port at any time.



NOTE:

*UPPER ADDRESS EXTENSION MAY BE 0, 4 OR 8 LINES.

Figure 9. Bus Extension Mode Block Diagram

PROGRAMMABLE PERIPHERAL TO A HOST MODE

An overall block diagram of a system using an R65C00/21 as an intelligent controller is shown in Figure 10.

In this configuration, three of the R65C00/21 input/output ports have special significance. Port C becomes the interface with the host data bus (Port C's Data Direction Register must specify as the input; i.e., all zeros). Pin PF7 becomes an active-low Host Interrupt ($\overline{\text{HINT}}$) line, and the 4-bit input Port G becomes the control pins interface to the Host computer.

The R65C00/21 is configured to operate as a peripheral for either the R6500 or 6800 families, or the Z80 or 8080 families. When operating in the 6500/6800 mode, PG0 is an input for the host $\overline{\text{O2}}$ ($\text{H}\overline{\text{O2}}$) and PG1 is the input for the host R/W (HRW) control lines.

When operating in the Z80/8080 mode, PG0 accepts the host $\overline{\text{RD}}$ (HRD) control and PG1 provides the host WR (HWR) control.

In both cases, PG2 serves as a register select (HRS) and PG3 acts as an active-low chip select ($\overline{\text{CS}}$) from the host. HRS is used in conjunction with the $\overline{\text{CS}}$ and HWR to control reading or writing of data or status information as shown in Table 4.

Control of the host mode options is provided by the Host Control and Status Register (HCSR).

When the host writes a byte into the Input Buffer (Port C), the Input Buffer Full (IBF) flag is set to a 1. Similarly, when a byte is read from the Output Buffer (Port C) by the host, the Output Buffer Full (OBF) flag is cleared to a 0. Setting bit 3 of the HCSR enables generation of an internal interrupt request (IRQ) when either the IBF flag is a 1 or the OBF flag is a 0. This logic is duplicated for both CPU's.

Setting bit 2 of the HCSR to a 1 enables generation of any interrupt signal to the host computer. In this case, bit 7 of Port F is pulled low by either a write to Port C (Output Buffer) or a read from Port C (Input Buffer), by either of the R65C00/21 CPU's.

Bit 5 of the HCSR is actually two different bits representing Register Select Input (RSI) and Register Select Output (RSO). The R65C00/21 writes bit RSO and reads bit RSI, while the host writes RSI and reads RSO. The R65C00/21 writes a 0 to this bit when Port C is addressed at 0002 and a 1 when Port C is addressed at 0003. When the host writes to the R65C00/21 through Port C, the level of the HRS input is copied into the RSI bit. This bit allows the communications between the host system and the R65C00/21 to flag the type of data being transferred so that command information may be distinguished from data.

Table 4. Register Select Control

CS (PG3)	HRS (PG2)	HRW (PG1)	H $\overline{\text{O2}}$ (PG0)	Host Function (6500/6800 Mode)
H	—	—	—	Host Interface Deselected
L	L	L	H	Write Input Buffer, HCSR5 RSI cleared, set IBF
L	L	H	H	Read Output Buffer, Clear OBF
L	H	L	H	Write Input Buffer, HCSR5 RSI set, set IBF
L	H	H	H	Read upper 3 bits of HCSR; OBF, IBF & RSO
CS (PG3)	HRS (PG2)	HWR (PG1)	HRD (PG0)	Host Function (8080/Z80 Mode)
H	—	—	—	Deselected
L	L	L	H	Write Input Buffer, HCSR5 RSI cleared, set IBF
L	L	H	H	Read Output Buffer, Clear OBF
L	H	L	L	Write Input Buffer, HCSR5 RSI set, set IBF
L	H	H	L	Read upper 3 bits of HCSR; OBF, IBF & RSO

Host Control and Status Register (HCSR)

7	6	5	4	3	2	1	0
O/P BUFF FULL INT FLAG (OBE)	I/O BUFF FULL INT FLAG (IBF)	I/O REG SEL (RSI) (RSO)	NOT USED	I/OA INT ENBL I/OB INT ENBL	HOST INT ENBL	HOST BUS ENBL	HOST BUS TYPE

Bit 7 Output Buffer Empty (OBE) Flag

- 1 Output Buffer Full
- 0 Output Buffer Empty

Bit 6 Input Buffer Full (IBF) Flag

- 1 Input Buffer Full
- 0 Input Buffer Empty

Bit 5 Register Select

Distinguishes commands from data. Host reads RSO and R65C00/21 reads RSI. Selection of 1 or 0 to represent commands or data is user defined.

Bit 4 Not Used. (Don't care)

Bit 3 Input/Output Buffer Interrupt Enable

- 1 Enable IRQ IBF = 1)
- 0 Disable IRQ

Bit 2 Host Interrupt ($\overline{\text{HINT}}$) Output Enable

- 1 Disable $\overline{\text{HINT}}$ Output to Host
- 0 Enable $\overline{\text{HINT}}$ Output to Host (OBF = 1)

Bit 1 Host Bus Enable

- 1 Disable Host Bus
- 0 Enable Host Bus

Bit 0 Host Bus Type

- 1 Host Bus is Z80/8080
- 0 Host Bus is 6500/6800

Note:

Register is cleared to all zeros by $\overline{\text{RES}}$.

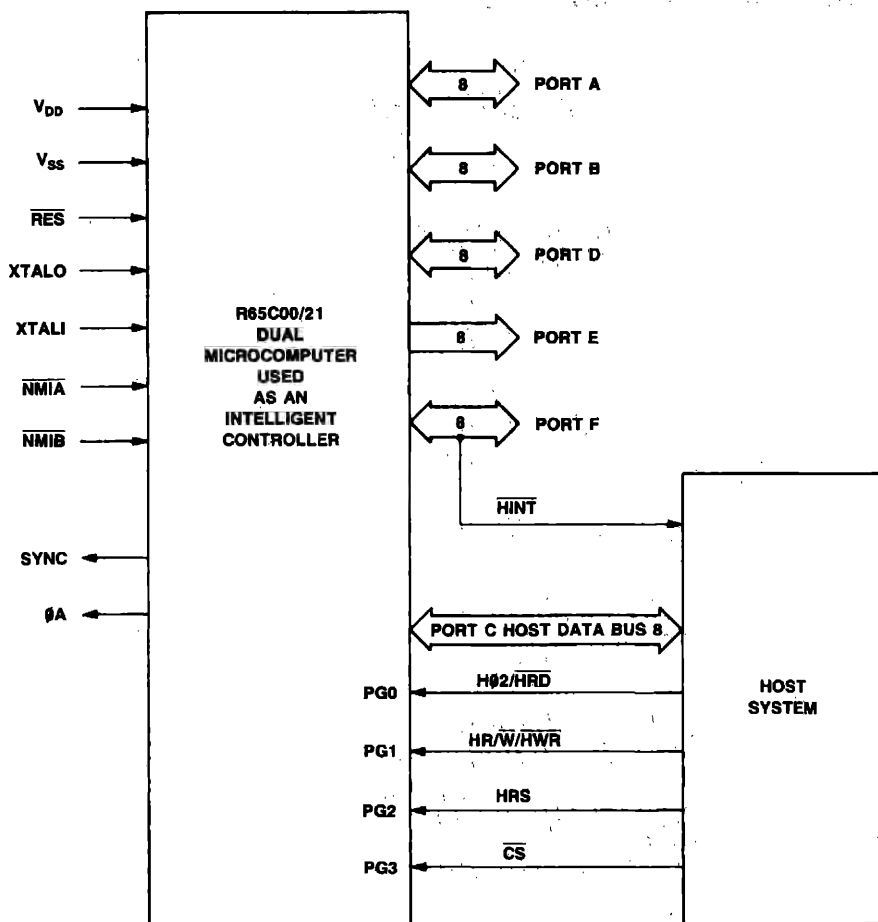


Figure 10. Host Mode Block Diagram

EMULATION MODE

The R65C00/21 can operate in an emulation mode under external signal control.

Emulation mode deselects the internal ROM and enables the 16-bit Expanded Bus mode, independent of the bus mode programmed in the Bus Control Register. Since the Expanded Bus mode uses peripheral Ports D and E, provision is made for these to be emulated in external hardware. This is accomplished by forcing all memory references to Ports D and E to be External Bus cycles. Accesses to the Data Direction Register for Port D are also forced external.

To further aid program development in emulation mode, all bus cycles which perform a memory or I/O write operation, whether the true destination is internal or external, will assert the External Memory Strobe (EMS) signal. This allows a copy of internal register and memory values to be kept in external memory.

Emulation mode is selected by applying the Ø2 output clock signal to the RES input pin.

INSTRUCTION SET IN ALPHABETIC SEQUENCE

The following table contains a summary of the R65C00/21 and R65C29 CPU instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Order No. 202.

The instructions notated with a * are added instructions for the R65C00/21 and R65C29 which are not part of the standard 6502 instruction set.

Instruction Set in Alphabetic Sequence

Mnemonic	Description	Mnemonic	Description
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
*BRA	Branch Always	LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative	*MUL	Multiply
*BBS	Branch on Bit Set Relative	NOP	No Operation
BCC	Branch on Carry Clear	ORA	"OR" Memory with Accumulator
BCS	Branch on Carry Set	PHA	Push Accumulator on Stack
BEQ	Branch on Result Zero	PHP	Push Processor Status on Stack
BIT	Test Bits in Memory with Accumulator	*PHX	Push Index X
BMI	Branch on Result Minus	*PHY	Push Index Y
BNE	Branch on Result not Zero	PLA	Pull Accumulator from Stack
BPL	Branch on Result Plus	PLP	Pull Processor Status from Stack
BRK	Force Break	*PLX	Pull Index X
BVC	Branch on Overflow Clear	*PLY	Pull Index Y
BVS	Branch on Overflow Set	*RMB	Reset Memory Bit
CLC	Clear Carry Flag	ROL	Rotate One Bit Left (Memory or Accumulator)
CLD	Clear Decimal Mode	ROR	Rotate One Bit Right (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit	RTI	Return from Interrupt
CLV	Clear Overflow Flag	RTS	Return from Subroutine
CMP	Compare Memory and Accumulator	SBC	Subtract Memory from Accumulator with Borrow
CPX	Compare Memory and Index X	SEC	Set Carry Flag
CPY	Compare Memory and Index Y	SED	Set Decimal Mode
DEC	Decrement Memory by One	SEI	Set Interrupt Disable Status
DEX	Decrement Index X by One	*SMB	Set Memory Bit
DEY	Decrement Index Y by One	STA	Store Accumulator in Memory
EOR	"Exclusive-Or" Memory with Accumulator	STX	Store Index X in Memory
INC	Increment Memory by One	STY	Store Index Y in Memory
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index Y by One	TAY	Transfer Accumulator to Index Y
JMP	Jump to New Location	TSX	Transfer Stack Pointer to Index X
JSR	Jump to New Location Saving Return Address	TXA	Transfer Index X to Accumulator
		TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator

3

Notes:	LEGEND	M_n	= Memory Bit 6
1. Add 1 to N if page boundary is crossed.	X = Index X	+ = Add	
2. Add 1 to N if branch occurs to same page	- = Index Y	- = Subtract	
Add 2 to N if branch occurs to different page	∧ = And	∨ = Or	
Carry not (C) = Borrow	M = Accumulator	V = Exclusive or	
3. If in decimal mode Z flag is invalid	M ₁ = Memory per effective address:	m = Number of cycles	
accumulator must be checked on zero result.	M ₂ = Memory per stack pointer	# = Number of Bytes	
	M ₃ = Selecter zero page memory bit		
	M ₇ = Memory Bit 7		

Notes:

1. Add 1 1/2
2. Add 1 1/2
3. Carry 1/2
4. If in debt, account
5. Effects of

INSTRUCTION SET OPERATION CODE MATRIX

The following matrix shows the op codes associated with the R65C00/21 and R65C29 CPUs. The matrix identifies the hexadecimal code, the mnemonic code, the addressing mode,

the number of instruction bytes, and the number of machine cycles associated with each op code. Also, refer to the instruction set summary for additional information on these op codes.

MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	BRK Implied 1 7	ORA (IND, X) 2 6	MUL Implied 1 10			ORA ZP, X 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*	PHY Implied 1 3			EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*	PLY Implied 1 4			ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8	BRA Relative 2 3*	STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBR8 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBR9 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBR10 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBR11 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBR12 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*	PHX Implied 1 3			CMP ABS, X 3 4*	DEC ABS, X 3 7	BBR13 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBR14 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*	PLX Implied 1 4			SBC ABS, X 3 4*	INC ABS, X 3 7	BBR15 ZP 3 5**	F

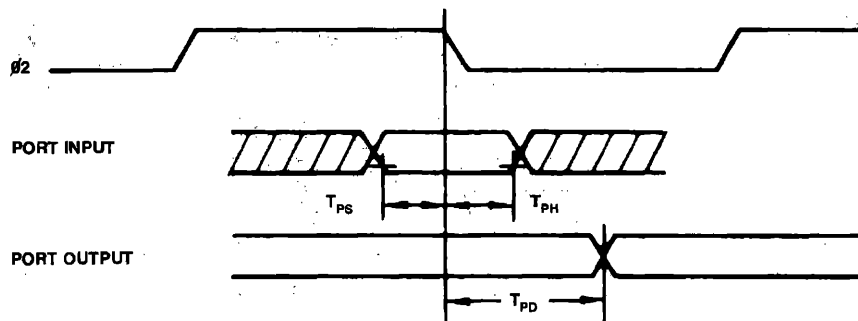
0
BRK
Implied
1 7

—OP Code
—Addressing Mode
—Instruction Bytes; Machine Cycles

—New Opcode

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
Add 2 to N if branch occurs to different page.

I/O PORT WAVEFORMS—ALL PORTS



3

I/O PORT TIMING—ALL PORTS

Parameter	Symbol	2MHz	4 MHz	Min	Max
		Min	Max		
Input Data Setup Time	T_{PS}	50	—	35	—
Input Data Hold Time (Port D)	T_{PH}	10	—	10	—
Input Data Hold Time (All ports except D)		25	—	25	—
Output Data Delay Time	T_{PD}	—	120	—	100

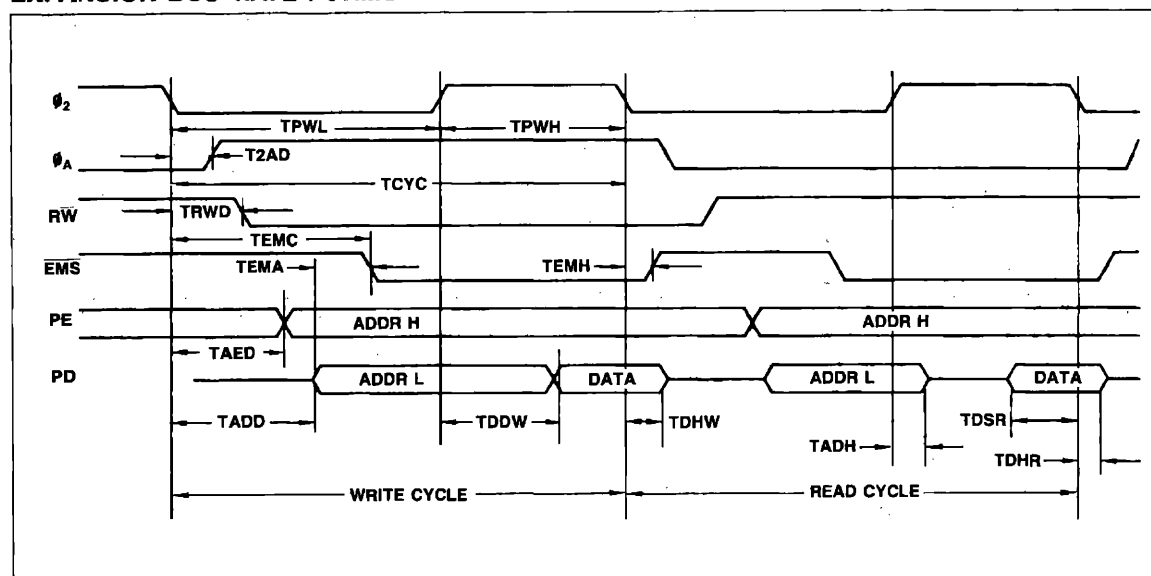
EXPANSION BUS TIMING

 $V_{CC} = 5.0V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$

Parameter	Symbol	2 MHz*		4 MHz*		Unit
		Min	Max	Min	Max	
RW Delay Time	T_{RWD}	20	100	10	80	ns
PE Address Delay Time	T_{AED}	20	100	10	80	ns
PD Address Delay Time	T_{ADD}	20	120	10	100	ns
PD Address Hold Time—Read	T_{ADH}	0	80	0	60	ns
Data Delay Time—Write	T_{DDW}	—	120	—	100	ns
Data Hold Time—Write	T_{DHW}	20	—	20	—	ns
Data Setup Time—Read	T_{DSR}	50	—	35	—	ns
Data Hold Time—Read	T_{DHR}	10	—	10	—	ns
EMS Delay Time—Address Valid to EMS Low	T_{EMA}	10	—	10	—	ns
EMS Delay Time— $\phi 2$ to EMS Low	T_{EMC}	—	150	—	115	ns
EMS Hold Time	T_{EMH}	10	—	10	—	ns
$\phi 2$ Cycle Time	T_{CYC}	500	—	250	—	ns
Pulse Width $\phi 2$ Low	T_{PWL}	235	265	115	135	ns
Pulse Width $\phi 2$ High	T_{PWH}	235	265	115	135	ns
ϕA Delay Time— $\phi 2$ to ϕA	T_{2AD}	0	60	0	50	ns

Note:
* $\phi 2$ Frequency

EXPANSION BUS WAVE FORMS



MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to V_{CC} +0.3	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

DC CHARACTERISTICS

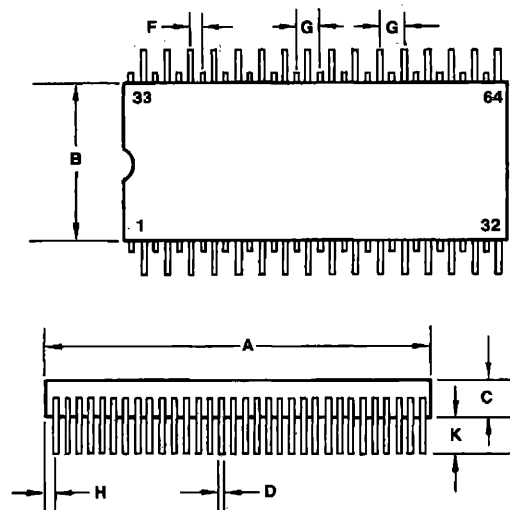
$V_{CC} = +5.0V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise specified)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input High Voltage	V_{IH}	+2.0	—	V	
Input Low Voltage	V_{IL}	—	+0.8	V	
Output High Voltage	V_{OH}	+2.4	—	V	$V_{CC} = 4.5V$ $I_{LOAD} = -100\mu A$
Input Leakage Current	I_{IN}	—	± 10	μA	$V_{IN} = 0V$ or V_{CC} $V_{CC} = 0V$
Output Low Voltage	V_{OL}	—	+0.4	V	$V_{CC} = 4.5V$ $I_{LOAD} = 1.6 mA$
Output Low Current (All ports except Port G)	I_{OUT}	—	-1.6	mA	$V_{OL} = 0.4V$
Input Capacitance (XTALO, XTALI) (All Others)	C_{IN}	—	25 5	pF pF	$V_{CC} = 5V$ $f = 2 MHz$ $T_A = 25^\circ C$
Output Capacitance	C_{OUT}	—	10	pF	
Operating Frequency Crystal or Master Clock 02 Clock	—	.02 .01	8.0 4.0	MHz MHz	
Power Dissipation	P_D	—	40	mW	$V_{CC} = 5V$ $f = 2 MHz$ $T_A = 25^\circ C$

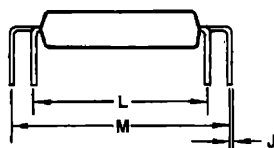
Note: Negative sign indicates outward current flow, positive sign indicates inward current flow.

PACKAGE DIMENSIONS

64 PIN PLASTIC QUIP (QUAD IN-LINE PACKAGE)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	41.15	41.66	1.620	1.640
B	17.02	17.53	0.670	0.690
C	3.05	4.57	0.120	0.180
D	0.38	0.51	0.024	0.020
F	1.27 BSC		0.050 BSC	
G	2.54 BSC		0.100 BSC	
H	1.02	1.14	0.040	0.045
J	—	7°	—	7°
K	2.79	4.32	0.110	0.170
L	18.92	19.81	0.745	0.755
M	23.37	23.62	0.920	0.930





R65F11 AND R65F12 FORTH BASED MICROCOMPUTERS

SECTION 1 INTRODUCTION

3

1.1 FEATURES

- FORTH kernel in ROM
- Enhanced 6502 CPU
 - Four new bit manipulation instructions:
 - Set Memory Bit (SMB)
 - Reset Memory Bit (RMB)
 - Branch on Bit Set (BBS)
 - Branch on Bit Reset (BBR)
 - Decimal and binary arithmetic modes
 - 13 addressing modes
 - True indexing
- 192-byte static RAM
- 16 bidirectional, TTL-compatible I/O lines (two ports, R65F11) or 40 bidirectional, TTL-compatible I/O lines (five ports, R65F12)
- One 8-bit port with programmable latched input
- Two 16-bit programmable counter/timers, with latches
 - Pulse width measurement
 - Asymmetrical pulse generation
 - Pulse generation
 - Interval timer
 - Event counter
 - Retriggerable interval timer
- Serial port
 - Full-duplex asynchronous operation mode
 - Selectable 5- to 8-bit characters
 - Wake-up feature
 - Synchronous shift register mode
 - Standard programmable bit rates, programmable up to 62.5K bits/sec
- Ten interrupts
 - Four edge-sensitive lines; two positive, two negative
 - Reset
 - Non-maskable
 - Two counter
 - Serial data received
 - Serial data transmitted
- Expandable to 16K bytes of external memory

- Flexible clock circuitry
 - 2-MHz or 1-MHz internal operation
 - Internal clock with external XTAL at two times internal frequency
 - External clock input divided by one or two
- 1 μ s minimum instruction execution time @ 2 MHz
- NMOS silicon gate, depletion load technology
- Single +5V power supply
- 12 mW standby power for 32 bytes of the 192-byte RAM
- 40-pin DIP (R65F11)
- 64-pin QUIP (R65F12) has three additional 8-bit I/O ports to provide a total of 40 I/O lines.

1.2 SUMMARY

The Rockwell R65F11 and R65F12 are complete, high-performance 8-bit NMOS single chip microcomputers, and are compatible with all members of the R6500 family.

The kernel of the high level Rockwell Single Chip RSC-FORTH language is contained in the preprogrammed ROM of the R65F11 and R65F12. RSC-FORTH is based on the popular fig-FORTH model with extensions. All of the run time functions of RSC-FORTH are contained in the ROM, including 16- and 32-bit mathematical, logical and stack manipulation, plus memory and input/output operators. The RSC-FORTH Operating System allows an external user program written in RSC-FORTH or Assembly Language to be executed from external EPROM, or development of such a program under the control of the R65F11 RSC-FORTH Development ROM. Other development ROM's can also be accommodated.

The R65F11 and R65F12 consist of an enhanced 6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 16 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of

computational power. These features in combination with the FORTH high level operating system make the R65F11 and R65F12 ideal for microcomputer applications.

For systems requiring additional I/O ports, the 64-pin QUIP version, the R65F12, provides three additional 8-bit ports.

A complete RSC-FORTH development system can be created with three MOS parts: the R65F11, one RAM chip and the R65FR1 Development ROM.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual

(Order Number 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order Number 202).

1.3 ORDERING INFORMATION

Part No.	Description
R65F11P	40-Pin FORTH Based Microcomputer at 1 MHz
R65F11AP	40-Pin FORTH Based Microcomputer at 2 MHz
R65F12Q	64-Pin FORTH Based Microcomputer at 1 MHz
R65F12AQ	64-Pin FORTH Based Microcomputer at 2 MHz
R65FR1P	FORTH Development ROM for R65F11 or R65F12
R65FR2P	FORTH Development ROM for expanded capacity
R65FK2P	FORTH Kernel ROM for expanded capacity development
R65FR3P	FORTH Development ROM for R6501Q
R65FK3P	FORTH Kernel ROM for R6501Q
Order No.	Description
2148	FORTH Based Microcomputer User's Manual*
Note:	
*Included with R65FR1.	

SECTION 2

INTERFACE REQUIREMENTS

This section describes the interface requirements for the R65F11 and R65F12 single chip microcomputers. Figure 2-1 is the Interface Diagram for the R65F11 and R65F12. Figure 2-2 shows the pin out configuration and Table 2-1 describes the function of each pin of the R65F11 and R65F12. Figure 3-1 is a detailed block diagram.

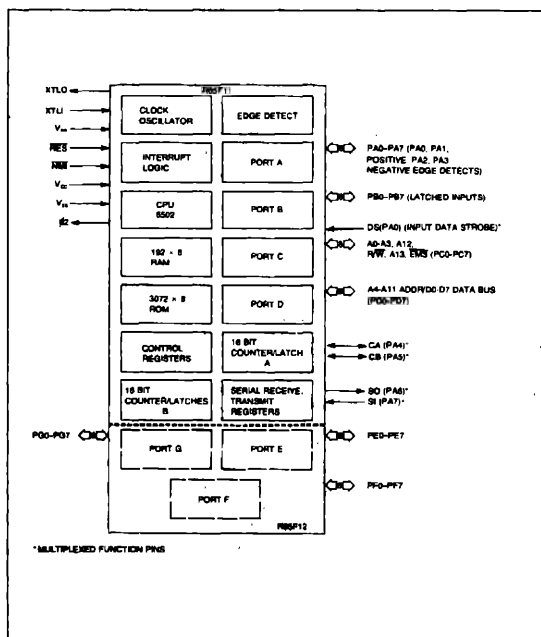
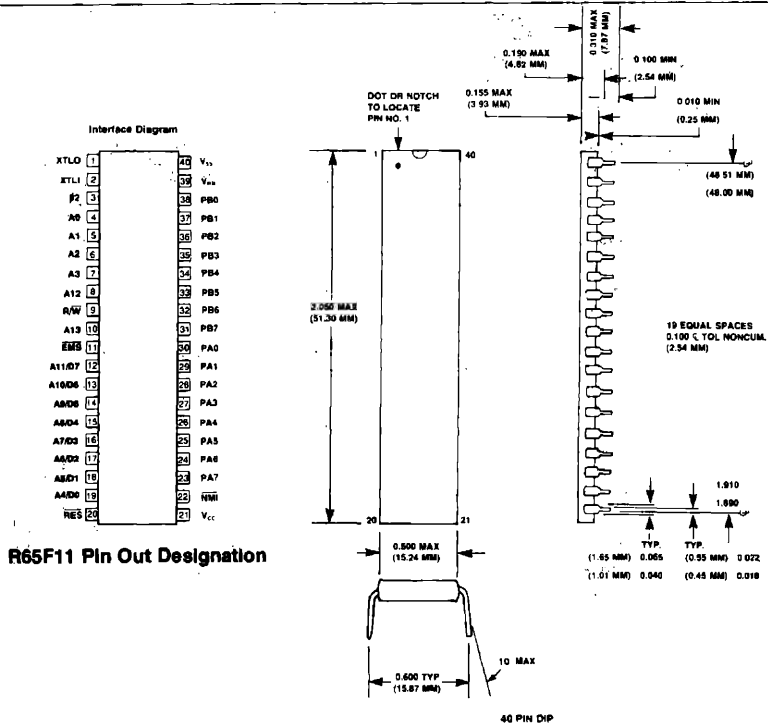


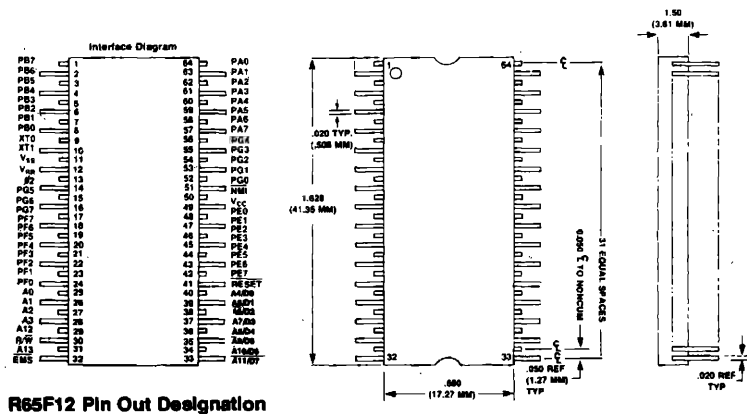
Figure 2-1. R65F11 and R65F12 Interface Diagram

Table 2-1. R65F11 and R65F12 Pin Descriptions

Signal Name	Pin No. R65F11	Pin No. R65F12	Description
V _{CC}	21	50	Main power supply +5V
V _{RR}	39	12	Separate power pin for RAM. In the event that V _{CC} power is lost, this power retains RAM data.
V _{SS}	40	11	Signal and power ground (0V)
XTLI	2	10	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to V _{SS} or X2 or X4 clock if XTLO is floated.
XTLO	1	9	Crystal output from internal clock oscillator.
RES	20	41	The Reset input is used to initialize the R65F11. This signal must not transition from low to high for at least eight cycles after V _{CC} reaches operating range and the internal oscillator has stabilized.
#2	3	13	Clock signal output at internal frequency.
NMI	22	51	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7	30-23 38-31	57-64 1-8	Two 8-bit ports used for either input/output. Each line of Ports A and B consist of an active transistor to V _{SS} and a passive pull-up to V _{CC} .
PC0-PC7 A0-A3 A12, R/W A13, EMS	4-11	25-32	Port C has an active pull-up transistor. Port D has active pull-up and pull-down transistors. Ports C and D lines form the external multiplexed address and data bus to allow external memory addressing.
PD0-PD7 A4-A11 D0-D7	19-12	33-40	
PE0-PE7 PF0-PF7 PG0-PG7		42-49 24-17 14-18, 52-56	On the R65F12, Port E may be used for output only. Ports F and G are similar to Ports A and B in construction and may be used for inputs or outputs.



R65F11 Dimensional Outline



R65F12 Dimensional Outline

Figure 2-2. Pin Out Configuration

SECTION 3

SYSTEM ARCHITECTURE

This section provides a functional description of the R65F11 and R65F12. Functionally the R65F11 consists of a CPU, RAM memory, two 8-bit parallel I/O ports (five in the 64-pin R65F12), a serial I/O port, dual counter/latch circuits, a mode control register, an interrupt flag/enable dual register circuit, and an internal Operating System. The kernel of FORTH in ROM complements the system hardware. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The R65F11 internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, and ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal IRQ interrupt, or the external interrupt line NMI. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Processor Status Register

The 8-bit Processor Status Register contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. See Appendix B for details.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Arithmetic And Logic Unit (ALU)

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.7 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

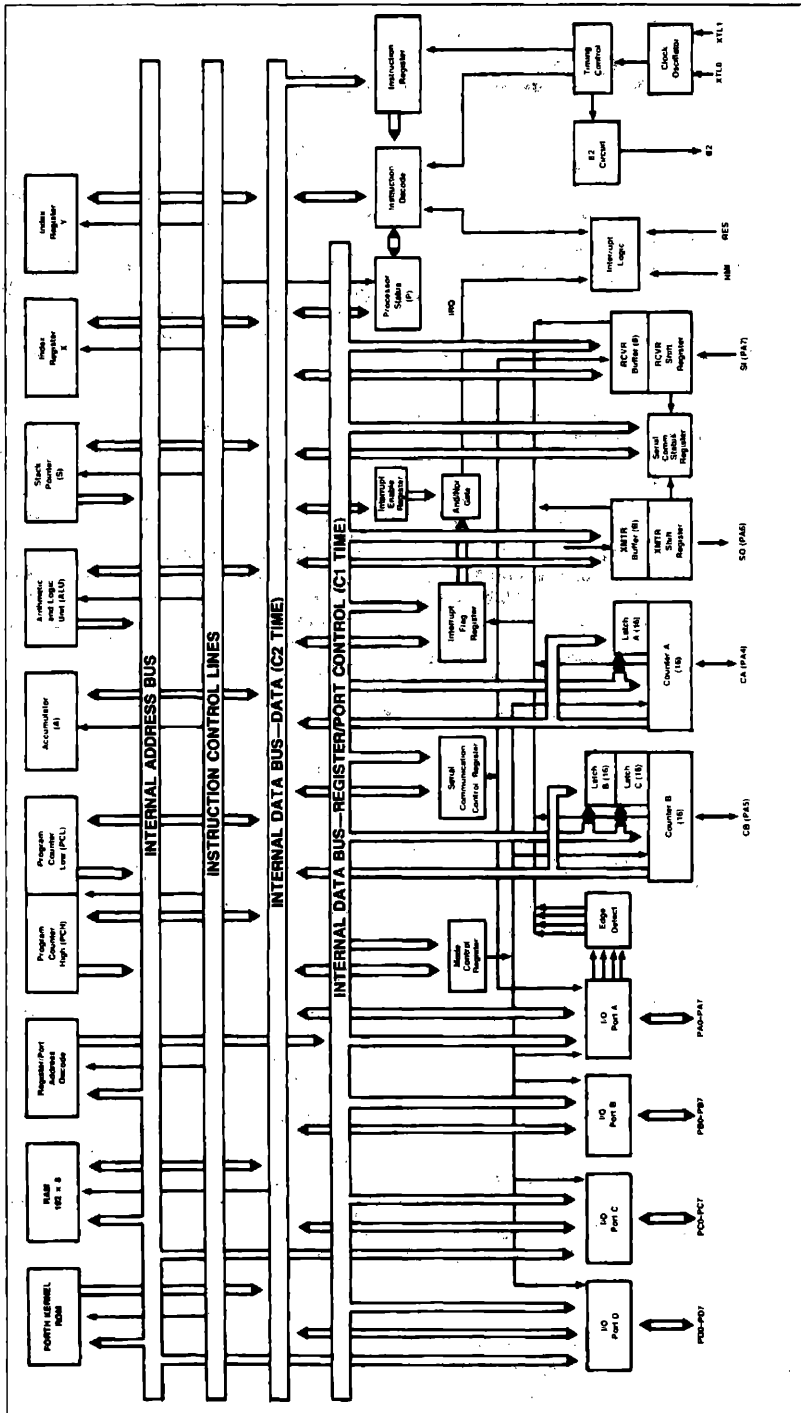


Figure 3-1. Detailed Block Diagram

3.1.8 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

3.1.9 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; RES, NMI and IRQ. IRQ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 CPU INSTRUCTION SET

The machine code instruction set of the R65F11 and R65F12 microcomputers are based on the popular R6500 microprocessor set. They contain all the instructions in the standard R6502 set, with the addition of the four new bit instructions added to the R6511 processor family. Refer to Appendix A for the Op Code mnemonics addressing matrix for details on these instructions.

3.3 READ-ONLY-MEMORY (ROM)

The ROM consists of preprogrammed memory with an address space from F400 to FFFF. It contains the run time kernel of the high level language Rockwell Single Chip FORTH. There are 133 included functions stored in the ROM. Codes are in the format of a two byte code field, which identifies the interpreter assigned to execute that word, followed by a variable length Parameter Field, which contains the instructions and data used by that interpreter according to the programmed intention of that definition. See Appendix D for a complete list of the names of all included words. All words needed for support of the run time operation of dedicated applications programs are included. The RSC-FORTH Operating System is also part of the ROM code and is entered upon Reset. This Operating System allow the R65F11 and R65F12 to auto start a user program written in either RSC-FORTH or Assembly Language, or enter a Development ROM if one is present. If no auto start program is found, an attempt will be made to boot an operating program from floppy disk.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R65F11 and R65F12 provide a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC} . During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC} , V_{RR} must be supplied within operating range and RES must be driven low at least eight $\emptyset 2$ clock pulses before V_{CC} falls out of operating range. RES must then be held low while V_{CC} is out of operating range and until at least eight $\emptyset 2$ clock cycles after V_{CC} is again within operating range and the internal $\emptyset 2$ oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3-2 shows typical waveforms.

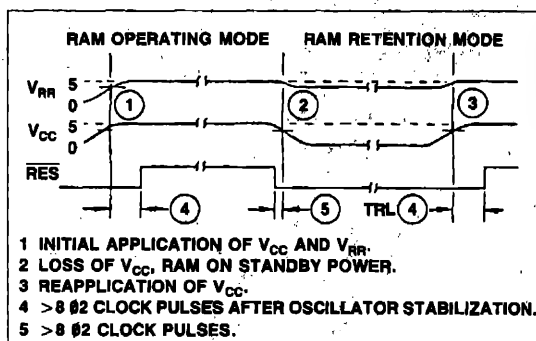


Figure 3-2. Data Retention Timing

3.5 CLOCK OSCILLATOR

A reference frequency can be generated with the on-chip oscillator using an external crystal. The oscillator reference frequency passes through an internal countdown network (divide by 2) to obtain the internal operating frequency (see Figure 3-3a).

Internal timing can also be controlled by driving the XTLL pin with an external frequency source. Figure 3-3b shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS} , the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

The R65F11 and R65F12 operate in the CLOCK MASTER mode. In this mode a frequency source (crystal or external source) must be applied to the XTLL and XTLO pins.

NOTE: When operating at a 1 MHz internal frequency place a 15-22 pF capacitor between XTLO and GND.

$\emptyset 2$ is a buffered output signal which closely approximates the internal timing. When a common external source is used to drive multiple devices the internal timing between devices as well as their $\emptyset 2$ outputs will be skewed in time. If skewing represents a system problem, it can be avoided by the Master/Slave connection and options shown in Figure 3-4.

The R65F11 and R65F12 is operated in the CLOCK MASTER MODE. A second processor could be operated in the CLOCK

SLAVE MODE. Mask options in the SLAVE unit convert the $\phi 2$ signal into a clock input pin which is tightly coupled to the internal timing generator. As a result the internal timing of the MASTER and SLAVE units are synchronized with minimum skew. If the $\phi 2$ signal to the SLAVE unit is inverted, the MASTER and SLAVE UNITS WILL OPERATE OUT OF PHASE. This approach allows the two devices to share external memory using cycle stealing techniques.

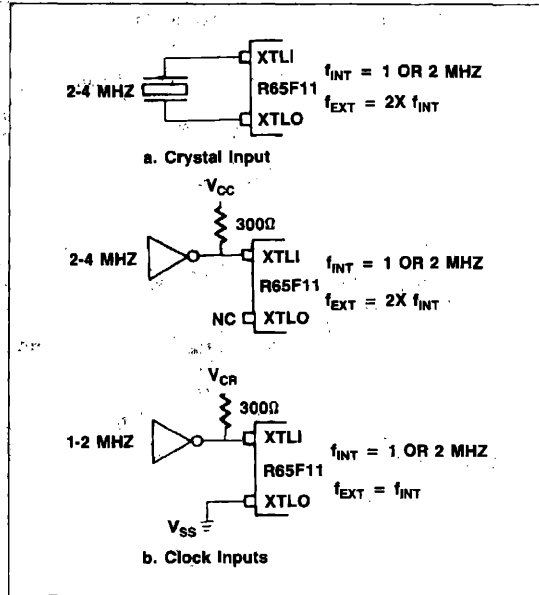


Figure 3-3. Clock Oscillator Input Options

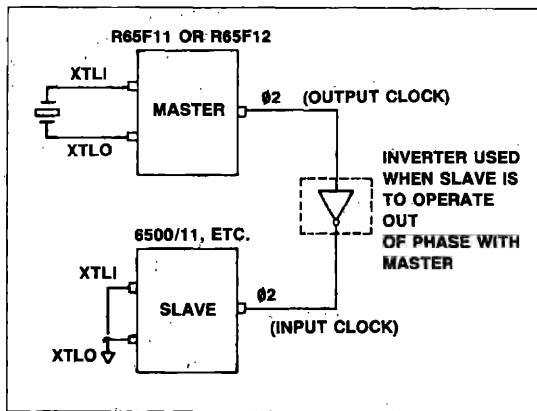


Figure 3-4. Master/Slave Connections

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the R65F11 and R65F12 in any application. The Mode Control Register bit assignment is shown in Figure 3-5. MCR Bits 7, 6, 5 must remain 1's in order for external memory referencing to be enabled.

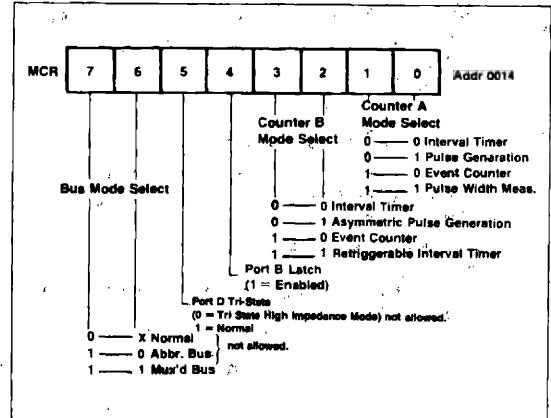


Figure 3-5. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An IRQ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the IRQ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared in low level code by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by RES. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-6 and the functions of each bit are explained in Table 3-1.

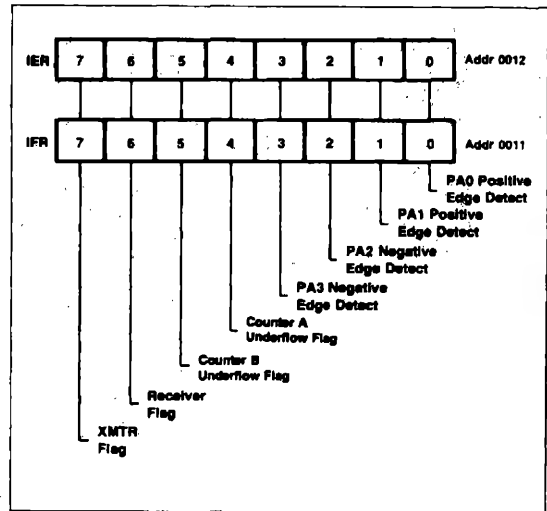


Figure 3-6. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Flag Register Bit Codes

Bit Code	Function
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB 0 (0010) instruction or by RES.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by RES.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by RES.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by RES.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by RES.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by RES.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by RES.
IFR 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by RES.

3.8 OPERATING SYSTEM

The system startup function, COLD, is executed upon Reset. COLD, a high level FORTH word, forms the basis of the RSC Operating System. Upon reset this function initializes the R65F11 or R65F12 registers to establish the external 16K byte memory map and disable all interrupt sources. It also sets up the serial channel for 1200 baud (assuming a 1 MHz internal clock) asynchronous transmission (seven bits, parity disabled). The internal FORTH structure "W" is prepared for use and the low level input/output vectors are forced to point to the system serial channel routines. The FORTH User Area Pointer, UP, is assigned the value 0300 Hex.

A test is made of the variable CLD/WRM in memory location 030E. If this contains a value other than A55A Hex a cold reset is assumed. In this case, the low level IRQ vector, IRQVEC; the low level NMI Vector, NMIVector, and the high level interrupt vector, INTVEC, are all forced to point to the system reset routine. This prevents an unintentionally generated interrupt from crashing the system. System variables TIB, RO, SO, UC/L, UPAD, UR/W and BASE are also initialized to their default values.

Whether a warm or cold reset, the memory map is then searched at every 1K byte boundary starting at location 0400 Hex. The first two bytes at each boundary are checked against an A55A Hex bit pattern. This pattern indicates that an auto start program is installed. The next two bytes are assumed to point to the Parameter Field of the high level RSC-FORTH word to be executed upon reset. This may be the main function of a user defined program or the start up routine of a Development ROM. Figure 3-7 details proper alignment.

If no auto start ROM is found, the Operating System turns control over to a program that issues a "NO ROM" message to the systems terminal via the serial channel and attempts to boot a program from disk. A floppy disk controller, compatible with the WD1793 type, is assumed to be present at address 0100 Hex. The first half of Track 0 Sector 1 is loaded from a double density boot diskette into RAM starting at address 005F. When successfully loaded execution will be turned over to this boot program.

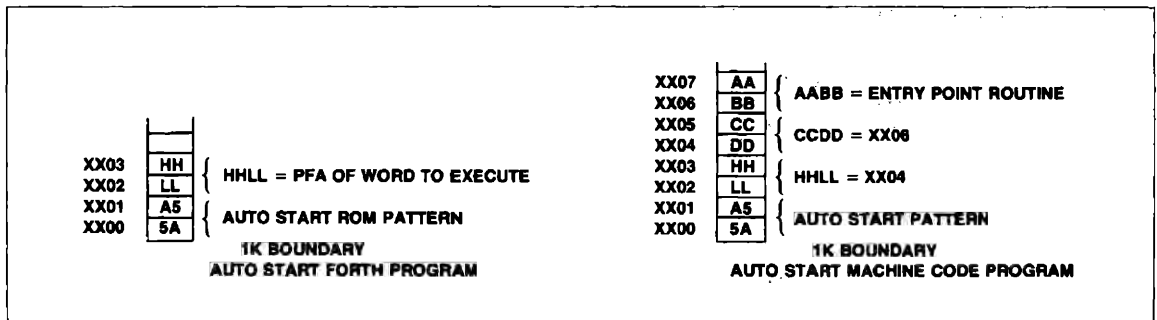


Figure 3-7. Auto Start ROM

SECTION 4

PARALLEL INPUT/OUTPUT PORTS

The R65F11 has 16 I/O lines grouped into two 8-bit ports (PA, PB) and 16 lines programmed as an Address/Data bus (PC & PD). Ports A and B may be used either for input or output individually or in groups of any combination. The R65F12 has 24 additional port lines grouped into three 8-bit ports (PE, PF, PG).

Multifunction I/O's such as Port A are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of $3K \leq R_{pu} \leq 12K \text{ ohm}$) are provided on all port pins.

The direction of the I/O lines are controlled by 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 4-1.

Table 4-1. I/O Port Addresses

Port	Address
A	0000
B	0001
E	0004
F	0005
G	0006

Appendix F.4 shows the I/O Port Timing.

4.1 INPUTS

Inputs for Ports A and B are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low ($<0.8V$) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high ($>2.0V$) input will cause a logic 1 to be read. An \overline{RES} signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA and PB. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A and B are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high ($>2.4V$) output while a logic 0 will force a low ($<0.4V$) output.

4.3 PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-3 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges, and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the $\phi 2$ clock rate. Edge detection timing is shown in Appendix F.4.

4.4 PORT B (PB)

Port B can be programmed as an 8 bit, bit independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-2 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Appendix F.4.

Table 4-2. Port B Control & Usage

Pin No. R65F11	Pin No. R65F12	I/O Mode		Latch Mode	
		MCR4 = 0		MCR4 = 1 (2)	
		Signal		Signal	
		Name	Type (1)	Name	Type
38	8	PB0	I/O	PB0	INPUT
37	7	PB1	I/O	PB1	INPUT
36	6	PB2	I/O	PB2	INPUT
35	5	PB3	I/O	PB3	INPUT
34	4	PB4	I/O	PB4	INPUT
33	3	PB5	I/O	PB5	INPUT
32	2	PB6	I/O	PB6	INPUT
31	1	PB7	I/O	PB7	INPUT

(1) Resistive pull-up, active buffer pull down

(2) Input data is stored in port B latch by PA0 pulse

Table 4-3. Port A Control and Usage

R65F11/R65F12 PORT ⁽⁵⁾	PA0 I/O		PORT B LATCH MODE	
	MCR4 = 0		MCR4 = 1	
PA0 ⁽²⁾	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA0	I/O	PORT B LATCH STROBE	INPUT ⁽¹⁾
PA1 ⁽²⁾ PA2 ⁽³⁾ PA3 ⁽³⁾	PA1-PA3 I/O			
	SIGNAL			
	NAME	TYPE		
	PA1 PA2 PA3	I/O I/O I/O		
PA4	PA4 I/O		COUNTER A I/O	
	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 ⁽⁴⁾ (6)		MCR0 = 1 MSR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 ⁽⁴⁾	SCCR7 = 0 SCCR6 = 0 MCR1 = 1
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA4	I/O	CNTA	OUTPUT
	SERIAL I/O SHIFT REGISTER CLOCK			
	SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1 ⁽⁴⁾	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)
PA5	PA5 I/O		COUNTER B I/O	
	MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1	MCR3 = 1 MCR2 = X
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA5	I/O	CNTB	OUTPUT
PA6	PA6 I/O		SERIAL I/O XMTR OUTPUT	
	SCCR7 = 0		SCCR7 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA6	I/O	XMTR	OUTPUT
PA7	PA7 I/O		SERIAL I/O RCVR INPUT	
	SCCR6 = 0		SCCR6 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA7	I/O	RCVR	INPUT (1)

- (1) HARDWARE BUFFER FLOAT
 (2) POSITIVE EDGE DETECT
 (3) NEGATIVE EDGE DETECT
 (4) RCVR S/R MODE = 1 WHEN
 SCCR6 • SCCR5 • SCCR4 = 1
 (5) APPLIES TO EITHER R65F11
 OR R65F12 PORT (SEE PIN
 DIAGRAM)
 (6) FOR THE FOLLOWING MODE
 COMBINATIONS PA4 IS
 AVAILABLE AS AN INPUT
 ONLY PIN:
 SCCR7 • SCCR6 • SCCR5 •
 MCR1 • SCCR7 • SCCR6 •
 SCCR4 • MCR1 • SCCR7 •
 SCCR6 • SCCR5 • SCCR7 •
 SCCR5 • SCCR4

4.5 PORT C (PC)

Port C is preprogrammed as part of the Address/Data bus. PC0-PC7 function as A0-A3, A12, R/W, A13, and EMS, respectively, as shown in Table 4-4. EMS (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0100 and 3FFF. (See Memory Map, Appendix C). The leading edge of EMS may be used to strobe the eight address lines multiplexed on Port D. See Appendix F.3 for Port C timing.

4.6 PORT D (PD)

Port D is also preprogrammed as part of the Address/Data bus. Data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix C) for Multiplexed memory assignments. See Appendix F.3 for Port D timing.

4.7 PORT E (PE), PORT F (PF), PORT G (PG)

Ports E, F and G are available on the R65F12 only. Port E can only be used as outputs. Port F and Port G can be used for inputs or outputs and are similar to Port A and Port B in operation.

Table 4-4. Port C Control and Usage

R65F11/ R65F12 Port	Multiplexed Mode	
	MCR7 = 1 MCR6 = 1	
	Signal	
	Name	Type (1)
PC0	A0	OUTPUT
PC1	A1	OUTPUT
PC2	A2	OUTPUT
PC3	A3	OUTPUT
PC4	A12	OUTPUT
PC5	R/W	OUTPUT
PC6	A13	OUTPUT
PC7	EMS	OUTPUT

Table 4-5. Port D Control and Usage

R65F11/ R65F12 Port	Multiplexed Mode			
	MCR7 = 1 MCR6 = 1 MCR5 = 1			
	Signal		Signal	
	Phase 1		Phase 2	
	Name	Type (2)	Name	Type (3)
PD0	A4	OUTPUT	DATA0	I/O
PD1	A5	OUTPUT	DATA1	I/O
PD2	A6	OUTPUT	DATA2	I/O
PD3	A7	OUTPUT	DATA3	I/O
PD4	A8	OUTPUT	DATA4	I/O
PD5	A9	OUTPUT	DATA5	I/O
PD6	A10	OUTPUT	DATA6	I/O
PD7	A11	OUTPUT	DATA7	I/O

(1) Active Buffer Pull-up and Pull-Down
(2) Tri-State Buffer is in Active Mode
(3) Tri-State Buffer is in Active Mode only during the Phase 2 Portion of a Write Cycle

SECTION 5

SERIAL INPUT/OUTPUT CHANNEL

The R65F11 and R65F12 Microcomputers provide a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (@ $\phi 2 = 1$ MHz). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

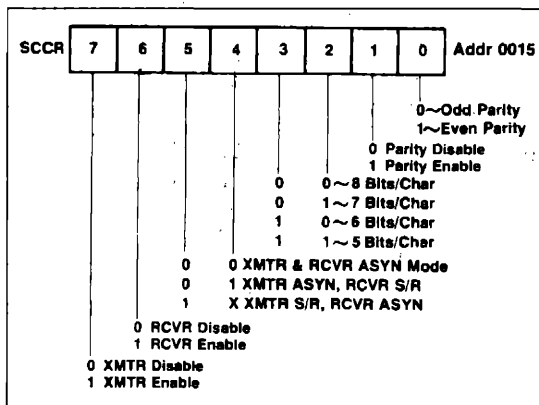


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XMTR)

The XMTR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are shown below. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

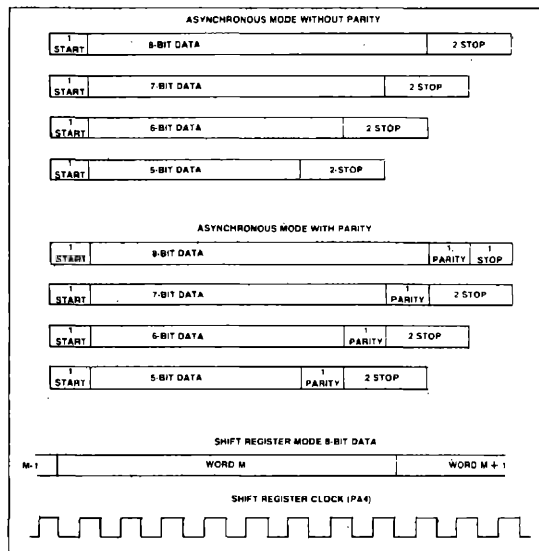


Figure 5-2. Bit Allocations

In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter under-runs in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCCR5, SCCR6 and SCCR7.

$$\text{IFR7} = \text{SCSR6} (\text{SCCR5} + \text{SCCR7})$$

5.2 RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, appropriate number of data bits, a parity bit (if enabled) and one stop bit. Refer to Figure 5-2 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits, and any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.

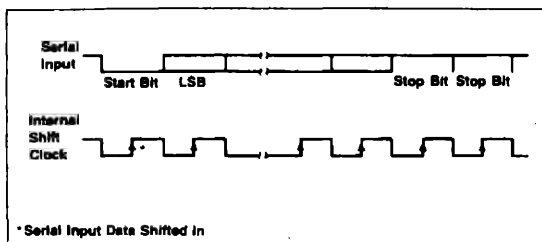


Figure 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.

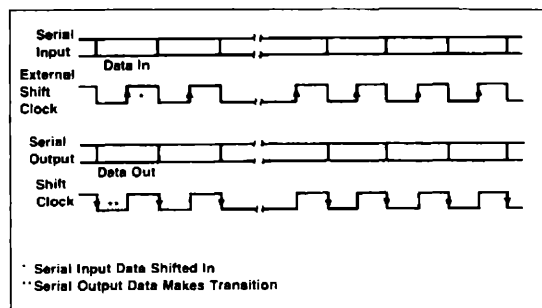


Figure 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR 0: Receiver Data Register Full—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by RES and is disabled if SCSR 6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition, however, a corresponding error bit will be set to a logic 1 instead.

SCSR 1: Over-Run Error—Set to a logic 1 when a new character is transferred from the Receiver Shift Register, with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by RES.

SCSR 2: Parity Error—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the

received data has a parity error. This bit is cleared by reading the Receiver Data Register or by RES.

SCSR 3: Framing Error—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by RES. (ASYN Mode only).

SCSR 4: Wake-Up—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by RES or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR 5: End of Transmission—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by RES or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6: Transmitter Data Register Empty—Set to a logic 1 when the contents of the Transmitter Data Register is transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by RES.

SCSR 7: Transmitter Under-Run—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register, or by RES.

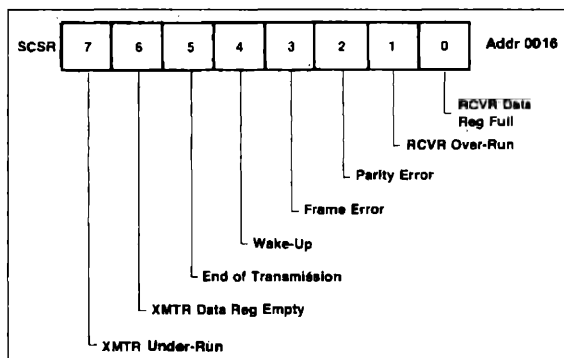


Figure 5-5. SCSR Bit Allocations

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of ten consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6

COUNTER/TIMERS

The R65F11 and R65F12 Microcomputers contain two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A

- Pulse width measurement
- Pulse Generation
- Interval Timer
- Event Counter

Counter B

- Retriggerable Interval Counter
- Asymmetrical Pulse Generation
- Interval Timer
- Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either $\emptyset 2$ clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the

Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by RES.

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register. See Table 6-1.

Table 6-1. Counter A Control Bits

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are $\emptyset 2$ clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a RES signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).
2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the $\emptyset 2$ clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore $1\mu\text{s}$ to 65 535 ms at the 1 MHz $\emptyset 2$ clock rate or $0.5\mu\text{s}$ to 32.767 ms at the 2 MHz $\emptyset 2$ clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting IRQ interrupt requests in the counter IRQ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an IRQ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the IRQ interrupt routine to determine that the IRQ was generated by the Counter A Underflow.

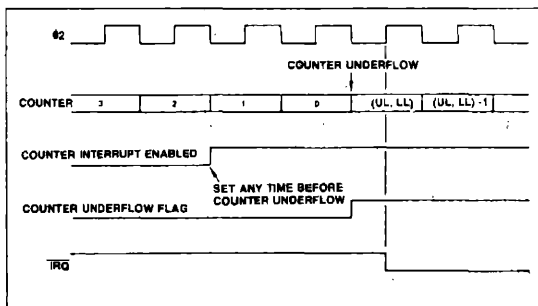


Figure 6-1. Interval Timer Timing Diagram

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs, or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

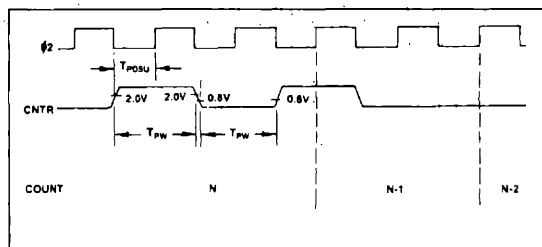


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the $\phi 2$ clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6-3.

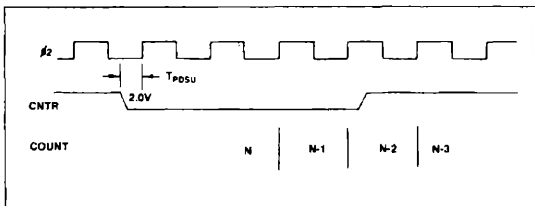


Figure 6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-2 identifies the values to be loaded in Counter A for selecting standard data rates with a $\phi 2$ clock rate of 1 MHz and 2 MHz. Although Table 6-2 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{.16 \times \text{bps}} - 1$$

where

N = decimal value to be loaded into Counter A using its hexadecimal equivalent.

$\phi 2$ = the clock frequency (1 MHz or 2 MHz)

bps = the desired data rate.

NOTE

In Table 6-2 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-2 for those baud rates which fall outside this limit.

Table 6-2. Counter A Values for Baud Rate Selection

Standard Baud Rate	Hexadecimal Value		Actual Baud Rate At		Clock Rate Needed To Get Standard Baud Rate	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600.96	1.0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either $\emptyset 2$ clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by RES.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge

occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

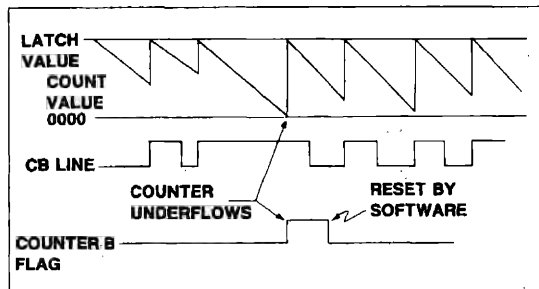


Figure 6-4. Counter B. Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value which corresponds to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C, and the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.
2. The lower 8 bits of D are loaded into LLB by writing to address 001C, and the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and causes the CB output to go low as shown in Figure 6-5.
3. When the Counter B underflow occurs the contents of the Latch C is loaded into the Counter B, and the CB output toggles to a high level and stays high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

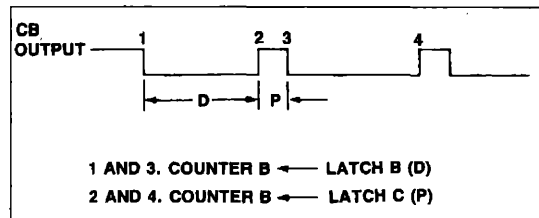


Figure 6-5. Counter B Pulse Generation

SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER-ON-RESET

The occurrence of \overline{RES} going from low to high will cause the R65F11 or R65F12 to reset and enter the RSC-FORTH Operating System. As was described in Section 3.8, upon reset certain system variables will be initialized. See Appendix C.4 for a list of these variables names, locations and contents. The external memory map will be searched for an auto start ROM.

A bit pattern of A55A at a 1K byte page boundary indicates that an auto start program follows. The next two bytes are assumed to be a pointer to the high level RSC-FORTH word that is the entry point to that program. Auto start programs is written in assembly language, rather than RSC-FORTH, a series of indirect pointers as shown in 3-7 can be used to initiate program execution.

7.2 POWER ON TIMING

After application of V_{CC} and V_{RR} power to the R65F11 or R65F12, \overline{RES} must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at $\phi 2$ (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

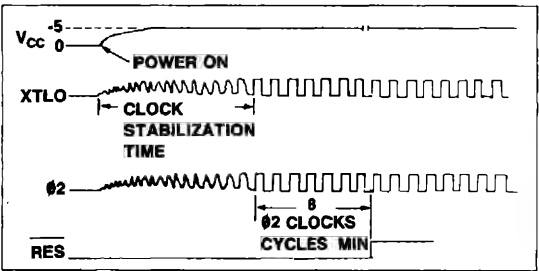


Figure 7-1. Power Turn-On Timing Detail

7.3 RESET (\overline{RES}) CONDITIONING

When \overline{RES} is driven from low to high the R65F11 or R65F12 is put in a reset state. The registers and I/O ports are configured as shown in Table 7-1 when the external ROM is autostarted.

Table 7-1. \overline{RES} Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
REGISTERS								
Mode Control (MCR)	1	1	1	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	1	1	0	0	0	1	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1

APPENDIX A

R65F11 AND R65F12 INSTRUCTION SET

This appendix contains a summary of the R6500 instruction set. For detailed information, consult the R6500 Microcomputer System Programming Manual, Document 29650 N30. The four instructions notated with a * are added instructions for the R65F11 and R65F12 which are not part of the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

Mnemonic	Instruction	Mnemonic	Instruction
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
*BBR	Branch on Bit Reset Relative	LSR	Shift One Bit Right (Memory or Accumulator)
*BBS	Branch on Bit Set Relative	NOP	No Operation
BCC	Branch on Carry Clear	ORA	"OR" Memory with Accumulator
BCS	Branch on Carry Set	PHA	Push Accumulator on Stack
BEQ	Branch on Result Zero	PHP	Push Processor Status on Stack
BIT	Test Bits in Memory with Accumulator	PLA	Pull Accumulator from Stack
BMI	Branch on Result Minus	PLP	Pull Processor Status from Stack
BNE	Branch on Result not Zero	*RMB	Reset Memory Bit
BPL	Branch on Result Plus	ROL	Rotate One Bit Left (Memory or Accumulator)
BRK	Force Break	ROR	Rotate One Bit Right (Memory or Accumulator)
BVC	Branch on Overflow Clear	RTI	Return from Interrupt
BVS	Branch on Overflow Set	RTS	Return from Subroutine
CLC	Clear Carry Flag	SBC	Subtract Memory from Accumulator with Borrow
CLD	Clear Decimal Mode	SEC	Set Carry Flag
CLI	Clear Interrupt Disable Bit	SED	Set Decimal Mode
CLV	Clear Overflow Flag	SEI	Set Interrupt Disable Status
CMP	Compare Memory and Accumulator	*SMB	Set Memory Bit
CPX	Compare Memory and Index X	STA	Store Accumulator in Memory
CPY	Compare Memory and Index Y	STX	Store Index X in Memory
DEC	Decrement Memory by One	STY	Store Index Y in Memory
DEX	Decrement Index X by One	TAX	Transfer Accumulator to Index X
DEY	Decrement Index Y by One	TAY	Transfer Accumulator to Index Y
EOR	"Exclusive-Or" Memory with Accumulator	TSX	Transfer Stack Pointer to Index X
INC	Increment Memory by One	TXA	Transfer Index X to Accumulator
INX	Increment Index X by One	TXS	Transfer Index X to Stack Register
INY	Increment Index Y by One	TYA	Transfer Index Y to Accumulator
JMP	Jump to New Location		
JSR	Jump to New Location Saving Return Address		

3

PROFESSOR STATUS CODES

NOTES		LEGEND		M ₆
1.	Add 1 to N if page boundary is crossed	X	Index X	Memory Bit 6
2.	Add 1 to N if branch occurs to same page	Y	Index Y	
3.	Add 2 to N if branch occurs to different page	A	Accumulator	
4.	Carry not = 0	M	Memory per effective address	
5.	Carry not = 0	M ₁	Memory per stack pointer	
6.	If in decimal mode Z flag is invalid	M ₂	Memory per effective address	
7.	accumulator must be checked on zero result	M ₃	Memory per stack pointer	
8.	Effects 8-bit field of the specified zero page address.	M ₄	Memory Bit 7	

1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
3. Add 2 to N if branch occurs to different page
4. Carry not = Borrow
5. If in decimal mode Z flag is invalid
6. accumulator must be checked on zero result
7. Effects 8-bit data field of the specified zero page address.

A.3 INSTRUCTION CODE MATRIX

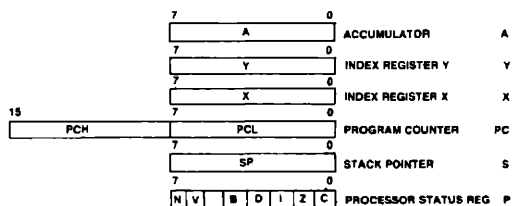
MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND, Y) 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6		BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2			BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*			AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*					AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6			EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2			JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND, Y) 2 5*			EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*					EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6			ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2			JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*			ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*					ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6		STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2			STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBR8 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6		STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2				STA ABS, X 3 5		BBR9 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2	LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2			LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBR10 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND, Y) 2 5*		LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2			LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBR11 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6		CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2			CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBR12 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND, Y) 2 5*			CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*					CMP ABS, X 3 4*	DEC ABS, X 3 7	BBR13 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6		CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2			CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBR14 ZP 3 5**	E
F	BEQ Relative 2 2**	JBC (IND, Y) 2 5*			SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*					SBC ABS, X 3 4*	INC ABS, X 3 7	BBR15 ZP 3 5**	F

0
BRK —OP Code
Implied —Addressing Mode
1 7 —Instruction Bytes; Machine Cycles

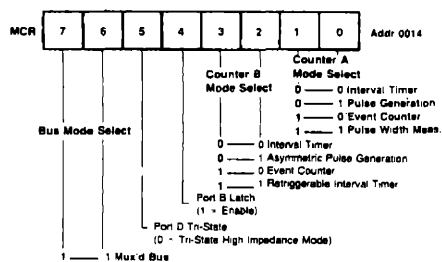
*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

APPENDIX B

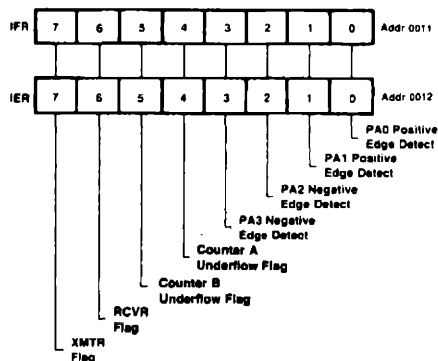
KEY REGISTER SUMMARY



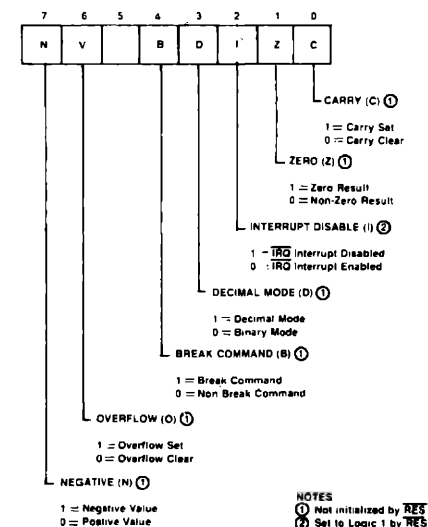
CPU Registers



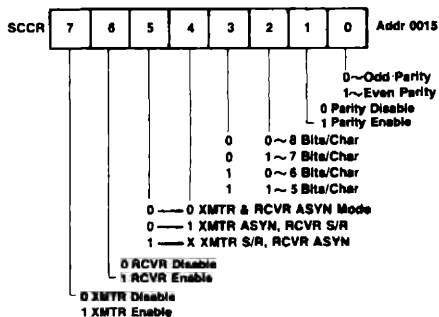
Mode Control Register



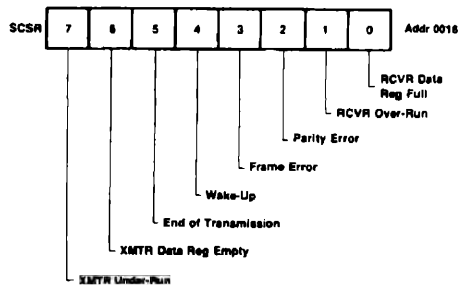
Interrupt Enable and Flag Registers



Processor Status Register



Serial Communications Control Register



Serial Communications Status Register

APPENDIX C

ADDRESS ASSIGNMENTS/MEMORY MAPS/PIN FUNCTIONS

C.1 I/O AND INTERNAL REGISTER ADDRESSES

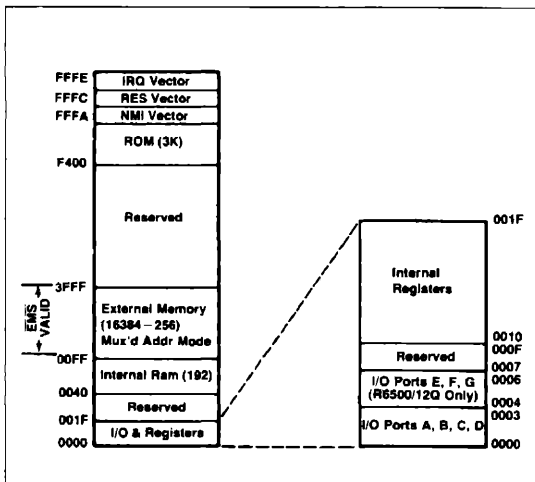
ADDRESS (HEX)	READ	WRITE
001F	---	---
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B.
1B	---	---
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	---	---
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	---
10	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
0F	---	---
0E	---	---
0D	---	---
0C	---	---
0B	---	---
0A	---	---
09	---	---
08	---	---
07	---	---
06	Port G*	Port G*
05	Port F*	Port F*
04	Port E*	Port E*
03	---	---
02	---	---
01	Port B	Port B
0000	Port A	Port A

NOTE: *R65F12 Only

C.2 MULTIPLE FUNCTION PIN ASSIGNMENTS— PORT C AND PORT D

PIN NUMBER		I/O PORT FUNCTION REPLACED	MULTIPLEXED PORT FUNCTION
R65F11	R65F12		
4	25	PC0	A0
5	26	PC1	A1
6	27	PC2	A2
7	28	PC3	A3
8	29	PC4	A12
9	30	PC5	R/W
10	31	PC6	A13
11	32	PC7	EMS
19	40	PD0	A4/D0
18	39	PD1	A5/D1
17	38	PD2	A6/D2
16	37	PD3	A7/D3
15	36	PD4	A8/D4
14	35	PD5	A9/D5
13	34	PD6	A10/D6
12	33	PD7	A11/D7

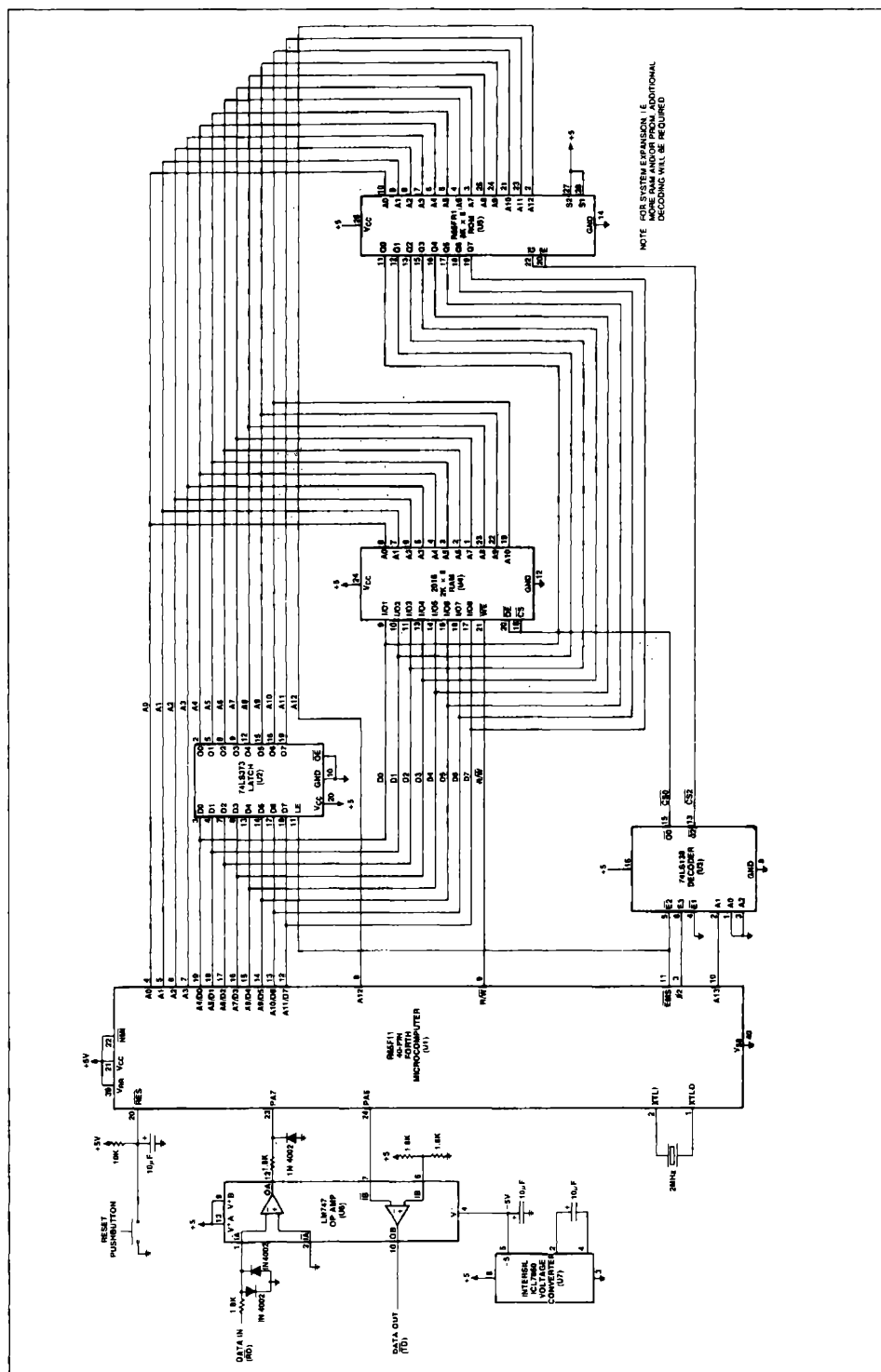
C.3 MULTIPLEXED MODE MEMORY MAP



C.4 SYSTEM VARIABLES IN RAM

ADDRESS	NAME	COLD START VALUE	WARM START VALUE
0040	IRQVEC	(COLD)	—
0042	NMIVEC	(COLD)	—
0044	UKEY	(INK)	(INK)
0046	UEMIT	(OUT)	(OUT)
0048	UP	0300	0300
004A	INTFLG	00	00
004B	(W-1)	6C	6C
004C	W	—	—
004E	IP	—	—
0050	(N-1)	—	—
0051	N	—	—
0059	XSAVE	—	—
005B	INTVEC	(COLD)	—
005D	TOS	—	—
0300	TIB	0380	0380
0302	R0	00FF	00FF
0304	S0	00C2	00C2
0306	UC/L	0050	—
0308	UPAD	037E	—
030A	UR/W	(DISK)	—
030C	BASE	0010	—
030E	CLD/WRM	—	—
0310	IN	—	—
0312	DPL	—	—
0314	HLD	—	—
0316	DISKNO	—	—
0318	CURCYL	—	—
031C	B/SIDE	—	—

APPENDIX D TYPICAL MINIMUM HOOKUP



APPENDIX E

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Commercial	T	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

DC CHARACTERISTICS

($V_{CC} = 5V \pm 5\%$, $V_{SS} = 0$, $T_A = 0$ to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Dissipation (Outputs High) Commercial at 25°C	P_D	—	—	1000	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial at 25°C	I_{RR}	—	4	—	mAdc
Input High Voltage (Except XTLI)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	—	+0.8	Vdc
Input Leakage Current (RES, NMI) $V_{IN} = 0$ to 5.0 Vdc	I_{IN}	—	—	± 10.0	μAdc
Input Low Current PA, PB, PC, PF*, and PG* ($V_{IL} = 0.4$ Vdc)	I_{IL}	—	-1.0	-1.6	mAdc
Output High Voltage (Except XTLO) ($I_{LOAD} = .100 \mu\text{Adc}$)	V_{OH}	+2.4	—	V_{CC}	Vdc
Output Low Voltage ($I_{LOAD} = 1.6$ mAdc)	V_{OL}	—	—	+0.4	Vdc
Darlington Current Drive, PE* ($V_O = 1.5$ Vdc)	I_{OH}	-1.0	—	—	mAdc
Input Capacitance ($V_{IN} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz) PA, PB, PC, PD, PF*, and PG* XTLI, XTLO	C_{in}	—	—	10 50	pF
I/O Port Pull-Up Resistance PA0-PA7, PB0-PB7, PC0-PC7, PF0-PF7 and PG0-PG7	R_L	3.0	6.0	11.5	K Ω
Output Leakage Current Tri-State I/Os while in High Impedance State	I_{OUT}	—	—	± 10	μAdc
Output Capacitance Tri-State I/Os while in High Impedance State $V_{IN} = 0V$, $T_A = 25^\circ\text{C}$, $f = 25^\circ\text{C}$, $f = 1.0$ MHz	C_{OUT}	—	—	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

*R65F12 only.

APPENDIX F

TIMING REQUIREMENTS AND CHARACTERISTICS

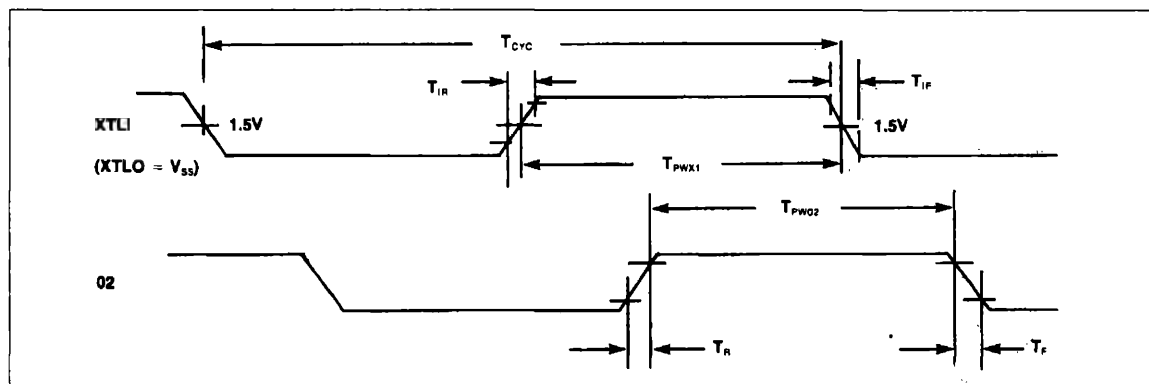
F.1 GENERAL NOTES

1. $V_{CC} = 5V \pm 5\%$, $0^\circ C \leq T_A \leq 70^\circ C$
2. A valid $V_{CC} - RES$ sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pf maximum, except as noted below:

PA, PB, PE, PF, PG — 50pf maximum

F.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 ± 25	—	250 ± 10	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1} ± 25	—	T_{PWX1} ± 20	—
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10



3

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T _{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T _{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	225	—	140
T _{PBAS}	(PD) Address Setup Time	—	225	—	140
T _{PBSU}	(PD) Data Setup Time	50	—	35	—
T _{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T _{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T _{PBDD}	(PD) Data Output Delay	—	175	—	150
T _{PCHA}	(PC0-PC4, PC8) Address Hold Time	30	—	30	—
T _{PBHA}	(PD) Address Hold Time	10	100	10	80
T _{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T _{PCHV}	(PC7) EMS Hold Time	10	—	10	—
T _{PCVD} ⁽¹⁾	(PC7) Address to EMS Delay Time	30	—	30	—
T _{PCVP}	(PC7) EMS Stabilization Time	30	—	30	—
T _{ESU}	EMS Set Up Time	—	350	—	210

F.3.1 Multiplex Mode Timing Diagram

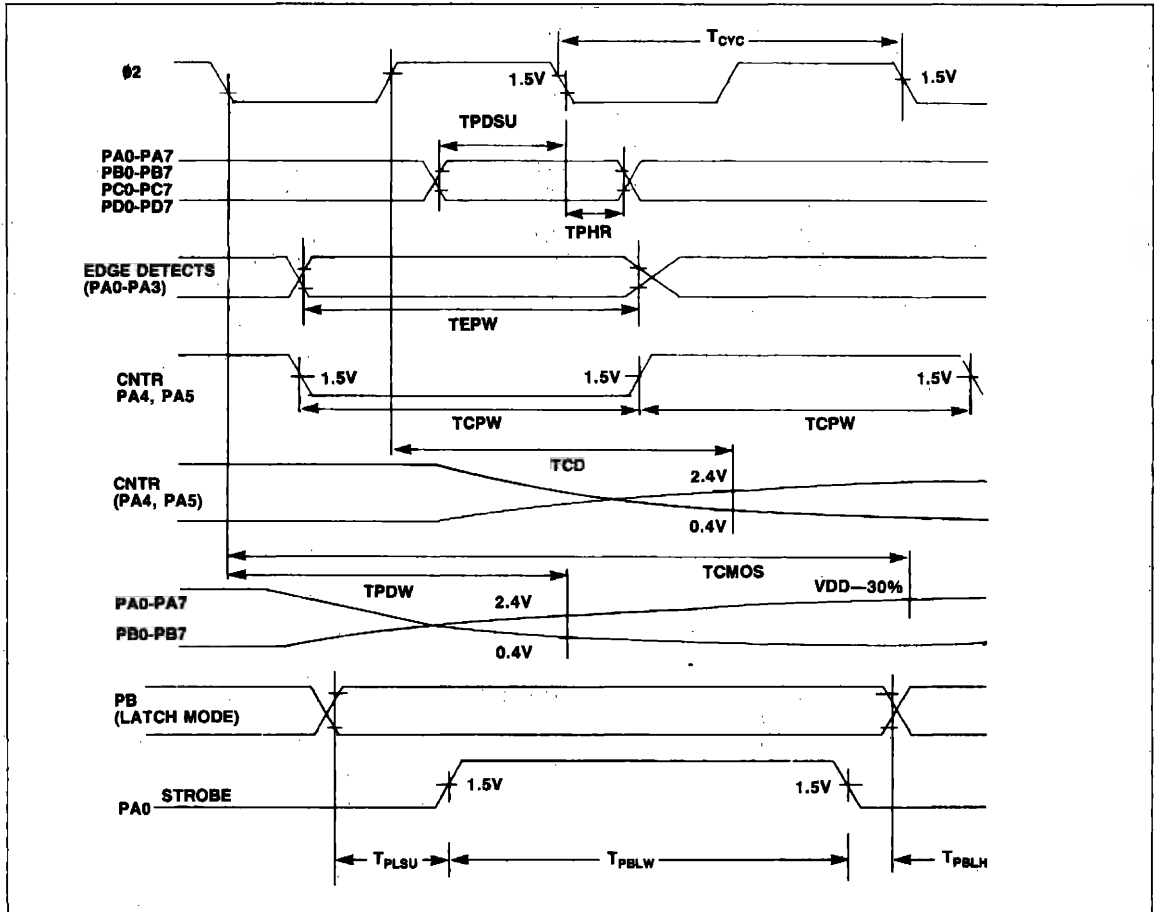


F.4 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
$T_{PDW}^{(1)}$ $T_{CMOS}^{(1)}$	Internal Write to Peripheral Data Valid PA, PB TTL PA, PB CMOS	— —	500 1000	— —	500 1000
T_{PDSU}	Peripheral Data Setup Time PA, PB	200	—	200	—
T_{PHR}	Peripheral Data Hold Time PA, PB	75	—	75	—
T_{EPW}	PA0-PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CPW} $T_{CD}^{(1)}$	Counters A and B PA4, PA5 Input Pulse Width PA4, PA5 Output Delay	T_{CYC} —	— 500	T_{CYC} —	— 500
T_{PBLW} T_{PLSU} T_{PBLH}	Port B Latch Mode PA0 Strobe Pulse Width PB Data Setup Time PB Data Hold Time	T_{CYC} 175 30	— — —	T_{CYC} 150 30	— — —
$T_{PDW}^{(1)}$ $T_{CMOS}^{(1)}$ T_{CPW} $T_{PDW}^{(1)}$ $T_{CMOS}^{(1)}$	Serial I/O PA6 XMTR TTL PA6 XMTR CMOS PA4 RCVR S/R Clock Width PA4 XMTR Clock—S/R Mode (TTL) PA4 XMTR Clock—S/R Mode (CMOS)	— — 4 T_{CYC} — —	500 1000 — 500 1000	— — 4 T_{CYC} — —	500 1000 — 500 1000

NOTE 1: Maximum Load Capacitance: 50pF Passive Pull-Up Required.

F.4.1 I/O Edge Detect, Counter, and Serial I/O Timing



APPENDIX G

INCLUDED FORTH FUNCTIONS IN ROM

BANKEXECUTE
 EEC!
 ?
 D.R
 #>
 INIT
 DISK
 MOD
 M/
 DABS
 S->D
 BLANKS
 EXPECT
 COUNT
 SPACE
 <
 2-
 PAD
 IN
 UPAD
 TIB
 2
 !
 +!
 SWAP
 DNEGATE
 0<
 >R
 RP!
 OR
 CMOVE
 EMIT
 (DO)
 BRANCH

BANKEEC!
 *
 #S
 <#
 DWRITE
 M/MOD
 /
 M*
 ABS
 COLD
 ERASE
 (.)
 DECIMAL
 PICK
 U<
 1-
 C/L
 CLD/WRM
 UC/L
 BL
 1
 C@
 BOUNDS
 2DROP
 NEGATE
 0=
 LEAVE
 SP!
 AND
 CR
 ENCLOSE
 (+LOOP)
 EXECUTE

BANKC@
 .R
 #
 SPACES
 DREAD
 */
 /MOD
 MAX
 D+-
 (NUMBER)
 FILL
 -TRAILING
 HEX
 ROT
 =
 2+
 HLD
 BASE
 R0
 4
 0.
 @
 2DUP
 DROP
 D+
 R
 ;S
 SP@
 U/
 ?TERMINAL
 (FIND)
 (LOOP)
 CLIT

BANKC!
 D.
 SIGN
 SEEK
 SELECT
 */MOD
 *
 MIN
 +-
 HOLD
 QUERY
 TYPE
 -DUP
 >
 -
 1+
 DPL
 UR/W
 S0
 3
 C!
 TOGGLE
 DUP
 OVER
 +
 R>
 RP@
 XOR
 U*
 KEY
 DIGIT
 OBRANCH
 LIT



R65FRx AND R65FKx RSC FORTH DEVELOPMENT AND KERNEL ROMS

INTRODUCTION

The Rockwell Single Chip (RSC) FORTH System can be configured using the R65F11, R65F12 microcomputers or the R6501Q ROM-less microcomputer. One of these microcomputers, when used in conjunction with a development ROM and a FORTH kernel ROM, provide the designer with maximum flexibility when developing FORTH applications.

RSC-FORTH is based on the popular fig-FORTH model with extensions. The R65F11 and R65F12 both have the kernel of the high level Rockwell Single Chip RSC-FORTH language contained in the preprogrammed ROM. The R65FK2 and R65FK3 Kernel ROMs are preprogrammed ROMs for use with the R6501Q when developing larger applications requiring more memory and I/O line support. All of the run time functions of the RSC-FORTH are contained in these ROMs, including 16- and 32-bit mathematical, logical and stack manipulation, plus memory and input/output operators. The RSC-FORTH Operating System allows an external user program written in RSC-FORTH or Assembly Language to be executed from external EPROM, or development of such a program under the control of the R65FR1, R65FR2 or R65FR3 RSC-FORTH Development ROMs.

This document describes five different RSC-FORTH system configurations using the development and kernel ROMs.

ORDERING INFORMATION

Part No.	Description
R65FR1P	FORTH Development ROM for R65F11 or R65F12
R65FR2P	FORTH Development ROM for R6501Q
R65FR3P	FORTH Development ROM for R6501Q
R65FK2P	FORTH Kernel ROM for R6501Q
R65FK3P	FORTH Kernel ROM for R6501Q
R65F11P	40-Pin FORTH Based Microcomputer at 1 MHz
R65F11AP	40-Pin FORTH Based Microcomputer at 2 MHz
R65F12Q	64-Pin FORTH Based Microcomputer at 1 MHz
R65F12AQ	64-Pin FORTH Based Microcomputer at 2 MHz
R6501Q	64-Pin One-Chip Microprocessor at 1 MHz
R6501AQ	64-Pin One-Chip Microprocessor at 2 MHz
Order No.	Description
2145	R6501Q One-Chip Microprocessor Product Description
2146	R65F11 and R65F12 FORTH Based Microcomputer Product Description
2148	RSC-FORTH User's Manual
2162	Application Note: A Low-Cost Development Module for the R65F11 FORTH Microcomputer

FEATURES

- R65FR1 FORTH Development ROM
 - 8K ROM
 - Addressable from \$2000 through \$3FFF in FORTH development configuration memory map
 - R65F11 and R65F12 compatible
 - Operates in the R65F11/F12 FORTH development configuration
- R65FR2 FORTH Development ROM
 - 8K ROM
 - Addressable from \$4000 through \$5FFF in the FORTH development configuration memory map
 - R6501Q compatible for use in emulation of the R65F11/F12 FORTH development configuration
- R65FR3 FORTH Development ROM
 - 8K ROM
 - Addressable from \$C000 through \$DFFF in the FORTH development configuration memory map
 - Operates in the R6501Q FORTH development configuration
- R65FK2 FORTH Kernel ROM
 - 4K ROM
 - Addressable from \$F400 through \$FFFF in the FORTH development configuration memory map
 - R6501Q compatible for use in the emulation of the R65F11/F12 FORTH development configuration
 - Replaces the FORTH kernel contained in the R65F11 and R65F12 microcomputers during development
- R65FK3 FORTH Kernel ROM
 - 4K ROM
 - Addressable from \$F400 through \$FFFF in the FORTH development and production configuration memory maps
 - R6501Q compatible
 - Operates in the R6501Q FORTH development and production configurations

RSC-FORTH SYSTEM CONFIGURATIONS

The three configurations of the RSC-FORTH System are identified by the CPU-Development ROM combinations listed below:

RSC-FORTH System Configurations

CPU	Kernel ROM	Development ROM	RSC Configuration
R65F11	none	R65FR1	1
R65F12	none	R65FR1	1
R6501Q	R65FK2	R65FR2	2
R6501Q	R65FK3	R65FR3	3

RSC-FORTH CONFIGURATION 1 (R65FR1)

R65F11/R65F12 DEVELOPMENT AND PRODUCTION

The RSC-FORTH Configuration 1 provides the designer with a FORTH development and application environment at a minimal cost. The application program is developed using an R65F11 or R65F12 microcomputer, an R65FR1 Development ROM and external RAM. Up to 8K bytes of RAM space is available using this configuration. However, Configuration 1 is limited to 5K or less bytes of RAM during development. This is the result of allocating 2K bytes of RAM for disk buffers and at least 1K bytes of RAM for the "Program heads". The program heads are contained in a dictionary containing the Name (NFA), Link Field Address (LFA) and the Parameter Field Address Pointer (PFA). This dictionary is a list of FORTH word words and user-defined FORTH words used in the development of a FORTH program and is not present during the execution of the FORTH program.

Although programs may reside in the upper 8K bytes of memory area, normally filled by the R65FR1 Development ROM, it is difficult to develop code for that area using this configuration of the RSC-FORTH System.

The difference in using the R65F11 or the R65F12 is in the number of I/O lines available to the user. The R65F11 supports 16 I/O lines, the R65F12 supports 40 I/O lines.

Figure 1 shows the development and production configurations for the R65F11/F12. Configurations 1A and 1B list the features, memory maps, and the relationship of the R65F11 and R65F12 to the R65FR1 Development ROM in the development and production environment.

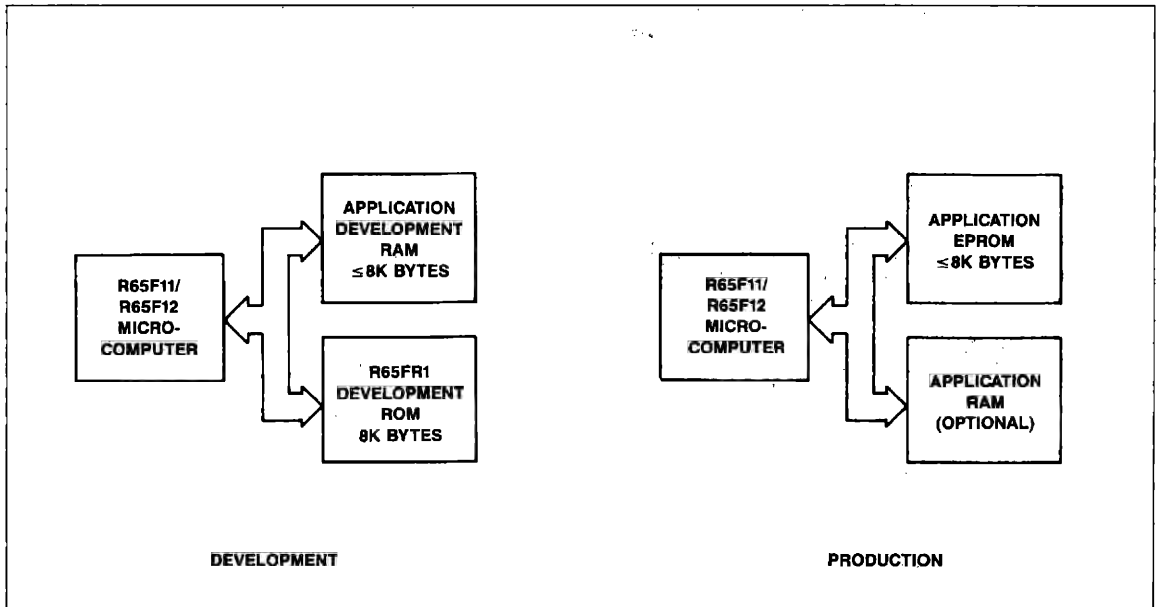


Figure 1. R65FR1 Configuration 1 Block Diagram

CONFIGURATION 1A CONSIDERATIONS

Features

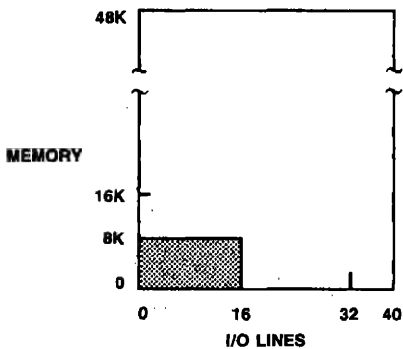
- 8K Bytes of User Memory
- 16 I/O Lines

Device Configuration

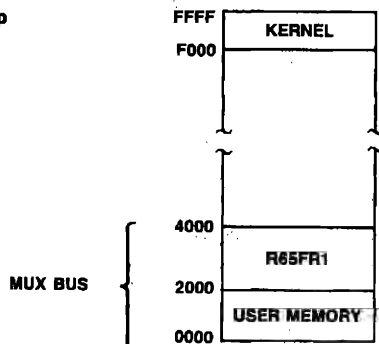
	DEVELOPMENT	PRODUCTION
R65F11 Microcomputer	✓	✓
R65FR1 Development ROM	✓	

User Memory—I/O Resource Matrix

User memory may be a mix of ROM, EEROM, UVPROM or RAM.



Memory Map



CONFIGURATION 1B CONSIDERATIONS

Features

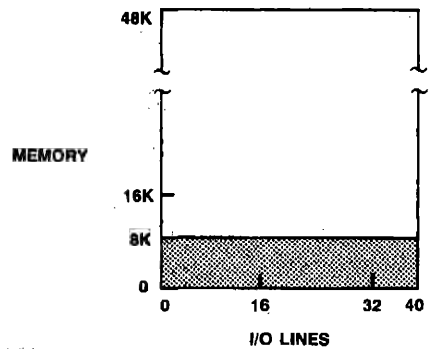
- 8K Bytes of User Memory
- 40 I/O Lines

Device Configuration

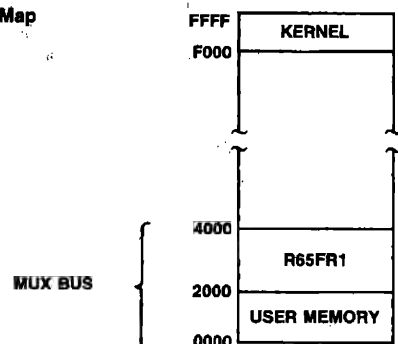
	DEVELOPMENT	PRODUCTION
R65F12 Microcomputer	✓	✓
R65FR1 Development ROM	✓	

User Memory—I/O Resource Matrix

User memory may be a mix of ROM, EEROM, UVPROM or RAM.



Memory Map



RSC-FORTH CONFIGURATION 2 (R65FR2, R65FK2)

R6501Q DEVELOPMENT AND R65F11/F12 PRODUCTION

The RSC-FORTH Configuration 2 provides the designer with the capability of using the full 16K bytes of external address space of the R65F11 and R65F12.

The R6501Q ROM-less microprocessor, when used with the R65FK2 Kernel ROM and the R65FR2 Development ROM, emulates the operation of the R65F11/F12. Because of the greater address space of the R6501Q, the R65FR2 Development ROM can be relocated to address \$4000 and the disk buffers and HEADS program to \$6000. This expands the available user memory space to 16K bytes, \$0000 through \$3FFF.

Using this configuration, the application program can be developed using the R6501Q and then later installed in an R65F11 or R65F12 microcomputer without modification.

Figure 2 shows the development and production configuration for the R6501Q. Configurations 2A and 2B list the features, memory maps, and the relationship of the R6501Q to the R65FR2 Development ROM and R65FK2 Kernel ROM in the development and production environment. Figure 3 is a schematic of the R6501Q, R65FR2, R65FK2 development setup.

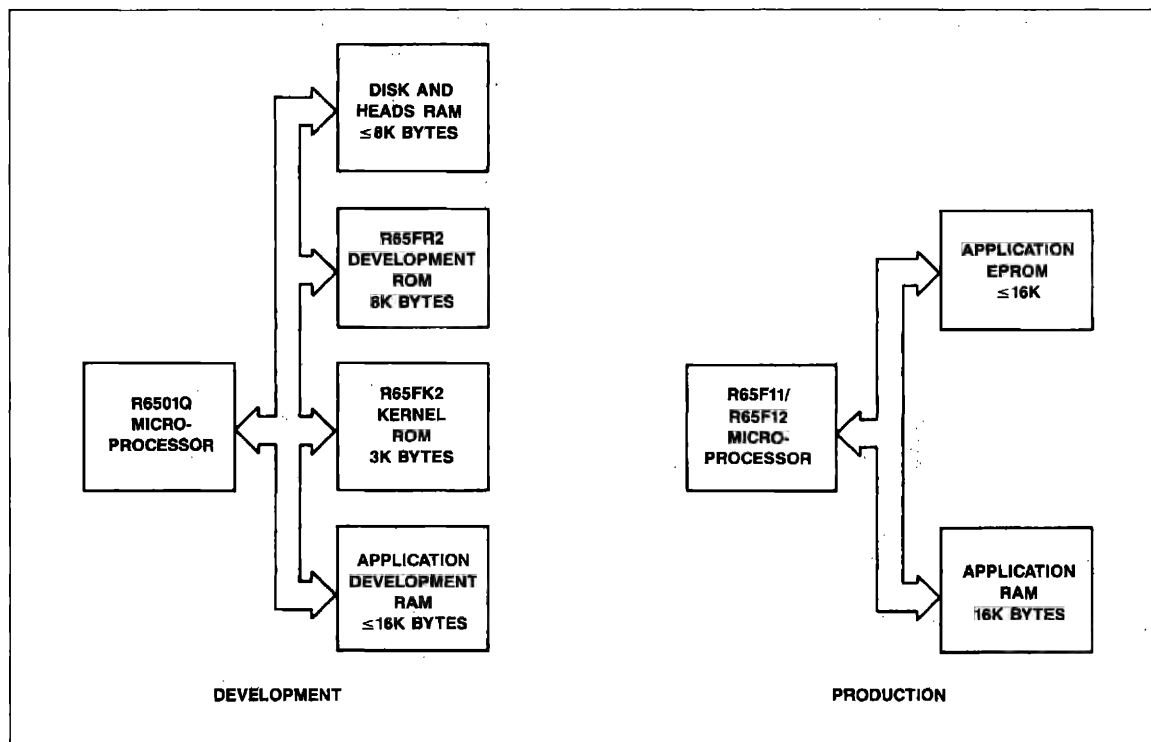


Figure 2. R65FR2 and R65FK2 Configuration 2 Block Diagrams

CONFIGURATION 2A CONSIDERATIONS

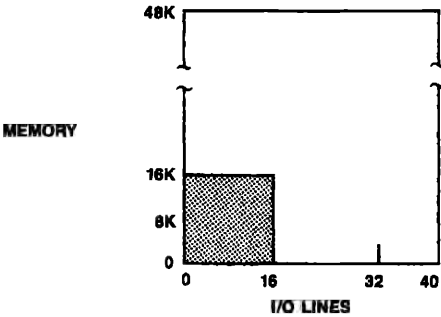
- Features
- 16K Bytes of User "Headerless" Memory
 - 16 I/O Lines

Device Configuration

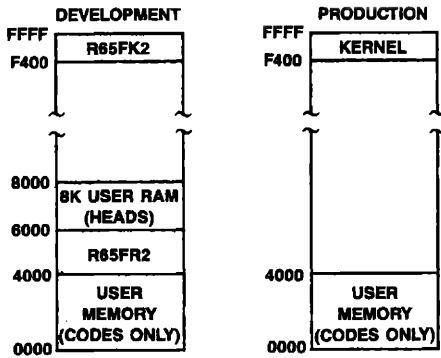
	DEVELOPMENT	PRODUCTION
R65F11 Microcomputer		✓
R6501Q Microprocessor	✓	
R65FR2 Development ROM	✓	
R65FK2 Kernel ROM	✓	

Memory—I/O Matrix

If floppy disk is used in the application, space for the disk buffers must be allocated in memory from \$0500 through \$3FFF or \$6000 through \$7FFF. User memory can be a mix of ROM, EEROM, UVROM or RAM.



Memory Maps



CONFIGURATION 2B CONSIDERATIONS

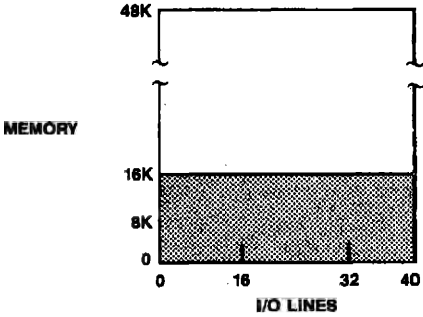
- Features
- 16K Bytes of User "Headerless" Memory
 - 40 I/O Lines

Device Configuration

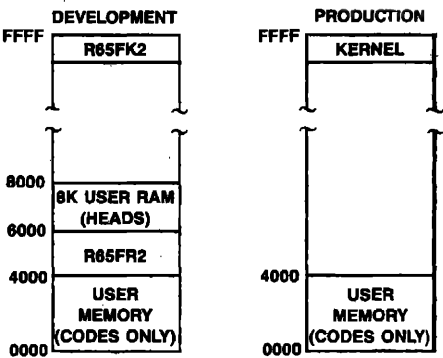
	DEVELOPMENT	PRODUCTION
R65F12 Microcomputer		✓
R6501Q Microprocessor	✓	
R65FR2 Development ROM	✓	
R65FK2 Kernel ROM	✓	

Memory—I/O Matrix

If floppy disk is used in the application, space for the disk buffers must be allocated in memory \$0000 through \$3FFF. User memory can be a mix of ROM, EEROM, UVROM or RAM.



Memory Maps



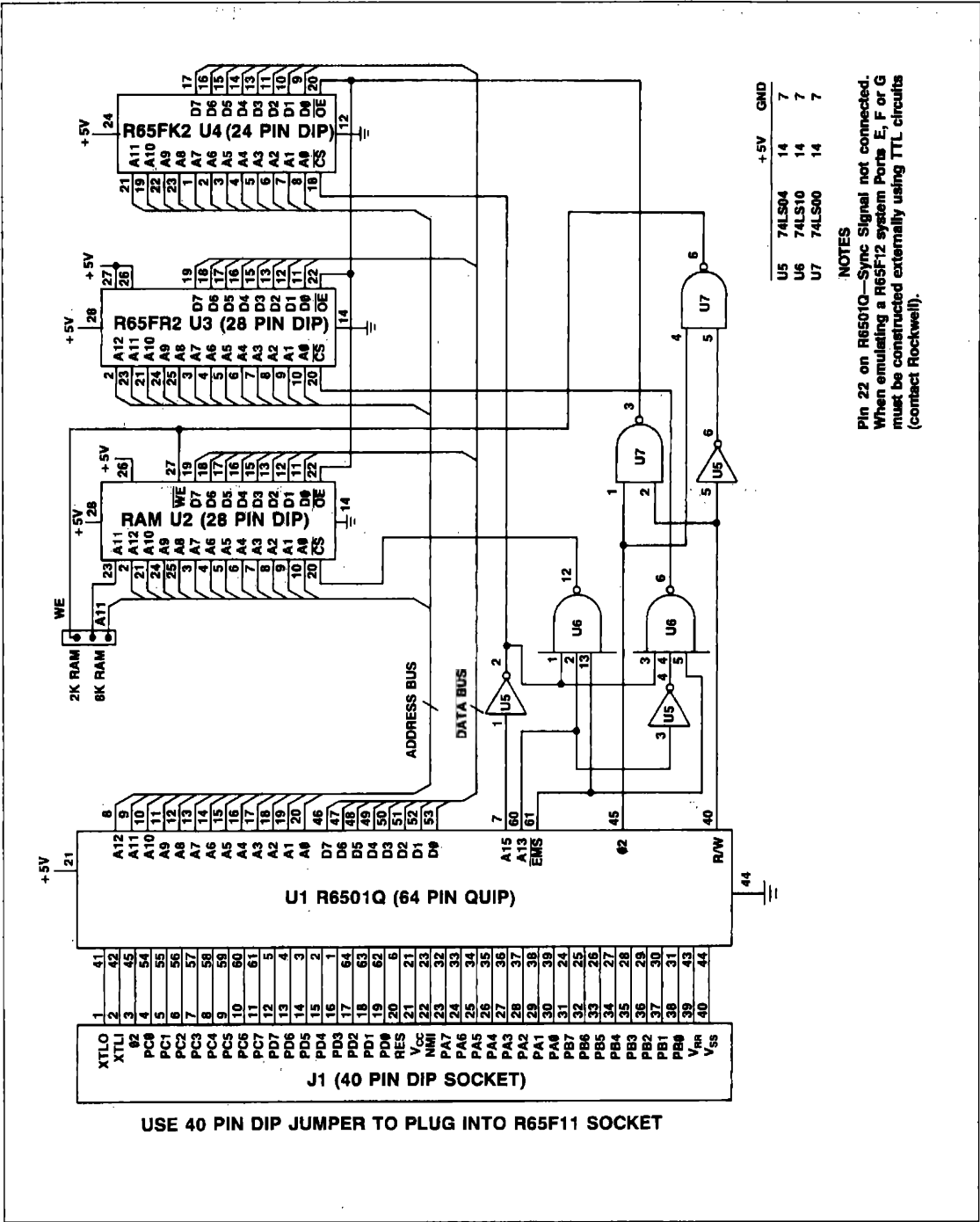


Figure 3. R6501Q, R65FR2 and R65FK2 Application Configuration Schematic

RSC-FORTH CONFIGURATION 3 (R65FR3, R65FK3)

R6501Q BASED SYSTEM DEVELOPMENT AND PRODUCTION

The RSC-FORTH Configuration 3 is designed for those applications which require a larger amount of ROM or RAM space than the R65F11 or R65F12 can provide.

In the development configuration, the user is provided with up to 48K bytes of memory. The user memory is located from \$0000 through \$BFFF. The program heads will use some of this area but the user will still have considerably more memory space available than in the previous configurations.

The production configuration provides up to 56K bytes of user memory. This is due to the fact that the R65FR3 Development ROM, used in the development configuration, is not required in the production configuration and releases the 8K bytes of memory space. This memory is located at \$C000 through \$DFFF.

Figure 4 shows the development and production configurations for the R6501Q. Configuration 3 lists the features, memory maps, and the relationship of the R6501Q to the R65FR3 Development ROM and the R65FK3 Kernel ROM in the development and production environment.

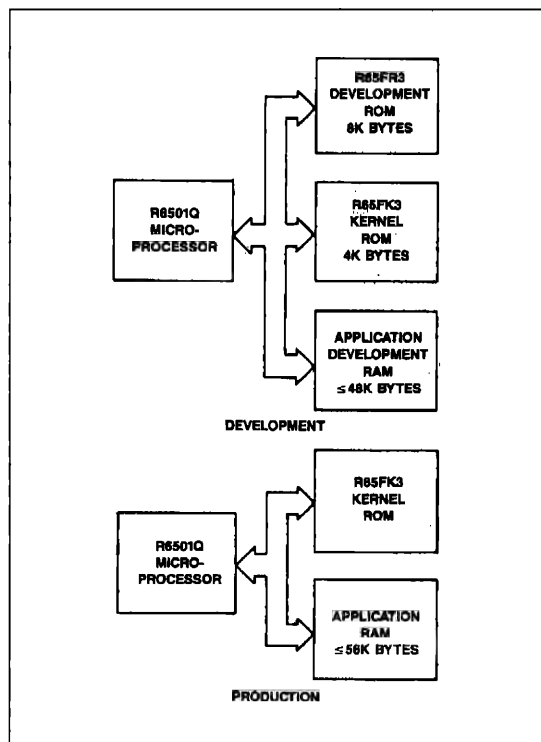


Figure 4. R65FR3 and R65FK3
Configuration 3 Block Diagrams

CONFIGURATION 3 CONSIDERATIONS

Features

- R6501Q w/FORTH
- 48K Bytes of User Memory
- 30 I/O Lines

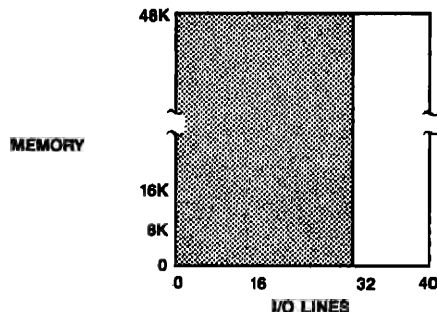
Device Configuration

	DEVELOPMENT	PRODUCTION
R6501Q Microcomputer	✓	✓
R65FK3 Development ROM	✓	
R65FR3 Kernel ROM	✓	✓

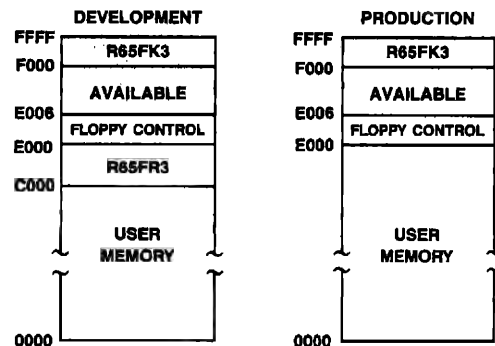
3

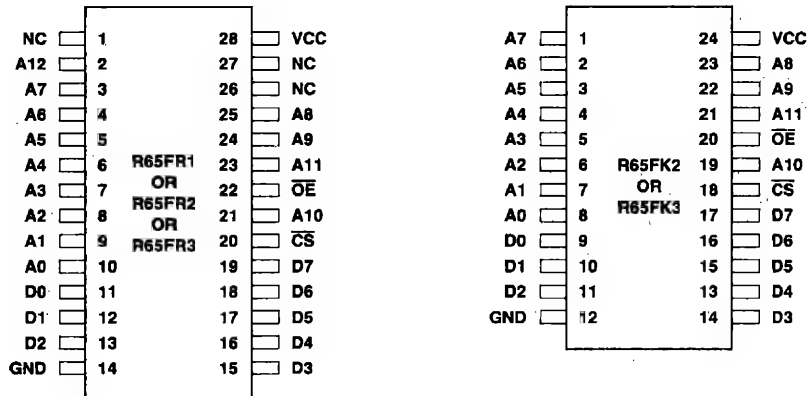
User Memory—I/O Resource Matrix

All ports act as I/O ports. Memory is on the bus. PC6 & PC7 (I/O lines) are assigned to memory. User memory can be a mix of ROM, EEROM, UVPROM or RAM.



Memory Maps





RSC-FORTH ROM Pin Assignments



R6501Q ONE-CHIP MICROPROCESSOR

SECTION 1 INTRODUCTION

3

1.1 FEATURES OF THE R6501Q

- Enhanced 6502 CPU
 - Four new bit manipulation instructions
 - Set Memory Bit (SMB)
 - Reset Memory Bit (RMB)
 - Branch on Bit Set (BBS)
 - Branch on Bit Reset (BBR)
 - Decimal and binary arithmetic modes
 - 13 addressing modes
 - True indexing
- 192-byte static RAM
- 32 bidirectional, TTL-compatible I/O lines (four ports)
- One 8-bit port may be tri-stated under software control
- One 8-bit port may have latched inputs under software control
- Two 16-bit programmable counter/timers, with latches
 - Pulse width measurement
 - Asymmetrical pulse generation
 - Pulse generation
 - Interval timer
 - Event counter
 - Retriggerable interval timer
- Serial port
 - Full-duplex asynchronous operation mode
 - Selectable 5- to 8-bit characters
 - Wake-up feature
 - Synchronous shift register mode
 - Standard programmable bit rates programmable up to 62.5K bits/sec @ 1 MHz
- Ten interrupts
 - Four edge-sensitive lines; two positive, two negative
 - Reset
 - Non-maskable
 - Two counter underflows
 - Serial data received
 - Serial data transmitted

- Bus expandable to 64K bytes of external memory
- Flexible clock circuitry
 - 2-MHz or 1-MHz internal operation
 - 4 MHz Crystal used to generate internal clocks
- 1 μ s minimum instruction execution time at 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- 64-pin QUIP

1.2 SUMMARY

The Rockwell R6501Q is a complete, high-performance 8-bit NMOS-3 microcomputer on a single chip and is compatible with all members of the R6500 family.

The R6501Q consists of an enhanced 6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory (RAM), and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts, and bus expandability.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the R6501Q a leading candidate for microcomputer applications.

Rockwell supports development of the R6501Q with the System 65 Microcomputer Development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This product description assumes that the reader is familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Number 29650N31). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Document Number 29650N30).

1.3 CUSTOMER OPTIONS

The R6501Q has no customer specified mask options. It has the following characteristics.

- Crystal Oscillator
- Clock Divide by 4
- Clock MASTER Mode
- Reset Vector at FFFF
- Internal pull-up resistors on Ports PA, PB, and PC

1.4 ORDERING INFORMATION

R6501Q — 4 MHz Xtal, 1 MHz Operation

R6501AQ — 4 MHz Xtal, 2 MHz Operation

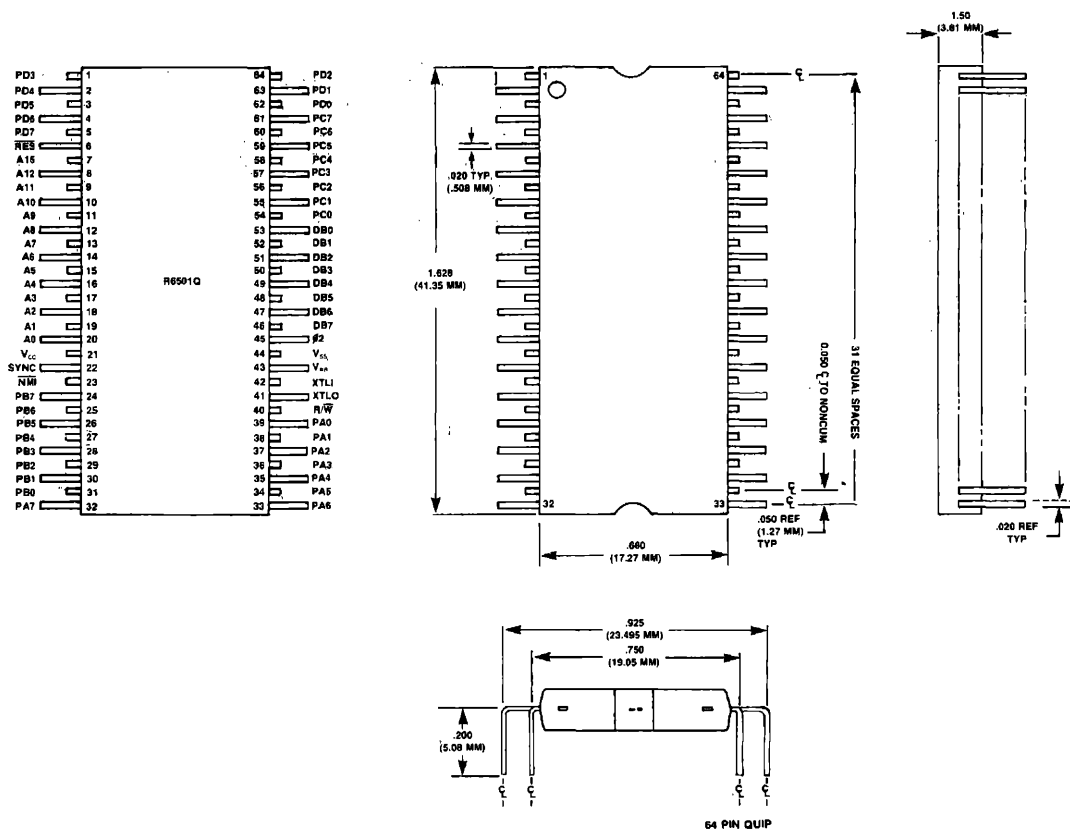


Figure 2-1. Mechanical Outline & Pin Out Configuration

SECTION 2

R6501Q INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6501Q. Figure 2-1 and 2-2 show the Interface Diagram and the pin out configuration for both devices. Table 2-1 describes the function of each pin. Figure 3-1 has a detailed block diagram of the R6501Q ports which illustrates the internal function of the device.

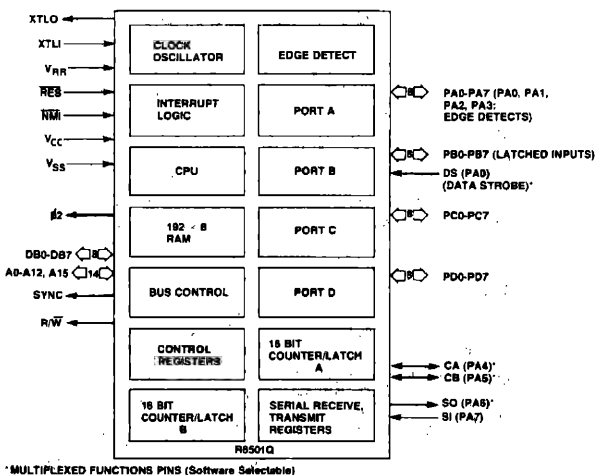


Figure 2-2. Interface Diagram

TABLE 2-1. R6501Q Pin Descriptions

SIGNAL NAME	PIN NO.	DESCRIPTION
V _{CC}	21	Main power supply +5V
V _{RR}	43	Separate power pin for RAM. In the event that V _{CC} power is off, this power retains RAM data.
V _{SS}	44	Signal and power ground (0V)
XTLI	42	Crystal or clock input for internal clock oscillator. Allows input of X1 clock signal if XTLO is connected to V _{SS} or of X4 clock if XTLO is floated.
XTLO	41	Crystal output from internal clock oscillator.
RES	6	The Reset input is used to initialize the device. This signal must not transition from low to high for at least eight cycles after V _{CC} reaches operating range and the internal oscillator has stabilized.
Ø2	45	Clock signal output at internal frequency.
NMI	23	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated with the CPU.
PA0-PA7	39-32	Four 8-bit ports used for either input/output. Each line of Ports A, B and C consists of an active transistor to V _{SS} and a passive pull-up to V _{CC} .
PB0-PB7	31-24	Port D functions as either an 8-bit input or 8-bit output port. It has active pull-up and pull-down transistors.
PC0-PC7	54-61	
PD0-PD7	62-64, 1-5	
A0-A12, A15	20-7	Fourteen address lines used to address a complete 65K external address space. Note: A13 & A14 are sourced through PC6 & PC7 when in the Full Address Mode.
DB0-DB7	53-46	Eight bidirectional data bus lines used to transmit data to and from external memory.
SYNC	22	SYNC is a positive going signal for the full clock cycle whenever the CPU is performing an OP CODE fetch.
R/W	40	Controls the direction of data transfer between the CPU and the external 65K address space. The signal is high when reading and low when writing.

SECTION 3

SYSTEM ARCHITECTURE

This section provides a functional description of the R6501Q. Functionally the R6501Q consists of a CPU, RAM, four 8-bit parallel I/O ports, a serial I/O port, dual counter/latch circuits, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The R6501Q internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal IRQ interrupt, or the external interrupt line NMI. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may be accessed only from the top. The address of a memory

location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Arithmetic And Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register, then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

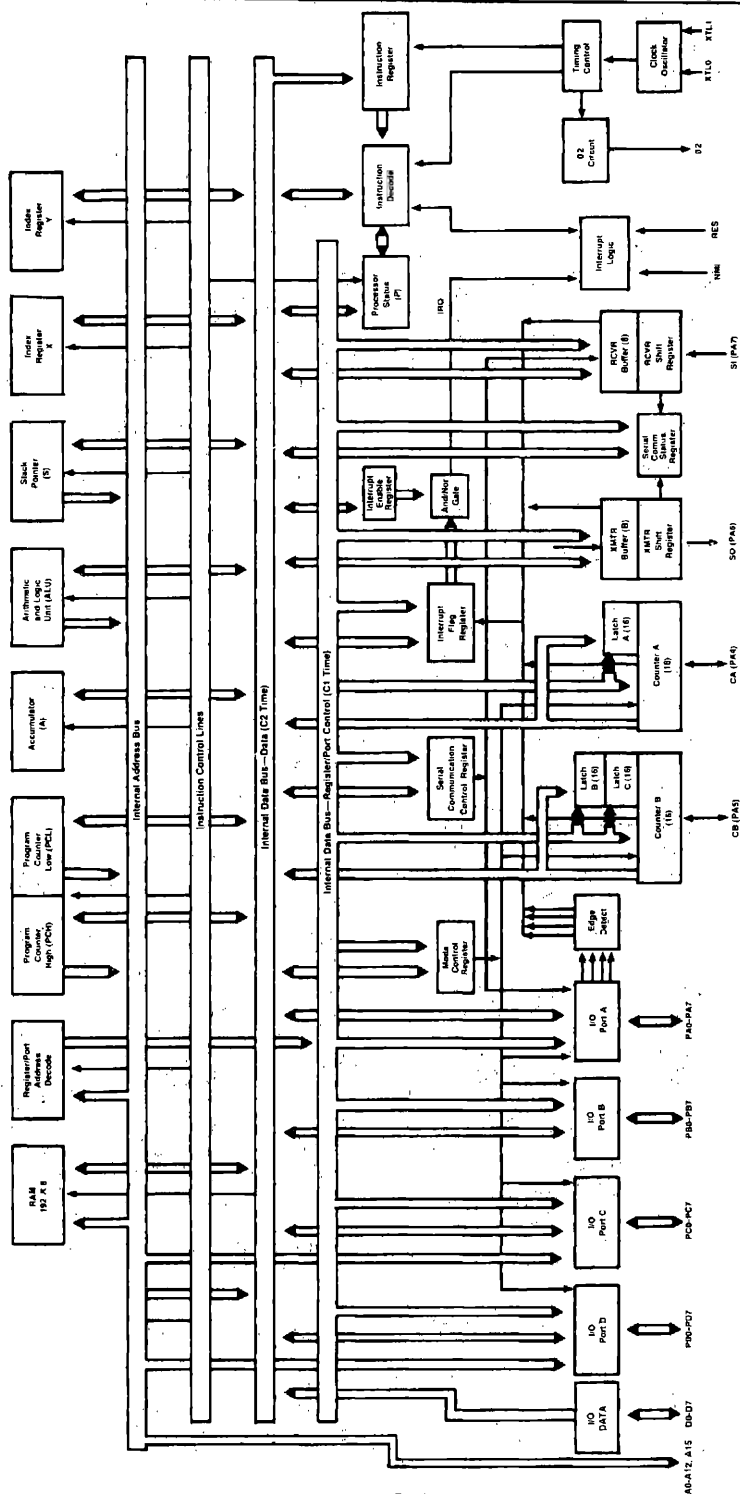


Figure 3-1. Detailed Block Diagram

3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; RES, NMI and IRQ. IRQ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 NEW INSTRUCTIONS

In addition to the standard R6502 instruction set, four new bit manipulation instructions have been added to the R6501Q. The added instructions and their format are explained in the following paragraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions. The four added instructions do not impact the CPU processor status register.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and one of eight bits to be set. The second byte of the instruction designates address (0-255) of the byte to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch On Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of eight bits designated by a 3-bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8-bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

3.3 READ-ONLY-MEMORY (ROM)

The R6501Q has no ROM and its Reset vector is at FFFC.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R6501Q provides a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC} . During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC} , V_{RR} must be supplied within operating range and RES must be driven low at least eight $\phi 2$ clock pulses before V_{CC} falls out of operating range. RES must then be held low while V_{CC} is out of operating range and until at least eight $\phi 2$ clock cycles after V_{CC} is again within operating range and the internal $\phi 2$ oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3-2 shows typical waveforms.

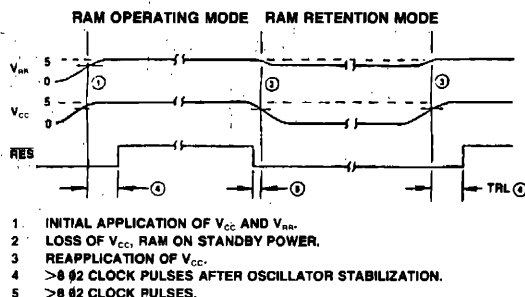


Figure 3-2. Data Retention Timing

3.5 CLOCK OSCILLATOR

The R6501Q has been configured for a crystal oscillator, a countdown network, and for Master Mode Operation.

A reference frequency can be generated with the on-chip oscillator using either an external crystal or an external oscillator. The oscillator reference frequency passes through an internal countdown network to obtain the internal operating frequency (see Figures 3-3a and 3-3b). The external crystal generated reference frequency is a preferred method since the resistor method can have tolerances approaching 50%.

Note:

When operating at 1 MHz interval frequency (R6501Q) place a 15-22 pF capacitor between XTLO and ground.

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 3-3c shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS} , the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

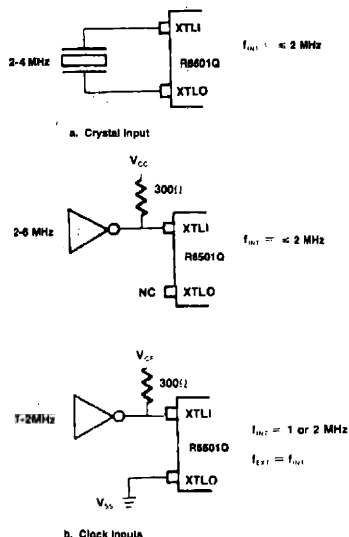


Figure 3-3. Clock Oscillator Input Options

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the R6501Q in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-5.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{\text{IRQ}}$ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple

simultaneous interrupts cause the $\overline{\text{IRQ}}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by RES. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-6 and the functions of each bit are explained in Table 3-1.

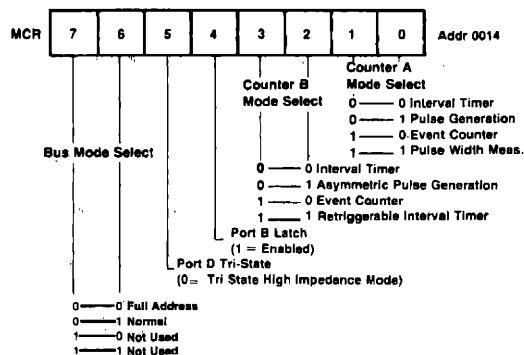


Figure 3-5. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4.

The use of Port D in Tri-State Enable is shown in Section 4.6.

The use of Bus Mode Select is shown in Section 4.5 and 4.6.

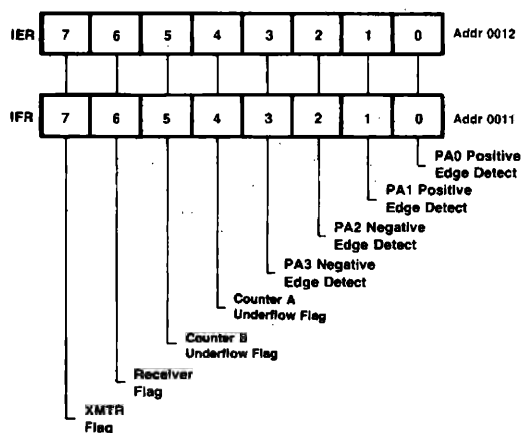


Figure 3-6. Interrupt Enable and Flag Registers

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-7, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

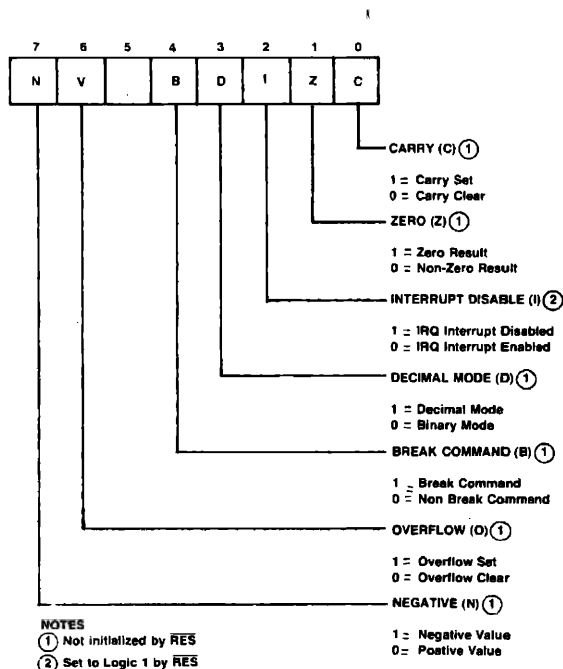


Figure 3-7. Processor Status Register

Table 3-1. Interrupt Flag Register Bit Codes

BIT CODE	FUNCTION
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB 0 (0010) instruction or by RES.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by RES.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by RES.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by RES.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by RES.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by RES.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by RES.
IFR 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by RES.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request ($\overline{\text{IRQ}}$). If the I Bit is reset to logic 0, the $\overline{\text{IRQ}}$ signal will be serviced. If the bit is set to logic 1, the $\overline{\text{IRQ}}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET (RES), $\overline{\text{IRQ}}$, or Non-Maskable Interrupt (NMI) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit is set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D) is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction clears it. The PLP and RTI instructions also affect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{\text{IRQ}}$ service routine to be entered. If the $\overline{\text{IRQ}}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{\text{IRQ}}$ routine was entered as the result of an $\overline{\text{IRQ}}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or -128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction—which may be used to sample interface devices—allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions affecting the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7) in the resulting value of a data movement or data arithmetic operation is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4

PARALLEL INPUT/OUTPUT PORTS & BUS MODES

The devices have 32 I/O lines grouped into four 8-bit ports (PA, PB, PC, and PD). Ports A through C may be used either for input or output individually or in groups of any combination. Port D may be used as all inputs or all outputs.

Multifunction I/O's such as Port A and Port C are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of $3K \leq R_L \leq 12K \text{ ohm}$) are provided on all port pins except Port D.

The direction of the 32 I/O lines are controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, thus simplifying I/O handling. The I/O addresses are shown in Table 4-1. Appendix E.4 shows the I/O Port Timing.

Table 4-1. I/O Port Addresses

PORT	ADDRESS
A	0000
B	0001
C	0002
D	0003

4.1 INPUTS

Inputs for Ports A, B, and C are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low ($<0.8V$) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high ($>2.0V$) input will cause a logic 1 to be read. An RES signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port D may only be all inputs or all outputs. All inputs is selected by setting bit 5 of the Mode Control Register (MCR5) to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, & PD. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru D are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high ($>2.4V$) output while a logic 0 will force a low ($<0.4V$) output.

Port D all outputs is selected by setting MCR5 to a "1".

4.3 Port A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the $\phi 2$ clock rate. Edge detection timing is shown in Appendix E.3.

Table 4-2. Port A Control and Usage

PA0 (2) PIN 39	PA0 I/O		PORT B LATCH MODE	
	MCR4 = 0		MCR4 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA0	I/O	PORT B LATCH STROBE	INPUT (1)
PA1 (2) PIN 38 PA2 (3) PIN 37 PA3 (3) PIN 36	PA1-PA3 I/O			
	SIGNAL			
	NAME	TYPE		
	PA1	I/O		
	PA2	I/O		
	PA3	I/O		
PA4 PIN 35	PA4 I/O		COUNTER A I/O	
	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4) (5)		MCR0 = 1 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4)	
			SCCR7 = 0 SCCR6 = 0 MCR1 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA4	I/O	CNTA	OUTPUT
			NAME	TYPE
			CNTA	INPUT (1)
	SERIAL I/O SHIFT REGISTER CLOCK			
	SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1 (4)	
PA5 PIN 34	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)
PA6 PIN 33	PA5 I/O		COUNTER B I/O	
	MCR3 = 0 MCR2 = 0		MCR3 = 1 MCR2 = X	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA5	I/O	CNTB	OUTPUT
			CNTB	INPUT (1)
PA7 PIN 32	PA6 I/O		SERIAL I/O XMTR OUTPUT	
	SCCR7 = 0		SCCR7 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA6	I/O	XMTR	OUTPUT
PA7 PIN 32	PA7 I/O		SERIAL I/O RCVR INPUT	
	SCCR6 = 0		SCCR6 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA7	I/O	RCVR	INPUT (1)

- (1) HARDWARE BUFFER FLOAT
- (2) POSITIVE EDGE DETECT
- (3) NEGATIVE EDGE DETECT
- (4) RCVR S/R MODE = 1 WHEN
SCCR6 · SCCR5 · SCCR4 = 1
- (5) For the following mode combinations PA4 is available as an Input Only pin:
SCCR7·SCCR6·SCCR5·MCR1
+ SCCR7·SCCR6·SCCR4·MCR1
+ SCCR7·SCCR6·SCCR5
+ SCCR7·SCCR5·SCCR4

4.4 PORT B (PB)

Port B can be programmed as an 8-bit, bit-independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-3 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Appendix E.3.

Table 4-3. Port B Control & Usage

PIN #	PIN NAME	I/O MODE		LATCH MODE	
		MCR4 = 0		MCR4 = 1 (2)	
		SIGNAL		SIGNAL	
		NAME	TYPE (1)	NAME	TYPE
31	PB0	PB0	I/O	PB0	INPUT
30	PB1	PB1	I/O	PB1	INPUT
29	PB2	PB2	I/O	PB2	INPUT
28	PB3	PB3	I/O	PB3	INPUT
27	PB4	PB4	I/O	PB4	INPUT
26	PB5	PB5	I/O	PB5	INPUT
25	PB6	PB6	I/O	PB6	INPUT
24	PB7	PB7	I/O	PB7	INPUT

- (1) RESISTIVE PULL-UP, ACTIVE BUFFER PULL DOWN
(2) INPUT DATA IS STORED IN PORT B LATCH BY PA0 PULSE

4.5 PORT C (PC)

Port C can be programmed as an I/O port, or as part of the full address bus. When operating in the Full Address Mode PC6 and PC7 serve as A13 and A14 with PC0-PC5 operating as normal I/O pins.

4.6 PORT D (PD)

Port D can be programmed as an I/O Port. Mode selection for Port D is made by the Mode Control Register (MCR). The Port D output drivers can be selected as tri-state drivers by setting bit 5 of the MCR to 1 (one). Table 4-5 shows the necessary settings for the MCR to achieve the various modes for Port D.

4.7 BUS MODES

In the Full Address Mode, the separate address and data bus are used in conjunction with PC6 and PC7, which automatically provide A13 and A14. The remaining ports perform the normal I/O function.

In the I/O Bus Mode all ports serve as I/O. The address and data bus are still functional but without A13 and A14. Since the internal RAM and registers are in the OOOX location, A15 can be used for chip select and A0-A12 used for selecting 8K of external memory.

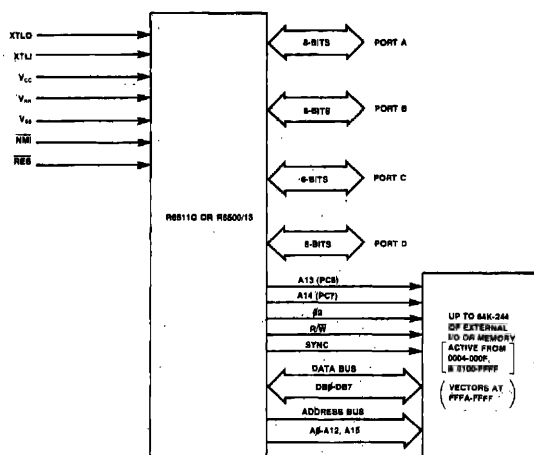


Figure 4-1a. Full Address Mode

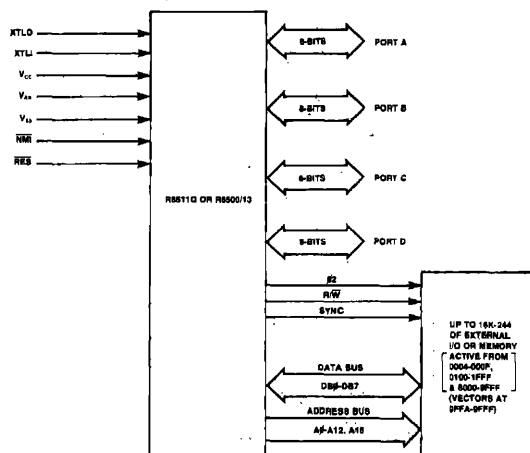


Figure 4-1b. Normal Bus Mode

Table 4-4. Port C Control and Usage

PIN #		FULL ADDRESS MODE		I/O MODE	
		MCR7 = 0 MCR6 = 0		MCR7 = 0 MCR6 = 1	
		SIGNAL		SIGNAL	
PIN #	PIN NAME	NAME	TYPE	NAME	TYPE (1)
54	PC0	PC0	I/O (1)	PC0	I/O
55	PC1	PC1	I/O (1)	PC1	I/O
56	PC2	PC2	I/O (1)	PC2	I/O
57	PC3	PC3	I/O (1)	PC3	I/O
58	PC4	PC4	I/O (1)	PC4	I/O
59	PC5	PC5	I/O (1)	PC5	I/O
60	PC6	A13	OUTPUT (2)	PC6	I/O
61	PC7	A14	OUTPUT (2)	PC7	I/O

NOTES:

1. Resistive Pull-Up, Active Buffer Pull-Down
2. Active Buffer Pull-Up and Pull-Down

Table 4-5. Port D Control and Usage

PIN #		I/O MODES			
		MCR7 = 0 MCR6 = X MCR5 = 0		MCR7 = 0 MCR6 = X MCR5 = 1	
		SIGNAL		SIGNAL	
PIN #	PIN NAME	NAME	TYPE (1)	NAME	TYPE (2)
62	PD0	PD0	INPUT	PD0	OUTPUT
63	PD1	PD1	INPUT	PD1	OUTPUT
64	PD2	PD2	INPUT	PD2	OUTPUT
1	PD3	PD3	INPUT	PD3	OUTPUT
2	PD4	PD4	INPUT	PD4	OUTPUT
3	PD5	PD5	INPUT	PD5	OUTPUT
4	PD6	PD6	INPUT	PD6	OUTPUT
5	PD7	PD7	INPUT	PD7	OUTPUT

NOTES:

1. Tri-State Buffer is in High Impedance Mode
2. Tri-State Buffer is in Active Mode

SECTION 5

SERIAL INPUT/OUTPUT CHANNEL

The device provides a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (at $f_2 = 1$ MHz). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

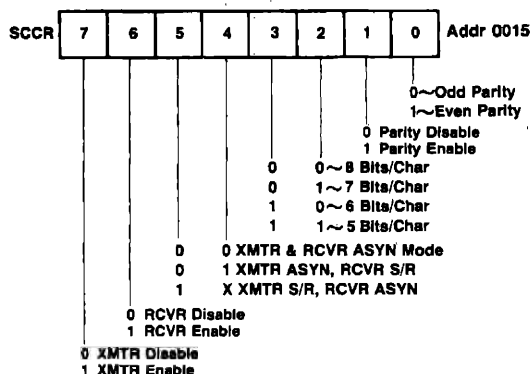


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XMTR)

The XMTR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are shown in Figure 5-2. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

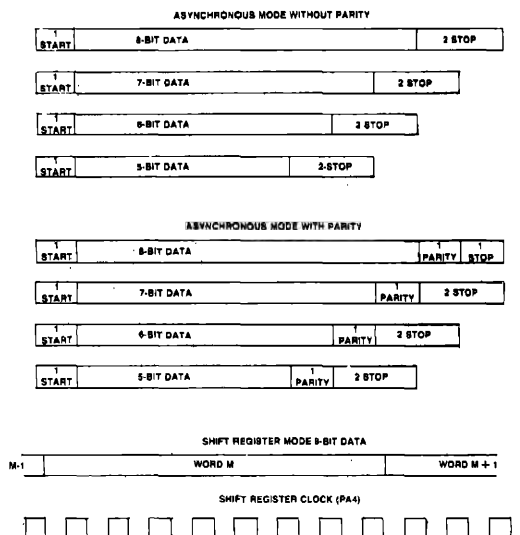


Figure 5-2. SIO Data Modes

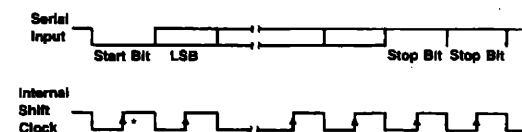
In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter under-runs in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCSR5, SCSR6 and SCSR7.

$$\text{IFR7} = \text{SCSR6} (\text{SCSR5} + \text{SCSR7})$$

5.2 RECEIVER OPERATION (RCVR)

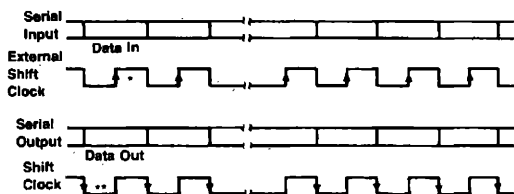
The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, the appropriate number of data bits, a parity bit (if enabled), and one stop bit. Refer to paragraph 5.1 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits. Any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.



* Serial Input Data Shifted In

Figure 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.



* Serial Input Data Shifted In

** Serial Output Data Makes Transition

Figure 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR 0: Receiver Data Register Full—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by RES and is disabled if SCCR 6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition; instead, a corresponding error bit will be set to a logic 1.

SCSR 1: Over-Run Error—Set to a logic 1 when a new character is transferred from the Receiver Shift Register with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register or by RES.

SCSR 2: Parity Error—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the

received data has a parity error. This bit is cleared by reading the Receiver Data Register or by RES.

SCSR 3: Framing Error—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by RES (ASYN Mode only).

SCSR 4: Wake-Up—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by RES or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR 5: End of Transmission—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by RES or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6: Transmitter Data Register Empty—Set to a logic 1 when the contents of the Transmitter Data Register are transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmitter Data Register. This bit is initialized to a logic 1 by RES.

SCSR 7: Transmitter Under-Run—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register or by RES.

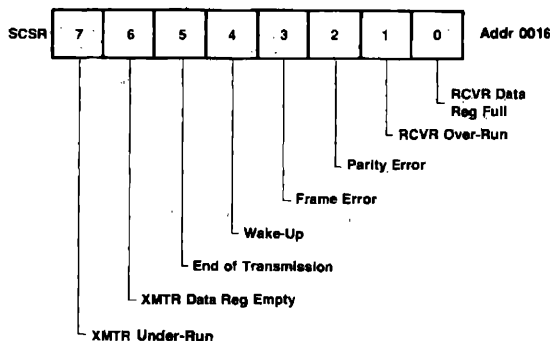


Figure 5-5. SCSR Bit Allocations

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of eleven consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6

COUNTER/TIMERS

The device contains two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A

- Pulse width measurement
- Pulse Generation
- Interval Timer
- Event Counter

Counter B

- Retriggerable Interval Counter
- Asymmetrical Pulse Generation
- Interval Timer
- Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either $\phi 2$ clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the

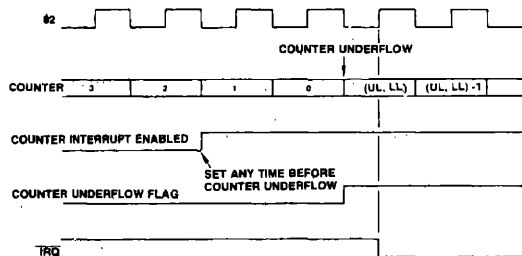


Figure 6-1. Interval Timer Timing Diagram

Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value—not FFFF—and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by RES.

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are $\phi 2$ clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a RES signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).
2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the $\phi 2$ clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore $1\mu\text{s}$ to 65.535 ms at the 1 MHz $\phi 2$ clock rate or $0.5\mu\text{s}$ to 32.767 ms at the 2 MHz $\phi 2$ clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting IRQ interrupt requests in the counter IRQ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an IRQ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the IRQ interrupt routine to determine that the IRQ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

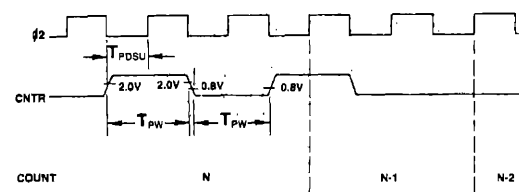


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the $\phi 2$ clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6.3.

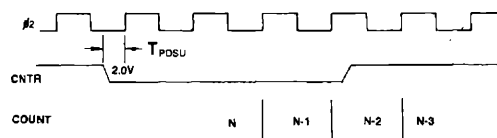


Figure 6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-1 identifies the values to be loaded in Counter A for selecting standard data rates with a $\phi 2$ clock rate of 1 MHz and 2 MHz. Although Table 6-1 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{16 \times \text{bps}} - 1$$

where

- N = decimal value to be loaded into Counter A using its hexadecimal equivalent.
- $\phi 2$ = the clock frequency (1 MHz or 2 MHz)
- bps = the desired data rate.

NOTE

In Table 6-1 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-1 for those baud rates which fall outside this limit.

Table 6-1. Counter A Values for Baud Rate Selection

STANDARD BAUD RATE	HEXADECIMAL VALUE		03 ACTUAL BAUD RATE AT		CLOCK RATE NEEDED TO GET STANDARD BAUD RATE	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600.96	1.0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either $\phi 2$ clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a Read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A Read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value and can be loaded at any time by executing a Write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by RES.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode. Mode Control Register bits MCR2 and MCR3 select the four Counter B modes in a similar manner and coding as MCR0 and MCR1 select the modes of Counter A.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

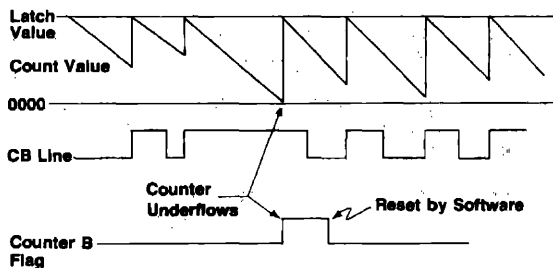


Figure 6-4. Counter B Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value corresponding to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C; the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.
2. The lower 8 bits of D are loaded into LLB by writing to address 001C; the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and the CB output to go low as shown in Figure 6-5.
3. When Counter B underflow occurs the contents of the Latch C are loaded into the Counter B and the CB output toggles to a high level, staying high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

SECTION 7

POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER ON TIMING

After application of V_{CC} and V_{RR} power to the device, \overline{RES} must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at $\phi 2$ (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

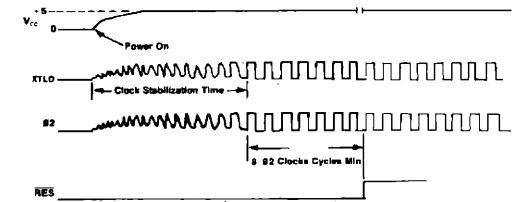


Figure 7-1. Power Turn-On Timing Detail

7.2 POWER-ON RESET

When \overline{RES} goes from low to high, the device sets the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiates a reset vector fetch at address FFFC and FFFD to begin user program execution. All of the I/O ports (PA, PB, PC, PD) will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timers counter mode (mode 00) to be selected and all interrupt enabled bits to be reset.

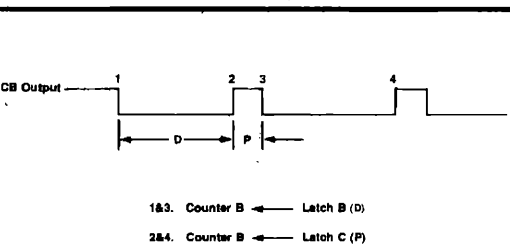


Figure 6-5. Counter B Pulse Generation

7.3 RESET (\overline{RES}) CONDITIONING

When \overline{RES} is driven from low to high the device is put in a reset state causing the registers and I/O ports to be configured as shown in Table 7-1.

Table 7-1. \overline{RES} Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
REGISTERS								
Processor Status	—	—	—	—	—	1	—	—
Mode Control (MCR)	0	0	0	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	0	0	0	0	0	0	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1
PC Latch	1	1	1	1	1	1	1	1
PD Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

7.4 INITIALIZATION

Any initialization process for the device should include a \overline{RES} , as indicated in the preceeding paragraphs. After stabilization of the internal clock (if a power on situation) an initialization routine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required
5. Clear Interrupts

A typical initialization subroutine could be as follows:

- LDX Load stack pointer starting address into X Register
- TXS Transfer X Register value to Stack Pointer
- CLD Clear Decimal Mode
- SEC Set Carry Flag
- ... Set-up Mode Control and
- ... special function registers
- ... and clear RAM as required
- CLI Clear Interrupts

APPENDIX A

ENHANCED R6502 INSTRUCTION SET

This appendix contains a summary of the Enhanced R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Document 29650 N30. The four instructions notated with a * are added instructions to enhance the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative	NOP	No Operation
BCC	Branch on Carry Clear		
BCS	Branch on Carry Set	ORA	"OR" Memory with Accumulator
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator	PHA	Push Accumulator on Stack
BMI	Branch on Result Minus	PHP	Push Processor Status on Stack
BNE	Branch on Result not Zero	PLA	Pull Accumulator from Stack
BPL	Branch on Result Plus	PLP	Pull Processor Status from Stack
BRK	Force Break		
BVC	Branch on Overflow Clear	*RMB	Reset Memory Bit
BVS	Branch on Overflow Set	ROL	Rotate One Bit Left (Memory or Accumulator)
		ROR	Rotate One Bit Right (Memory or Accumulator)
CLC	Clear Carry Flag	RTI	Return from Interrupt
CLD	Clear Decimal Mode	RTS	Return from Subroutine
CLI	Clear Interrupt Disable Bit		
CLV	Clear Overflow Flag	SBC	Subtract Memory from Accumulator with Borrow
CMP	Compare Memory and Accumulator	SEC	Set Carry Flag
CPX	Compare Memory and Index X	SED	Set Decimal Mode
CPY	Compare Memory and Index Y	SEI	Set Interrupt Disable Status
		*SMB	Set Memory Bit
DEC	Decrement Memory by One	STA	Store Accumulator in Memory
DEX	Decrement Index X by One	STX	Store Index X in Memory
DEY	Decrement Index Y by One	STY	Store Index Y in Memory
EOR	"Exclusive-Or" Memory with Accumulator	TAX	Transfer Accumulator to Index X
		TAY	Transfer Accumulator to Index Y
INC	Increment Memory by One	TSX	Transfer Stack Pointer to Index X
INX	Increment Index X by One	TXA	Transfer Index X to Accumulator
INY	Increment Index Y by One	TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator
JMP	Jump to New Location		
JSR	Jump to New Location Saving Return Address		

ENHANCED R6502 INSTRUCTION SET

[illegible]

1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
3. Add 2 to N if branch occurs to different page
4. Carry not = Borrow
5. If in decimal mode Z flag is invalid
6. If accumulator must be checked on zero result
7. Effects 8-bit data field of the specified zero page address.

LEGEND

X	=	Index X
Y	=	Index Y
A	=	Accumulator
M	=	Memory per effective address
M ₁	=	Memory per stack pointer
M ₂	=	Selector zero page memory bit
M ₃	=	Memory Bit 7

+	Add	memory bit 0
-	Subtract	
^	And	
v	Or	
+	Exclusive Or	
n	Number of cycles	
#	Number of Bytes	

A.3 INSTRUCTION CODE MATRIX

0	BRK	—OP Code
0	Implied	—Addressing Mode
1	7	—Instruction Bytes; Machine Cycles

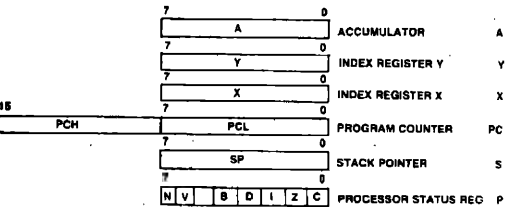
MSD	LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	1	BPL Relative 2 2**	ORA (IND, Y) 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	5	BVC Relative 2 2**	EOR (IND, Y) 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8	8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBR8 ZP 3 5**	8
9	9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBR9 ZP 3 5**	9
A	A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBR10 ZP 3 5**	A
B	B	BCS Relative 2 2**	LDA (IND, Y) 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBR11 ZP 3 5**	B
C	C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBR12 ZP 3 5**	C
D	D	BNE Relative 2 2**	CMP (IND, Y) 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBR13 ZP 3 5**	D
E	E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBR14 ZP 3 5**	E
F	F	BEQ Relative 2 2**	SBC (IND, Y) 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBR15 ZP 3 5**	F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

*Add 1 to N if page boundary is crossed.

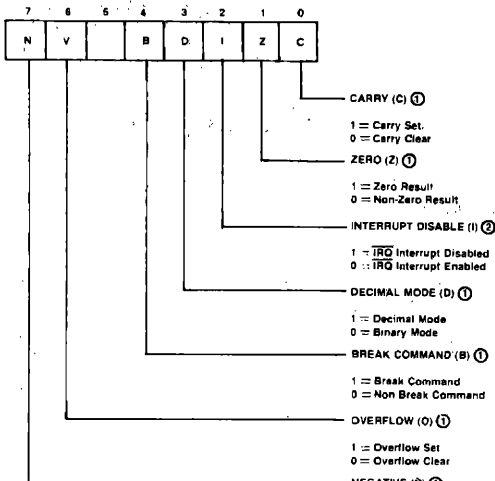
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

APPENDIX B

KEY REGISTER SUMMARY



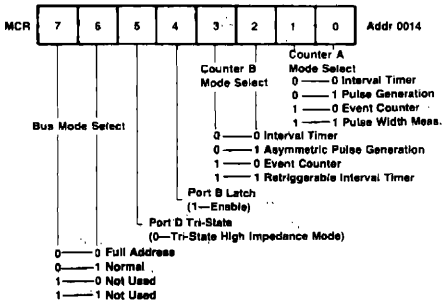
CPU Registers



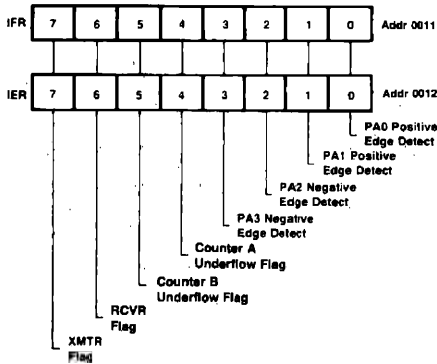
NOTES

- ① Not initialized by RES
- ② Set to Logic 1 by RES

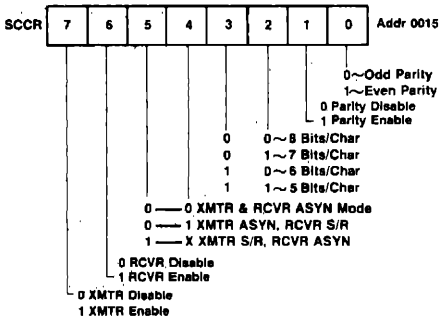
Processor Status Register



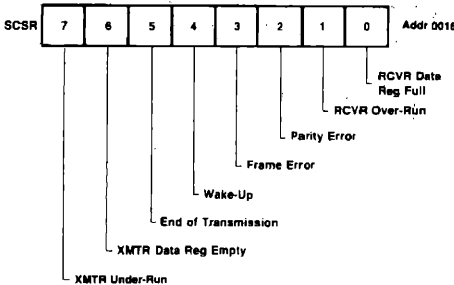
Mode Control Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



Serial Communications Status Register

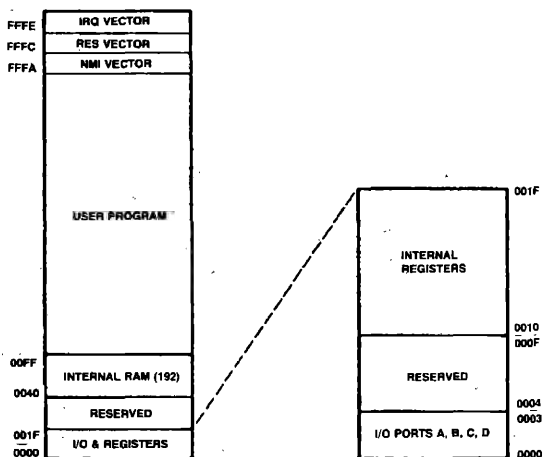
APPENDIX C

ADDRESS ASSIGNMENTS/MEMORY MAPS/PIN FUNCTIONS

C.1 I/O AND INTERNAL REGISTER ADDRESSES

ADDRESS (HEX)	READ	WRITE
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B.
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
0010	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
0F	<div style="border: 1px solid black; padding: 10px; text-align: center;"> RESERVED These addresses are reserved and are used by the CPU during Read and Write operation over the external Data Bus (D0-D7). </div>	
0E		
0D		
0C		
0B		
0A		
09		
08		
07		
06		
05		
04		
03	Port D	Port D
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

C.2 FULL ADDRESS MODE MEMORY MAP R6501Q



C.4 MULTIPLE FUNCTION PIN ASSIGNMENTS —PORT C AND PORT D

PIN NUMBER	FULL ADDRESS MODE	I/O PORT FUNCTION
54	PC0	PC0
55	PC1	PC1
56	PC2	PC2
57	PC3	PC3
58	PC4	PC4
59	PC5	PC5
60	A13	PC6
61	A14	PC7
62	PD0	PD0
63	PD1	PD1
64	PD2	PD2
1	PD3	PD3
2	PD4	PD4
3	PD5	PD5
4	PD6	PD6
5	PD7	PD7

APPENDIX D

ELECTRICAL SPECIFICATIONS

Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC} & V_{RR}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range, Commercial		0 to +70	°C
Storage Temperature Range	T_{sto}	-55 to +150	°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. Characteristics ($V_{CC} = 5V \pm 5\%$; $V_{RR} = V_{CC}$; $V_{SS} = 0$; $T_A = 0$ to 70°C)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Power Dissipation (Outputs High) Commercial @ 0°C	P_D	—	750 ⁽¹⁾	1100	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial @ 25°C	I_{RR}	—	4	—	mAdc
Input High Voltage (Except XTLI)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	—	+0.8	Vdc
Input Leakage Current (RES, NMI) $V_{in} = 0$ to 5.0 Vdc	I_{IN}	—	—	± 10.0	μAdc
Input Low Current PA, PB, PC, PD ($V_{IL} = 0.4$ Vdc)	I_{IL}	—	-1.0	-1.6	mAdc
Output High Voltage (Except XTLO) ($I_{Load} = .100 \mu\text{Adc}$)	V_{OH}	+2.4	—	V_{CC}	Vdc
Output Low Voltage ($I_{Load} = 1.6$ mAdc)	V_{OL}	—	—	+0.4	Vdc
Input Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz) XTLI, XTLO All Others	C_{in}	— —	— —	50 10	pF
I/O Port Pull-Up Resistance PA0-PA7, PB0-PB7, PC0-PC7	R_L	3.0	6.0	11.5	K Ω
Output Leakage Current Tri-State I/O's while in High Impedance State	I_{OUT}	—	—	± 10	μAdc
Output Capacitance Tri-State I/O's while in High Impedance State $V_{in} = 0V$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz	C_{OUT}	—	—	10	pF

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

(1) at 25°C

APPENDIX E

TIMING REQUIREMENTS AND CHARACTERISTICS

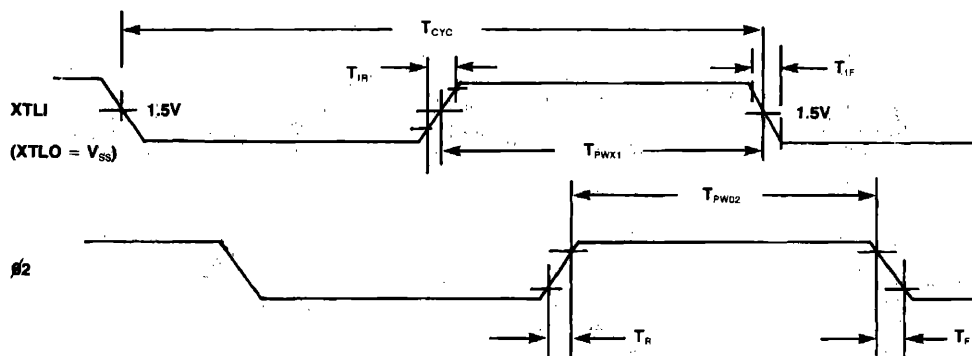
E.1 GENERAL NOTES

1. $V_{CC} = 5V \pm 5\%$, $0^\circ C \leq T_A \leq 70^\circ C$
2. A valid $V_{CC} - \overline{RES}$ sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pf maximum, except as noted below:

PA, PB	— 50pf maximum
PC (I/O Modes Only)	— 50pf maximum
PC (ABB and Mux Mode)	— 130pf maximum
PC6, PC7 (Full Address Mode)	— 130pf maximum

E.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 ± 25	—	250 ± 10	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1}	$T_{PWX1} \pm 25$	T_{PWX1}	$T_{PWX1} \pm 20$
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10

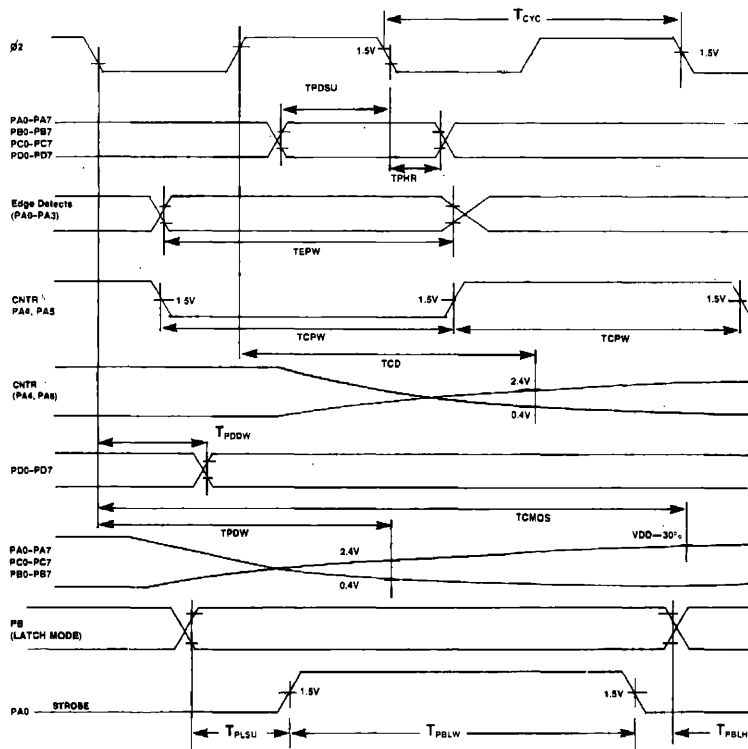


E.3 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
$T_{PDW}^{(1)}$	Internal Write to Peripheral Data Valid	—	500	—	500
$T_{CMOS}^{(1)}$	PA, PB, PC TTL	—	1000	—	1000
T_{PDW}	PA, PB, PC CMOS	—	175	—	150
T_{PDSU}	Peripheral Data Setup Time	200	—	200	—
T_{PHR}	Peripheral Data Hold Time	75	—	75	—
T_{PDW}	PA, PB, PC	10	—	10	—
T_{PDW}	PD	—	—	—	—
T_{PDW}	PA0-PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CPW}	Counters A and B	T_{CYC}	—	T_{CYC}	—
$T_{CD}^{(1)}$	PA4, PA5 Input Pulse Width	—	500	—	500
$T_{CD}^{(1)}$	PA4, PA5 Output Delay	—	—	—	—
T_{PBLW}	Port B Latch Mode	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PA0 Strobe Pulse Width	175	—	150	—
T_{PBLH}	PB Data Setup Time	30	—	30	—
T_{PBLH}	PB Data Hold Time	—	—	—	—
$T_{PDW}^{(1)}$	Serial I/O	—	500	—	500
$T_{CMOS}^{(1)}$	PA6 XMTR TTL	—	1000	—	1000
$T_{CMOS}^{(1)}$	PA6 XMTR CMOS	—	—	—	—
T_{CPW}	PA4 RCVR S/R Clock Width	$4 T_{CYC}$	—	$4 T_{CYC}$	—
$T_{PDW}^{(1)}$	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
$T_{CMOS}^{(1)}$	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

NOTE 1: Maximum Load Capacitance: 50pF
Passive Pull-Up Required

E.3.1 I/O, Edge Detect, Counter, and Serial I/O Timing

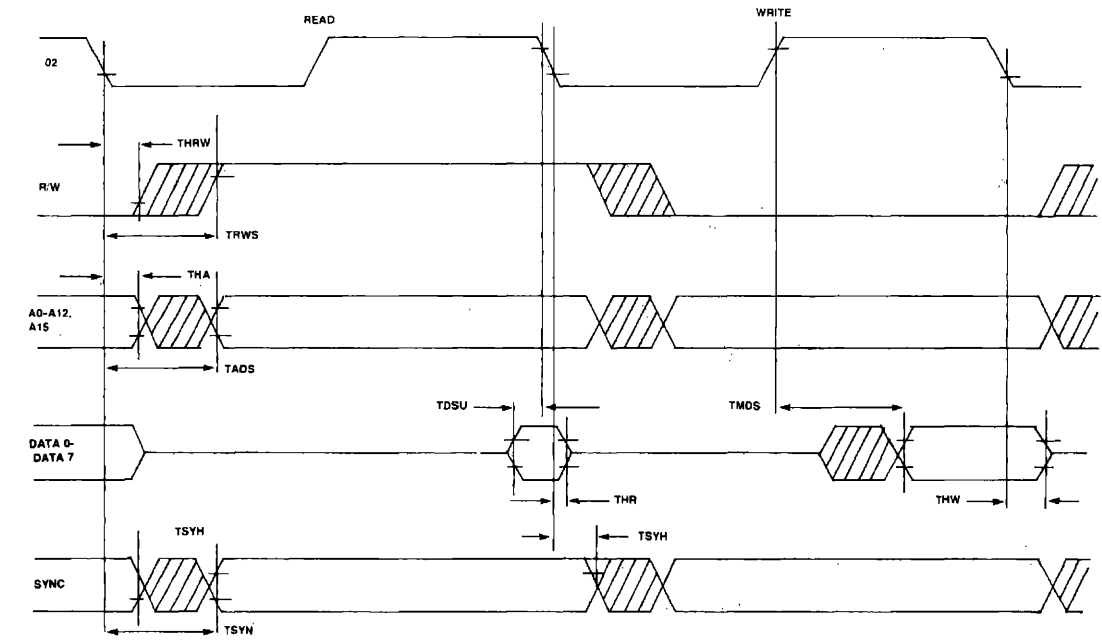


E.4 MICROPROCESSOR TIMING (D0-D7, A0-A12, A15, SYNC, R/W)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T _{RWS}	R/W Setup Time	—	225	—	140
T _{ADS}	A0-A12, A15 Setup Time	—	150	—	75
T _{DSU}	D0-D7 Data Setup Time	50	—	35	—
T _{HR}	D0-D7 Read Hold Time	10	—	10	—
T _{HW}	D0-D7 Write Hold Time	30	—	30	—
T _{MOS}	D0-D7 Write Output Delay	—	175	—	130
T _{SYN}	SYNC Setup	—	225	—	175
T _{HA}	A0-A12, A15 Hold Time	30	—	30	—
T _{HRW}	R/W Hold Time	30	—	30	—
T _{ACC}	External Memory Access Time $T_{ACC} = T_{CYC} - T_F - T_{ADS} - T_{DSU}$	—	T _{ACC}	—	T _{ACC}
T _{SYH}	SYNC Hold Time	30	—	30	—

3

E.4.1 Microprocessor Timing Diagram





R6500/1 **ONE-CHIP MICROCOMPUTER**

SECTION 1 **INTRODUCTION**

The Rockwell R6500/1 microcomputer is a complete 8-bit computer fabricated on a single chip using an N-channel silicon gate MOS process. The R6500/1 complements an established and growing line of R6500 products and has a wide range of microcomputer applications.

The R6500/1 consists of an R6502 Central Processing Unit (CPU), 2048 bytes of Read Only Memory (ROM), 64 bytes of Random Access Memory (RAM) and interface circuitry for peripheral devices.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the R6500/1 a leading candidate for microcomputer applications.

To facilitate system and program development for the R6500/1, Rockwell has developed an R6500/1E Emulator part. A description of the R6500/1E is contained in Appendix D.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Number 29650N31). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Document Number 29650N30).

FEATURES

- Single-chip microcomputer
- R6502 software compatible
- Eight-bit parallel processing
- Decimal or binary arithmetic
- Variable length stack
- True indexing capability
- Thirteen addressing modes
- 1 or 2 MHz clock operation, with the following options:
 - External single clock input
 - RC time base input
 - Crystal time base input
- Single +5V power supply
- 500 mw operating power
- Separate power pin for RAM with standby power only 10% of operating power
- 2K x 8 ROM on chip
- 64 x 8 RAM on chip
- 40-pin dual in-line package
- 64-pin Emulator part available, with 40 signals identical to production part
- Pipeline architecture
- 32 bidirectional TTL compatible I/O lines
 - 1 positive edge sensitive I/O line
 - 1 negative edge sensitive I/O line
- 1 bidirectional TTL compatible counter I/O line
- 16-bit timer/counter
- Four timer/counter modes
 - Internal timer
 - Pulse generator
 - Event counter
 - Pulse width measurement
- Three maskable interrupts
 - 1 counter overflow
 - 2 I/O edge detect
- NMI and Reset interrupts

SECTION 2
R6500/1 INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6500/1 single chip microcomputer. Figure 2-1 is the Interface Diagram for the R6500/1. Figure 2-2 shows the pin out

configuration and Table 2-1 describes the function of each pin of the R6500/1.

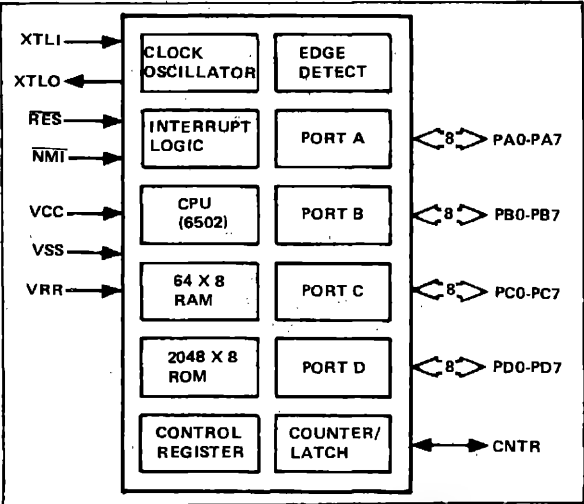


Figure 2-1. R6500/1 Interface Diagram

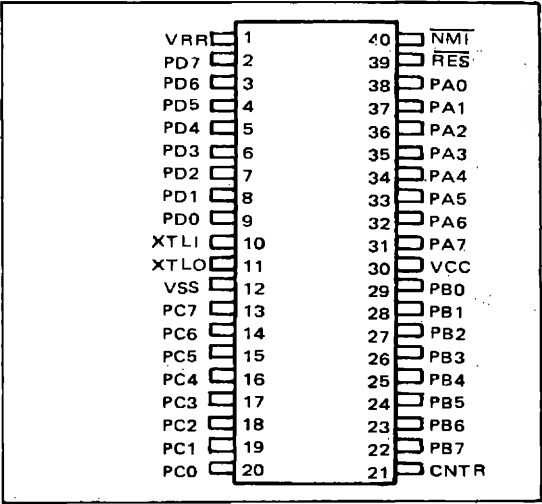


Figure 2-2. R6500/1 Pin Out Designation

Table 2-1. R6500/1 Pin Description

Signal Name	Pin No.	Description
VCC	30	Main power supply +5V
VRR	1	Separate power pin for RAM. In the event that VCC power is lost, this power retains RAM data.
VSS	12	Signal and power ground (0V)
XTLI	10	Crystal, clock or RC network input for internal clock oscillator.
XTLO	1	Crystal or RC network output from internal clock oscillator.
RES	39	The Reset input is used to initialize the R6500/1. The signal must not transition from low to high for at least eight cycles after VCC reaches operating range and the internal oscillator has stabilized (see section 5). +10V input enables the test mode.
NMI	40	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	38-31 29-22 20-13 9-2	Four 8-bit ports used for either input/output. Each line consists of an active transistor to VSS and an optional passive pull-up to VCC. The two lower bits of the PA port (PA0-PA1) also serve as edge detect inputs with maskable interrupts.
CNTR	21	This line is used as a Counter input/output line. CNTR is an input in the Event Counter and Pulse Width Measurement modes and is an output in the Interval Timer and Pulse Generator modes. It consists of an active transistor to VSS and an optional passive pull-up to VCC.

SECTION 3 SYSTEM ARCHITECTURE

This section provides a functional description of the R6500/1. A block diagram of the R6500/1 is presented in Figure 3-1.

3.1 INDEX REGISTERS

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address — the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.2 STACK POINTER

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to

either user instructions or the interrupt lines $\overline{\text{NMI}}$ and $\overline{\text{IRQ}}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

3.3 ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers

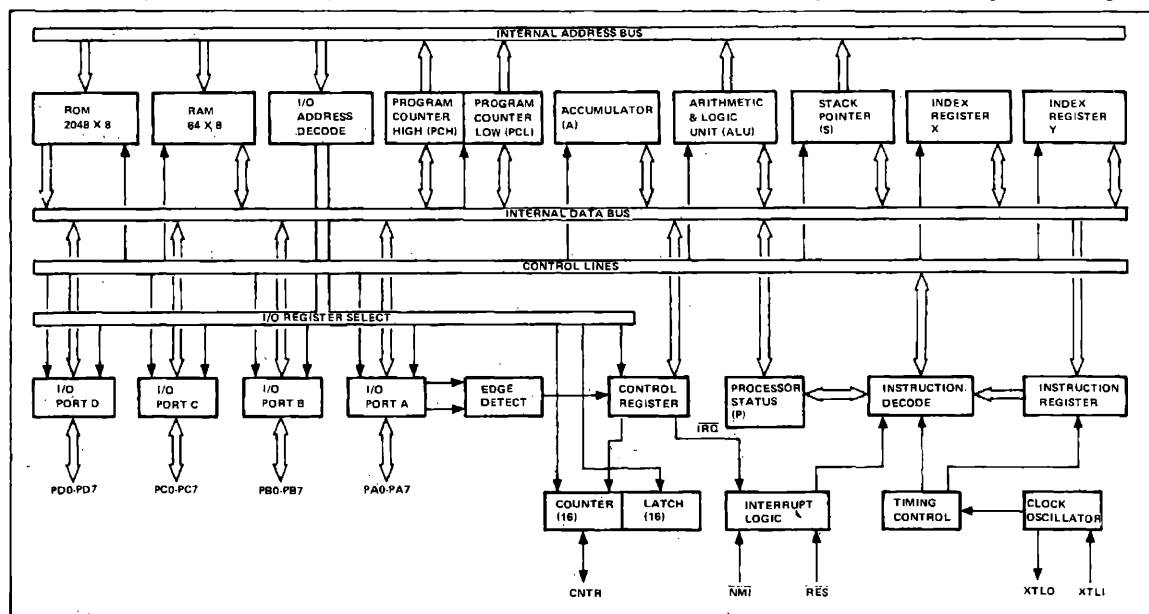


Figure 3-1. R6500/1 Block Diagram

(except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.4 ACCUMULATOR

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.5 PROGRAM COUNTER

The 12-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 4 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.6 INSTRUCTION REGISTER AND INSTRUCTION DECODE

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.7 TIMING CONTROLS

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

3.8 INTERRUPT LOGIC

Interrupt logic controls the sequencing of three interrupts; RES, NMI and IRQ. IRQ is generated by any one of three conditions: Counter Overflow, PA0 Positive Edge Detected, and PA1 Negative Edge Detected.

3.9 CLOCK OSCILLATOR

The Clock Oscillator provides the basic timing signals used by the R6500/1 CPU. The reference frequency is provided by an external source, and can be from a crystal, clock or RC network input. The RC network mode is a mask option. The external frequency can vary from 200 kHz to 4 MHz. The internal Phase 2 (Ø2) frequency is one-half the external reference frequency. Figure 3-2 shows typical connections.

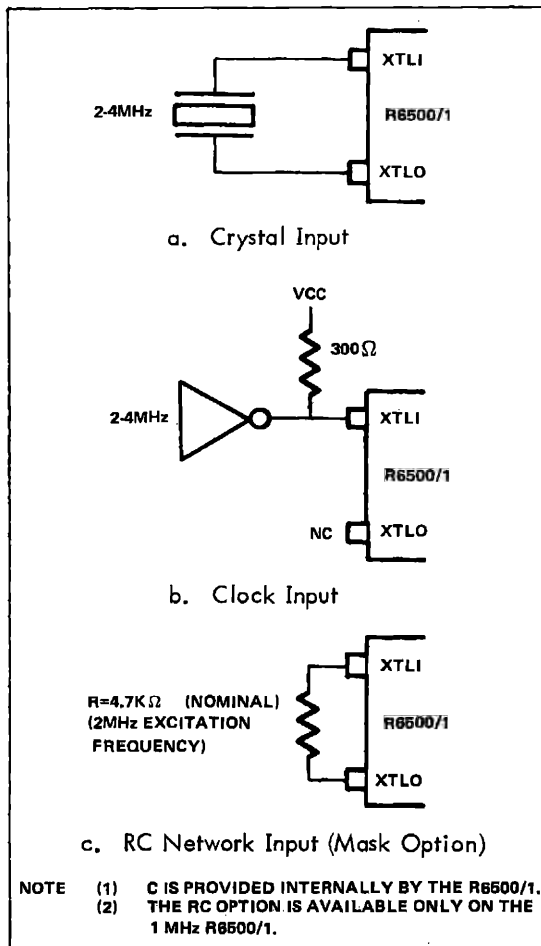


Figure 3-2. Clock Oscillator Input Options

3.10 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-3, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6500 instruction

set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.10.1 CARRY BIT (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.10.2 ZERO BIT (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are

not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.10.3 INTERRUPT DISABLE BIT (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request (IRQ). If the I Bit is reset to logic 0, the IRQ signal will be serviced. If the bit is set to logic 1, the IRQ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET (RES) or Non-Maskable Interrupt (NMI) signal is detected.

The I bit is cleared by the Clear Interrupt (CLI) instruction, the Pull Processor Status from Stack (PLP) instruction, or as the result of executing a Return from Interrupt (RTI) instruction (providing the Interrupt Disable Bit was cleared prior to the interrupt). The Interrupt Disable Bit may be set or cleared under program control using a Set Interrupt Disable (SEI) or a Clear Interrupt Disable (CLI) instruction, respectively.

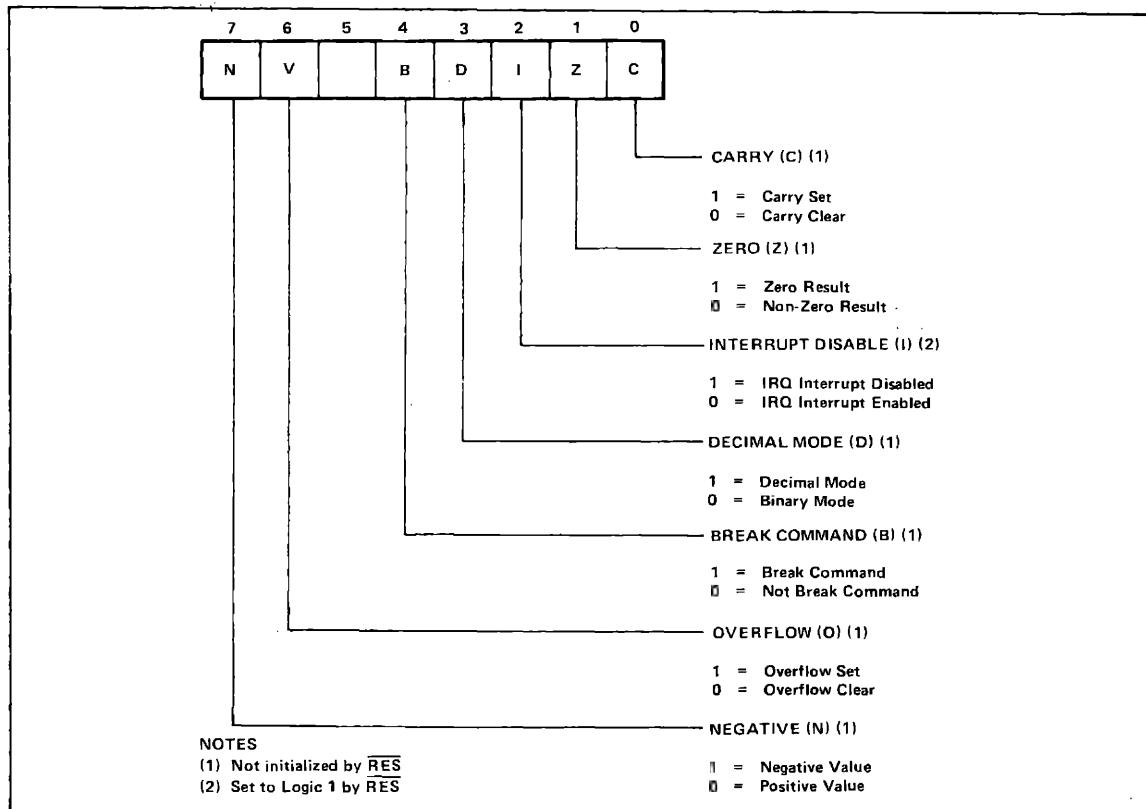


Figure 3-3. Processor Status Register

3.10.4 DECIMAL MODE BIT (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application to R6500/1. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.10.5 BREAK BIT (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{\text{IRQ}}$ service routine to be entered. If the $\overline{\text{IRQ}}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{\text{IRQ}}$ routine was entered as the result of an $\overline{\text{IRQ}}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.10.6 OVERFLOW BIT (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or -128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.10.7 NEGATIVE BIT (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or

arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

3.11 $2K \times 8$ ROM

The R6500/1 2048 byte \times 8-bit Read Only Memory (ROM) usually contains the user's program instructions and other fixed constants. These program instructions and constants are mask-programmed into the ROM during fabrication of the R6500/1 device. The R6500/1 ROM is memory mapped from 800 to FFF.

3.12 64×8 RAM

The 64 byte \times 8-bit Random Access Memory (RAM) contains the user program stack and is used for scratchpad memory during system operation. This RAM is completely static in operation and requires no clock or dynamic refresh. The data contained in RAM is read out nondestructively with the same polarity as the input data. A standby power pin, VRR allows RAM memory to be maintained on 10% of the operating power. In the event that VCC power is lost and execution stops, this standby power retains RAM data until execution resumes.

In order to take advantage of zero page addressing capabilities, the R6500/1 RAM is assigned page zero memory address 0 to 03F.

3.13 CONTROL REGISTER

The Control Register (CR), shown in Figure 3-4, is located at address 08F. The CR contains five control signals and three status signals.

The control signals are summarized in Table 3-1. The control signals are set to logic 1 by writing logic 1 into the respective bit positions and cleared to logic 0 either by writing logic 0 into the respective bit position or by the occurrence of a RES signal.

Table 3-1. CR Control Signals

Control Signal Name	Bit Number
Counter Mode Control 0 (CMC0)	0
Counter Mode Control 1 (CMC1)	1
PA1 Interrupt Enabled (A1IE)	2
PA0 Interrupt Enabled (A0IE)	3
Counter Interrupt Enabled (CIE)	4

The three status signals are summarized in Table 3-2.

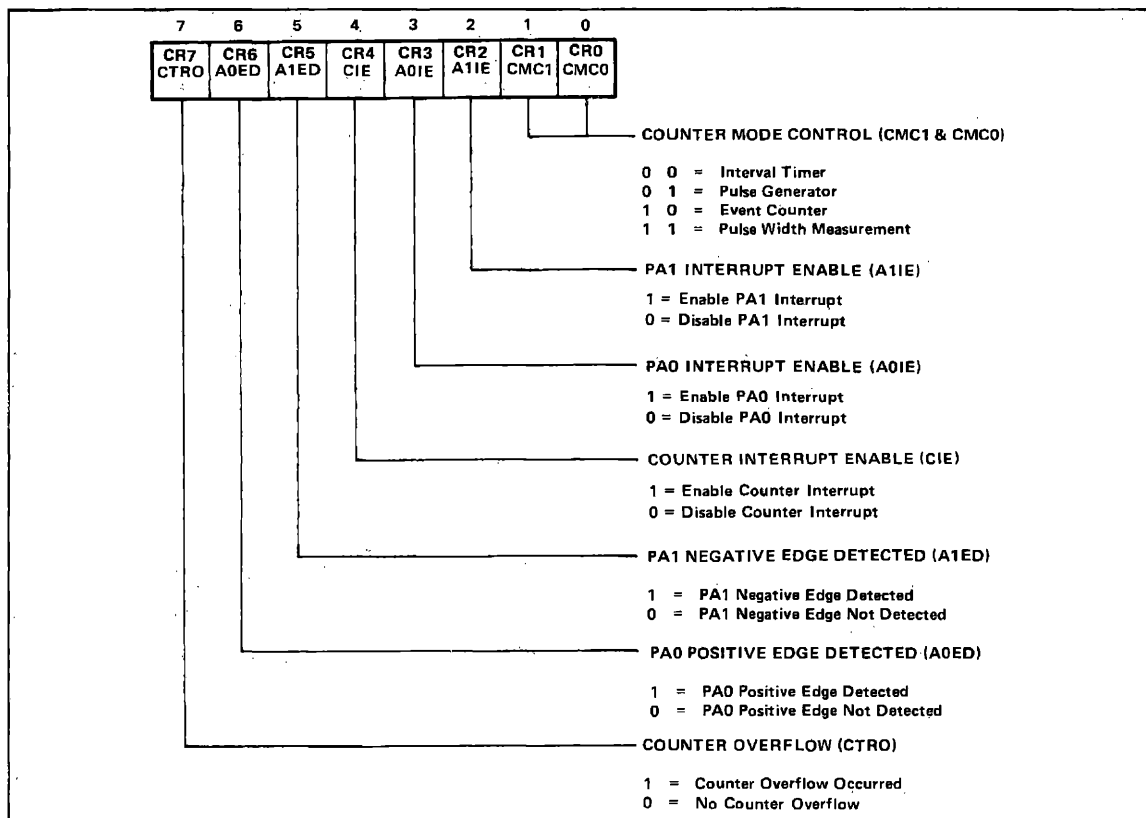


Figure 3-4. Control Register (CR)

Table 3-2. CR Status Signals

Status Signal Name	Bit Number
PA1 Negative Edge Detected (A1ED)	5
PA0 Positive Edge Detected (A0ED)	6
Counter Overflow (CTRO)	7

The status signals are read-only information. The status bits are set to logic 1 by hardware monitoring logic and cleared to logic 0 by the occurrence of $\overline{\text{RES}}$ signal or by specific address commands. Each of these signals is described in the following sections.

3.13.1 COUNTER MODE CONTROL 0 AND 1

Counter Mode Control signals CMC0 and CMC1 (bits 0 and 1) control the Counter operating modes. The modes of operation and the corresponding configuration of CMC0 and CMC1 are summarized in Table 3-3.

These modes are controlled by writing the appropriate bit values into the Counter Mode Control bits.

Table 3-3. Counter Mode Control Selection

CMC1 (Bit 1)	CMC0 (Bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generator
1	0	Event Counter
1	1	Pulse Width Measurement

The Counter is set to the Interval Timer Mode (00) when a $\overline{\text{RES}}$ signal is generated or if the user program stores logic 0 into Bits 0 and 1 of the Control Register. A complete description of each of the Counter modes is given in Section 3.14.1.

3.13.2 PA1 INTERRUPT ENABLE BIT (A1IE)

If the PA1 Interrupt Enable Bit (CR2) is set to logic 1, an $\overline{\text{IRQ}}$ interrupt request signal will be generated when the PA1 Negative Edge Detected Bit (CR5) is set.

3.13.3 PA0 INTERRUPT ENABLE BIT (AOIE)

If the PA0 Interrupt Enable Bit (CR3) is set to logic 1, the IRQ interrupt request signal will be generated when the PA0 Positive Edge Detected Bit (CR6) is set.

3.13.4 COUNTER INTERRUPT ENABLE BIT (CIE)

If the Counter Interrupt Enable Bit (CR4) is set to logic 1, the IRQ interrupt request signal will be generated when Counter Overflow (CR7) is set.

3.13.5 PA1 NEGATIVE EDGE DETECTED BIT (A1ED)

The PA1 Negative Edge Detected Bit (CR5) is set to logic 1 whenever a negative (falling) edge is detected on PA1. This bit is cleared to logic 0 by $\overline{\text{RES}}$ or by writing to address 08A.

The edge detecting circuitry is active when PA1 is used either as an input or as an output. When PA1 is used as an output, A1ED will be set when the negative edge is detected during a logical 1 to 0 transition.

When PA1 is used as an input and the negative edge detecting circuitry is used, A1ED should be cleared by the user program upon initialization and when the PA1 Negative Edge Detected IRQ processing is completed.

3.13.6 PA0 POSITIVE EDGE DETECTED BIT (A0ED)

The PA0 Positive Edge Detected Bit (CR6) is set to logic 1 whenever a positive (rising) edge is detected on PA0. The bit is cleared to logic 0 by $\overline{\text{RES}}$ or by writing to address 089.

The edge detecting circuitry is active when PA0 is used either as an input or as an output. When PA0 is used as an output, A0ED will be set when the positive edge is detected during a logical 0 to 1 transition.

When PA0 is used as an input and the positive edge detecting circuitry is used, A0ED should be cleared by the user program upon initialization and upon completion of PA0 Positive Edge Detected IRQ processing.

3.13.7 COUNTER OVERFLOW BIT (CTRO)

The Counter Overflow Bit (CR7) is set to logic 1 whenever a counter overflow occurs in any of the four counter operating modes. Overflow occurs when the counter is decremented one count from 0000. This bit is cleared to logic 0 by $\overline{\text{RES}}$ or by reading from address 087 or writing to address 088.

This bit should be cleared by the user program upon initialization and upon completion of Counter Overflow IRQ interrupt processing.

When a Counter Overflow occurs, the Upper Count (UC) in address 086 and the Lower Count (LC) in address 087 are reset to

the values contained in the Upper Latch (UL) in address 084 and in the Lower Latch (LL) in address 085, respectively. Therefore, it is important to load the Lower Latch value prior to executing the Write to Upper Latch and Transfer Latch to Counter (address 088) in order to prevent an unpredicted reoccurrence of Counter Overflow and, if enabled, an IRQ interrupt request.

3.14 COUNTER/LATCH

The Counter/Latch consists of a 16-bit Counter and a 16-bit Latch. The Counter resides in two 8-bit registers: address 086 contains the Upper Count value (bits 8-15 of the Counter) and address 087 contains the Lower Count value (bits 0-7 of the Counter). The Counter contains the count of either $\emptyset 2$ clock periods or external events depending on which counter mode is selected in the Control Register (Section 3.13.1).

The Latch contains the Counter initialization value. The Latch resides in two 8-bit registers: address 084 contains the Upper Latch value (bits 8-15 of the Latch) and address 085 contains the Lower Latch value (bits 0-7 of the Latch). The 16-bit Latch can hold values from 0 to 65535.

The Latch registers can be loaded at any time by executing a write to the Upper Latch Address (084) and the Lower Latch Address (085). In each case, the contents of the Accumulator are copied into the applicable Latch register. The Upper Latch and Lower Latch can be loaded independently; it is not required to load both registers at the same time or sequentially. The Upper Latch can also be loaded by writing to address 088.

The Counter can be initialized at any time by writing to address 088. The contents of the Accumulator will be copied into the Upper Latch before the value in the Upper Latch is transferred to the Upper Counter.

The Counter will also be initialized to the Latch value whenever the Counter overflows. When the Counter decrements from 0000, the next Counter value will be the Latch value, not FFFF.

Whenever the Counter overflows, the Counter Overflow Bit (CR7) is set to logic 1. This bit is cleared whenever the lower eight bits of the counter are read from address 087 or by writing to address 088.

3.14.1 COUNTER MODES

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register.

Mode	CMC1	CMC0
Interval Timer	0	0
Pulse Generator	0	1
Event Counter	1	0
Pulse Width Measurement	1	1

The Interval Timer, Pulse Generator, and Pulse Width Measurement Modes are $\phi 2$ clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

Interval Timer (Mode 0)

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).
2. When a write operation is performed to the Load Upper Latch and Transfer Latch to counter address (088), the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the $\phi 2$ clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The

Counter Timer capacity is therefore $1\mu\text{s}$ to 65.535ms at the 1 MHz $\phi 2$ clock rate or $0.5\mu\text{s}$ to 32.768ms at the 2 MHz $\phi 2$ clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting IRQ interrupt requests in the counter IRQ interrupt routine.

When the Counter decrements from 0000, the Counter Overflow (CR7) is set to logic 1 at the next $\phi 2$ clock pulse. If the Counter Interrupt enable bit (CR4) is also set, an IRQ interrupt request will be generated. The Counter Overflow bit in the Control Register can be examined in the IRQ interrupt routine to determine that the IRQ was generated by the Counter Overflow.

While the timer is operating in the Interval Timer Mode, the Counter Out/Event line is held in the high (output disabled) state.

A timing diagram of the Interval Timer Mode is shown in Figure 3-5.

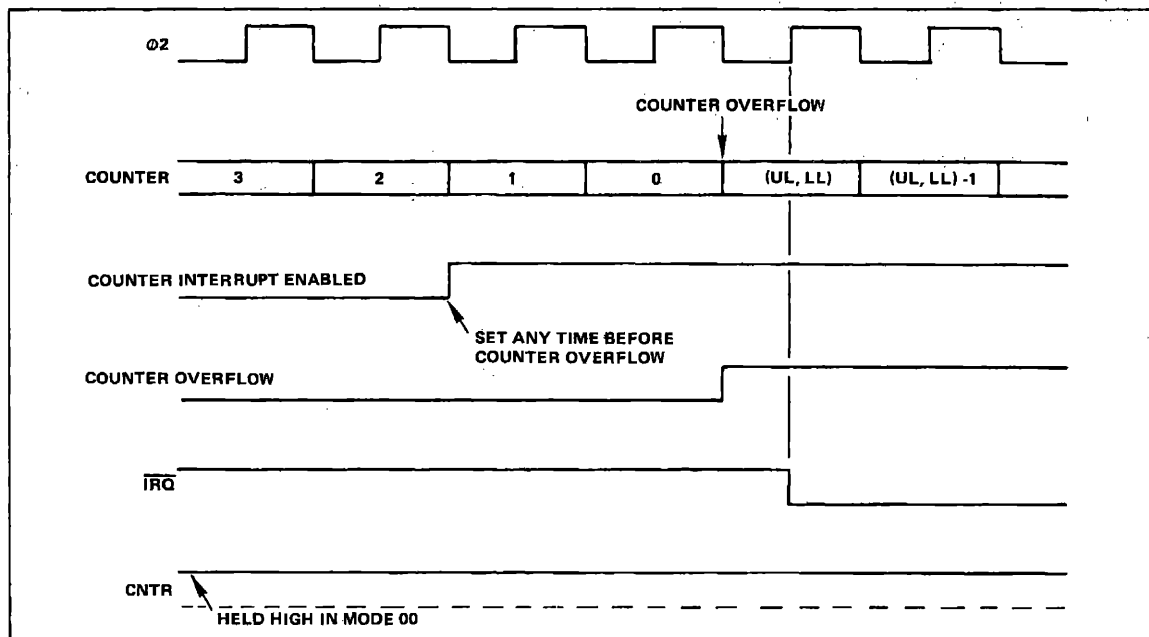


Figure 3-5. Interval Timer (Mode 0) Timing Diagram

Pulse Generator Mode (Mode 1)

In the Pulse Generator mode, the Counter Out/Event In line (CNTR) operates as a Counter Out. The CNTR line toggles from low to high or from high to low whenever a Counter Overflow occurs, or a write is performed to address 088.

Either a symmetric or asymmetric output waveform can be

output on the CNTR line in this mode. The CNTR output is initialized high by a RES since the Interval Timer mode is established by RES.

A one-shot waveform can be easily generated by changing from Mode 1 Pulse Generator to Mode 0 (Interval Timer) after only one occurrence of the output toggle condition.

Event Counter Mode (Mode 2)

In this mode the CNTR line is used as an Event In line, and the Counter with decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate.

The Counter can count up to 65,535 occurrences before overflowing. As in the other modes, the Counter Overflow bit (CR7) is set to logic 1 if the overflow occurs.

Figure 3-6 is a timing diagram of the Event Counter Mode.

Pulse Width Measurement Mode (Mode 3)

This mode allows the accurate measurement of a low pulse duration on the CNTR line. In this mode, CNTR is used in the Event In capacity. The Counter decrements by one

count at the $\phi 2$ clock rate as long as the CNTR line is held in the low state. The Counter is stopped when CNTR is in the high state.

If the CNTR pin is left disconnected, this mode may be selected to stop the Counter since the internal pull-up device will cause the CNTR input to be in the high (>2.0V) state.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 3-7.

3.15 INPUT/OUTPUT PORTS

The R6500/1 provides four 8-bit Input/Output (I/O) ports (PA, PB, PC, PD). These 32 I/O lines are completely bidirectional. All lines may be used either for input or output in any combination; that is, there are no line grouping or port association restrictions.

3

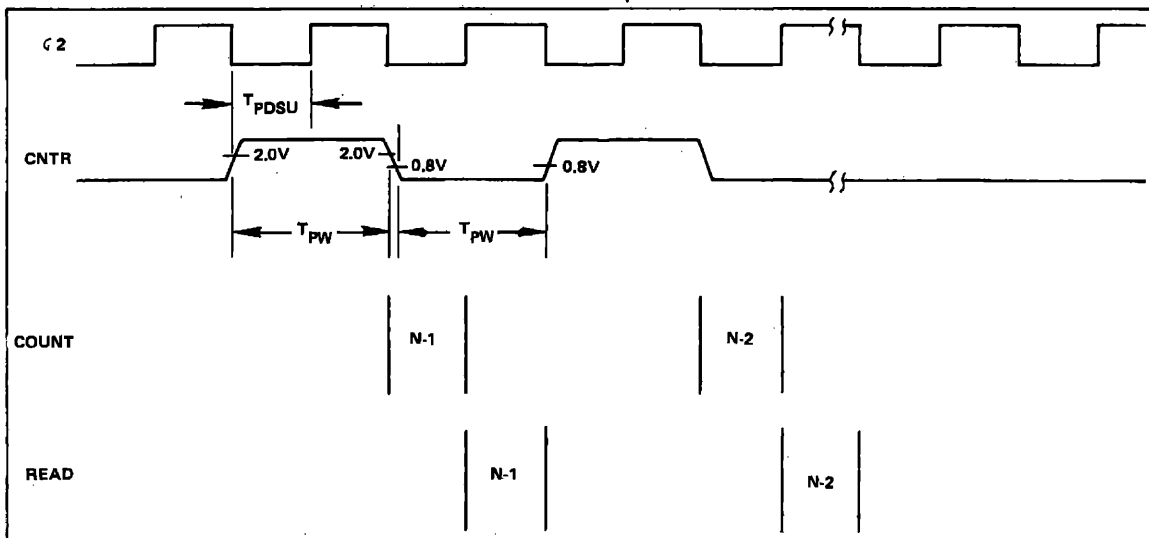


Figure 3-6. Event Counter Mode (Mode 2)

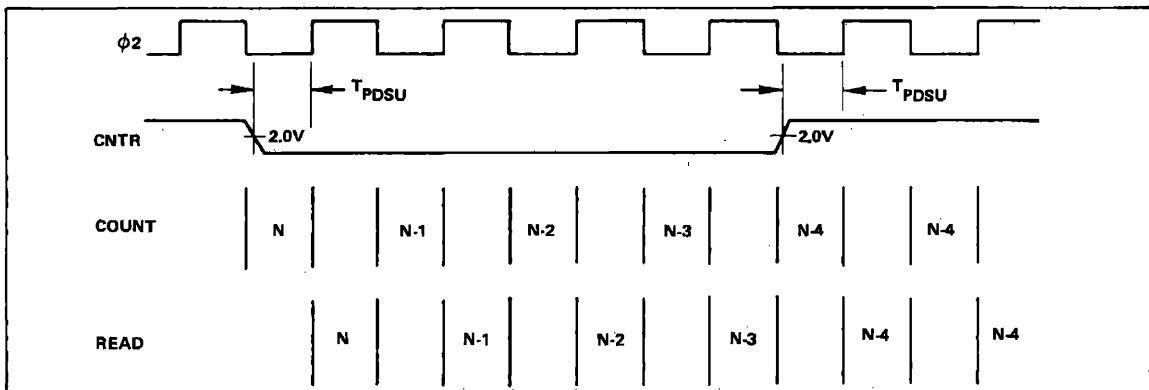


Figure 3-7. Pulse Width Measurement (Mode 3)

The direction of the 32 I/O lines are controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 3-4.

Table 3-4. I/O Port Addresses

Port	Address
A	080
B	081
C	082
D	083

Figure 3-8 shows the I/O Port Timings.

3.15.1 INPUTS

Inputs are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low ($<0.8V$) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high ($>2.0V$) input will cause a logic 1 to be read. An \overline{RES} signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

3.15.2 OUTPUTS

Outputs are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high ($>2.4V$) output while a logic 0 will force a low ($<0.4V$) output.

3.15.3 EDGE DETECTION CAPABILITY

Ports PA0 and PA1 have an edge detection capability. Figure 3-9 shows the edge detection timing.

PA0 Positive Edge Detecting Capability

In addition to its normal I/O function, PA0 will detect an asynchronous positive (rising) edge signal and set the PA0 Positive Edge Detected signal (CR6) to logic 1. The maximum rate at which this positive edge can be detected is one-half the $\phi 2$ clock rate.

If the PA0 Interrupt Enable Bit (CR3) is set, an \overline{IRQ} interrupt request will also be generated. The PA0 Positive Edge Detected signal can be cleared by writing to address 089.

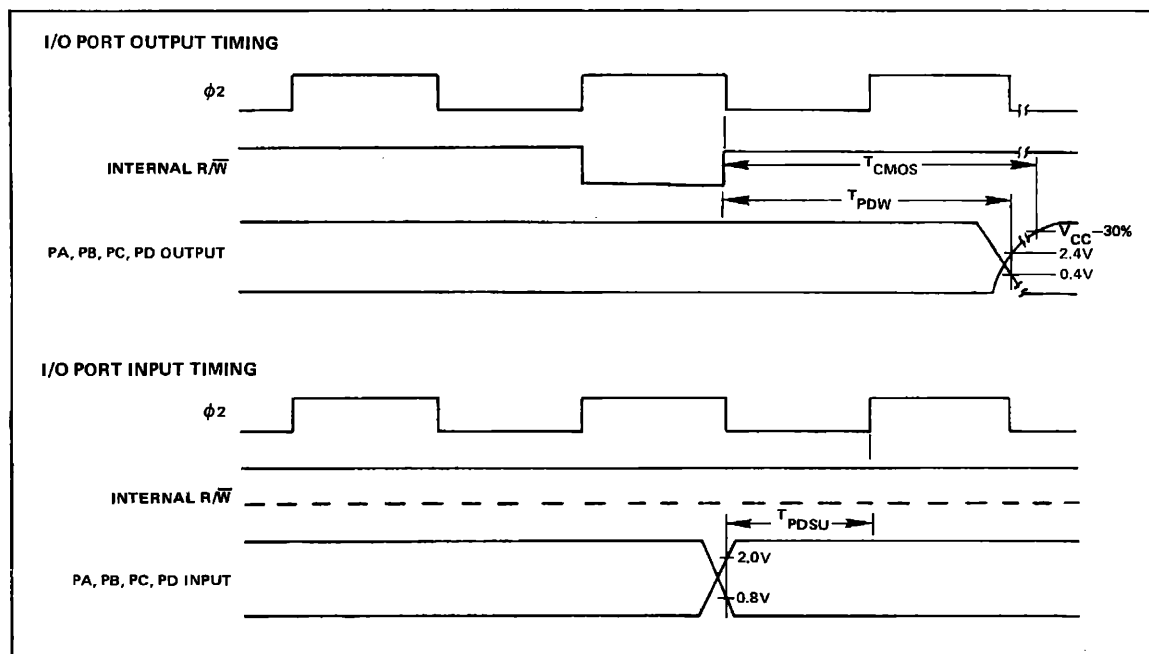


Figure 3-8. I/O Port Timing

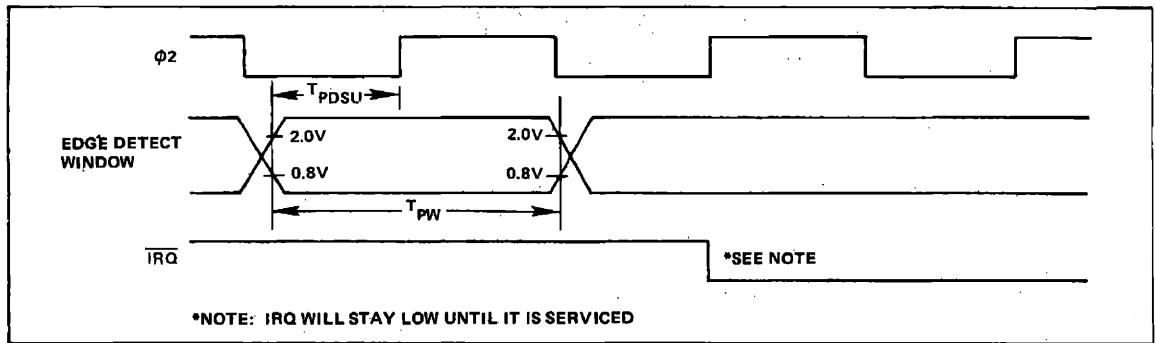


Figure 3-9. PA0 and PA1 Edge Detection Timing

PA1 Negative Edge Detecting Capability

In addition to its normal I/O function, PA1 will detect an asynchronous negative (falling) edge signal and set the PA1 Negative Edge Detected signal (CR5) to logic 1. The maximum rate at which this negative edge can be detected is one-half the $\phi 2$ clock rate.

If the PA1 Interrupt Enable signal (CR2) is set, an $\overline{\text{IRQ}}$ interrupt request will also be generated. The PA1 Negative Edge Detected signal may be cleared by writing to address 08A.

3.16 MASK OPTIONS

An option is provided to delete the internal pull-up resistance from PA, PB, PC and/or PD ports at mask time. This option is available for 8-bit port groups only, not for individual port lines. This option may be used to aid interface with CMOS drivers, or in order to interface with external pull-up devices.

An option is also provided to delete the internal pull-up resistance on the CNTR line.

SECTION 4

IRQ INTERRUPT REQUEST GENERATION

An $\overline{\text{IRQ}}$ interrupt request can be initiated by any or all of three possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Control Register.

The first source of $\overline{\text{IRQ}}$ is Counter Overflow. The $\overline{\text{IRQ}}$ interrupt request will be driven low whenever both the Counter Interrupt Enable (CR4) and the Counter Overflow (CR7) are logic 1.

The second source of $\overline{\text{IRQ}}$ is detection of a positive edge on PA0. The $\overline{\text{IRQ}}$ interrupt request will be driven low whenever both the PA0 Interrupt Enable (CR3) and the PA0 Positive Edge Detected (CR6) are logic 1.

The third source of $\overline{\text{IRQ}}$ is detection of a negative edge on PA1. The $\overline{\text{IRQ}}$ interrupt request will be driven low whenever both the PA1 Interrupt Enable (CR2) and the PA1 Negative Edge Detected (CR5) are logic 1.

Multiple simultaneous interrupts will cause the $\overline{\text{IRQ}}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

CAUTION

If the same data, i.e., the same RAM, counter/latch or I/O addresses, are operated on asynchronously by a normal processing routine and by an interrupt service routine, care must be taken to prevent loss of data due to the interrupt routine altering the data during update of the data by the normal processing routine. This situation can be prevented by disabling the $\overline{\text{IRQ}}$ interrupt with the SEI instruction before starting the data update in the normal processing and then enabling the interrupt with the CLI instruction upon completion of data update.

SECTION 5

POWER ON/OFF CONSIDERATIONS

5.1 POWER-ON RESET

The occurrence of $\overline{\text{RES}}$ going from low to high will cause the R6500/1 to set the Interrupt Mask Bit — bit 2 of the Processor Status Register — and initiate a reset vector fetch at address FFE and FFF to begin user program execution. All of the I/O ports (PA, PB, PC, and PD) and CNTR will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timer counter mode (mode 00) to be selected and causing all interrupt enabled bits to be reset.

5.2 POWER ON/OFF TIMING

After application of VCC power to the R6500/1, $\overline{\text{RES}}$ must be held low for at least eight $\phi 2$ clock cycles after VCC reaches operating range and the internal clock oscillator has stabilized. This stabilization time is dependent upon the input VCC voltage and performance of the crystal, clock, or RC network input circuit. The clock oscillator output can be monitored on XTLO (pin 11).

Figure 5-1 illustrates the power turn-on waveforms.

5.3 RAM DATA RETENTION — VRR REQUIREMENTS

For the RAM to retain data upon loss of VCC, VRR must be supplied within operating range and $\overline{\text{RES}}$ must be driven

low at least eight $\phi 2$ clock pulses before VCC falls out of operating range. $\overline{\text{RES}}$ must then be held low while VCC is out of operating range and until at least eight $\phi 2$ clock cycles after VCC is again within operating range and the internal $\phi 2$ oscillator is stabilized. VRR must remain within VCC operation range during normal R6500/1 operation. When VCC is out of operating range, VRR must remain within the VRR retention range in order to retain data. Figure 5-2 shows typical waveforms.

5.4 RAM DATA RETENTION OPERATION

The requirement for R6500/1 RAM data retention and re-start operation is application dependent. If R6500/1 RAM data retention is not required during loss of VCC, then VRR can be connected to the same power source as VCC. With this configuration a complete initialization of R6500/1 program variables in RAM is required upon VCC and VRR power application.

If the R6500/1 RAM is to retain data during loss of VCC, the following is required:

1. Connection of VCC and VRR to separate power supplies or to the same primary power supply with isolation diodes and battery or other backup power for VRR.
2. VCC power monitor hardware with power loss and cold/warm start indications to the R6500/1.
3. Power loss detection as well as cold and warm start initialization in the R6500/1 program.

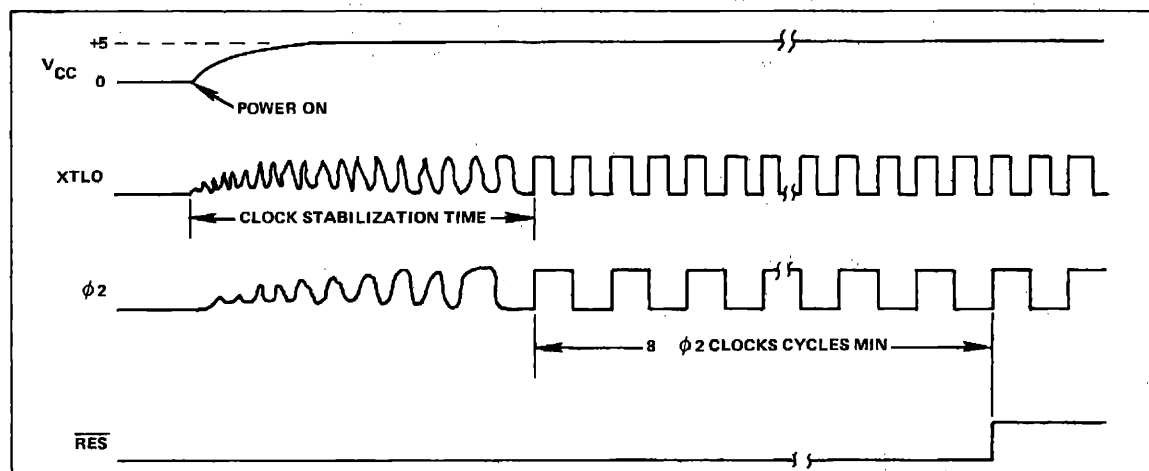


Figure 5-1. Power Turn-On Timing Detail

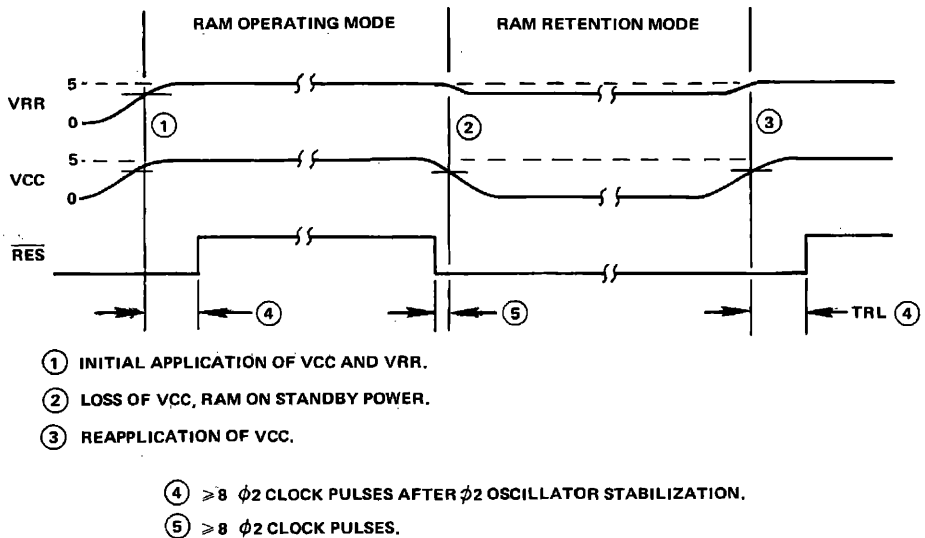


Figure 5-2. RAM Retention Mode Timing

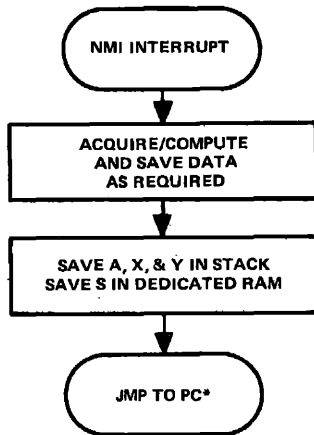
The power monitor hardware must sense the loss of VCC power in sufficient time to allow the R6500/1 to save required CPU register data in RAM. The power loss indication line can be connected to the NMI interrupt input in order to cause an immediate R6500/1 interrupt upon power loss detection.

The power monitor hardware should also provide an indication of cold start (initial VCC and VRR power application) or warm start (VCC power re-application while VRR is retained on backup power) provided as input on a data I/O pin.

A level indication is sufficient. The R6500/1 program can then initialize all, or partial, program variables upon initialization then jump to any other starting address as required

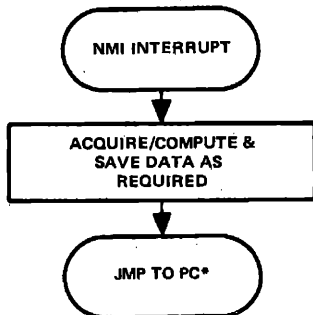
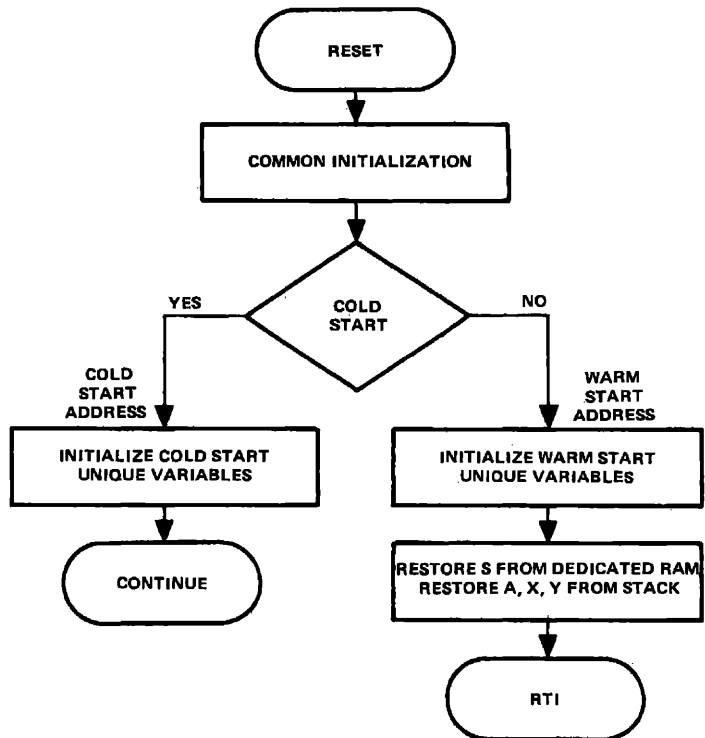
depending upon cold/warm start condition.

Upon power loss detection, the R6500/1 should save all required CPU register data in either the stack or dedicated RAM. The stack may be preferred if dedicated RAM is not available. If the program is to restart at the interrupted address, then all CPU registers must be saved, i.e., S, P, PC, A, X, and Y. The stack pointer must be saved in a dedicated RAM address. Note that processor status P and the program counter, PC, are already saved on the stack by the NMI interrupt R6500/1 hardware processing. If the warm start can be performed at a specific address, then the saving of the register data at power loss detection may not be required. Figure 5-3 shows top level flowcharts of typical power down and power-up processing.



*HANG UP IN SHORT LOOP UNTIL EXECUTION TERMINATES

a. Program Recovery at
Address of Interruption



*HANG UP IN SHORT LOOP UNTIL EXECUTION TERMINATES

b. Program Recovery at
Specific Restart Address

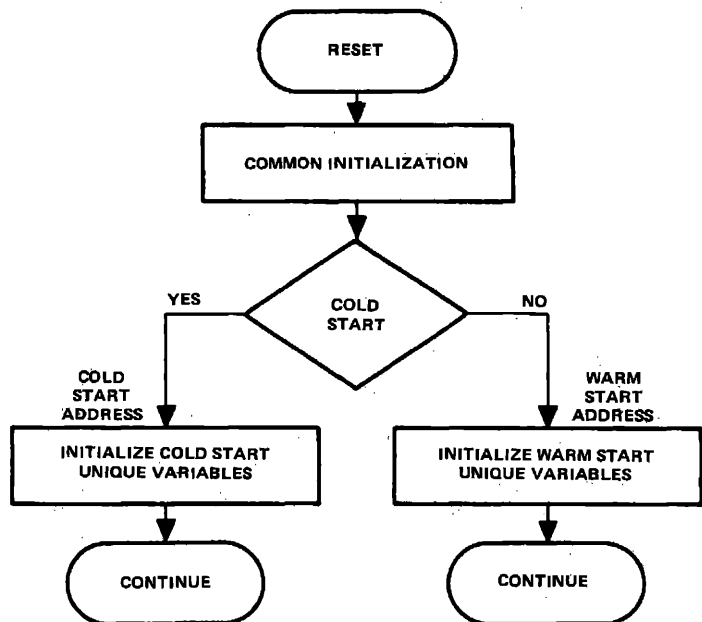


Figure 5-3. Typical R6500/1 Power Loss Recovery Flowcharts

SECTION 6 TEST

6.1 TEST MODE

The R6500/1 test function is multiplexed on the $\overline{\text{RES}}$ input pin. The three input states for this pin are:

1. $<0.8\text{V}$ **Reset state.** All R6500/1 outputs are forced to the high state.
2. $>2.0\text{V}$ and $<5.5\text{V}$ **Normal run state.** The low to high transition on the $\overline{\text{RES}}$ pin initiates fetch of the reset vector from address FFC and FFD and starts user program execution at the vectored address.
3. $>10.0\text{V}$ and $<10.5\text{V}$ **Test state.** The only internal action that takes place is switching of the data source for instruction memory from internal ROM to I/O port "C". Bit 0 of port "C" is the data least significant bit (LSB).

The test mode allows instructions and data to be input externally through I/O port "C". This capability is used at Rockwell to test all of the R6500/1 logic, registers and internal data RAM. A ROM dump may be accomplished by using the test feature to load into the internal RAM a small program to fetch each byte of ROM and output it to an I/O port. After this program is loaded the CPU is directed to begin execution out of RAM, e.g., JMP to 00. After the jump is executed, the $\overline{\text{RES}}$ line is returned to the normal run state. The normal run state allows data fetches to occur out of the internal ROM and returns port "C" to its normal function.

The detail support hardware and software required to use the R6500/1 test mode is fairly complex and time critical. For normal application testing, it is recommended that a test program be loaded into RAM and executed as explained in Section 6.2.

6.2 PROGRAM LOADING INTO RAM

A test or application program can easily be loaded into the R6500/1 RAM and executed without forcing the R6500/1 into the test mode. To do this, a short program loader function must be permanently included in the application program stored in ROM. Upon test mode selection during R6500/1 initialization, the loader reads instructions or data from an I/O port and stores them into RAM. At the first completion of the load, the loader then jumps to the first instruction in RAM to start program execution.

A program is described which may be used to load test or

application program into RAM. It can easily be adapted to specific requirements by re-assigning I/O as required. The loader uses positive handshake between the R6500/1 and the interfacing host equipment. One I/O line is dedicated to the test mode selection. The other pins assigned to loader interface signals may be assigned to normal application I/O interface signals when the test mode is not selected.

I/O is assigned for the RAM Program Loader as follows:

PA0	Data Ready (DR) — Positive edge indicates data is ready for sampling by the R6500/1.
PA1	End of Data ($\overline{\text{EOD}}$) — Negative edge indicates that all the data has been transferred to the R6500/1.
PA2	Data Taken (DT) — 0 = Data Not Taken 1 = Data Taken
PA7	Normal Mode Select (NMS) — 0 = Test Mode 1 = Normal Mode
PB7-PB0	Data input, i.e., instruction or data (PB7 = MSB, PB0 = LSB)

The flowchart in Figure 6-1 shows the loader operation. The handshake waveforms between the R6500/1 and the host are illustrated in Figure 6-2. The following description corresponds to the handshake events identified in Figure 6-2:

- 1) Host sees PA2 high, which indicates previous data, if any, has been taken by the R6500/1. The host then drops PA0 low to indicate new data is not ready. This signal should be initialized low by the host.
- 2) R6500/1 detects PA0 low then drops PA2 low to indicate that data has not been taken.
- 3) Host sees PA2 low then sets up new data.
- 4) Host sets PA0 high to indicate new data is ready.
- 5) Upon detecting positive edge of PA0, R6500/1 reads data on PB7-PB0. R6500/1 then sets PA2 high to indicate that the data has been taken.
- 6) When no more data is available, the host drops PA1 low to indicate end of data ($\overline{\text{EOD}}$). The R6500/1 then jumps to address \$000 to start program execution. If all RAM is loaded without $\overline{\text{EOD}}$ detected, the R6500/1 also jumps to address \$000.

An assembly listing of the RAM Program Loader is shown in Table 6-1.

3-121

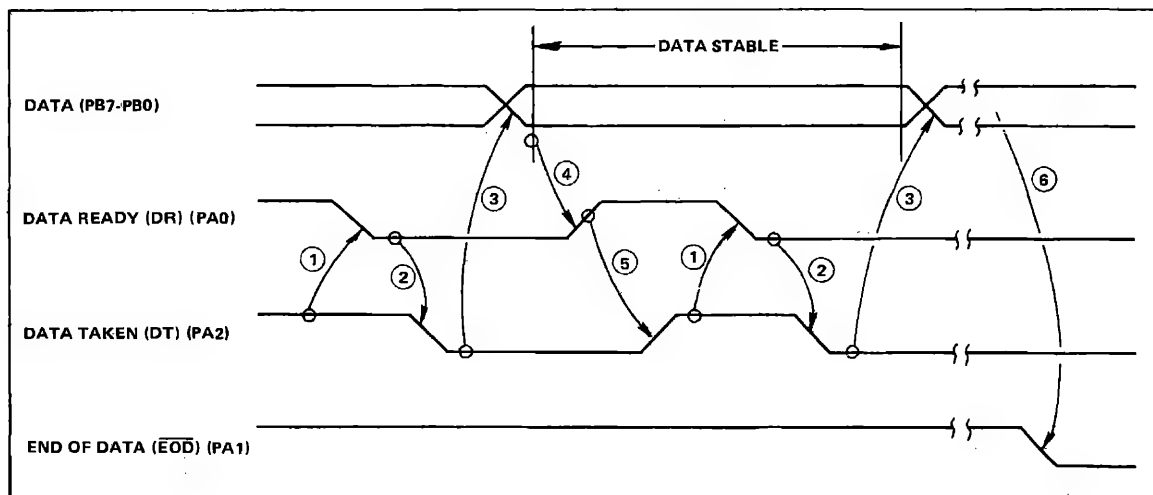


Figure 6-2. R6500/1 RAM Program Load Handshake

Table 6-1. RAM Program Loader Assembly Listing

R6500/1 RAM LOADER PAGE 001

LINE #	LOC	CODE	LINE	
0002	0000		PORTB = \$81	;Port B Address
0003	0000		PORTA = \$80	;Port A Address
0004	0000		CLRPA0 = \$89	;CLR PA0 Edge Detect
0005	0000		CTLREG = \$8F	;Control Register
0006	0000		BEGIN = \$000	;RAM First Address
0008	0000		* = \$0800	
0009	0800	A2 3F	Reset LDX #\$3F	
0010	0802	9A	TXS	;Initialize Stack Pointer
0011	0803	D8	CLD	;Set Binary Add Mode
0012	0804	A2 00	LDX #\$00	;Initialize RAM Index
0013	0806	A5 80	LDA PORTA	
0014	0808	30 2D	BMI INIT	;Test Mode Selected (PA7 = 0)?
0016	080A	A5 80	PAZCK LDA PORTA	;Yes
0017	080C	4A	LSR A	
0018	080D	B0 1C	BCS EODCK1	;Data Ready High (PA0 = 1)?
0020	080F	A9 FB	LDA #\$FB	;No, Reset Data Taken
0021	0811	B5 80	STA PORTA	;0->PA2
0023	0813	A9 20	RDYCK LDA #\$20	
0024	0815	24 8F	BIT CTLREG	
0025	0817	50 1A	BVC EODCK2	;Data Ready (PA0 Pos Edge Detected)?
0027	0819	85 89	STA CLRPA0	;Yes, Clear PA0 Pos Edge Detected
0028	081B	A5 81	LDA PORTB	;Load Data From Port B
0029	0081D	95 00	STA BEGIN,X	;Store in RAM
0030	081F	A9 FF	LDA #\$FF	
0031	0821	85 80	STA PORTA	;Set Data Taken (1->PA2)
0032	0823	E8	INX	;Increment RAM Index
0033	0824	E0 40	CPX #\$40	
0034	0826	D0 E2	BNE PAZCK	;Is RAM Full?
0036	0828	4C 00 00	JMPBEG JMP BEGIN	;Yes, Go To RAM Program Execution
0038	082B	A9 20	EODCK1 LDA #\$20	
0039	082D	25 8F	AND CTLREG	
0040	082F	F0 D9	BEQ PAZCK	;End of Data (PA1 Neg Edge Detected)?
0041	0831	D0 F5	BNE JMPBEG	;Yes, Go To RAM Program Execution
0043	0833	F0 DE	EODCK2 BEQ RDYCK	;End of Data (PA1 Neg Edge Detected)?
0044	0835	D0 F1	BNE JMPBEG	;Yes, Go To Ram Program Execution
0046	0837		INIT	;First Address of Normal Program
0048	0837		* = \$FFC	
0049	OFFC	00 08	RES .WOR RESET	;Reset Vector
0050	OFFE		.END	

Errors = 0000 <0000>

End of Assembly

APPENDIX A — SYSTEM MEMORY MAP

	HEX	
IRQ Vector High	FFF	ROM
IRQ Vector Low	FFE	
RES Vector High	FFD	
RES Vector Low	FFC	
NMI Vector High	FFB	
NMI Vector Low	FFA	
User Program	FF9	}
	800	
R6500/1E User Program	7FF	
	400	}
Unassigned	3FF	
	900	
Control Register	08F	Input/Output
Unassigned	08E	
	08B	
Clear PA1 Neg Edge Detected (Write Only) (1)	08A	
Clear PA0 Pos Edge Detected (Write Only) (1)	089	
Upper Latch and Transfer Latch to Counter (Write Only) (2)	088	
Lower Count (Read Only) (2)	087	
Upper Count (Read Only)	086	
Lower Latch (Write Only)	085	
Upper Latch (Write Only)	084	
PORT D	083	
PORT C	082	
PORT B	081	
PORT A	080	
Unassigned		}
User RAM	03F	
	000	RAM

Notes:

- (1) I/O command only; i.e., no stored data.
 (2) Clears Counter Overflow — Bit 7 in Control Register.

APPENDIX B — R6500 INSTRUCTION SET

This appendix contains a summary of the R6500 instruction set. For detailed information, consult the R6500 Microcomputer System Programming Manual, Document 29650 N30.

B.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch On Carry Set	ORA	"OR" Memory with Accumulator
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator	PHA	Push Accumulator on Stack
BMI	Branch on Result Minus	PHP	Push Processor Status on Stack
BNE	Branch on Result not Zero	PLA	Pull Accumulator from Stack
BPL	Branch on Result Plus	PLP	Pull Processor Status from Stack
BRK	Force Break		
BVC	Branch on Overflow Clear	ROL	Rotate One Bit Left (Memory or Accumulator)
BVS	Branch on Overflow Set	ROR	Rotate One Bit Right (Memory or Accumulator)
		RTI	Return from Interrupt
CLC	Clear Carry Flag	RTS	Return from Subroutine
CLD	Clear Decimal Mode		
CLI	Clear Interrupt Disable Bit	SBC	Subtract Memory from Accumulator with Borrow
CLV	Clear Overflow Flag	SEC	Set Carry Flag
CMP	Compare Memory and Accumulator	SED	Set Decimal Mode
CPX	Compare Memory and Index X	SEI	Set Interrupt Disable Status
CPY	Compare Memory and Index Y	STA	Store Accumulator in Memory
		STX	Store Index X in Memory
DEC	Decrement Memory by One	STY	Store Index Y in Memory
DEX	Decrement Index X by One		
DEY	Decrement Index Y by One	TAX	Transfer Accumulator to Index X
		TAY	Transfer Accumulator to Index Y
EOR	"Exclusive-Or" Memory with Accumulator	TSX	Transfer Stack Pointer to Index X
		TXA	Transfer Index X to Accumulator
INC	Increment Memory by One	TXS	Transfer Index X to Stack Register
INX	Increment Index X by One	TYA	Transfer Index Y to Accumulator
INY	Increment Index Y by One		
JMP	Jump to New Location		
JSR	Jump to New Location Saving Return Address		

B2. INSTRUCTION SET SUMMARY TABLE

INSTRUCTIONS		IMMEDIATE		ABSOLUTE		ZERO PAGE		ACCUM		IMPLIED		(IND. X)		(IND. Y)		Z PAGE, X		ABS. X		ABS. Y		RELATIVE		INDIRECT		Z PAGE, Y		PROCESSOR STATUS CODES										Mnemonic																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																				
Mnemonic	OPERATION	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	7	6	5	4	3	2	1	0																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																					
ADC	A ← M ← C ← A (4) (1)	69	2	2	6D	4	3	65	3	2			61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															</

APPENDIX C — SYSTEM SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T	0 to +70 -40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

STATIC DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$, for R6500/1, $V_{CC} = 5V \pm 5\%$ for R6500/1A)

Parameter	Symbol	Min	Typ	Max.	Unit
Power Dissipation (Outputs High) 0°C to +70°C -40°C to +85°C	P_D	— —	500 550	— —	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.5	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) 0°C to +70°C -40°C to +85°C	I_{RR}	— —	10 12	— —	mAdc
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	—	+0.8	Vdc
Input Leakage Current $V_{IN} = 0$ to 5.0 Vdc RES, NMI	I_{IN}	—	± 1.0	± 2.5	μ Adc
Input High Voltage (XTLI)	V_{IHXT}	+4.0	—	V_{CC}	Vdc
Input Low Voltage (XTLI)	V_{ILXT}	-0.3	—	+0.8	Vdc
Input Low Current ($V_{IL} = 0.4$ Vdc)	I_{IL}	—	-1.0	-1.6	mAdc
Output High Voltage ($V_{CC} = \min$, $I_{LOAD} = -100 \mu$ Adc)	V_{OH}	-2.4	—	—	Vdc
Output High Voltage ($V_{CC} = \min$)	V_{CMOS}	$V_{CC} - 30\%$	—	—	Vdc
Output Low Voltage ($V_{CC} = \min$, $I_{LOAD} = 1.6$ mAdc)	V_{OL}	—	—	+0.4	Vdc
Output High Current (Sourcing) ($V_{OH} = 2.4$ Vdc)	I_{OH}	-100	—	—	μ Adc
Output Low Current (Sinking) ($V_{OL} = 0.4$ Vdc)	I_{OL}	1.6	—	—	mAdc
Input Capacitance ($V_{IN}=0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz) PA, PB, PC, PD, CNTR XTLI, XTLO	C_{IN}	— —	— —	10 50	pF
Output Capacitance ($V_{IN}=0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz)	C_{OUT}	—	—	10	pF
I/O Port Resistance PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, CNTR	R_L	3.0	6.0	11.5	K Ω

Note: Negative sign indicates outward current flow, positive indicates inward flow.

AC CHARACTERISTICS(V_{CC} = 5V ± 10% for R6500/1, V_{CC} = 5V ± % for R6500/1A)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T _{cyc}	0.500	5.0	0.250	5.0	μsec
Internal Write to Peripheral Data Valid (TTL)	T _{PDW}	1.0		0.5		μsec
Internal Write to Peripheral Data Valid (CMOS)	T _{CMOS}	2.0		1.0		μsec
Peripheral Data Setup Time	T _{PDSU}	400		200		nsec
Count and Edge Detect Pulse Width	T _{PW}	1.0		0.5		μsec

APPENDIX D — R6500/1E EMULATOR PART

D.1 INTRODUCTION

To aid the user in designing R6500/1 microcomputer systems, Rockwell has developed an R6500/1E Emulator. The basic architecture of the Emulator is the same as that of the R6500/1 single-chip microcomputer except the Emulator brings the address, data, and required control lines off the chip to an external memory.

This appendix describes only the differences between the R6500/1 single-chip microcomputer and the R6500/1E Emulator. All sections of the Emulator not described in this appendix are identical to the corresponding section of the R6500/1 single chip microcomputer.

D.2 R6500/1 EMULATOR INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6500/1E Emulator. Figure D-1 is the Emulator Interface diagram. Figure D-2 shows the Emulator pin configuration. Table D-1 describes the function of each pin of the Emulator that differs from the R6500/1 device.

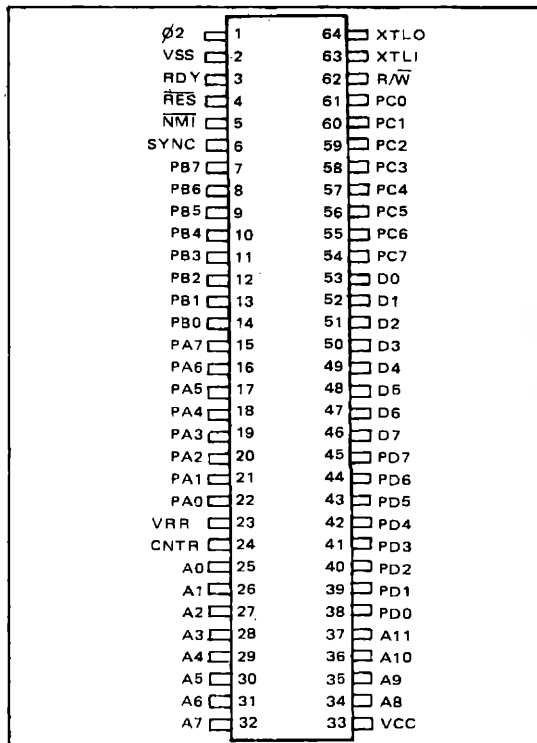


Figure D-2. Emulator Pin Configuration

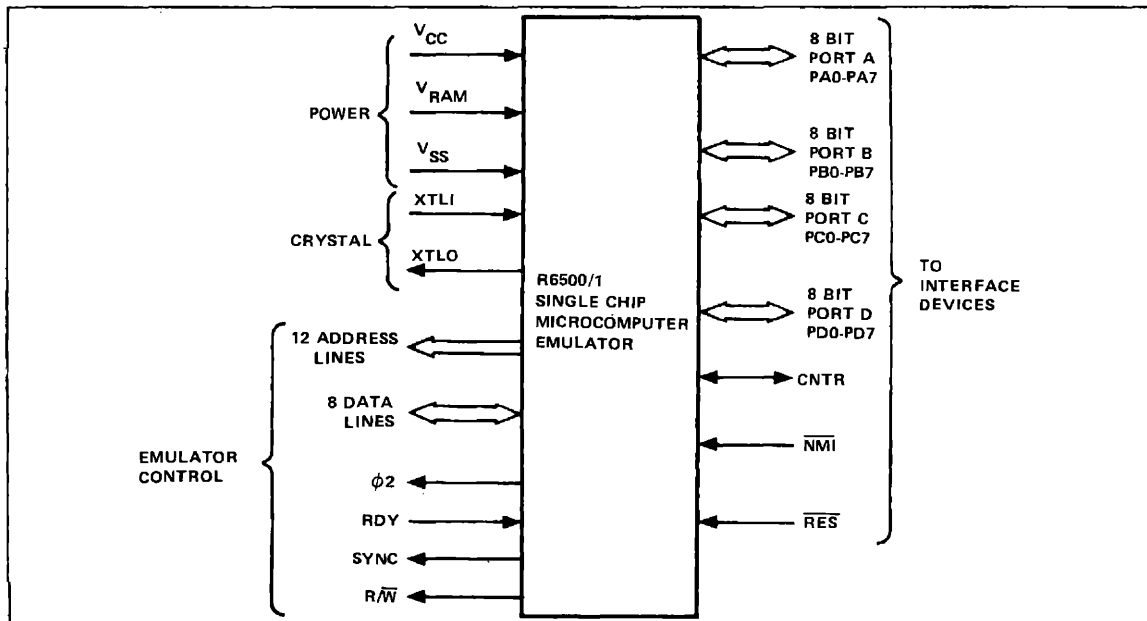


Figure D-1. R6500/1 Emulator Interface Diagram

Table D-1. R6500/1E Emulator Pin Description

Signal Name	Pin No.	Description
R/W	62	Read/Write allows the CPU to control the direction of data transfers between the R6500/1E Emulator CPU and external memory. This line is high when reading data from memory and is low when writing data to memory.
RDY	3	The Ready input delays execution of any cycle during which the RDY line is low. This allows the user to halt or single step the CPU on all cycles except write cycles. A negative transition to the low state during the $\phi 2$ clock low pulse will halt the CPU with the address lines containing the current address being fetched. If RDY is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent $\phi 2$ clock pulse in which the RDY line is low. This feature allows the CPU to interface with memories having slow access times, such as EPROMS used with the R6500/1 Emulator part during prototype system development.
SYNC	6	The Sync signal is provided to identify cycles in which the CPU is performing OP CODE fetch. SYNC goes high during the $\phi 2$ clock low pulse of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\phi 2$ clock low pulse in which SYNC went high, the CPU will halt in its current state and will remain in that state until the RDY line goes high. Using this technique, the SYNC signal can be used to control RDY to cause single instruction execution.
$\phi 2$	1	Phase 2 ($\phi 2$) clock pulse. Data transfer takes place only during $\phi 2$ clock pulse high.
A0-A11	25-37	Address Bus lines. The address bus buffers on the R6500/1E are push/pull type drivers capable of driving at least 130 pf and one standard TTL load. The address bus always contains known data. The addressing technique involves putting an address on the address bus which is known to be either in program sequence, on the same page in program memory, or at a known point in memory. The I/O address commands are also placed on these lines.
D0-D7	53-46	Data Bus lines. All transfers of instructions and data between the CPU and memory, I/O, and other interfacing circuitry take place on the data bus lines. The buffers driving the data bus lines have full three-state capability, which is necessitated by the fact that the lines are bidirectional. Each data bus pin is connected to an input and output buffer, with the output buffer remaining in the floating condition.

D.3 SYSTEM ARCHITECTURE

Figure D-3 is a block diagram of the R6500/1E Emulator. The function of each block is identical to its counterpart in the R6500/1 microcomputer. The main differences between the two products are in the ROM, the clock oscillator, the input/output ports and write-only monitoring.

D.3.1 ROM

To facilitate debugging, the R6500/1 ROM has been removed from the R6500/1E Emulator, and has been replaced by external memory. Also, an additional 1024 bytes of memory (400-7FF) are addressable.

D.3.2 CLOCK OSCILLATOR

The external frequency reference for the R6500/1E Emulator may be either a crystal or a clock. The RC option is not available for this device.

D.3.3 INPUT/OUTPUT PORTS

The R6500/1E has the internal I/O and CNTR port pull-up resistance only. The option to delete the pull-up resistance is not included in this device.

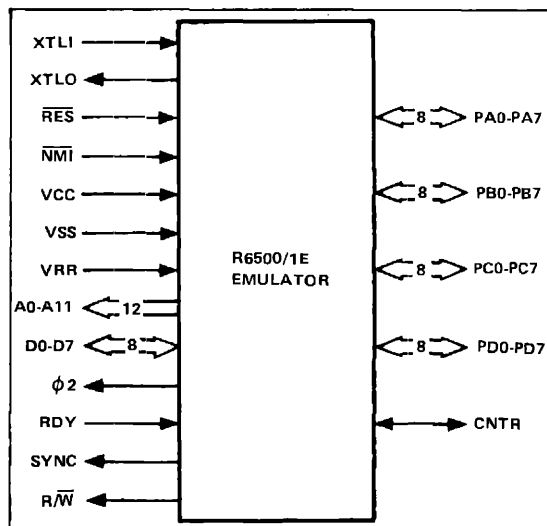


Figure D-3. R6500/1E Emulator Block Diagram

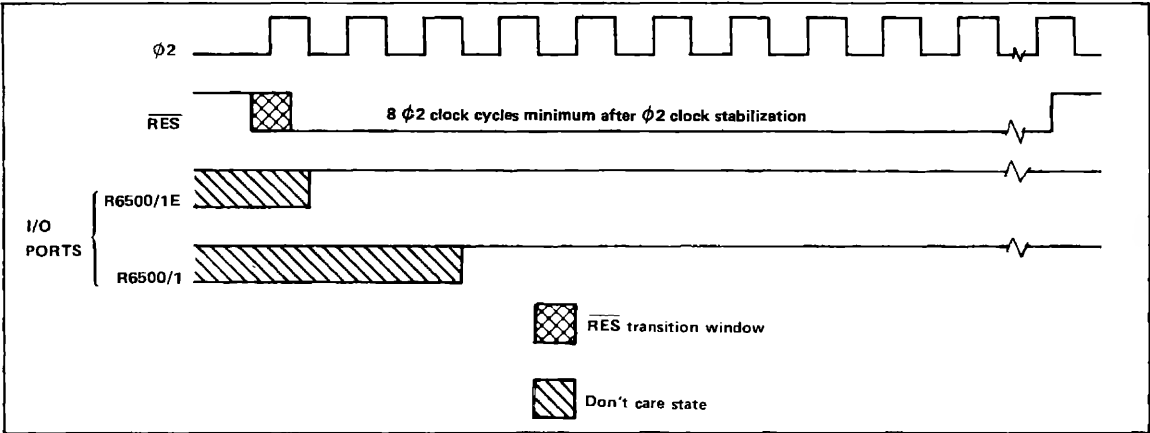
D.3.4 WRITE-ONLY MONITORING

The R6500/1E allows the user to monitor write operations to the internal RAM and I/O by routing those operations externally as well as internally. Read operations are not routed externally.

D.4 R6500/1E I/O PORT INITIALIZATION

Ports A, B, C and D and the CNTR line in R6500/1E are initialized to the logic high state two $\phi 2$ clock cycles earlier

than in the R6500/1. It is still required, however, that the $\overline{\text{RES}}$ line to the R6500/1E be held low for at least eight $\phi 2$ clock cycles after VCC reaches operating range and the $\phi 2$ clock oscillator has stabilized.

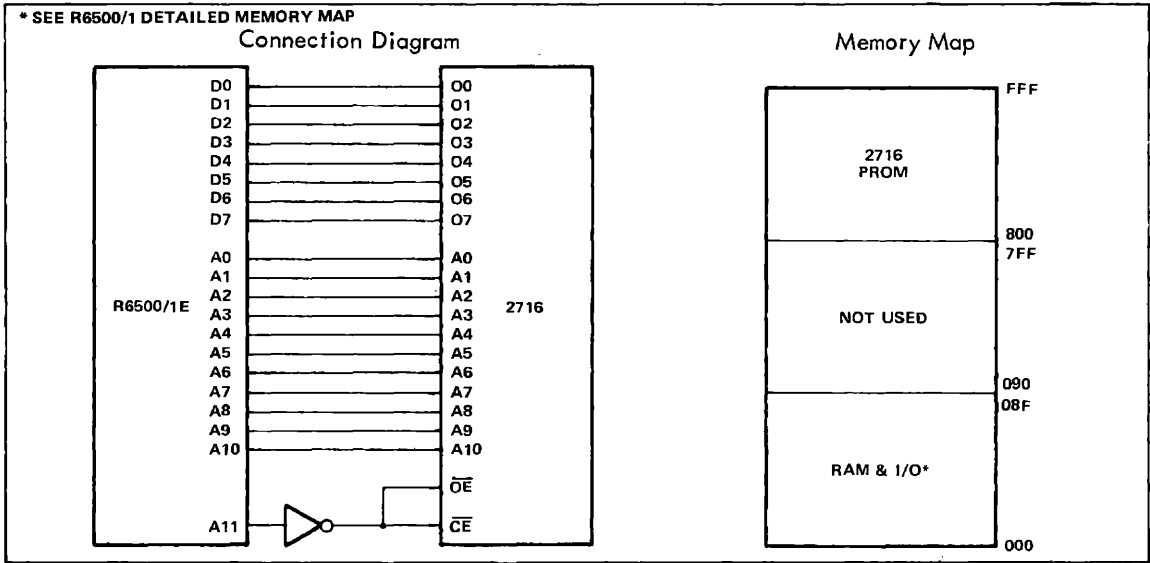


D.5 TYPICAL R6500/1E PROGRAM MEMORY INTERCONNECTIONS

Shown below and on the following page are two typical connections between the R6500/1E and program memory (in

this case, type 2716 and 2708 PROMs). Example 1 shows a connection to a 2K 2716 PROM. Since the R6500/1 has a 2K ROM capacity, the contents of the PROM could be masked directly into the production R6500/1 ROM.

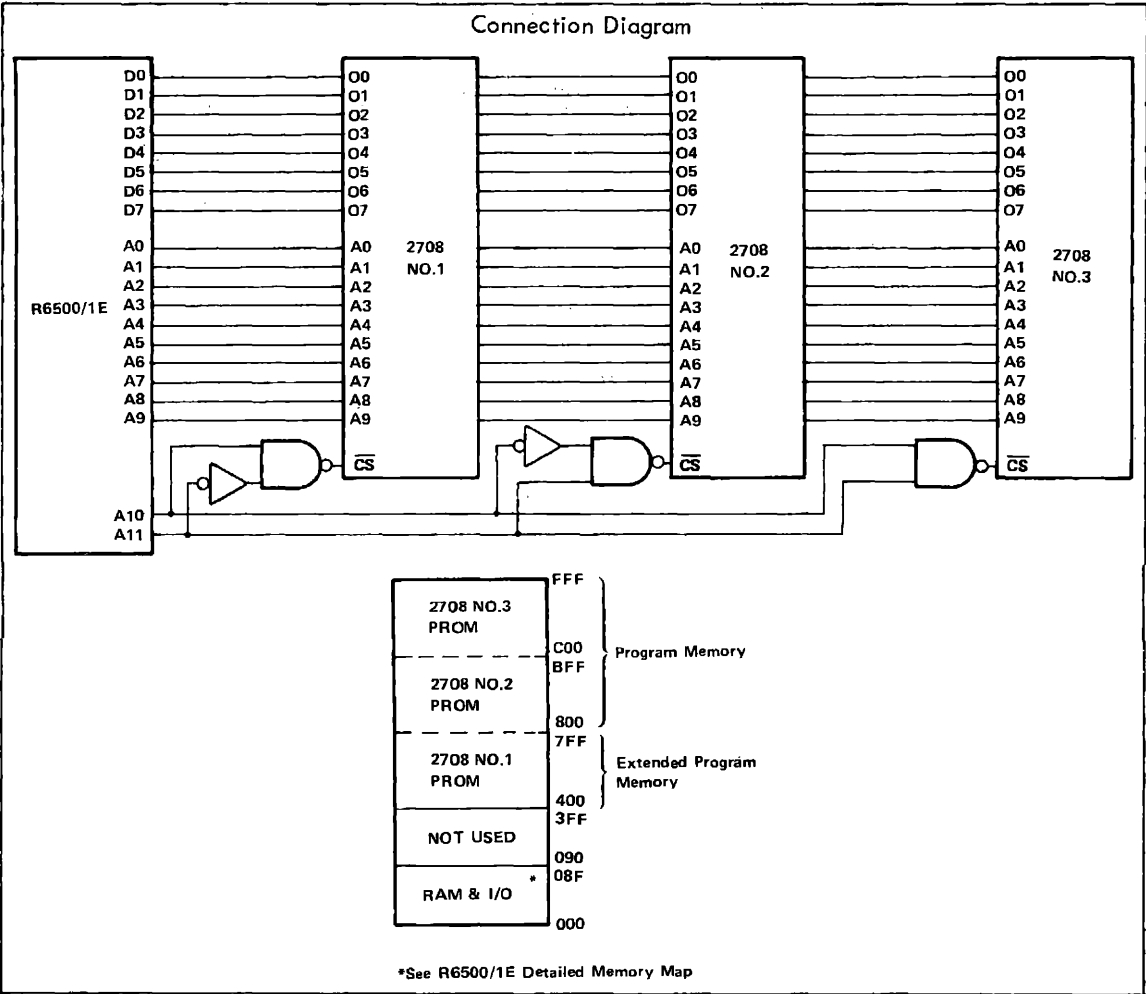
Example 1. R6500/1E Connected to One 2716 PROM (2K Bytes)



Example 2 shows a connection to 3K of 2708 PROMs. The extra 1K PROM allows expanded or additional programs be used during R6500/1 firmware development. The production

program, however, must be reduced to 2K maximum (between addresses 800 and FFF) before committing to R6500/1 ROM.

Example 2. R6500/1E Connected to Three PROMs (3K Bytes)



Truth Table

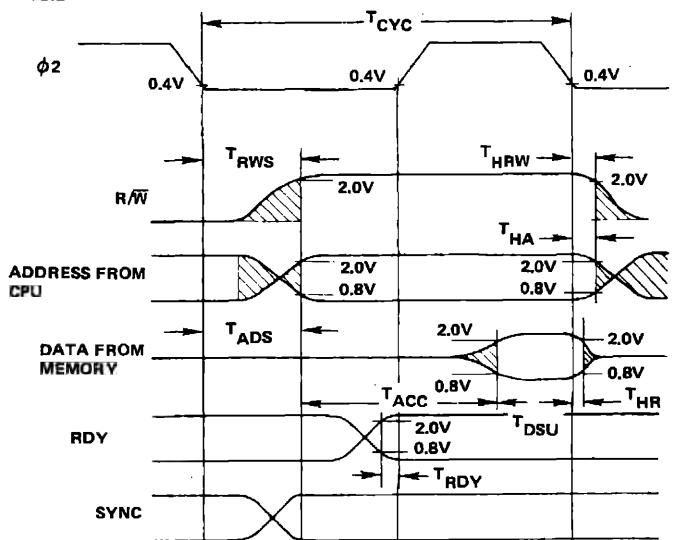
Address		PROM Select			Selected Address Range
A11	A10	2708 No. 1 CE	2708 No. 2 CE	2708 No. 3 CE	
0	0	1	1	1	000-3FF
0	1	0	1	1	400-7FF
1	0	1	0	1	800-BFF
1	1	1	1	0	C00-FFF

D.6 R6500/1E TIMING

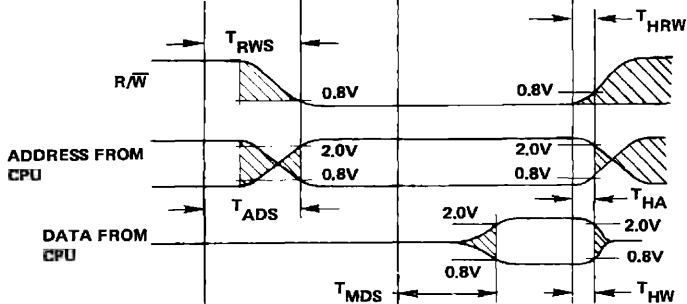
Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
R/W setup time from CPU	T_{RWS}		300		200	ns
Address setup time from CPU	T_{ADS}		300		200	ns
Memory read access time	T_{ACC}		525		225	ns
Data stabilization time	T_{DSU}	150		75		ns
Data hold time — Read	T_{HR}	10		10		ns
Data hold time — Write	T_{HW}	30		30		ns
Data delay time from CPU	T_{MDS}		200		150	ns
RDY setup time	T_{RDY}	100		50		ns
SYNC delay time from CPU	T_{SYNC}		350		175	ns
Address hold time	T_{HA}	30		30		ns
R/W hold time	T_{HRW}	30		30		ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μ s

PHASE 2 ($\phi 2$) TIMING REFERENCE

TIMING FOR READING DATA FROM EXTERNAL MEMORY



TIMING FOR WRITING DATA TO EXTERNAL MEMORY



D.7 R6500/1E ELECTRICAL CHARACTERISTICS(V_{CC} = 5.0 ±5%, V_{SS} = 0; T_A, 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Threshold Voltage D0-D7, RDY,	V _{IHT}	V _{SS} + 2.4	—	—	V _{dc}
Input Low Threshold Voltage D0-D7, RDY,	V _{ILT}	—	—	V _{SS} + 0.8	V _{dc}
Three-State (Off State) Input Current (V = 0.4 to 2.4V, V _{CC} = 5.25V) D0-D7	I _{TSI}	—	—	10	μA
Output High Voltage (I _{LOAD} = 100 μAdc, V _{CC} = 4.75V) D0-D7, SYNC, A0-A11, $\overline{R}/\overline{W}$, ϕ 2	V _{OH}	V _{SS} + 2.4	—	—	V _{dc}
Output Low Voltage (I _{LOAD} = 1.6 mAdc, V _{CC} = 4.75V) D0-D7, SYNC, A0-A11, $\overline{R}/\overline{W}$, ϕ 2	V _{OL}	—	—	V _{SS} + 0.6	V _{dc}
Power Dissipation	P _D	—	0.50	1.00	W
Capacitance (V _{in} = 0, T _A = 25°C, f = 1 MHz)	C				pF
RDY	C _{in}	—	—	10	
D0-D7		—	—	15	
A0-A11, $\overline{R}/\overline{W}$, SYNC	C _{out}	—	—	12	
ϕ 2	C ₀₂	—	50	80	



R6500/1E MICROPROCESSOR EMULATOR DEVICE

INTRODUCTION

The R6500/1EC and R6500/1EQ devices provide all the features of the R6500/1 Microcomputer in a ROMless form suitable for use as an advanced microprocessor complete with 16 bit counter and 32 I/O lines, and an address and data bus for 4K of external memory.

To aid in designing R6500/1 microcomputer systems, it may also be used as an Emulator device. Device architecture is basically the same as the R6500/1 except that the address, data, and associated control lines are routed off the chip for connection to an external memory.

The functions and operation of the devices are identical to the R6500/1 except for minor differences. The R6500/1 Data Sheet Order No. D51 (Document No. 2900D51) contains a description

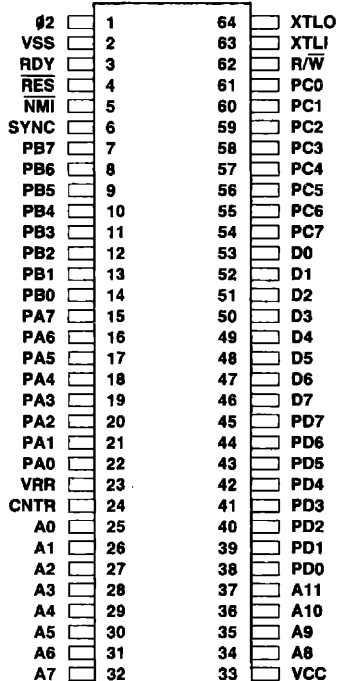
of R6500/1 and R6500/1 common interface signals and functions.

The device is available in both 64-pin DIP ceramic (R6500/1EC) and 64-pin QIP Plastic (R6500/1EQ).

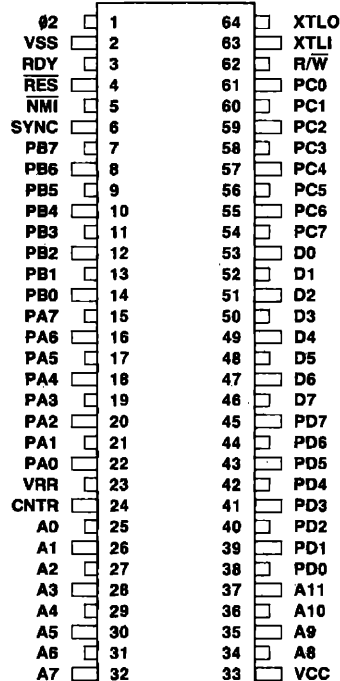
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ORDERING INFORMATION

Part Number	Package Type	Frequency Option	Temperature Range
R6500/1EC	Ceramic	1 MHz	0°C to 70°C
R6500/1EAC	Ceramic	2 MHz	0°C to 70°C
R6500/1EQ	Plastic	1 MHz	0°C to 70°C
R6500/1EAQ	Plastic	2 MHz	0°C to 70°C



R6500/1E



R6500/1EQ

Pin Configuration

SIGNAL DESCRIPTIONS

All R6500/1 interface signals are provided in the device. While the pin assignments are different from the R6500/1 in order to accommodate the 64-pin package, the interface electrical characteristics are identical. The device provides 24 additional signals to route the address bus (12 lines), the data bus (8 lines), and control signals (4 lines) off the chip for connection to external memory.

MEMORY MAP

An additional 1024 bytes of memory (400-7FF) are addressable in the device.

EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock — the RC option is not available in the device.

I/O PORT PULLUPS

The device has internal I/O port pullup resistance only.

DEVICE ADDITIONAL SIGNALS

Signal Name	Pin No.	Description
R/W	62	Read/Write. The Read/Write output controls the direction of data transfer between the CPU and external memory. This line is high when reading data from memory and low when writing data to memory.
RDY	3	Ready. The Ready input delays execution of any cycle during which the RDY line is low. This allows the user to halt or single step the CPU on any cycle except a write cycle. A negative transition to the low state during the $\Phi 2$ clock low pulse will halt the CPU with the address lines containing the current address being fetched. If RDY is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent $\Phi 2$ clock pulse in which the RDY line is low.
SYNC	6	Sync. The Sync signal is provided to identify those cycles in which the CPU is performing an OP CODE fetch. SYNC goes high during $\Phi 2$ clock-low pulse during an OP CODE fetch and stay high for the remainder of that cycle. If the RDY line is pulled low during the $\Phi 2$ clock low pulse in which SYNC went high, the CPU will halt in its current state and will remain in that state until the RDY line goes high. Using this technique, the SYNC signal can be used to control RDY to cause single instruction execution.

Signal Name	Pin No.	Description
$\Phi 2$	1	Phase 2 ($\Phi 2$) clock pulse. Data transfer can take place only during $\Phi 2$ clock pulse.
A0-A11	25-32 34-37	Address Bus Lines. The address bus buffers on the device are push/pull type drivers capable of driving at least 130 pF and one standard TTL load. The address bus always contains known data. The addressing technique involves putting an address on the address bus which is known to be either in program sequence, on the same page in program memory, or at a known point in memory. The I/O addresses are also placed on these lines.
D0-D7	53-46	Data bus Lines. All transfers of instructions and data between the CPU and external memory take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.

I/O PORT INITIALIZATION

Ports A, B, C and D and the CNTR line in the device are initialized to the logic high state two $\Phi 2$ clock cycles earlier than in the R6500/1. It is still required, however, that the \overline{RES} line be held low for at least eight $\Phi 2$ clock cycles after V_{CC} reaches operating range (Figure 1).

TYPICAL PROGRAM MEMORY INTERCONNECTIONS

Illustrated are two typical connections between the R6500/1E and program memory (in this case, type 2716 and 2708 PROMS). Figure 2 shows a connection to a 2K 2716 PROM. Since the R6500/1 has a 2K ROM capacity, the contents of the PROM could be masked directly into the production R6500/1 ROM.

Figure 3 shows a connection to 3K of 2708 PROMS. The extra 1K PROM allows expanded or additional programs be used during R6500/1 firmware development. The production program, however, must be reduced to 2K maximum (between addresses 800 and FFF) before committing to R6500/1 ROM.

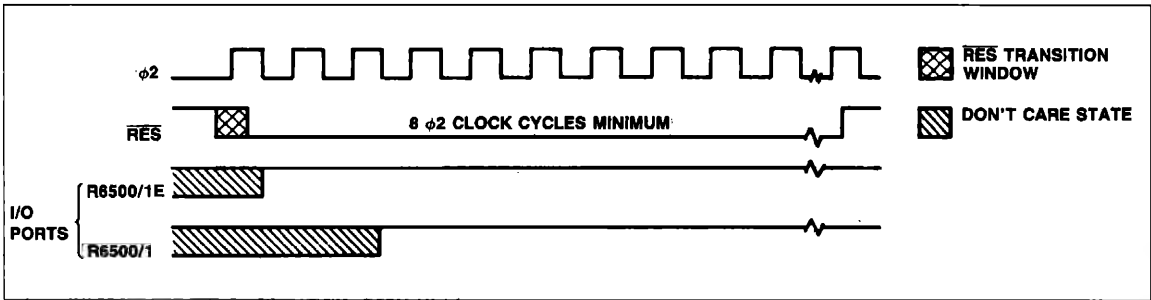


Figure 1. I/O Port Initialization

3

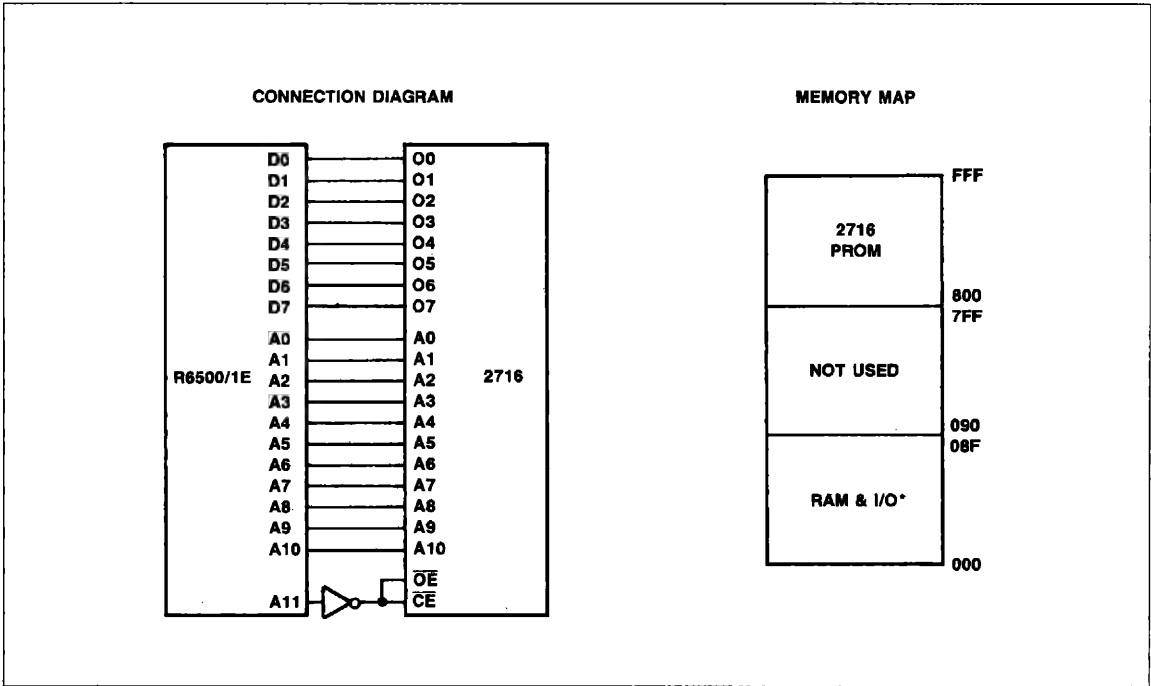


Figure 2. Device Connected to One 2716 PROM (2K Bytes)

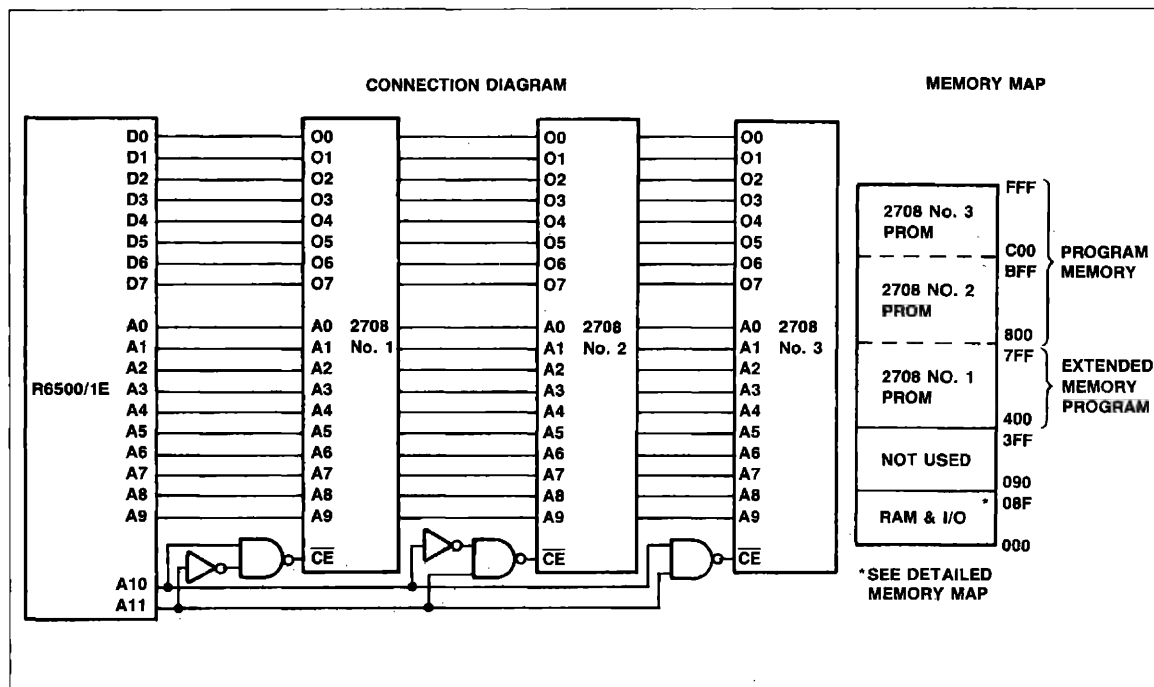


Figure 3. Device Connected to Three PROMS (3K Bytes)

TRUTH TABLE

Address		PROM Select			Selected Address Range
A11	A10	2708 No. 3 CE	2708 No. 2 CE	2808 No. 1 CE	
0	0	1	1	1	000-3FF
0	1	1	1	0	400-7FF
1	0	1	0	1	800-BFF
1	1	0	1	1	C00-FFF

DEVICE TIMING

Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
R/W setup time from CPU	T _{RWS}		300		200	ns
Address setup time from CPU	T _{ADS}		300		200	ns
Memory read access time	T _{ACC}		525		225	ns
Data stabilization time	T _{DSU}	150		75		ns
Data hold time — Read	T _{HR}	10		10		ns
Data hold time — Write	T _{HW}	30		30		ns
Data delay time from CPU	T _{MDS}		200		150	ns
RDY setup time	T _{RDY}	100		50		ns
SYNC delay time from CPU	T _{SYNC}		350		175	ns
Address hold time	T _{HA}	30		30		ns
R/W hold time	T _{HRW}	30		30		ns
Cycle Time	T _{CYC}	1.0	10.0	0.5	10.0	μs

3

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ± 5%, V_{SS} = 0, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Threshold Voltage DO-D7, RDY,	V _{IHT}	V _{SS} + 2.4	—	—	V _{dc}
Input Low Threshold Voltage DO-D7, RDY,	V _{ILT}	—	—	V _{SS} + 0.8	V _{dc}
Three-State (Off State) Input Current (V = 0.4 to 2.4V, V _{CC} = 5.25V) D0-D7	I _{TSI}	—	—	10	μA
Output High Voltage (I _{LOAD} = 100μAdc, V _{CC} = 4.75V) D0-D7, SYNC, A0-A11, R/W, φ2	V _{OH}	V _{SS} + 2.4	—	—	V _{dc}
Output Low Voltage (I _{LOAD} = 1.6 mAdc, V _{CC} = 4.75V) D0-D7, SYNC, A0-A11, R/W, φ2	V _{OL}	—	—	V _{SS} + 0.6	V _{dc}
Power Dissipation	P _D	—	0.75	1.20	W
Capacitance (V _{in} = 0, T _A = 25°C, f = 1 MHz)	C				pF
RDY	C _{in}	—	—	10	
D0-D7		—	—	15	
A0-A11, R/W, SYNC	C _{out}	—	—	12	
φ2	C _{φ2}	—	50	80	
I/O Port Pull-up Resistance	R _L	3.0	6.0	11.5	kohm

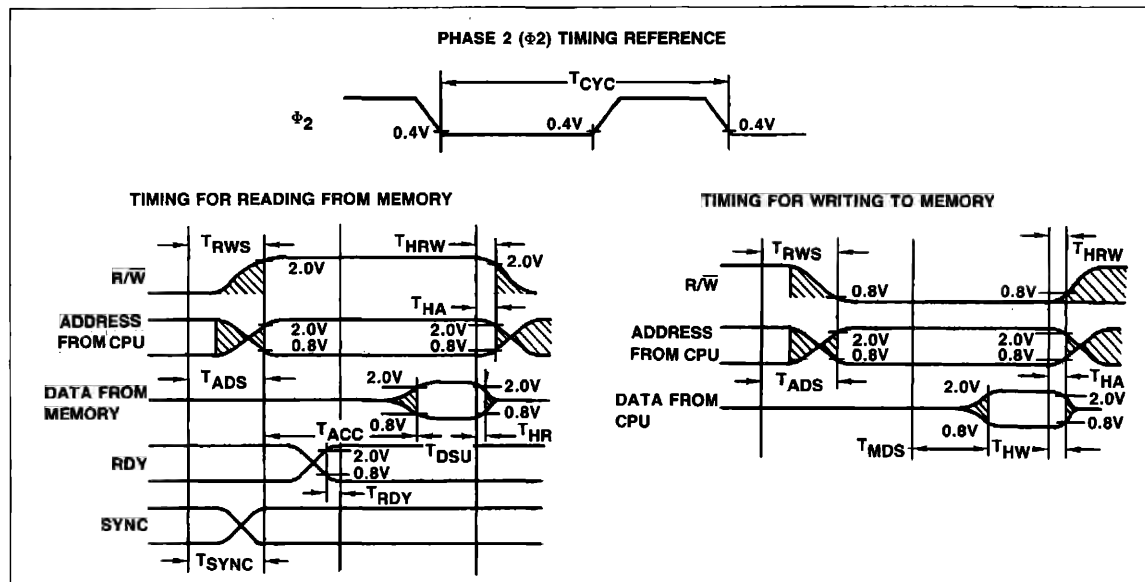
DETAILED MEMORY MAP

IRQ VECTOR HIGH	FFF	} ROM
IRQ VECTOR LOW	FFE	
RES VECTOR HIGH	FFD	
RES VECTOR LOW	FFC	
NMI VECTOR HIGH	FFB	
NMI VECTOR LOW	FFA	
R6500/1 USER PROGRAM	FF9	}
	800	
R6500/1E EXTENDED PROGRAM AREA (1)	7FF	
	400	}
UNASSIGNED		
CONTROL REGISTER	08F	
	08E	}
UNASSIGNED	08B	
	08A	
CLEAR PA1 NEG EDGE DETECTED (2)	089	} INPUT/OUTPUT
CLEAR PA0 POS EDGE DETECTED (2)	088	
UPPER LATCH AND TRANSFER LATCH TO COUNTER (3)	087	
LOWER COUNT (3)	086	
UPPER COUNT	085	
LOWER LATCH	084	
UPPER LATCH	083	
PORT D	082	
PORT C	081	
PORT B	080	
PORT A	07F	
UNASSIGNED	03F	
USER RAM	000	} RAM(4)

NOTES:

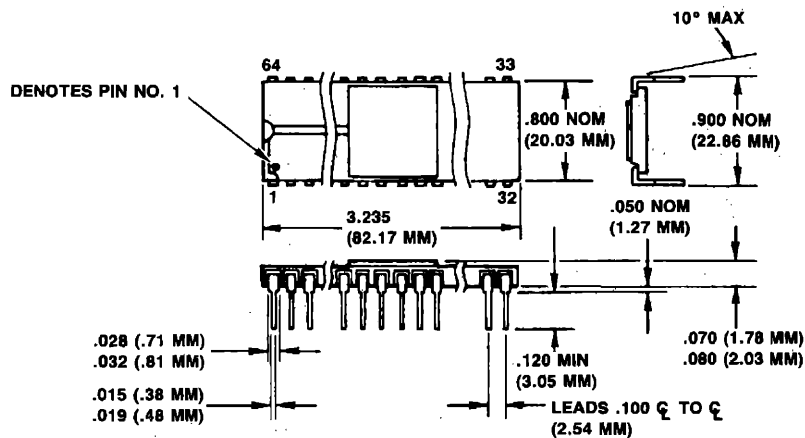
- (1) Additional 1024 bytes are decoded for external memory addressing. This area can be used during debut, but cannot be used in a masked ROM R6500/1.
- (2) I/O command only; i.e., no stored data.
- (3) Clears Counter Overflow — Bit 7 in Control Register
- (4) CAUTION: The device allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F, and 340-37F; as well as 000-03F. The production R6500/1, however allows RAM mapping only at 000-03F.

TIMING DIAGRAMS

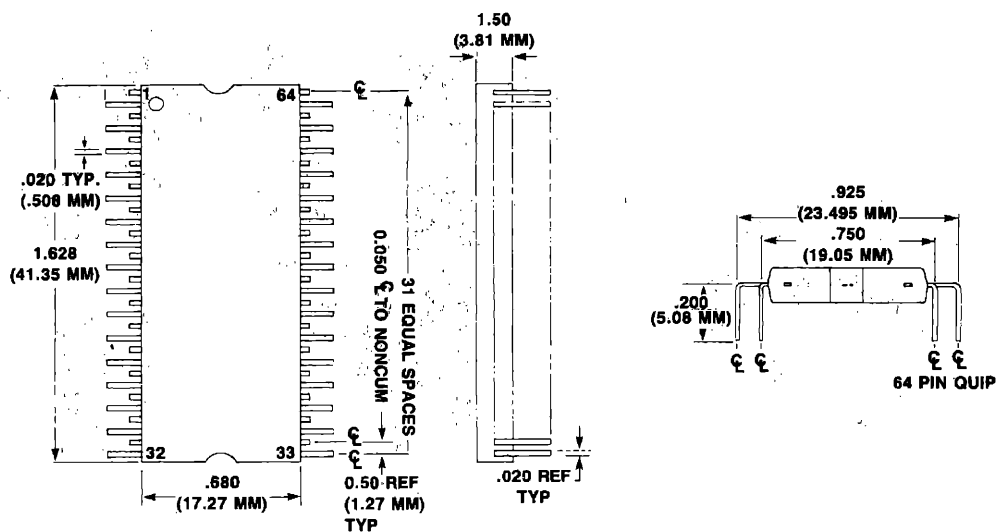


PACKAGE DIMENSIONS

R6500/1EC 64-PIN DIP CERAMIC



R6500/1EQ 64-PIN QUIP PLASTIC





R6500/1EB and R6500/1EAB BACKPACK EMULATOR

INTRODUCTION

The Rockwell R6500/1EB and R6500/1EAB Backpack Emulator is the PROM prototyping version of the 8-bit, masked-ROM R6500/1 one-chip microcomputer. Like the R6500/1, the backpack device is totally upward/downward compatible with all members of the R6500/1 family. It is designed to accept standard 5-volt, 24-pin EPROMs or ROMs directly, in a socket on top of the Emulator. This packaging concept allows a standard EPROM to be easily removed, reprogrammed, then reinserted as often as desired.

The backpack devices have the same pinouts as the masked-ROM R6500/1 microcomputer. These 40 pins are functionally and operationally identical to the pins on the R6500/1, with some minor differences (described herein). The R6500/1 Microcomputer Data Sheet (Rockwell Document No. 29000D51) includes a description of the interface signals and their functions. Whereas the masked-ROM R6500/1 provides 2K bytes of read-only memory, the R6500/1EB will address 3K bytes of external program memory. This extra memory accommodates program patches, test programs or optional programs during breadboard and prototype development states.

ORDERING INFORMATION

BACKPACK EMULATOR

Part Number	Memory Capacity	Compatible Memories	Temperature Range and Speed
R6500/1EB1	2K × 8	2716, 2516 2316B	0°C to 70°C 1 MHz
R6500/1EB3	3K × 8	2732	0°C to 70°C 1 MHz
R6500/1EAB3	3K × 8	2732A (250 ns)	0°C to 70°C 2 MHz

SUPPORT PRODUCTS

Part Number	Description
S65-101	SYSTEM 65 Microcomputer Development System
M65-040	PROM Programmer Module
M65-081	1-MHz R6500/1 Personality Module
M65-082	2-MHz R6500/1 Personality Module

FEATURES

- PROM version of the R6500/1
- Completely pin compatible with R6500/1 single-chip microcomputers
- Profile approaches 40-pin DIP of R6500/1
- Accepts 5-volt, 24-pin industry-standard EPROMs
 - 4K memories—2732, 2732A (3K bytes addressable)
 - 2K memories—2716, 2516, 2316B
- Use as prototyping tool or for low volume production
- 3K bytes of memory capacity (1K, 2K, 4K memories)
- 64 × 8 static RAM
- Separate power pin for RAM
- Software compatibility with the R6500 family
- 32 bi-directional TTL compatible I/O lines (4 ports)
- 1 bi-directional TTL compatible counter I/O line
- 16-bit programmable counter/latch with four modes (interval timer, pulse generator, event counter, pulse width measurement)
- 5 interrupts (reset, non-maskable, two external edge sensitive, counter)
- Crystal or external time base
- Single +5V power supply



R6500/1EB-R6500/1EAB Backpack Emulator

CONFIGURATIONS

The Backpack Emulator is available in three different versions, to accommodate various 24-pin 2K- and 4K-memories and speeds. All three versions provide 64 bytes of RAM and I/O, as well as 24 signals to support the external memory "backpack" socket. The 24 backpack signals differ somewhat between versions (due to memory pin differences) but always consist of the address bus (12 lines), the data bus (8 lines) and the \overline{OE} , \overline{CE} , V_{CC} and V_{SS} signals (one line each). See the Interface Diagram.

The external memories must always occupy the upper 2K of available memory (addresses 800 through FFF) for implementation of interrupt vectors. See Memory Map. The Backpack Emulator provides a read block to the external memory where internal RAM or I/O are located in the same addresses as that occupied by external memory.

EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock—the RC option is not available in the emulator device. The R6500/1EB and R6500/1EAB divide the input clock by two regardless of the source.

I/O PORT PULLUPS

The emulator devices have internal I/O port pullup resistors.

TEST MODE DELETED

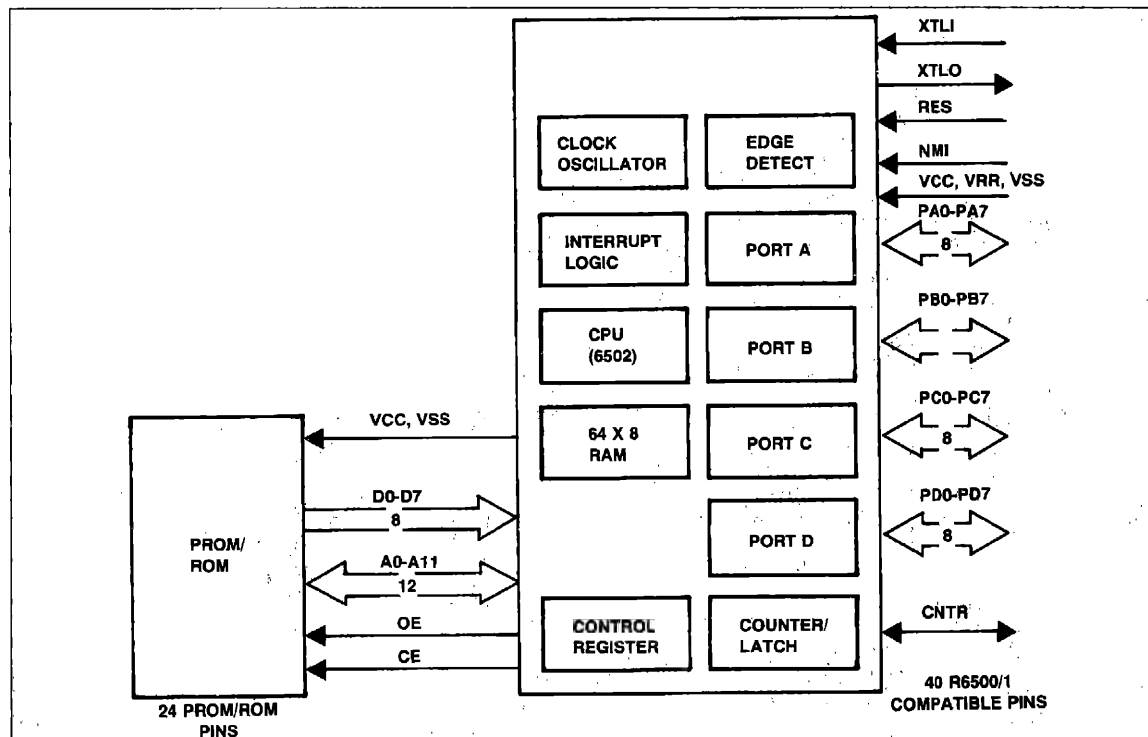
The test mode of the R6500/1 is not available on the Backpack Emulator.

PRODUCT SUPPORT

The Backpack Emulator is just one of the products that Rockwell offers to facilitate system and program development for the R6500/1.

The SYSTEM 65 Microcomputer Development System with R6500/1 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/1 Personality Module allows total system test and evaluation. With the optional PROM Programmer, SYSTEM 65 can also be used to program EPROMs for the development activity. When PROM programs have been finalized, the PROM device can be sent to Rockwell for masking into the 2K ROM of the R6500/1.

In addition to support products, Rockwell offers regularly-scheduled designer's courses at regional centers.



R6500/1EB Interface Diagram

DETAILED MEMORY MAP

		HEX
PROM	IRQ VECTOR HIGH	FFF
	IRQ VECTOR LOW	FFE
	RES VECTOR HIGH	FFD
	RES VECTOR LOW	FFC
	NMI VECTOR HIGH	FFB
	NMI VECTOR LOW	FFA
	R6500/1 USER PROGRAM	FF9
		400
PROM	R6500/1EB EXTENDED PROGRAM AREA (1)	3FF
		400
NOT USED	UNASSIGNED	
I/O	CONTROL REGISTER	08F
	UNASSIGNED	08E
		08B
	CLEAR PA1 NEG EDGE DETECTED (2)	08A
	CLEAR PA0 POS EDGE DETECTED (2)	089
	UPPER LATCH AND TRANSFER LATCH TO COUNTER (3)	088
	LOWER COUNT (3)	087
	UPPER COUNT	086
	LOWER LATCH	085
	UPPER LATCH	084
	PORT D	083
	PORT C	082
	PORT B	081
	PORT A	080
NOT USED	UNASSIGNED	03F
RAM	USER RAM	000

NOTES

- (1) Additional 1024 bytes are decoded for external memory addressing by the Backpack Emulator Device. This area can be used during debug, but cannot be used in a masked ROM R6500/1. (Available only on R6500/1EB3a)
- (2) I/O command only; i.e., no stored data.
- (3) Clears Counter Overflow—Bit 7 in Control Register
- (4) CAUTION: The device allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F, and 340-37F; as well as 000-03F. The production R6500/1, however, allows RAM mapping only at 000-03F.

RAM MAPPING

The Backpack Emulator allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F and 340-37F, as well as 000-03F. The production R6500/1, however, allows RAM mapping only at 000-03F. This means that a write to location 40, for example, will write to location 0 in the Backpack Emulator, and to invalid RAM in the R6500/1 production part.

I/O PORT INITIALIZATION

Ports A, B, C, and D and the CNTR line in the Backpack Emulator are initialized to the logic high state two $\phi 2$ clock cycles earlier than in the R6500/1. The RES line to the device must, however, still be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range. See timing diagram.

BACKPACK MEMORY SIGNAL DESCRIPTION

Signal Name	Pin No.	Description
D0-D7	9S-11S, 13S-17S	Data Bus Lines. All instruction and data transfers take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.
A0-A9	1S-8S, 23S, 24S	Address Bus Lines. The address bus lines are buffered by push/pull type drivers that can drive one standard TTL load.
A10	19S	Address Bus Line 10. This address line has the same characteristics and functions as Lines A0-A9.
\overline{CE}	18S	Chip Enable. In the R6500/1EB1, \overline{CE} is active when the address is 800-FF. In the R6500/1EB3 and R6500/1EAB3, \overline{CE} is active when the address is 400-FFF. This line can drive one TTL load.
\overline{OE}	20S	Memory Enable Line. This signal provides the output enable for the memory to place information on the data bus lines. This signal is driven by the R/W signal from the CPU and then inverted by a standard TTL inverter, to form \overline{OE} .
V_{CC}	24S	Main Power Supply +5V. This pin is tied directly to pin 30 (V_{CC}).
$V_{CC}/A11$	21S	Main Power Supply +5V. This pin is tied directly to pin 30 (V_{CC}), except in the R6500/1EB3 and R6500/1EAB3, where it is tied to A11. During backup power, power is supplied only to the RAM memory, and not to the PROMs.
V_{SS}	12S	Signal and Power Ground (zero volts). This pin is tied directly to pin 12 (V_{SS}).

V_{RR}	1	A7	1s	24s	V_{CC}	40	NMI
PD7	2	A6	2s	23s	A8	39	RES
PD6	3	A5	3s	22s	A9	38	PA0
PD5	4	A4	4s	21s	$V_{CC}/A11^{(1)}$	37	PA1
PD4	5	A3	5s	20s	\overline{OE}	36	PA2
PD3	6	A2	6s	19s	A10	35	PA3
PD2	7	A1	7s	18s	\overline{CE}	34	PA4
PD1	8	A0	8s	17s	D7	33	PA5
PD0	9	D0	9s	16s	D6	32	PA6
XTL1	10	D1	10s	15s	D5	31	PA7
XTL0	11	D2	11s	14s	D4	30	V_{CC}
V_{SS}	12	V_{SS}	12s	13s	D3	29	PB0
PC7	13					28	PB1
PC6	14					27	PB2
PC5	15					26	PB3
PC4	16					25	PB4
PC3	17					24	PB5
PC2	18					23	PB6
PC1	19					22	PB7
PC0	20					21	CNTR

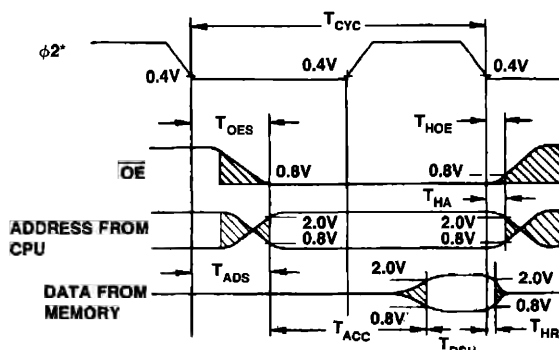
NOTE: (1) PIN 21 IS V_{CC} FOR R6500/1EB1 OR A11 FOR R6500/1EB3

READ TIMING CHARACTERISTICS

Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{\text{OE}}$ setup time from CPU	T_{OES}	—	300	—	150	ns
Address setup time from CPU	T_{ADS}	—	300	—	150	ns
Memory read access time	T_{ACC}	—	525	—	250	ns
Data stabilization time	T_{DSU}	150	—	100	—	ns
Data hold time—Read	T_{HR}	10	—	10	—	ns
Address hold time	T_{HA}	30	—	30	—	ns
$\overline{\text{OE}}$ hold time	T_{HOE}	30	—	30	—	ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μs

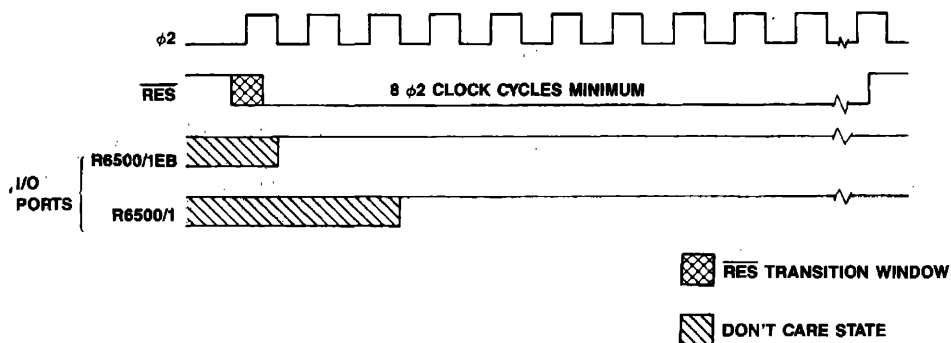
3

READ TIMING WAVEFORMS



* $\phi 2$ IS SHOWN FOR REFERENCE ONLY AND IS NOT AVAILABLE EXTERNAL TO THE DEVICE.

I/O PORT INITIALIZATION TIMING



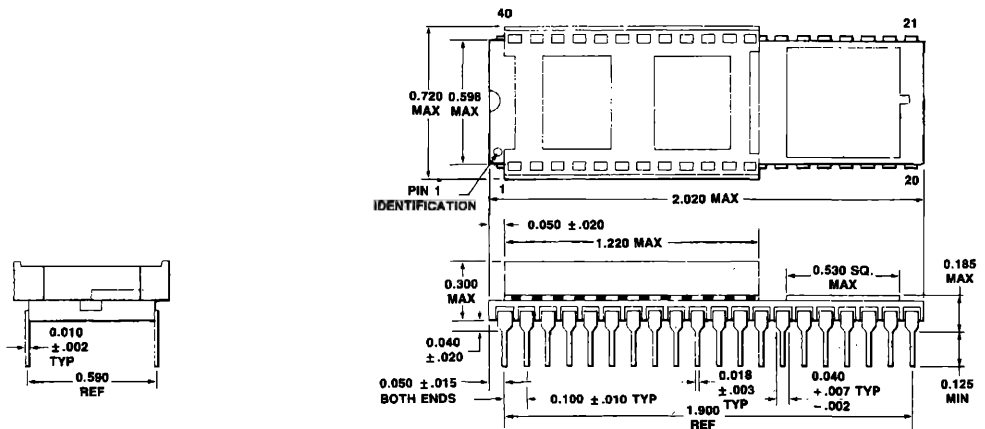
ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ± 5%, V_{SS} = 0, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Threshold Voltage D0-D7	V _{IHT}	V _{SS} + 2.4	—	—	Vdc
Input Low Threshold Voltage D0-D7	V _{ILT}	—	—	V _{SS} + 0.8	Vdc
Three-State (Off State) Input Current (V = 0.4 to 2.4V, V _{CC} = 5.25V) D0-D7	I _{TSI}	—	—	10	μA
Output High Voltage (I _{LOAD} = 100 μA, V _{CC} = 4.75V) D0-D7, A0-A11, OE	V _{OH}	V _{SS} + 2.4	—	—	Vdc
Output Low Voltage (I _{LOAD} = 1.6 mA, V _{CC} = 4.75V) D0-D7, A0-A11, OE	V _{OL}	—	—	V _{SS} + 0.6	Vdc
Power Dissipation	P _D	—	0.80	1.30	W
Capacitance (V _{in} = 0, T _A = 25°C, f = 1 MHz) D0-D7 A0-A11	C	—	—	—	pF
	C _{in}	—	—	15	
	C _{out}	—	—	12	
I/O Port Pull-up Resistance	R _L	3.0	6.0	11.5	kohm

PACKAGE DIMENSIONS

40-PIN BACKPACK





R6500/11 AND R6500/12 ONE-CHIP MICROCOMPUTERS

SECTION 1 INTRODUCTION

3

1.1 FEATURES OF THE R6500/11 & /12

- Enhanced 6502 CPU
 - Four new bit manipulation instructions:
 - Set Memory Bit (SMB)
 - Reset Memory Bit (RMB)
 - Branch on Bit Set (BBS)
 - Branch on Bit Reset (BBR)
 - Decimal and binary arithmetic modes
 - 13 addressing modes
 - True indexing
- 3K-byte mask-programmable ROM
- 192-byte static RAM
- 32 TTL-compatible I/O lines (R6500/11)
- 56 TTL-compatible I/O lines (R6500/12)
- One 8-bit port may be tri-stated under software control
- One 8-bit port with programmable latched input
- Two 16-bit programmable counter/timers, with latches
 - Pulse width measurement
 - Asymmetrical pulse generation
 - Pulse generation
 - Interval timer
 - Event counter
 - Retriggerable interval timer
- Serial port
 - Full-duplex asynchronous operation mode
 - Selectable 5- to 8-bit characters
 - Wake-up feature
 - Synchronous shift register mode
 - Standard programmable bit rates, programmable up to 62.5K bits/sec @ 1 MHz
- Ten interrupts
 - Four edge-sensitive lines; two positive, two negative
 - Reset
 - Non-maskable
 - Two counter underflows
 - Serial data received
 - Serial data transmitted
- Bus expandable to 16K bytes of external memory

- Flexible clock circuitry
 - 2-MHz or 1-MHz internal operation
 - Internal clock with external 2 MHz to 4 MHz series resonant XTAL at two or four times internal frequency
 - External clock input divided by one, two or four
- 1 μ s minimum instruction execution time @ 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- 40-pin DIP (R6500/11)
- 64-pin QUIP (R6500/12)

1.2 SUMMARY

The Rockwell R6500/11 or R6500/12 is a complete, high-performance 8-bit NMOS-3 microcomputer on a single chip, and is compatible with all members of the R6500 family.

The R6500/11 consists of an enhanced 6502 CPU, an internal clock oscillator, 3072 bytes of Read-Only Memory, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability.

The R6500/12 consists of all the features of the R6500/11 plus three additional I/O ports. It is packaged in a 64 pin QUIP.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make either device a leading candidate for microcomputer applications.

To allow prototype circuit development, Rockwell offers a PROM-compatible 64-pin extended microprocessor device. This device, the R6511Q, provides all R6500/11 interface lines, plus the address bus, data bus and control lines to interface with external memory. With the addition of external circuits it can also be used to emulate the R6500/12 (contact Rockwell offices for details).

A backpack emulator, the R65/11EB, is available for developing R6500/11 applications. No backpack part is available for the R6500/12.

The R6511Q may also be used as a CPU-RAM-I/O counter device in multichip systems.

Rockwell supports development of the devices with the System 65 Microcomputer Development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Order Number 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order Number 202).

1.3 CUSTOMER OPTIONS

The R6500/11 microcomputer is available with the following customer specified mask options:

- Option 1 Crystal or RC oscillator
- Option 2 Clock divide by 2 or 4
- Option 3 Clock MASTER Mode or SLAVE Mode
- Option 4 Port A with or without internal pull-up resistors
- Option 5 Port B with or without internal pull-up resistors
- Option 6 Port C with or without internal pull-up resistors

All options should be specified on an R6500/11 order form.

The R6500/12 is available with all of the above options plus:

- Option 7 Port F with or without internal pull-up resistors
- Option 8 Port G with or without internal pull-up resistors

SECTION 2

INTERFACE REQUIREMENTS

This section describes the interface requirements for the single chip microcomputer devices. Figure 2-1 is the Interface Diagram for the devices, Figure 2-2 and Figure 2-3 show the mechanical outline and pin out configurations and Table 2-1 describes the function of each pin. Figure 3-1 has a detailed block diagram of the device which illustrates its internal functions.

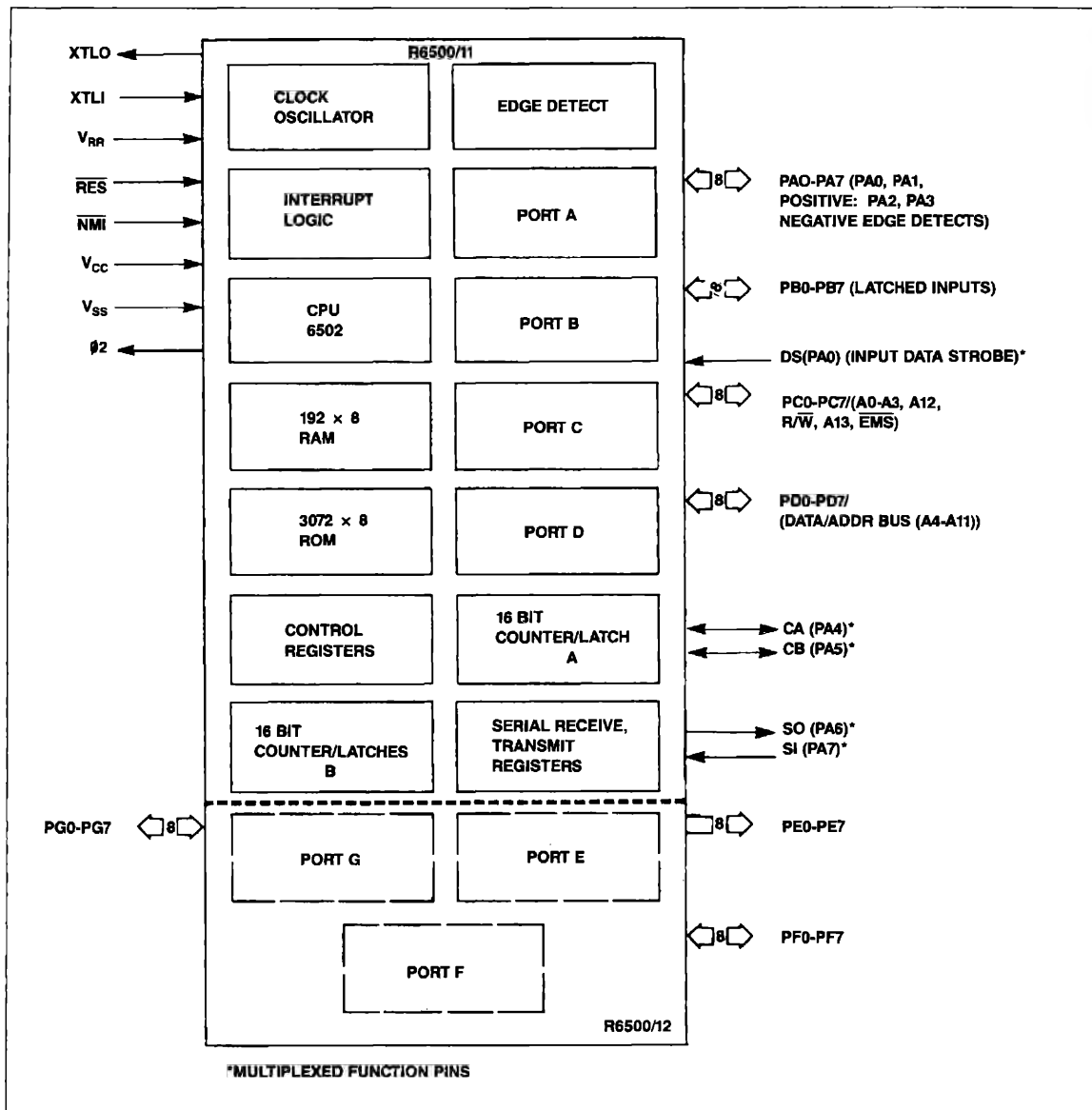


Figure 2.1 Interface Diagram

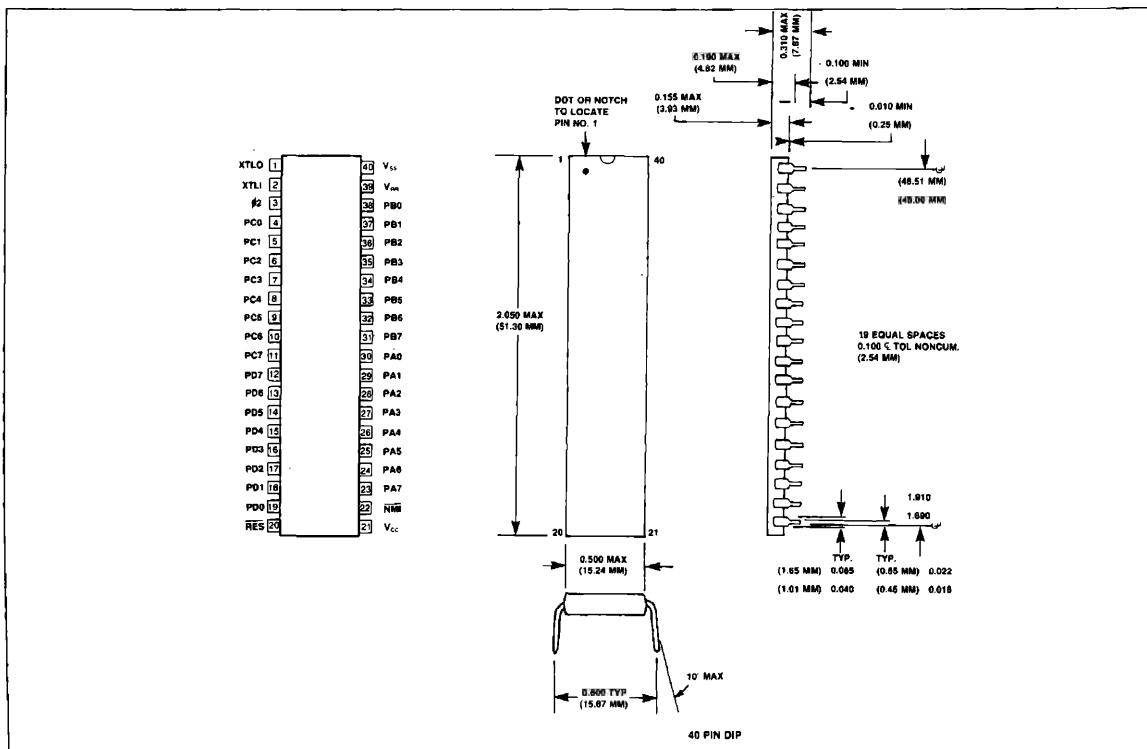


Figure 2-2. R6500/11 Mechanical Outline and Pin Out Configuration

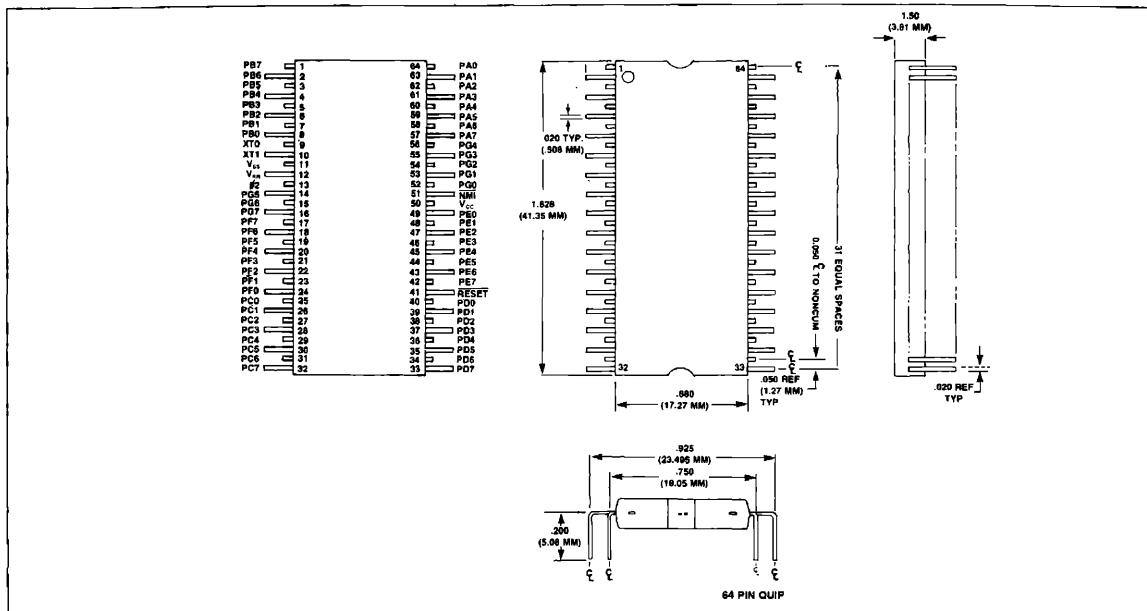


Figure 2-3. R6500/12 Mechanical Outline and Pin Out Configuration

Table 2-1. R6500/11 and R6500/12 Pin Descriptions

Signal Name	Pin Number		Description
	R6500/11	R6500/12	
V _{CC}	21	50	Main power supply +5V
V _{RR}	39	12	Separate power pin for RAM. In the event that V _{CC} power is lost, this power retains RAM data.
V _{SS}	40	11	Signal and power ground (0V)
XTLI	2	10	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to V _{SS} , or X2 or X4 clock if XTLO is floated.
XTLO	1	9	Crystal output from internal clock oscillator.
$\overline{\text{RES}}$	20	41	The Reset input is used to initialize the device. This signal must not transition from low to high for at least eight cycles after V _{CC} reaches operating range and the internal oscillator is stabilized.
$\phi 2$	3	13	Clock signal output at internal frequency.
$\overline{\text{NMI}}$	22	51	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7	30-23	64-57	Four 8-bit ports used for either input/output. Each line of Ports A, B and C consist of an active transistor to V _{SS} and an optional passive pull-up to V _{CC} . In the abbreviated or multiplexed modes of operation Port C has an active pull-up transistor. Port D functions as either an 8-bit input or 8-bit output port. It has active pull-up and pull-down transistors.
PB0-PB7	38-31	8-1	
PC0-PC7	4-11	25-32	
PD0-PD7	19-12	40-33	
PE0-PE7	N/A	49-42	For the R6500/42, the 64 pin QUIP version, three additional ports (24 lines) are provided. Each line consists of an active transistor to V _{SS} . PF0-PF7 and PG0-PG7 are bidirectional, and an optional passive pull-up to V _{CC} is provided. PE0-PE7 is outputs only with an active pull-up. All ports will source 100 μ amps. at 2.4v except port E (PE0-PE7) which will source 1 ma. at 1.5v.
PF0-PF7	N/A	24-17	
PG0-PG7	N/A	52-56	
		4 14-16	

SECTION 3

SYSTEM ARCHITECTURE

This section provides a functional description of the devices. Functionally they consist of a CPU, both ROM and RAM memories, four 8-bit parallel I/O ports (seven in the 64-pin R6500/12), a serial I/O port, dual counter/latch circuits, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal \overline{IRQ} interrupt, or the external interrupt line NMI. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory

location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Arithmetic And Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.



3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{\text{RES}}$, NMI and IRQ. IRQ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 NEW INSTRUCTIONS

In addition to the standard 6502 instruction set, four instructions have been added to the devices to simplify operations that previously required a read/modify/write operation. In order for these instructions to be equally applicable to any I/O ports, with or without mixed input and output functions, the I/O ports have been designed to read the contents of the specified port data register during the Read cycle of the read/modify/write operation, rather than I/O pins as in normal read cycles. The added instructions and their format are explained in the following subparagraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and 1 of 8 bits to be set. The second byte of the instruction designates address (00-FF) of the byte or I/O port to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch On Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of 8 bits designated by a three bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8 bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

3.3 READ-ONLY-MEMORY (ROM)

The ROM consists of 3072 bytes (3K) mask programmable memory with an address space from F400 to FFFF. ROM locations FFFA through FFFF are assigned for interrupt and reset vectors.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R6500/11 provides a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC} . During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC} , V_{RR} must be supplied within operating range and $\overline{\text{RES}}$ must be driven low at least eight $\emptyset 2$ clock pulses before V_{CC} falls out of operating range. $\overline{\text{RES}}$ must then be held low while V_{CC} is out of operating range and until at least eight $\emptyset 2$ clock cycles after V_{CC} is again within operating range and the internal $\emptyset 2$ oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3-2 shows typical waveforms.

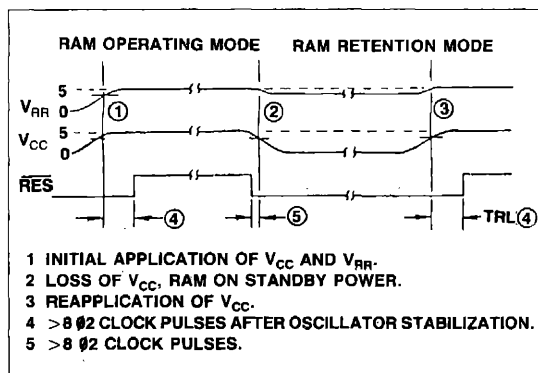


Figure 3-2. Data Retention Timing

3.5 CLOCK OSCILLATOR

Three customer selectable mask options are available for controlling the device timing. It can be ordered with a *crystal* or *RC* oscillator, a *divide by 2* or *divide by 4* countdown network and for *clock master mode* or *clock slave mode* operation.

For 2 MHz internal operations the divide by two option must be specified.

A reference frequency can be generated with the on-chip oscillator using either an external crystal or an external resistor depending on the mask option selected. The oscillator reference frequency passes through an internal countdown network (divide by 2 or divide by 4 option) to obtain the internal operating frequency (see Figure 3-3a and 3-3b). The external crystal generated reference frequency is a preferred method since the resistor method can have tolerances approaching 50%.

Note:

When operating at a 1 MHz internal frequency place a 15-22 pf capacitor between XTLO and ground.

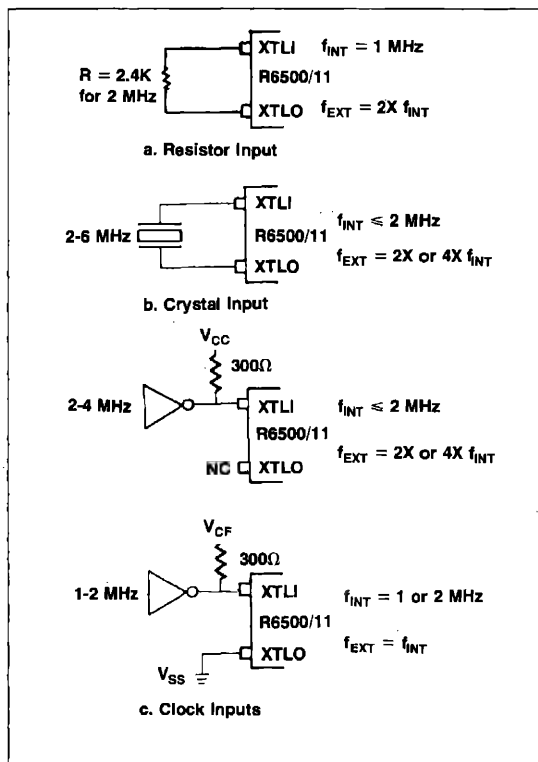


Figure 3-3. Clock Oscillator Input Options

Internal timing can also be controlled by driving the XTLO pin with an external frequency source. Figure 3-3c shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS} , the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

The operation described above assumed a CLOCK MASTER MODE mask option. In this mode a frequency source (crystal, RC network or external source) must be applied to the XTLO and XTLO pins. $\phi 2$ is a buffered output signal which closely approximates the internal timing. When a common external source is used to drive multiple devices the internal timing between devices as well as their $\phi 2$ outputs will be skewed in time. If skewing represents a system problem it can be avoided by the Master/Slave connection and options shown in Figure 3-4.

One device is operated in the CLOCK MASTER MODE and a second in the CLOCK SLAVE MODE. Mask options in the SLAVE unit convert the $\phi 2$ signal into a clock input pin which is tightly coupled to the internal timing generator. As a result the internal timing of the MASTER and SLAVE units are synchronized with minimum skew. If the $\phi 2$ signal to the SLAVE unit is inverted, the MASTER and SLAVE UNITS WILL OPERATE OUT OF PHASE. This approach allows the two devices to share external memory using cycle stealing techniques.

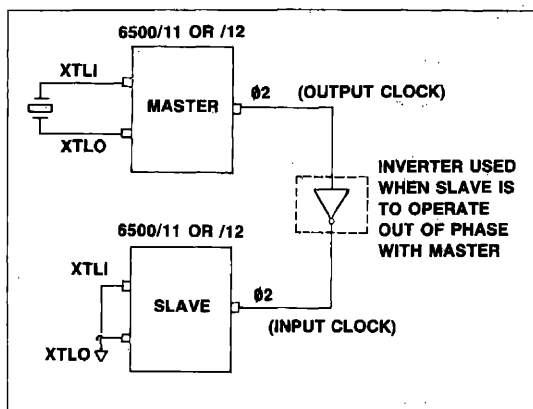


Figure 3-4. Master/Slave Connections

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the device in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-5.

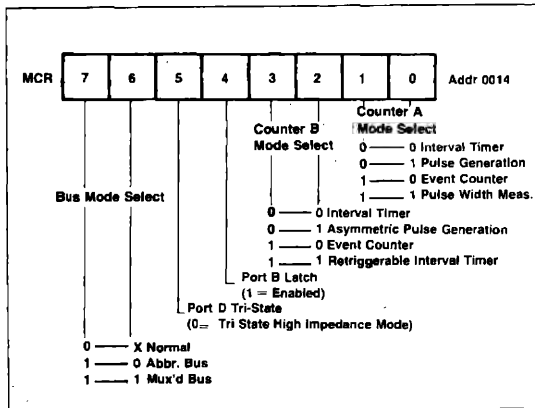


Figure 3-5. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4.

The use of Port D in Tri-State Enable is shown in Section 4.6.

The use of Bus Mode Select is shown in Section 4.5 and 4.6.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{\text{IRQ}}$ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the $\overline{\text{IRQ}}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by RES. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-6 and the functions of each bit are explained in Table 3-1.

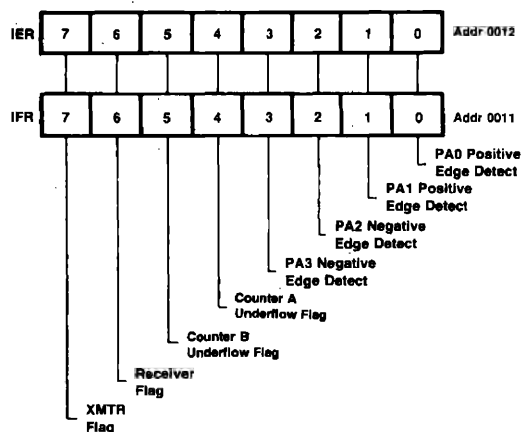


Figure 3-6. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Flag Register Bit Codes

BIT CODE	FUNCTION
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB 0 (0010) instruction or by RES.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by RES.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by RES.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by RES.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by RES.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by RES.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by RES.
IFR 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by RES.

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-7, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to

zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request ($\overline{\text{IRQ}}$). If the I bit is reset to logic 0, the $\overline{\text{IRQ}}$ signal will be serviced. If the bit is set to logic 1, the $\overline{\text{IRQ}}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET (RES), $\overline{\text{IRQ}}$, or Non-Maskable Interrupt (NMI) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit is set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

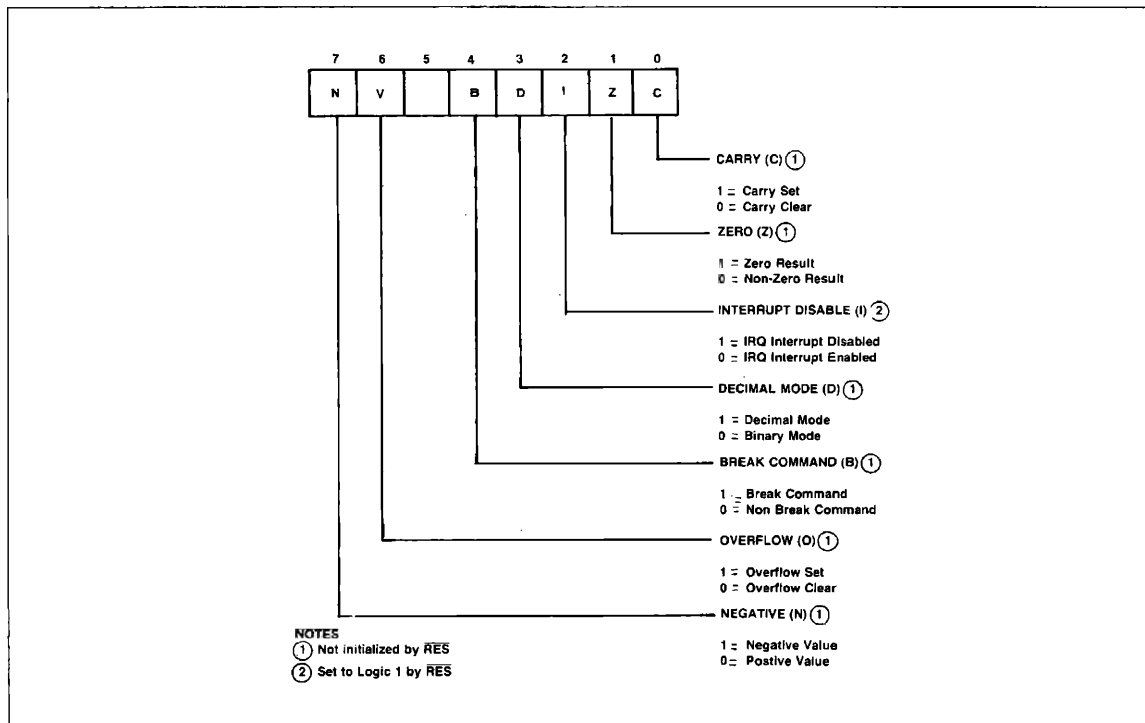


Figure 3-7. Processor Status Register

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{\text{IRQ}}$ service routine to be entered. If the $\overline{\text{IRQ}}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{\text{IRQ}}$ routine was entered as the result of an $\overline{\text{IRQ}}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$).

This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or -128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4

PARALLEL INPUT/OUTPUT PORTS

The R6500/11 has 32 I/O lines grouped into four 8-bit ports (PA, PB, PC, and PD). Ports A through C may be used either for input or output individually or in groups of any combination. Port D may be used as all inputs or all outputs.

The R6500/12, a 64 pin QUIP device, has three additional ports: PE, PF and PG. PE is outputs only; PF and PG are bidirectional.

Multifunction I/O's such as Port A and Port C are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of $3K \leq R_{pu} \leq 12K \text{ ohm}$) may be provided on all port pins except Port D and E as a mask option.

The direction of the I/O lines are controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 4-1. Section E.6 shows the I/O Port Timing.

Table 4-1. I/O Port Addresses

Port	Address
A	0000
B	0001
C	0002
D	0003
E	0004
F	0005
G	0006

4.1 INPUTS

Inputs for Ports A, B, and C and also Ports F and G of the R6500/12 are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low ($<0.8V$) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high ($>2.0V$) input will cause a logic 1 to be read. An RES signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port D may only be all inputs or all outputs. All inputs is selected by setting bit 5 of the Mode Control Register (MCR5) to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, & PD and also ports PF and PG of the R6500/12. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru D and Ports E thru G of the R6500/12 are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high ($>2.4V$) output while a logic 0 will force a low ($<0.4V$) output.

Port D all outputs is selected by setting MCR5 to a "1".

Port E is always all outputs.

4.3 PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges, and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the 02 clock rate. Edge detection timing is shown in Section E.5.

Table 4-2. Port A Control & Usage

PA0 (2)	PA0 I/O		PORT B LATCH MODE	
	MCR4 = 0		MCR4 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA0	I/O	PORT B LATCH STROBE	INPUT (1)
PA1 (2) PA2 (3) PA3 (3)	PA1-PA3 I/O			
	SIGNAL			
	NAME	TYPE		
	PA1 PA2 PA3	I/O I/O I/O		
PA4	PA4 I/O		COUNTER A I/O	
	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4) (5)		MCR0 = 1 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4)	
			SCCR7 = 0 SCCR6 = 0 MCR1 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA4	I/O	CNTA	OUTPUT
			CNTA	INPUT (1)
	SERIAL I/O SHIFT REGISTER CLOCK			
	SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1 (4)	
	SIGNAL		SIGNAL	
PA5	PA5 I/O		COUNTER B I/O	
	MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1	
			MCR3 = 1 MCR2 = X	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
PA6	PA6 I/O		SERIAL I/O XMTR OUTPUT	
	SCCR7 = 0		SCCR7 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA6	I/O	XMTR	OUTPUT
PA7	PA7 I/O		SERIAL I/O RCVR INPUT	
	SCCR6 = 0		SCCR6 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA7	I/O	RCVR	INPUT (1)

Notes:

(1) Hardware Buffer Float

(2) Positive Edge Detect

(3) Negative Edge Detect

(4) RCVR S/R Mode = 1 when SCCR6 • SCCR5 • SCCR4 = 1

(5) For the following mode combinations PA4 is available as an input only pin:

SCCR7•SCCR6•SCCR5•MCR1
+ SCCR7•SCCR6•SCCR4•MCR1
+ SCCR7•SCCR6•SCCR5
+ SCCR7•SCCR5•SCCR4•

4.4 PORT B (PB)

Port B can be programmed as an 8 bit, bit independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-3 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Section E.5.

Table 4-3. Port B Control & Usage

Pin Name	I/O Mode		Latch Mode	
	MCR4 = 0		MCR4 = 1 (2)	
	Signal		Signal	
	Name	Type (1)	Name	Type
PB0	PB0	I/O	PB0	INPUT
PB1	PB1	I/O	PB1	INPUT
PB2	PB2	I/O	PB2	INPUT
PB3	PB3	I/O	PB3	INPUT
PB4	PB4	I/O	PB4	INPUT
PB5	PB5	I/O	PB5	INPUT
PB6	PB6	I/O	PB6	INPUT
PB7	PB7	I/O	PB7	INPUT
(1) Resistive pull-up, active buffer pull down				
(2) Input data is stored in port B latch by PA0 pulse				

4.5 PORT C (PC)

Port C can be programmed as an I/O port and in conjunction with Port D, as an abbreviated bus, or as a multiplexed bus. When used in the abbreviated or multiplexed bus modes, PC0-PC7 function as A0-A3, A12, R/W, A13, and EMS, respectively, as shown in Table 4-4. EMS (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0100 and 3FFF. (See Memory Map, Appendix B). The leading edge of EMS may be used to strobe the eight address lines multiplexed on Port D in the Multiplexed Bus Mode. See Appendix E.3 through E.5 for Port C timing.

4.6 PORT D (PD)

Port D can be programmed as an I/O Port, an 8-bit tri-state data bus, or as a multiplexed bus. Mode selection for Port D is made by the Mode Control Register (MCR). The Port D output drivers can be selected as tri-state drivers by setting bit 5 of the MCR to 0 (zero). Table 4-5 shows the necessary settings for the MCR to achieve the various modes for Port D. When Port D is selected to operate in the Abbreviated Mode PD0-PD7 serves as data register bits D0-D7. When Port D is selected to operate in the Multiplexed Mode data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix C) for Abbreviated and Multiplexed memory assignments. See Appendix E.3 through E.5 for Port D timing.

4.7 PORT E, PORT F AND PORT G (PE, PF & PG) R6500/12 ONLY

Port E only operates in the Output mode. It provides a Darlington output that can source current at the high (1) level. Port F and Port G operate identically and can be programmed as bidirectional I/O ports. They have standard output capability. See Appendix E.5 for Port E, F & Port G timing.

Table 4-4. Port C Control and Usage

Pin Name	I/O Mode		Abbreviated Mode		Multiplexed Mode	
	MCR7 = 0 MCR6 = X		MCR7 = 1 MCR6 = 0		MCR7 = 1 MCR6 = 1	
	Signal		Signal		Signal	
	Name	Type (1)	Name	Type (2)	Name	Type (2)
PC0	PC0	I/O	A0	OUTPUT	A0	OUTPUT
PC1	PC1	I/O	A1	OUTPUT	A1	OUTPUT
PC2	PC2	I/O	A2	OUTPUT	A2	OUTPUT
PC3	PC3	I/O	A3	OUTPUT	A3	OUTPUT
PC4	PC4	I/O	A12	OUTPUT	A12	OUTPUT
PC5	PC5	I/O	RW	OUTPUT	RW	OUTPUT
PC6	PC6	I/O	A13	OUTPUT	A13	OUTPUT
PC7	PC7	I/O	EMS	OUTPUT	EMS	OUTPUT

(1) Resistive Pull-Up, Active Buffer Pull-Down
(2) Active Buffer Pull-Up and Pull-Down

3

Table 4-5. Port D Control and Usage

Pin Name	I/O Modes				Abbreviated Mode		Multiplexed Mode			
	MCR7 = 0 MCR6 = X MCR5 = 0		MCR7 = 0 MCR6 = X MCR5 = 1		MCR7 = 1 MCR6 = 0 MCR5 = 1		MCR7 = 1 MCR5 = 1 MCR5 = 1			
	Signal		Signal		Signal		Signal		Signal	
							Phase 1		Phase 2	
	Name	Type (1)	Name	Type (2)	Name	Type (3)	Name	Type (2)	Name	Type (3)
PD0	PD0	INPUT	PD0	OUTPUT	DATA0	I/O	A4	OUTPUT	DATA0	I/O
PD1	PD1	INPUT	PD1	OUTPUT	DATA1	I/O	A5	OUTPUT	DATA1	I/O
PD2	PD2	INPUT	PD2	OUTPUT	DATA2	I/O	A6	OUTPUT	DATA2	I/O
PD3	PD3	INPUT	PD3	OUTPUT	DATA3	I/O	A7	OUTPUT	DATA3	I/O
PD4	PD4	INPUT	PD4	OUTPUT	DATA4	I/O	A8	OUTPUT	DATA4	I/O
PD5	PD5	INPUT	PD5	OUTPUT	DATA5	I/O	A9	OUTPUT	DATA5	I/O
PD6	PD6	INPUT	PD6	OUTPUT	DATA6	I/O	A10	OUTPUT	DATA6	I/O
PD7	PD7	INPUT	PD7	OUTPUT	DATA7	I/O	A11	OUTPUT	DATA7	I/O

(1) Tri-State Buffer is in High Impedance Mode
(2) Tri-State Buffer is in Active Mode
(3) Tri-State Buffer is in Active Mode Only During the Phase 2 Portion of a Write Cycle

SECTION 5

SERIAL INPUT/OUTPUT CHANNEL

The device provides a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (@ $\phi 2 = 1$ MHz). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

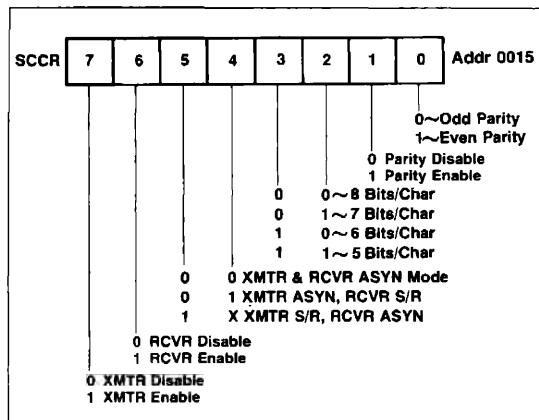


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XMTR)

The XMTR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are in Figure 5-2. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

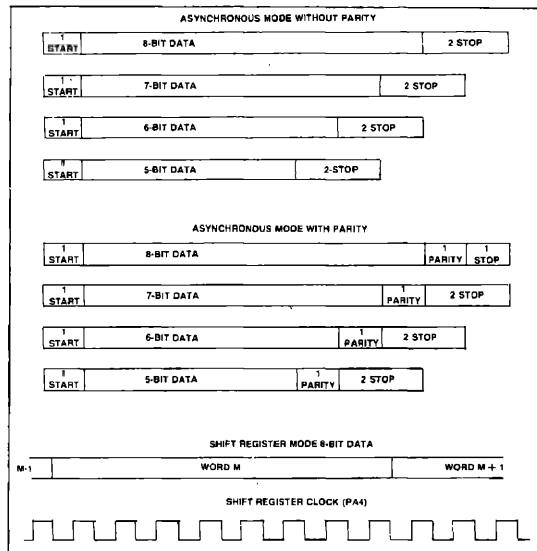


Figure 5-2. Transmitted Data Modes

In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter under-runs in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCSR5, SCSR6 and SCSR7.

$$IFR7 = SCSR6 (\overline{SCSR5} + SCSR7)$$

5.2 RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, appropriate number of data bits, a parity bit (if enabled) and one stop bit. Refer to paragraph 5.1 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits, and any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.

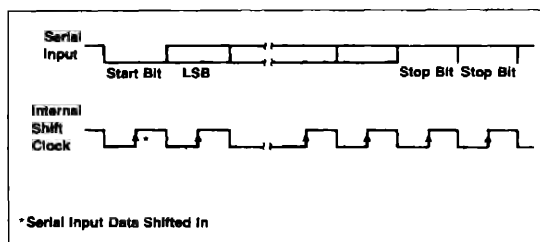


Figure 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.

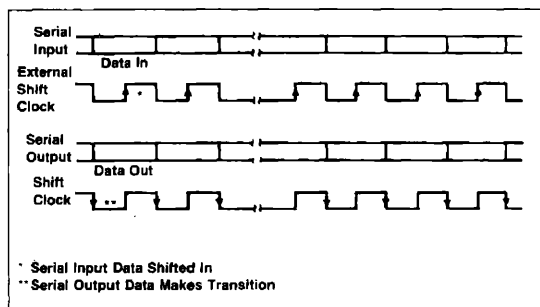


Figure 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR0: Receiver Data Register Full—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{\text{RES}}$ and is disabled if $\text{SCCR6} = 0$. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition, instead, a corresponding error bit will be set to a logic 1.

SCSR 1: Over-Run Error—Set to a logic 1 when a new character is transferred from the Receiver Shift Register, with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{\text{RES}}$.

SCSR 2: Parity Error—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the

received data has a parity error. This bit is cleared by reading the Receiver Data Register or by $\overline{\text{RES}}$.

SCSR 3: Framing Error—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by $\overline{\text{RES}}$. (ASYN Mode only).

SCSR 4: Wake-Up—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by $\overline{\text{RES}}$ or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR 5: End of Transmission—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by $\overline{\text{RES}}$ or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6: Transmitter Data Register Empty—Set to a logic 1 when the contents of the Transmitter Data Register is transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmitter Data Register. This bit is initialized to a logic 1 by $\overline{\text{RES}}$.

SCSR 7: Transmitter Under-Run—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register, or by $\overline{\text{RES}}$.

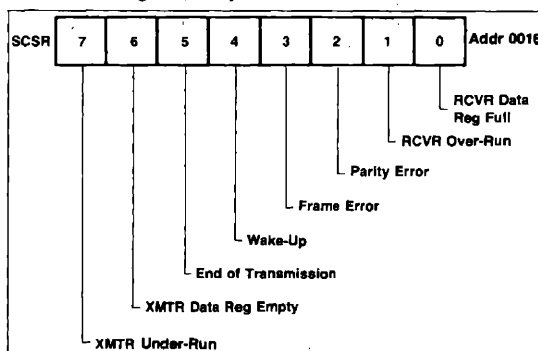


Figure 5-5. SCSR Bit Allocation

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of eleven consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6

COUNTER/TIMERS

The device contains two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A

- Pulse width measurement
- Pulse Generation
- Interval Timer
- Event Counter

Counter B

- Retriggerable Interval Counter
- Asymmetrical Pulse Generation
- Interval Timer
- Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either $\phi 2$ clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the

Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by RES.

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are $\phi 2$ clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a RES signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).
2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the $\phi 2$ clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore $1\mu s$ to 65.535 ms at the 1 MHz $\phi 2$ clock rate or $0.5\mu s$ to 32.767 ms at the 2 MHz $\phi 2$ clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting IRQ interrupt requests in the counter IRQ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an IRQ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the IRQ interrupt routine to determine that the IRQ was generated by the Counter A Underflow.

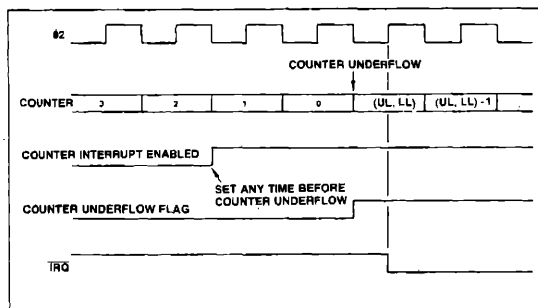


Figure 6-1. Interval Timer Timing Diagram

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs, or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

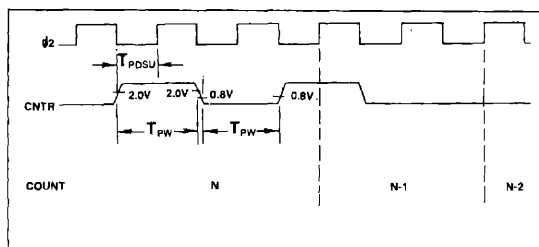


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the $\phi 2$ clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6.3.

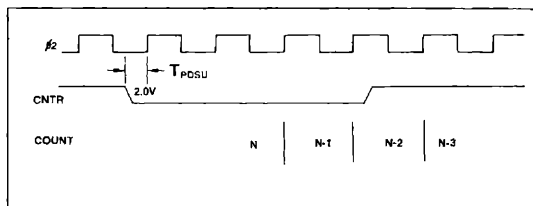


Figure 6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-1 identifies the values to be loaded in Counter A for selecting standard data rates with a $\phi 2$ clock rate of 1 MHz and 2 MHz. Although Table 6-1 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{16 \times \text{bps}} - 1$$

where

N = decimal value to be loaded into Counter A using its hexadecimal equivalent.

$\phi 2$ = the clock frequency (1 MHz or 2 MHz)

bps = the desired data rate.

NOTE

In Table 6-1 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-1 for those baud rates which fall outside this limit.

Table 6-1. Counter A Values for Baud Rate Selection

Standard Baud Rate	Hexadecimal Value		Actual Baud Rate At		Clock Rate Needed To Get Standard Baud Rate	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600.96	1.0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either $\phi 2$ clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by RES.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

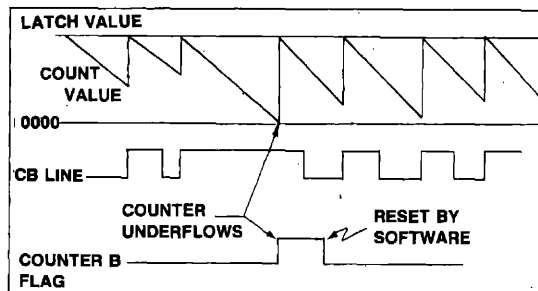


Figure 6-4. Counter B Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value which corresponds to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C, and the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.
2. The lower 8 bits of D are loaded into LLB by writing to address 001C, and the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and causes the CB output to go low as shown in Figure 6-5.
3. When the Counter B underflow occurs the contents of the Latch C is loaded into the Counter B, and the CB output toggles to a high level and stays high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

SECTION 7

POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER-ON TIMING

After application of V_{CC} and V_{RR} power to the R6500/11, \overline{RES} must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at $\phi 2$ (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

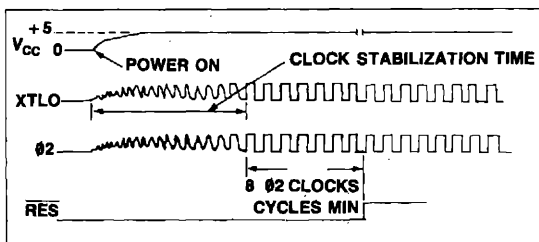


Figure 7-1. Power Turn-on Timing Detail

7.2 POWER-ON RESET

The occurrence of \overline{RES} going from low to high will cause the R6500/11 to set the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiate a reset vector fetch at address FFFC and FFFD to begin user program execution. All of the I/O ports (PA, PB, PC, PD) will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timers counter mode (mode 00) to be selected and causing all interrupt enabled bits to be reset.

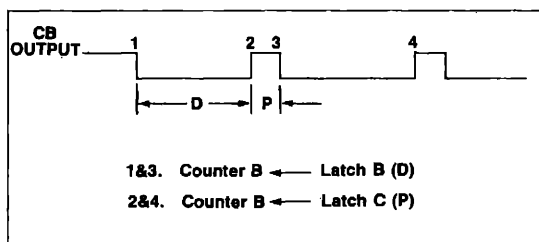


Figure 6-5. Counter B Pulse Generation

7.3 RESET (\overline{RES}) CONDITIONING

When \overline{RES} is driven from low to high the R6500/11 is put in a reset state causing the registers and I/O ports to be configured as shown in Table 7-1.

Table 7-1. \overline{RES} Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
Registers								
Processor Status	—	—	—	—	—	1	—	—
Mode Control (MCR)	0	0	0	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	0	0	0	0	0	0	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
Ports								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1
PC Latch	1	1	1	1	1	1	1	1
PD Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

7.4 INITIALIZATION

Any initialization process for the R6500/11 should include a \overline{RES} , as indicated in the preceding paragraphs. After stabilization of the internal clock (if a power on situation) an initialization subroutine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required
5. Clear Interrupts

A typical initialization subroutine could be as follows:

```
LDX    Load stack pointer starting address into X
        Register
TXS    Transfer X Register value to Stack Pointer
CLD    Clear Decimal Mode
SEC    Set Carry Flag
...    Set-up Mode Control and
...    special function
...    registers as required
CLI    Clear Interrupts
```

APPENDIX A

ENHANCED R6502 INSTRUCTION SET

This appendix contains a summary of the R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Document 29650 N30. The four instructions notated with a * are added instructions to enhance the standard 6502 instruction set.

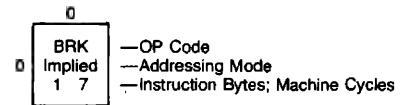
A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative	NOP	No Operation
*BBS	Branch on Bit Set Relative	ORA	"OR" Memory with Accumulator
BCC	Branch on Carry Clear		
BCS	Branch on Carry Set	PHA	Push Accumulator on Stack
BEQ	Branch on Result Zero	PHP	Push Processor Status on Stack
BIT	Test Bits in Memory with Accumulator	PLA	Pull Accumulator from Stack
BMI	Branch on Result Minus	PLP	Pull Processor Status from Stack
BNE	Branch on Result not Zero		
BPL	Branch on Result Plus	*RMB	Reset Memory Bit
BRK	Force Break	ROL	Rotate One Bit Left (Memory or Accumulator)
BVC	Branch on Overflow Clear	ROR	Rotate One Bit Right (Memory or Accumulator)
BVS	Branch on Overflow Set	RTI	Return from Interrupt
		RTS	Return from Subroutine
CLC	Clear Carry Flag		
CLD	Clear Decimal Mode	SBC	Subtract Memory from Accumulator with Borrow
CLI	Clear Interrupt Disable Bit	SEC	Set Carry Flag
CLV	Clear Overflow Flag	SED	Set Decimal Mode
CMP	Compare Memory and Accumulator	SEI	Set Interrupt Disable Status
CPX	Compare Memory and Index X	*SMB	Set Memory Bit
CPY	Compare Memory and Index Y	STA	Store Accumulator in Memory
		STX	Store Index X in Memory
DEC	Decrement Memory by One	STY	Store Index Y in Memory
DEX	Decrement Index X by One		
DEY	Decrement Index Y by One	TAX	Transfer Accumulator to Index X
		TAY	Transfer Accumulator to Index Y
EOR	"Exclusive-Or" Memory with Accumulator	TSX	Transfer Stack Pointer to Index X
		TXA	Transfer Index X to Accumulator
INC	Increment Memory by One	TXS	Transfer Index X to Stack Register
INX	Increment Index X by One	TYA	Transfer Index Y to Accumulator
INY	Increment Index Y by One		
JMP	Jump to New Location		
JSR	Jump to New Location Saving Return Address		

A6500/11 INSTRUCTION SET

[illegible]

A.3 INSTRUCTION CODE MATRIX



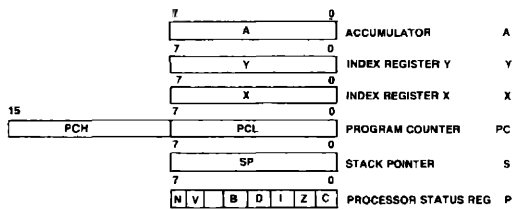
MSD	LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F		
0		BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2				ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1		BPL Relative 2 2**	ORA (IND, Y) 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*					ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2		JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2			BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3		BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*					AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4		RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2			JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5		BVC Relative 2 2**	EOR (IND, Y) 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*					EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6		RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2			JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7		BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*					ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8			STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2			STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBR8 ZP 3 5**	8
9		BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2				STA ABS, X 3 5		BBR9 ZP 3 5**	9
A		LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2			LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBR10 ZP 3 5**	A
B		BCS Relative 2 2**	LDA (IND, Y) 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2			LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBR11 ZP 3 5**	B
C		CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2			CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBR12 ZP 3 5**	C
D		BNE Relative 2 2**	CMP (IND, Y) 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*					CMP ABS, X 3 4*	DEC ABS, X 3 7	BBR13 ZP 3 5**	D
E		CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2			CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBR14 ZP 3 5**	E
F		BEQ Relative 2 2**	SBC (IND, Y) 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*					SBC ABS, X 3 4*	INC ABS, X 3 7	BBR15 ZP 3 5**	F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F		

*Add 1 to N if page boundary is crossed.

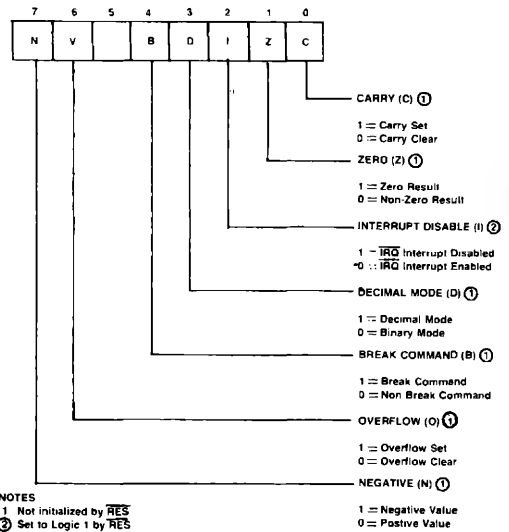
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

APPENDIX B

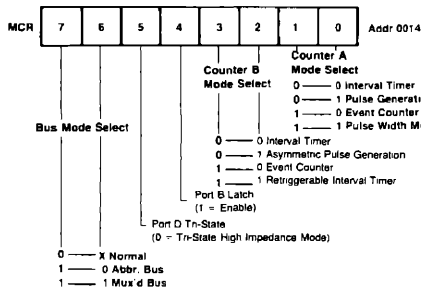
KEY REGISTER SUMMARY



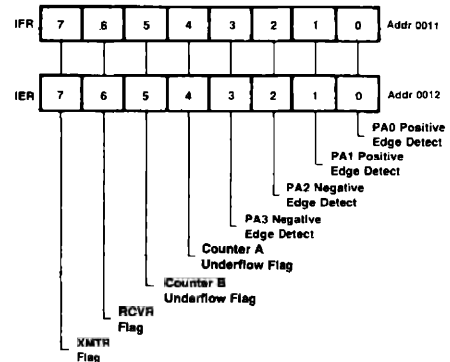
CPU Registers



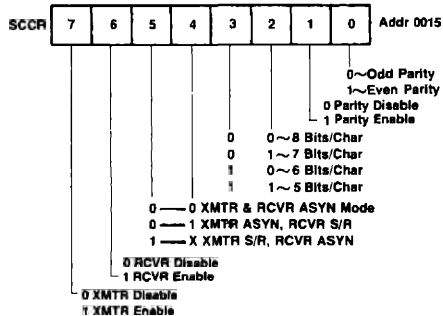
Processor Status Register



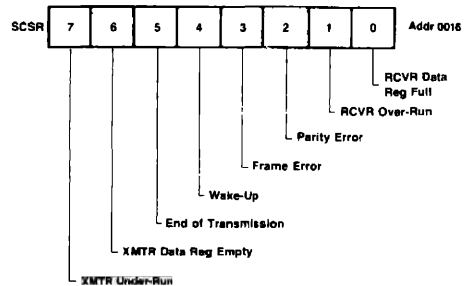
Mode Control Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



Serial Communications Status Register

APPENDIX C

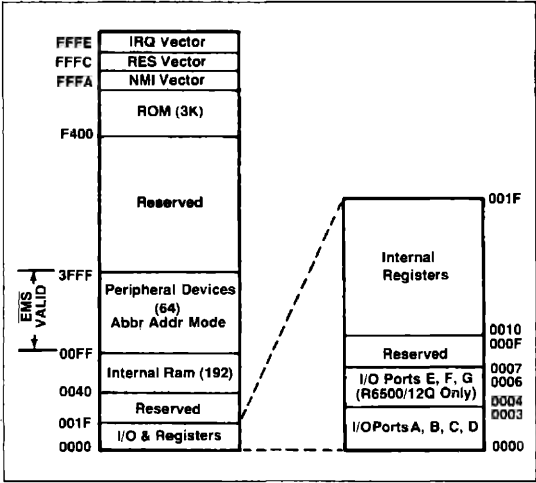
ADDRESS ASSIGNMENTS/MEMORY MAPS/PIN FUNCTIONS

C.1 I/O AND INTERNAL REGISTER ADDRESSES

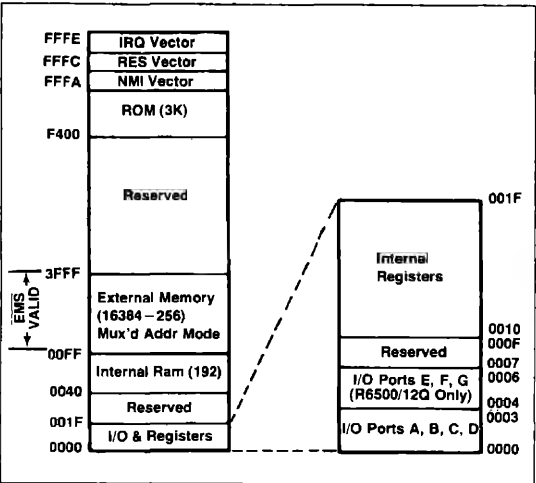
ADDRESS (HEX)	READ	WRITE
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B.
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
0010	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
0F	— —	— —
0E	— —	— —
0D	— —	— —
0C	— —	— —
0B	— —	— —
0A	— —	— —
09	— —	— —
08	— —	— —
07	— —	— —
06	Port G*	Port G*
05	Port F*	Port F*
04	Port E*	Port E*
03	Port D	Port D
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

NOTE: *R6500/12Q Only

C.2 ABBREVIATED MODE
MEMORY MAP



C.3 MULTIPLEXED MODE
MEMORY MAP



C.4 MULTIPLE FUNCTION PIN ASSIGNMENTS—PORT C AND PORT D

PIN NUMBER	I/O PORT FUNCTION	ABBREVIATED PORT FUNCTION	MULTIPLEXED PORT FUNCTION
4	PC0	A0	A0
5	PC1	A1	A1
6	PC2	A2	A2
7	PC3	A3	A3
8	PC4	A12	A12
9	PC5	R/W	R/W
10	PC6	A13	A13
11	PC7	EMS	EMS
19	PD0	D0	A4/D0
18	PD1	D1	A5/D1
17	PD2	D2	A6/D2
16	PD3	D3	A7/D3
15	PD4	D4	A8/D4
14	PD5	D5	A9/D5
13	PD6	D6	A10/D6
12	PD7	D7	A11/D7

APPENDIX D

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Commercial	T	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

($V_{CC} = 5V \pm 5\%$, $V_{SS} = 0$, $T_A = 0$ to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Dissipation (Outputs High) Commercial @ 25°C	P_D	—	—	1200	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial @ 25°C	I_{RR}	—	4	—	mAdc
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI and $\emptyset 2$ in Slave Option)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	—	+0.8	Vdc
Input Leakage Current (RES, NMI) $V_{in} = 0$ to 5.0 Vdc	I_{IN}	—	—	± 10.0	μAdc
Input Low Current PA, PB, PC, PD, PF*, and PG* ($V_{IL} = 0.4$ Vdc)	I_{IL}	—	-1.0	-1.6	mAdc
Output High Voltage (Except XTLO) ($I_{LOAD} = .100$ μAdc)	V_{OH}	+2.4	—	V_{CC}	Vdc
Output Low Voltage ($I_{LOAD} = 1.6$ mAdc)	V_{OL}	—	—	+0.4	Vdc
Darlington Current Drive, PE* ($V_O = 1.5$ Vdc)	I_{OH}	-1.0	—	—	mAdc
Input Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz) PA, PB, PC, PD, PF*, and PG* XTLI, XTLO	C_{in}	—	—	10 50	pF
I/O Port Pull-Up Resistance PA0-PA7, PB0-PB7, PC0-PC7, PF0-PF7 & PG0-PG7	R_L	3.0	6.0	11.5	K Ω
Output Leakage Current Tri-State I/Os while in High Impedance State	I_{OUT}	—	—	± 10	μAdc
Output Capacitance Tri-State I/Os while in High Impedance State $V_{IN} = 0V$, $T_A = 25^\circ\text{C}$, $f = 25^\circ\text{C}$, $f = 1.0$ MHz	C_{OUT}	—	—	10	pF
Note: Negative sign Indicates outward current flow, positive indicates inward flow.					*R6500/12Q only.

APPENDIX E

TIMING REQUIREMENTS AND CHARACTERISTICS

E.1 GENERAL NOTES

1. $V_{CC} = 5V \pm 5\%$, $0^{\circ}C \leq TA \leq 70^{\circ}C$
2. A valid $V_{CC} - \overline{RES}$ sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pf maximum, except as noted below:
- PA, PB

PC (I/O Modes Only)

PC (ABB and Mux Mode)

PC6, PC7 (Full Address Mode)

— 50pf maximum

— 50pf maximum

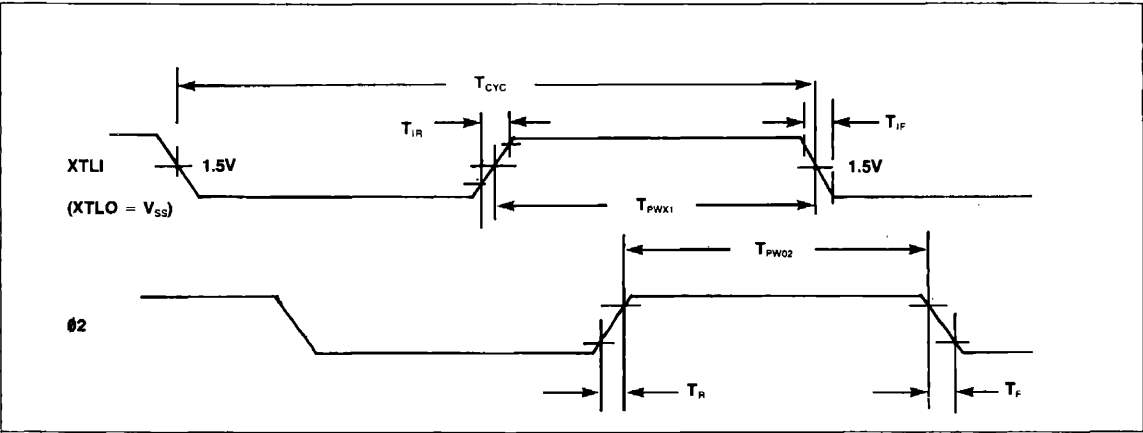
— 130pf maximum

— 130pf maximum

E.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 \pm 25	—	250 \pm 10	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1}	$T_{PWX1} \pm 25$	T_{PWX1}	$T_{PWX1} \pm 20$
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10

3



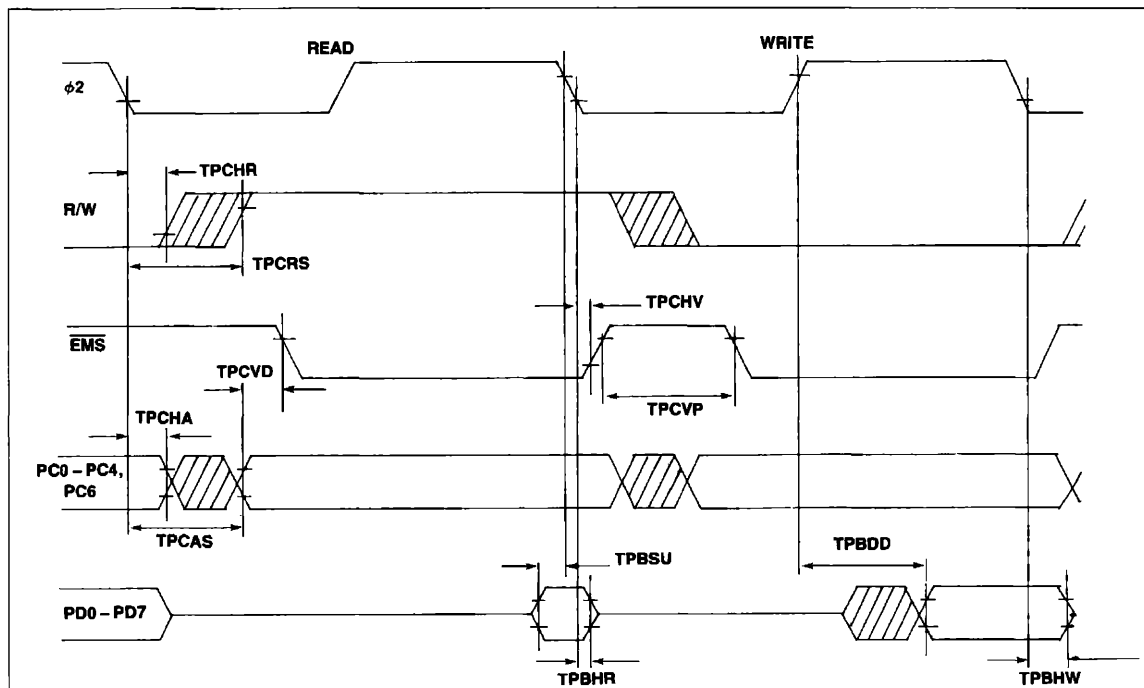
E.3 ABBREVIATED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 0, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	200	—	140
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	130
T_{PCHA}	(PC0-PC4, PC6) Address Hold Time	30	—	30	—
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) EMS Hold Time	10	—	10	—
$T_{PCVD}^{(1)}$	(PC7) Address to EMS Delay Time	30	220	30	130
T_{PCVP}	(PC7) EMS Stabilization Time	30	—	30	—

NOTE 1: Values assume PC0-PC4, PC6 and PC7 have the same capacitive load.

E.3.1 Abbreviated Mode Timing Diagram



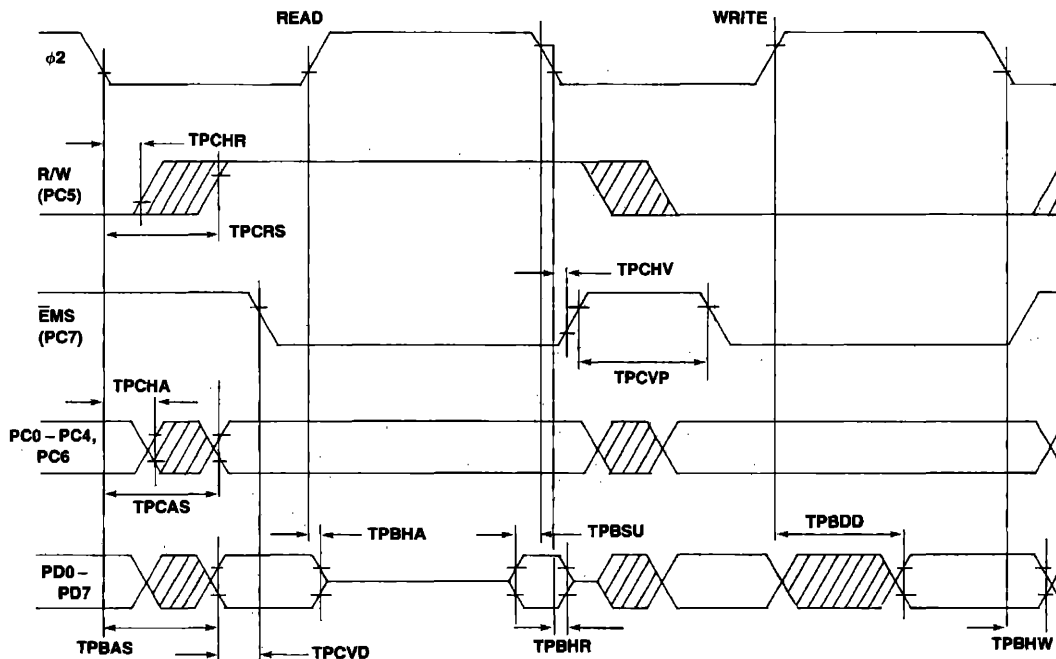
E.4 MULTIPLEXED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0–PC4, PC6) Address Setup Time	—	200	—	140
T_{PBAS}	(PD) Address Setup Time	—	220	—	120
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	140
T_{PCHA}	(PC0–PC4, PC6) Address Hold Time	30	—	30	—
T_{PBHA}	(PD) Address Hold Time	40	100	40	80
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) \overline{EMS} Hold Time	10	—	10	—
$T_{PCVD}^{(1)}$	(PC7) Address to \overline{EMS} Delay Time	30	200	30	150
T_{PCVP}	(PC7) \overline{EMS} Stabilization Time	30	—	30	—

NOTE 1: Values assume PD0–PD7 and PC7 have the same capacitive load.

E.4.1 Multiplex Mode Timing Diagram

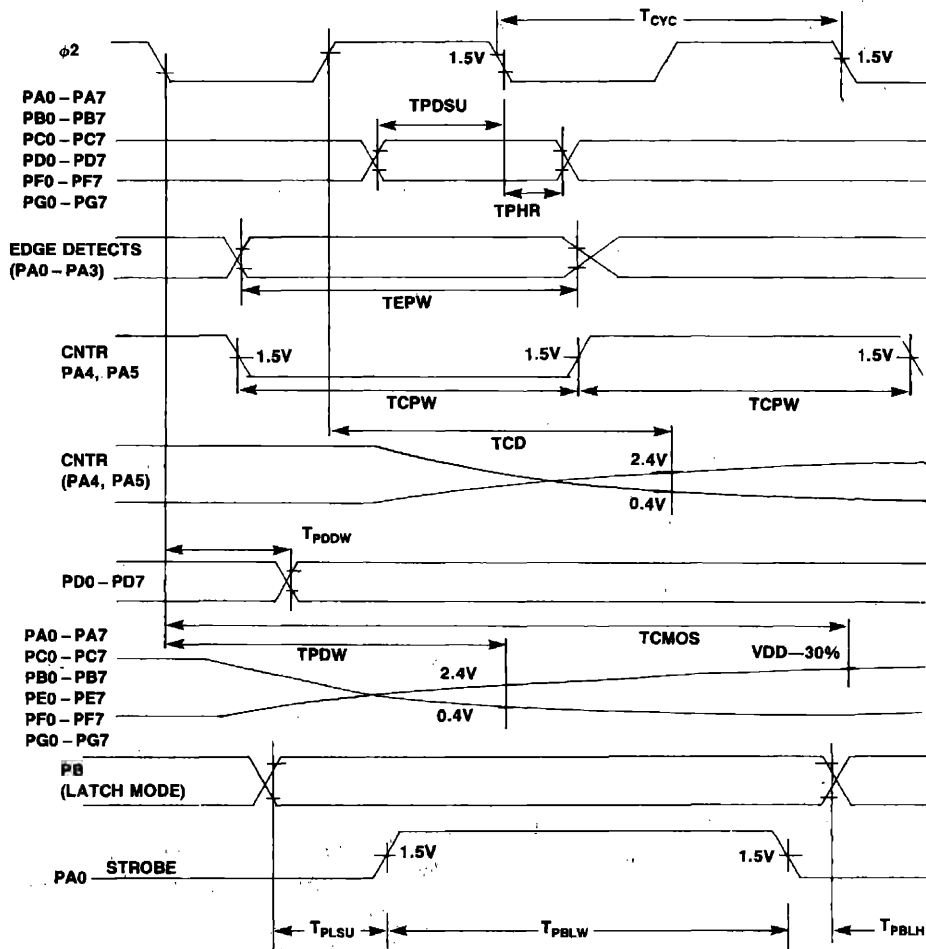


E.5 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
$T_{PDW}^{(1)}$	Internal Write to Peripheral Data Valid PA, PB, PC, PE, PF, PG, TTL	—	500	—	500
$T_{CMOS}^{(1)}$	PA, PB, PC, PE, PF, PG, CMOS	—	1000	—	1000
T_{PDDW}	PD	—	175	—	150
T_{PDSU}	Peripheral Data Setup Time PA, PB, PC, PF, PG	200	—	200	—
T_{PDSU}	PD	50	—	50	—
T_{PHR}	Peripheral Data Hold Time PA, PB, PC, PF, PG	75	—	75	—
T_{PHR}	PD	10	—	10	—
T_{EPW}	PA0-PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CPW}	Counters A and B PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
$T_{CD}^{(1)}$	PA4, PA5 Output Delay	—	500	—	500
T_{PBLW}	Port B Latch Mode PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PB Data Setup Time	175	—	150	—
T_{PBLH}	PB Data Hold Time	30	—	30	—
$T_{PDW}^{(1)}$	Serial I/O PA6 XMTR TTL	—	500	—	500
$T_{CMOS}^{(1)}$	PA6 XMTR CMOS	—	1000	—	1000
T_{CPW}	PA4 RCVR S/R Clock Width	$4 T_{CYC}$	—	$4 T_{CYC}$	—
$T_{PDW}^{(1)}$	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
$T_{CMOS}^{(1)}$	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

NOTE 1: Maximum Load Capacitance: 50pF Passive Pull-Up Required

E.5.1 I/O, Edge Detect, Counter, and Serial I/O Timing





R65/11EB AND R65/11EAB BACKPACK EMULATORS

INTRODUCTION

The Rockwell R65/11EB and R65/11EAB Backpack Emulator is the PROM prototyping version of the 8-bit, masked-ROM R6500/11 one-chip microcomputer. Like the R6500/11, the backpack device is totally upward/downward compatible with all members of the R6500/11 family. It is designed to accept standard 5-volt, 24-pin EPROMs or ROMs directly, in a socket on top of the Emulator. This packaging concept allows a standard EPROM to be easily removed, re-programmed, then reinserted as often as desired.

The backpack devices have the same pinouts as the masked-ROM R6500/11 microcomputer. These 40 pins are functionally and operationally identical to the pins on the R6500/11. The R6500/11 Microcomputer Product Description (Rockwell Document No. 29651N23, Order No. 2119) includes a description of the interface signals and their functions. Whereas the masked-ROM R6500/11 provides 3K bytes of read-only memory, the R65/11EB will address 4K bytes of external program memory. This extra memory accommodates program patches, test programs or optional programs during breadboard and prototype development states.

ORDERING INFORMATION

Backpack Emulator

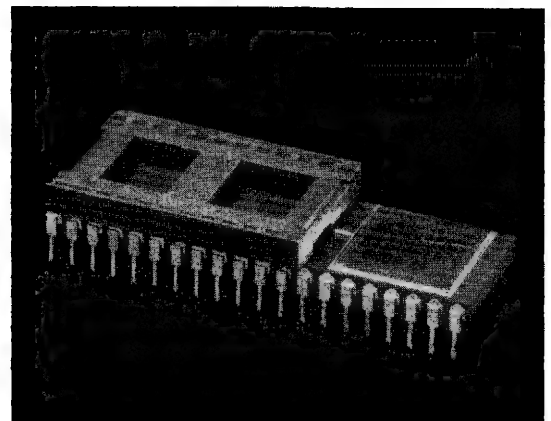
Part Number	Memory Capacity	Compatible Memories	Temperature Range and Speed
R65/11EB	4K × 8	2732	0°C to 70°C 1MHz
R65/11EAB	4K × 8	2732A	0°C to 70°C 2 MHz

Support Products

Part Number	Description
S65-101	SYSTEM 65 Microcomputer Development System
M65-040	PROM Programmer Module
M65-131	1-MHz R6500/11 Personality Module
M65-132	2-MHz R6500/11 Personality Module
RDC-1001	Rockwell Design Center
RDC-101	1 MHz R6500/11P Personality Module (RDC)
RDC-102	2 MHz R6500/11AP Personality Module (RDC)

FEATURES

- PROM version of the R6500/11
- Completely pin compatible with R6500/11 single-chip microcomputers
- Profile approaches 40-pin DIP of R6500/11
- Accepts 5 volt, 24-pin industry-standard EPROMs —4K memories—2732, 2732A (4K bytes addressable)
- Use as prototyping tool or for low volume production
- 4K bytes of memory capacity
- 192 × 8 static RAM
- Separate power pin for 32 bytes of RAM
- Software compatibility with the R6500 family
- 32 bi-directional TTL compatible I/O lines (4 ports)
- Two 16 bit programmable counter/latches with six modes (interval timer, pulse generator, event counter, pulse width measurement, asymmetrical pulse generator, and retriggerable interval timer)
- 10 interrupts (reset, non-maskable, four external edge sensitive, 2 counters, serial data received, serial data transmitted).
- Crystal or external time base
- Single +5V power supply



R65/11EB Backpack Emulator

CONFIGURATIONS

The Backpack Emulator is available in two different versions, to accommodate 1 MHz and 2 MHz speeds. Both versions provide 192 bytes of RAM and I/O, as well as 24 signals to support the external memory "backpack" socket.

The emulator will relocate the EPROM address space to FXXX (see Memory Map). EPROM addresses FFA through FFF must contain the interrupt vectors.

EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock—the RC option of the R6500/11 is not available in the emulator device. The R65/11EB and R65/11EAB divide the input clock by two regardless of the source.

I/O PORT PULLUPS

The devices have internal I/O port pullup resistors on ports A, B, & C. Port D has push-pull drivers.

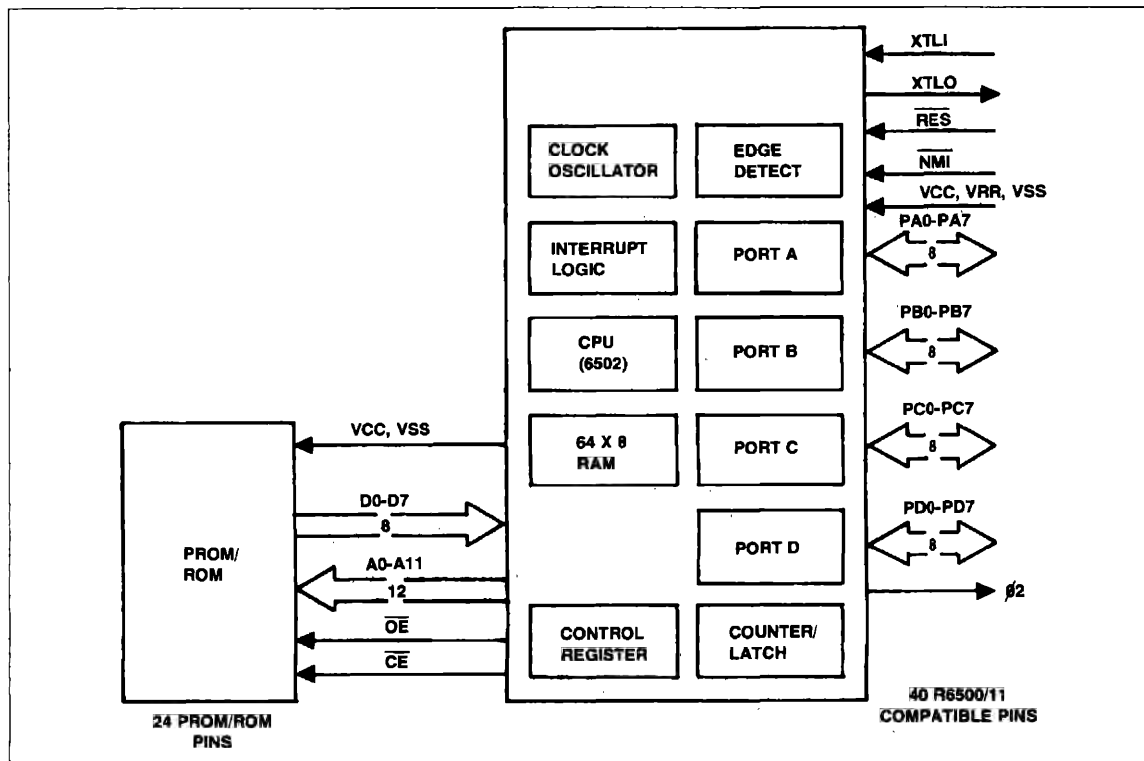
PRODUCT SUPPORT

The Backpack Emulator is just one of the products that Rockwell offers to facilitate system and program development for the R6500/11.

The SYSTEM 65 Microcomputer Development System with R6500/11 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/11 Personality Module allows total system test and evaluation. With the optional PROM Programmer, SYSTEM 65 can also be used to program EPROMs for the development activity. When PROM programs have been finalized, the PROM device can be sent to Rockwell for masking into the 3K ROM of the R6500/11.

In addition to support products, Rockwell offers regularly-scheduled designer courses at regional centers.

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R65/11EB Interface Diagram

XTLO	1	A7	1s	24s	V _{CC}	40	V _{SS}
XTLI	2	A6	2s	23s	A8	39	V _{RR}
β 2	3	A5	3s	22s	A9	38	PB0
PC0	4	A4	4s	21s	A11	37	PB1
PC1	5	A3	5s	20s	OE	36	PB2
PC2	6	A2	6s	19s	A10	35	PB3
PC3	7	A1	7s	18s	CE	34	PB4
PC4	8	A0	8s	17s	D7	33	PB5
PC5	9	D0	9s	16s	D6	32	PB6
PC6	10	D1	10s	15s	D5	31	PB7
PC7	11	D2	11s	14s	D4	30	PA0
PD7	12	V _{SS}	12s	13s	D3	29	PA1
PD6	13	24-PIN SOCKET				28	PA2
PD5	14					27	PA3
PD4	15					26	PA4
PD3	16					25	PA5
PD2	17					24	PA6
PD1	18					23	PA7
PD0	19					22	NMI
RES	20					21	V _{CC}

Pin Configuration

BACKPACK MEMORY SIGNAL DESCRIPTION

Signal Name	Pin No.	Description
D0-D7	9S-11S, 13S-17S	Data Bus Lines. All instruction and data transfers take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.
A0-A7, A8, A9, A10, A11	1S-8S, 23S, 24S, 19S, 21S	Address Bus Lines. The address bus lines are buffered by push/pull type drivers that can drive one standard TTL load.
CE	18S	Chip Enable. \overline{CE} is active when the address is 8000-FFFF. This line can drive one TTL load.
OE	20S	Memory Enable Line. This signal provides the output enable for the memory to place information on the data bus lines. This signal is driven by an inverted R/W signal from the CPU. It can drive 1 TTL load.
V _{CC}	24S	Main Power Supply +5V. This pin is tied directly to pin 21 (V _{CC}).
V _{SS}	12S	Signal and Power Ground (zero volts). This pin is tied directly to pin 40 (V _{SS}).

I/O AND INTERNAL REGISTER ADDRESSES

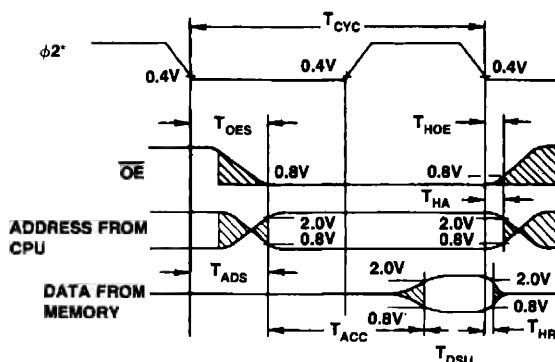
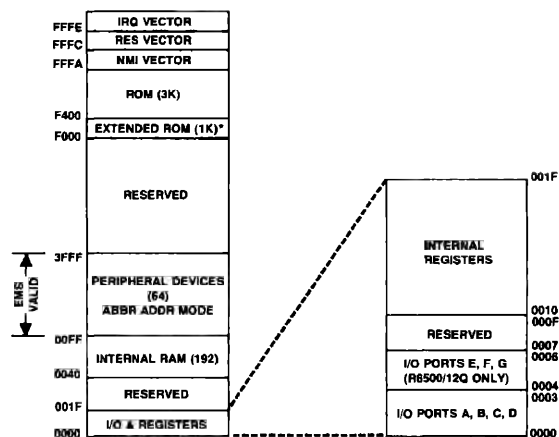
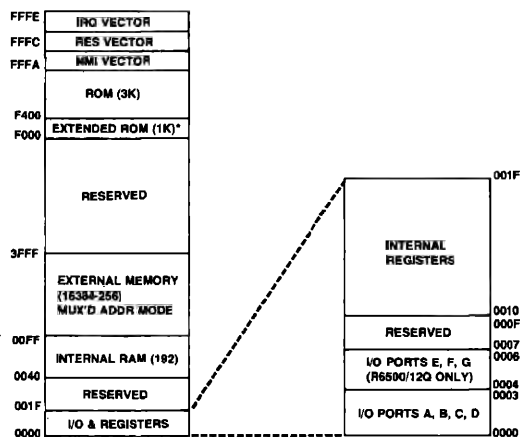
Address (Hex)	Read	Write
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
0010	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
04 thru 0F	— —	— —
03	Port D	Port D
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

READ TIMING CHARACTERISTICS

Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
\overline{OE} and \overline{CE} setup time from CPU	T_{OES}	—	225	—	140	ns
Address setup time from CPU	T_{ADS}	—	225	—	140	ns
Memory read access time	T_{ACC}	—	700	—	315	ns
Data set up time	T_{DSU}	50	—	35	—	ns
Data hold time—Read	T_{HR}	10	—	10	—	ns
Address hold time	T_{HA}	30	—	30	—	ns
\overline{OE} and \overline{CE} hold time	T_{HOE}	30	—	30	—	ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μs

3

READ TIMING WAVEFORMS

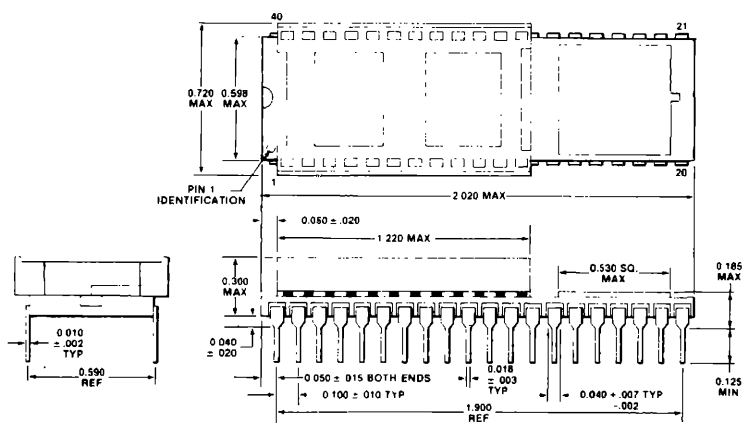
ABBREVIATED MODE
MEMORY MAPMULTIPLEXED MODE
MEMORY MAP

*NOT AVAILABLE FOR MASKED ROM R6500/11.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ± 5%, V_{SS} = 0, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Threshold Voltage D0-D7	V _{IHT}	V _{SS} + 2.0	—	—	Vdc
Input Low Threshold Voltage D0-D7	V _{ILT}	—	—	V _{SS} + 0.8	Vdc
Three-State (Off State) Input Current (V = 0.4 to 2.4V, V _{CC} = 5.25V) D0-D7	I _{TSI}	—	—	± 10	μA
Output High Voltage (I _{LOAD} = 100μA dc, V _{CC} = 4.75V) D0-D7, A0-A11, \overline{OE} , \overline{CE}	V _{OH}	V _{SS} + 2.4	—	—	Vdc
Output Low Voltage (I _{LOAD} = 1.6 mA dc, V _{CC} = 4.75V) D0-D7, A0-A11, \overline{OE} , \overline{CE}	V _{OL}	—	—	V _{SS} + 0.4	Vdc
Power Dissipation (less EPROM)	P _D	—	0.80	1.20	W
Capacitance (V _{in} = 0, T _A = 25°C, f = 1 MHz) D0-D7 (High Impedance State) Input Capacitance	C C _{out} C _{in}	— — —	— — —	10 10	pF
I/O Port Pull-up Resistance	R _L	3.0	6.0	11.5	kohm



40-Pin Backpack Package



R6500/13 and R6511Q ONE-CHIP MICROCOMPUTER and ONE-CHIP MICROPROCESSOR

SECTION 1 INTRODUCTION

3

1.1 FEATURES

- Enhanced 6502 CPU
 - Four new bit manipulation instructions
 - Set Memory Bit (SMB)
 - Reset Memory Bit (RMB)
 - Branch on Bit Set (BBS)
 - Branch on Bit Reset (BBR)
 - Decimal and binary arithmetic modes
 - 13 addressing modes
 - True indexing
- 256-byte mask-programmable ROM or no ROM*
- 192-byte static RAM
- 32 bidirectional, TTL-compatible I/O lines (four ports)
- One 8-bit port may be tri-stated under software control
- One 8-bit port may have latched inputs under software control
- Two 16-bit programmable counter/timers, with latches
 - Pulse width measurement
 - Asymmetrical pulse generation
 - Pulse generation
 - Interval timer
 - Event counter
 - Retriggerable interval timer
- Serial port
 - Full-duplex asynchronous operation mode
 - Selectable 5- to 8-bit characters
 - Wake-up feature
 - Synchronous shift register mode
 - Standard programmable bit rates programmable up to 62.5K bits/sec @ 1 MHz
- Ten interrupts
 - Four edge-sensitive lines; two positive, two negative
 - Reset
 - Non-maskable
 - Two counter underflows
 - Serial data received
 - Serial data transmitted
- Bus expandable to 64K bytes of external memory

*R6511Q has no ROM.

- Flexible clock circuitry
 - 2-MHz or 1-MHz internal operation
 - Internal clock with external XTAL at two or four times internal frequency
 - External clock input divided by one, two or four
- 1 μ s minimum instruction execution time @ 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- 64-pin QUIP

NOTE

This document uses the term R6500/13 to describe both parts. See section 1.3 for a description of the options available when using the R6500/13 and the fixed features of the R6511Q.

1.2 SUMMARY

The Rockwell R6500/13 is a complete, high-performance 8-bit NMOS-3 microcomputer on a single chip and is compatible with all members of the R6500 family.

The R6500/13 consists of an enhanced 6502 CPU, an internal clock oscillator, an optional 256 bytes of Read-Only Memory, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the R6500/13 a leading candidate for microcomputer applications.

The R6511Q contains all the features of the R6500/13 except it has no ROM and is thus intended as a high feature microprocessor with full 65K address bus.

R6511Q Microprocessor and R6500/13 Microcomputer

To allow prototype circuit development, Rockwell offers a PROM-compatible 64-pin extended microprocessor device. This device, the R6511Q, provides all R6500/11 interface lines, plus the address bus, data bus and control lines to interface with external memory. The R6511Q also can be used to emulate the R6500/13. With the addition of external circuits it can also emulate the R6500/12.

Rockwell supports development of the R6500/13 with the System 65 Microcomputer Development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This product description assumes that the reader is familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Number 29650N31). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Document Number 29650N30).

1.3 CUSTOMER OPTIONS

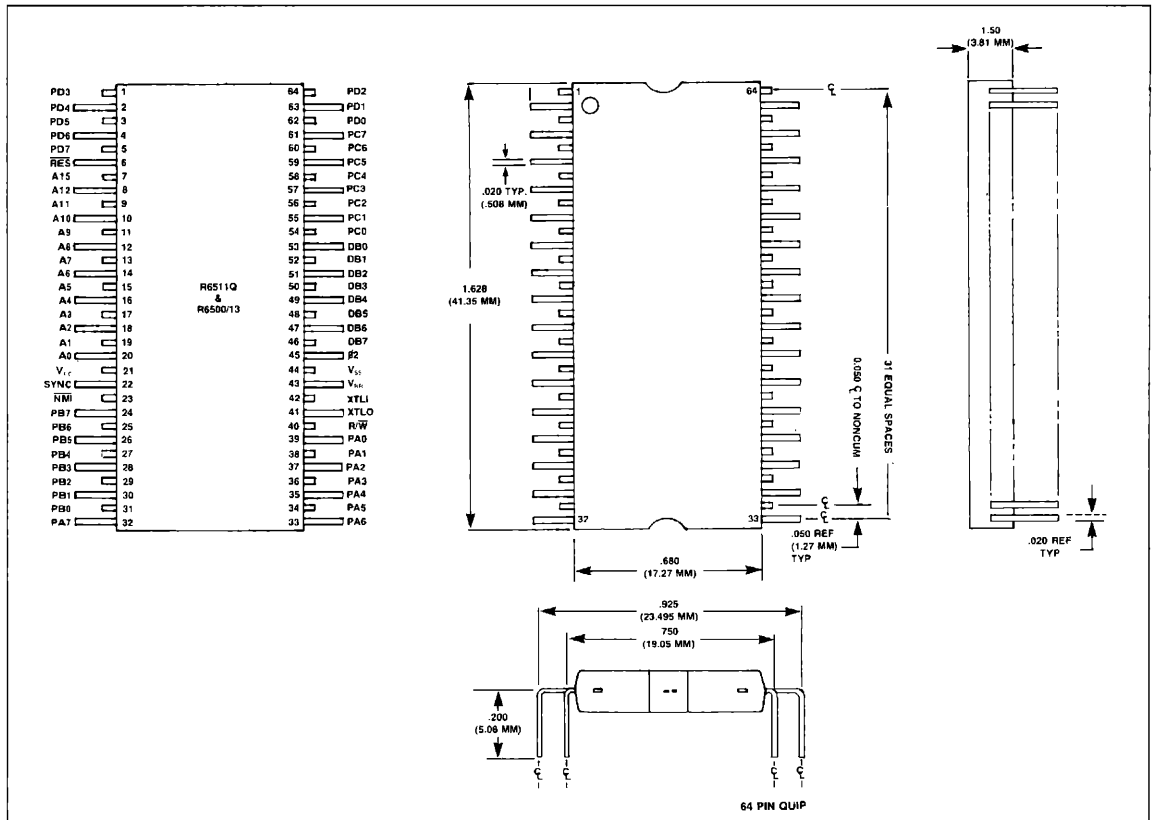
The R6500/13 microcomputer is available with the following customer specified mask options.

- Option 1 Crystal or RC oscillator
- Option 2 Clock divide by 2 or 4
- Option 3 Clock MASTER Mode or SLAVE Mode
- Option 4 with or without a 256 byte ROM
- Option 5 Reset Vector at FFFC or 7FFF
- Option 6 Port A with or without internal pull-up resistors
- Option 7 Port B with or without internal pull-up resistors
- Option 8 Port C with or without internal pull-up resistors

All options should be specified on an R6500/13 order form.

The R6511Q has no customer specified mask options. It has the following characteristics.

- Crystal Oscillator
- Clock Divide by 2
- Clock MASTER Mode
- Without ROM
- Reset Vector at FFFC
- No internal pull-up resistors or any Port (PA, PB, or PC)



SECTION 2

R6511Q AND R6500/13 INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6511Q and R6500/13. Figure 2-1 and 2-2 show the Interface Diagram and the pin out configuration for both devices. Table 2-1 describes the function of each pin. Figure 3-1 has a detailed block diagram of the R6500/13 ports which illustrates the internal function of the device.

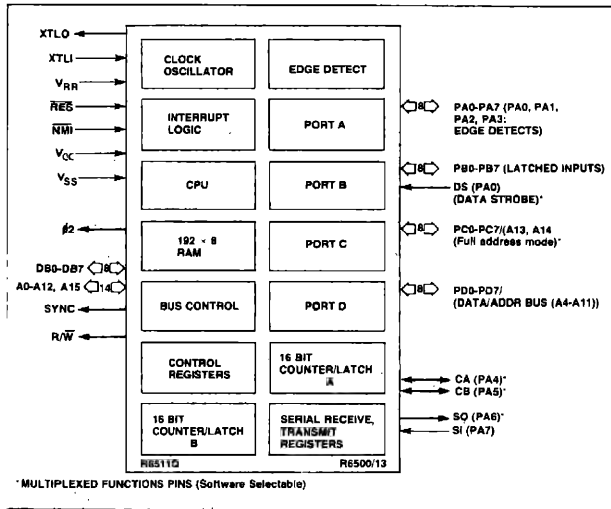


Figure 2-2. Interface Diagram

Table 2-1. R6500/13 Pin Descriptions

Signal Name	Pin No.	Description
V _{CC}	21	Main power supply +5V
V _{RR}	43	Separate power pin for RAM. In the event that V _{CC} power is off, this power retains RAM data.
V _{SS}	44	Signal and power ground (0V)
XTLO	42	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to V _{SS} , or X2 or X4 clock if XTLO is floated.
XTLO	41	Crystal output from internal clock oscillator.
RES	6	The Reset input is used to initialize the device. This signal must not transition from low to high for at least eight cycles after V _{CC} reaches operating range and the internal oscillator has stabilized.
#2	45	Clock signal output at internal frequency.
NMI	23	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated with the CPU.
PA0-PA7	39-32	Four 8-bit ports used for either input/output. Each line of Ports A, B and C consists of an active transistor to V _{SS} and an optional passive pull-up to V _{CC} . In the abbreviated or multiplexed modes of operation Port C has an active pull-up transistor. Port D functions as either an 8-bit input or 8-bit output port. It has active pull-up and pull-down transistors.
PB0-PB7	31-24	
PC0-PC7	54-61	
PD0-PD7	62-64, 1-5	
A0-A12, A15	20-7	Fourteen address lines used to address a complete 65K external address space. Note: A13 & A14 are sourced through PC6 & PC7 when in the Full Address Mode.
DB0-DB7	53-46	Eight bidirectional data bus lines used to transmit data to and from external memory.
SYNC	22	SYNC is a positive going signal for the full clock cycle whenever the CPU is performing an OP CODE fetch.
R/W	40	Controls the direction of data transfer between the CPU and the external 65K address space. The signal is high when reading and low when writing.

SECTION 3 SYSTEM ARCHITECTURE

This section provides a functional description of the R6500/13. Functionally the R6500/13 consists of a CPU, both RAM and optional ROM memories, four 8-bit parallel I/O ports, a serial I/O port, dual counter/latch circuits, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The R6500/13 internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address and modifies the address from memory by adding the Index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal \overline{IRQ} interrupt, or the external interrupt line \overline{NMI} . The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may be accessed only from the top. The address of a memory

location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Arithmetic And Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.5 Program Counter

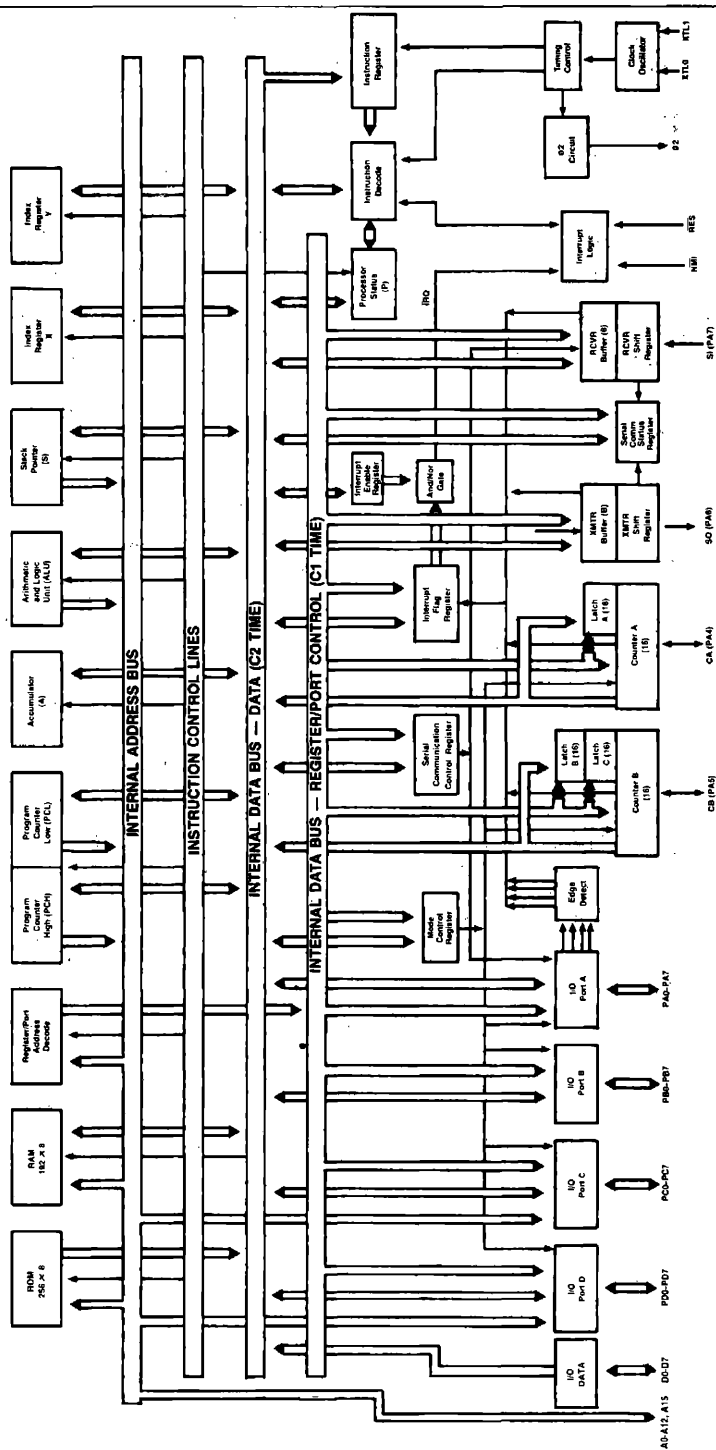
The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the internal Data Bus. These instructions are latched into the Instruction Register, then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.



3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; RES, NMI and IRQ. IRQ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 NEW INSTRUCTIONS

In addition to the standard R6502 instruction set, four new bit manipulation instructions have been added to the R6500/13. The added instructions and their format are explained in the following paragraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions. The four added instructions do not impact the CPU processor status register.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and one of eight bits to be set. The second byte of the instruction designates address (0-255) of the byte to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch On Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of eight bits designated by a 3-bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8-bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

3.3 READ-ONLY-MEMORY (ROM)

The optional ROM consists of 256 bytes mask programmable memory with an address space from 7F00 to 7FFF. ROM locations FFFA to FFFF are assigned for interrupt vectors. The reset vector can be optionally at 7FFE or FFFC.

The R6511Q has no ROM and its Reset vector is at FFFC.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R6500/13 provides a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC} . During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC} , V_{RR} must be supplied within operating range and RES must be driven low at least eight $\phi 2$ clock pulses before V_{CC} falls out of operating range. RES must then be held low while V_{CC} is out of operating range and until at least eight $\phi 2$ clock cycles after V_{CC} is again within operating range and the internal $\phi 2$ oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3-2 shows typical waveforms.

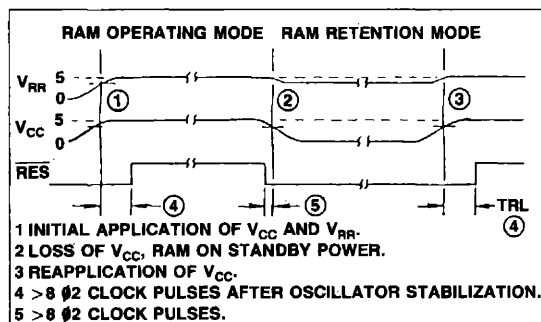


Figure 3-2. Data Retention Timing

R6511Q Microprocessor and R6500/13 Microcomputer

3.5 CLOCK OSCILLATOR

The R6511Q has been configured for a crystal oscillator, a divide by 2 countdown network, and for Master Mode Operation.

Three customer selectable mask options are available for controlling the R6500/13 timing. The R6500/13 can be ordered with a crystal or RC oscillator, a divide by 2 or divide by 4 countdown network and for clock master mode or clock slave mode operation.

For 2MHz interval operation the divide-by-2 options must be specified.

A reference frequency can be generated with the on-chip oscillator using either an external crystal or an external resistor depending on the mask option selected. The oscillator reference frequency passes through an internal countdown network (divide by 2 or divide by 4 option) to obtain the internal operating frequency (see Figures 3-3a and 3-3b). The external crystal generated reference frequency is a preferred method since the resistor method can have tolerances approaching 50%.

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 3-3c shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO

is tied to V_{SS} , the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

The operation escribed above assumed a CLOCK MASTER MODE mask option. In this mode a frequency source (crystal, RC network, or external source) must be applied to the XTLI and XTLO pins.

Note:

When operating at a 1 MHz internal frequency place a 15-22 pf capacitor between XTLO and GND.

$\phi 2$ is a buffered output signal which closely approximates the internal timing. When a common external source is used to drive multiple devices the internal timing between devices as well as their $\phi 2$ outputs will be skewed in time. If skewing represents a system problem it can be avoided by the Master/Slave connection and options shown in Figure 3-4.

One R6500/13 is operated in the CLOCK MASTER MODE and a second in the CLOCK SLAVE MODE. Mask options in the SLAVE unit convert to $\phi 2$ signal into a clock input pin which is tightly coupled to the internal timing generator. As a result the internal timing of the MASTER and SLAVE units are synchronized with minimum skew. If the $\phi 2$ signal to the SLAVE unit is inverted, the MASTER and SLAVE UNITS WILL OPERATE OUT OF PHASE. This approach allows the two devices to share external memory using cycle stealing techniques.

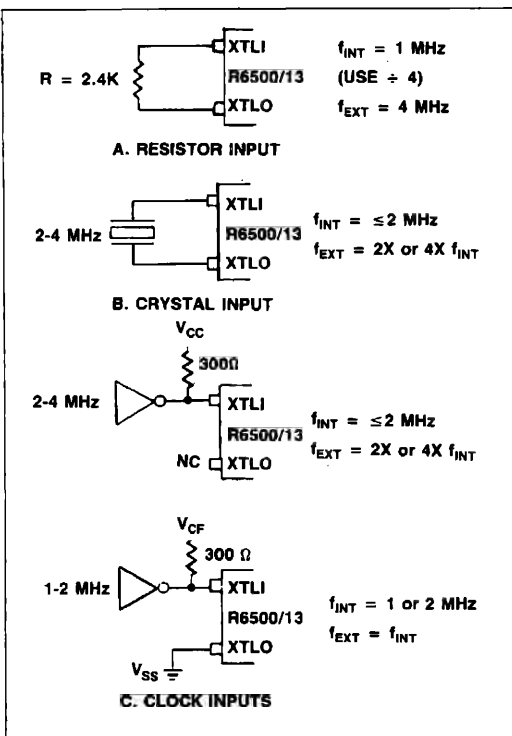


Figure 3-3. Clock Oscillator Input Options

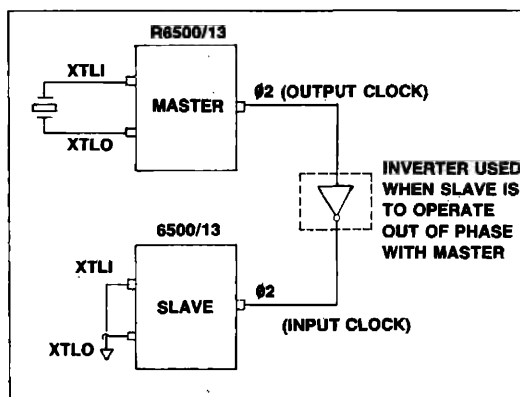


Figure 3-4. Master/Slave Connections

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the R6500/13 in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-5.

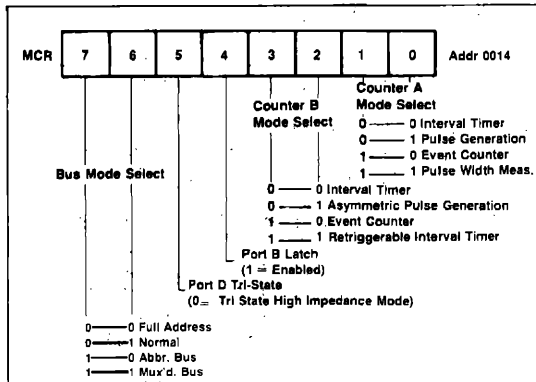


Figure 3-5. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4.

The use of Port D in Tri-State Enable is shown in Section 4.6.

The use of Bus Mode Select is shown in Section 4.5 and 4.6.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{\text{IRQ}}$ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts cause the $\overline{\text{IRQ}}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by RES. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-6 and the functions of each bit are explained in Table 3-1.

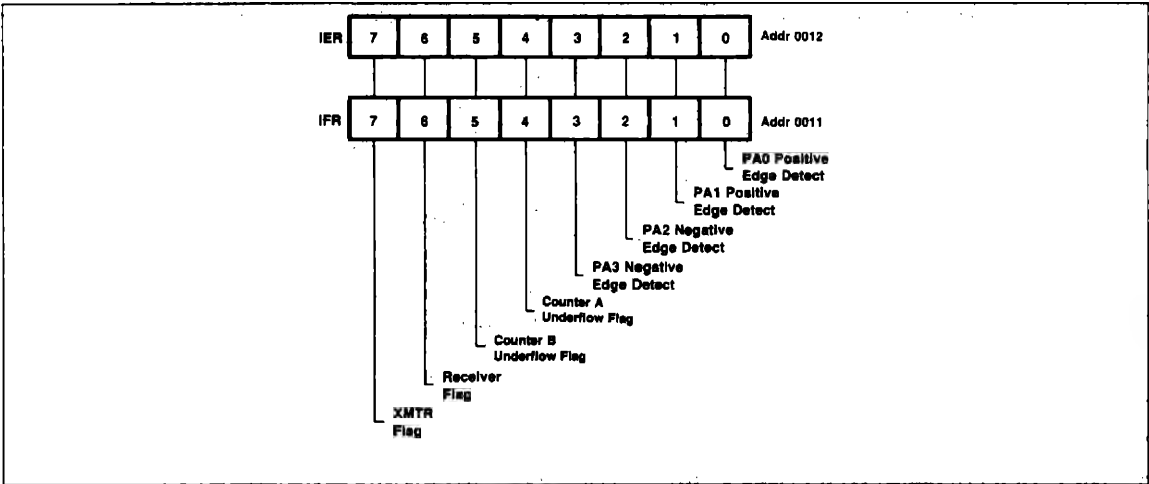


Figure 3-6. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Flag Register Bit Codes

Bit Code	Function
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB 0 (0010) instruction or by RES.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by RES.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by RES.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by RES.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by RES.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by RES.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by RES.
IFR 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by RES.

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-7, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to

zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request (IRQ). If the I Bit is reset to logic 0, the IRQ signal will be serviced. If the bit is set to logic 1, the IRQ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET (RES), IRQ, or Non-Maskable Interrupt (NMI) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit is set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

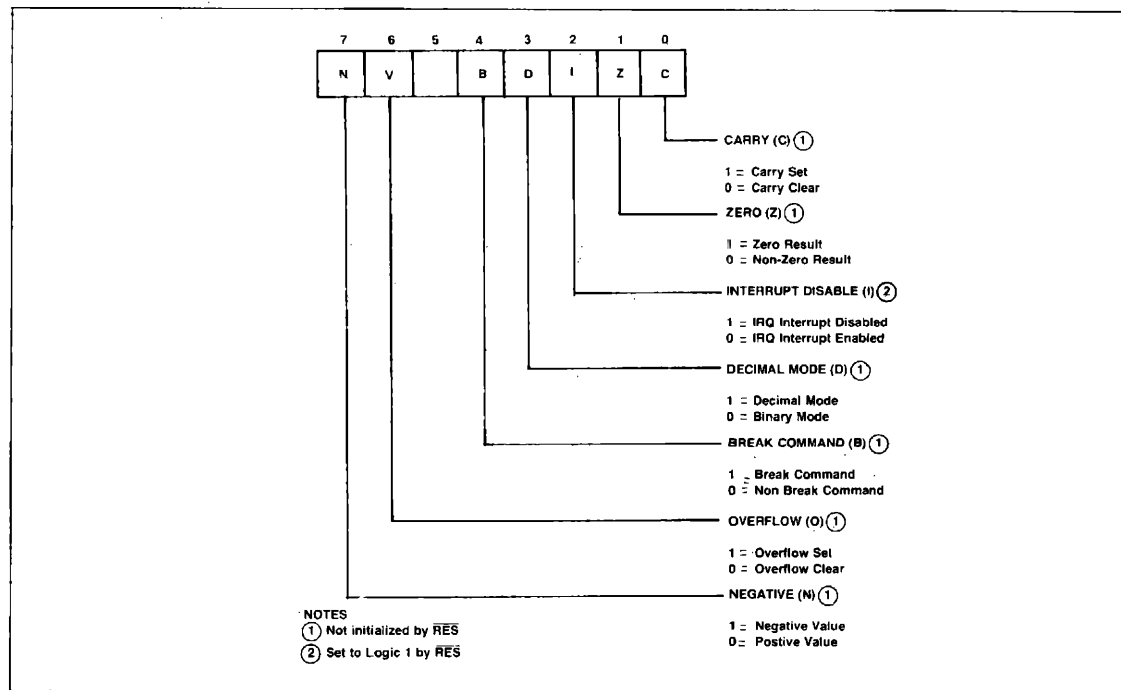


Figure 3-7. Processor Status Register

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D) is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction clears it. The PLP and RTI instructions also affect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{\text{IRQ}}$ service routine to be entered. If the $\overline{\text{IRQ}}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{\text{IRQ}}$ routine was entered as the result of an $\overline{\text{IRQ}}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$).

This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or -128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction—which may be used to sample interface devices—allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions affecting the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7) in the resulting value of a data movement or data arithmetic operation is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4

PARALLEL INPUT/OUTPUT PORTS & BUS MODES

The devices have 32 I/O lines grouped into four 8-bit ports (PA, PB, PC, and PD). Ports A through C may be used either for input or output individually or in groups of any combination. Port D may be used as all inputs or all outputs.

Multifunction I/O's such as Port A and Port C are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of $3K \leq R_L \leq 12K$ ohm) are provided on all port pins except Port D. A mask option to delete the internal pull-ups in 8-bit port groups is available.

The direction of the 32 I/O lines are controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, thus simplifying I/O handling. The I/O addresses are shown in Table 4-1. Appendix E.6 shows the I/O Port Timing.

Table 4-1. I/O Port Addresses

Port	Address
A	0000
B	0001
C	0002
D	0003

4.1 INPUTS

Inputs for Ports A, B, and C are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low ($<0.8V$) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high ($>2.0V$) input will cause a logic 1 to be read. An RES signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port D may only be all inputs or all outputs. All inputs is selected by setting bit 5 of the Mode Control Register (MCR5) to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, & PD. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru D are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high ($>2.4V$) output while a logic 0 will force a low ($<0.4V$) output.

Port D all outputs is selected by setting MCR5 to a "1".

4.3 Port A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the $\phi 2$ clock rate. Edge detection timing is shown in Appendix E.5.

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Table 4-2. Port A Control & Usage

PA0 (2) PIN 39	PA0 I/O		PORT B LATCH MODE				
	MCR4 = 0		MCR4 = 1				
	SIGNAL		SIGNAL				
	NAME	TYPE	NAME	TYPE			
	PA0	I/O	PORT B LATCH STROBE	INPUT (1)			
PA1 (2) PIN 38 PA2 (3) PIN 37 PA3 (3) PIN 36	PA1-PA3 I/O						
	SIGNAL						
	NAME	TYPE					
	PA1	I/O					
	PA2	I/O					
PA3	I/O						
PA4 PIN 35	PA4 I/O		COUNTER A I/O				
	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4) (5)		MCR0 = 1 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4)		SCCR7 = 0 SCCR6 = 0 MCR1 = 1		
	SIGNAL		SIGNAL		SIGNAL		
	NAME	TYPE	NAME	TYPE	NAME	TYPE	
	PA4	I/O	CNTA	OUTPUT	CNTA	INPUT (1)	
	SERIAL I/O SHIFT REGISTER CLOCK						
	SCCR7 = 1 SCCR5 = 1			RCVR S/R MODE = 1 (4)			
	SIGNAL			SIGNAL			
	NAME	TYPE	NAME	TYPE	NAME	TYPE	
	XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)			
	PA5 PIN 34	PA5 I/O		COUNTER B I/O			
		MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1		MCR3 = 1 MCR2 = X	
SIGNAL		SIGNAL		SIGNAL			
NAME		TYPE	NAME	TYPE	NAME	TYPE	
PA5		I/O	CNTB	OUTPUT	CNTB	INPUT (1)	
PA6 PIN 33	PA6 I/O		SERIAL I/O XMTR OUTPUT		(1) Hardware Buffer Float (2) Positive Edge Detect (3) Negative Edge Detect (4) RCVR S/R Mode = 1 when SCCR6 • SCCR5 • SCCR4 = 1 (5) For the following mode combina- tions PA4 is available as an input only pin: SCCR7•SCCR6•SCCR5•MCR1 + SCCR7•SCCR6•7SCCR4•MCR1 + SCCR7•SCCR6•SCCR5 + SCCR7•SCCR5C•SCCR4.		
	SCCR7 = 0		SCCR7 = 1				
	SIGNAL		SIGNAL				
	NAME	TYPE	NAME	TYPE			
	PA6	I/O	XMTR	OUTPUT			
PA7 PIN 32	PA7 I/O		SERIAL I/O RCVR INPUT				
	SCCR6 = 0		SCCR6 = 1				
	SIGNAL		SIGNAL				
	NAME	TYPE	NAME	TYPE			
	PA7	I/O	RCVR	INPUT (1)			

4.4 PORT B (PB)

Port B can be programmed as an 8-bit, bit-independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-3 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Appendix E.5.

Table 4-3. Port B Control & Usage

		I/O Mode		Latch Mode	
		MCR4 = 0		MCR4 = 1 (2)	
Pin #	Pin Name	Signal		Signal	
		Name	Type (1)	Name	Type
31	PB0	PB0	I/O	PB0	INPUT
30	PB1	PB1	I/O	PB1	INPUT
29	PB2	PB2	I/O	PB2	INPUT
28	PB3	PB3	I/O	PB3	INPUT
27	PB4	PB4	I/O	PB4	INPUT
26	PB5	PB5	I/O	PB5	INPUT
25	PB6	PB6	I/O	PB6	INPUT
24	PB7	PB7	I/O	PB7	INPUT

(1) Resistive Pull-Up, Active Buffer Pull-Down
(2) Input data is stored in Port B latch by PA0 Pulse

4.5 PORT C (PC)

Port C can be programmed as an I/O port, as part of the full address bus, and, in conjunction with Port D, as an abbreviated bus, or as a multiplexed bus. When operating in the Full Address Mode PC6 and PC7 serve as A13 and A14 with PC0-PC5 operating as normal I/O pins. When used in the abbreviated or multiplexed bus modes, PC0-PC7 function as A0-A3, A12, R/W, A13, and EMS, respectively, as shown in Table 4-4. EMS (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0100 and 3FFF. (See Memory Map, Appendix B). The leading edge of EMS may be used to strobe the eight address lines multiplexed on Port D in the Multiplexed Bus Mode. See Appendices E.3 through E.5 for Port C timing.

4.6 PORT D (PD)

Port D can be programmed as an I/O Port, an 8-bit tri-state data bus, or as a multiplexed bus. Mode selection for Port D is made by the Mode Control Register (MCR). The Port D output drivers can be selected as tri-state drivers by setting

bit 5 of the MCR to 1 (one). Table 4-5 shows the necessary settings for the MCR to achieve the various modes for Port D. When Port D is selected to operate in the Abbreviated Mode PD0-PD7 serves as data register bits D0-D7. When Port D is selected to operate in the Multiplexed Mode data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix C) for Abbreviated and Multiplexed memory assignments. See Appendices E.3 through E.5 for Port D timing.

4.7 BUS MODES

A special attribute of Port C and Port D is their capability to be configured via the Mode Control Register (see Section 3.6) into four different modes.

In the Full Address Mode, the separate address and data bus are used in conjunction with PC6 and PC7, which automatically provide A13 and A14. The remaining ports perform the normal I/O function.

In the I/O Bus Mode all ports serve as I/O. The address and data bus are still functional but without A13 and A14. Since the internal RAM and registers are in the OOOX location, A15 can be used for chip select and A0-A12 used for selecting 8K of external memory. Thus, the device can be used to emulate the R6500/11 in the Normal Bus Mode.

In the Abbreviated Bus Mode, the address and data lines can be used as in the I/O Bus Mode to emulate the R6500/11. Port C and Port D are automatically transformed into an abbreviated address bus and control signals (Port C) and a bidirectional data bus (Port D). 64 Peripheral addresses can be selected. In general usage, these 64 addresses would be distributed to several external I/O devices such as R6522 and R6520, etc., each of which may contain more than one unique address.

In the Multiplexed Bus Mode, the operation is similar to the Abbreviated Mode except that a full 16K of external addresses are provided. Port C provides the lower addresses and control signals. Port D multiplexes functions. During the first half of the cycle it contains the remaining necessary 8 address bits for 16K; during the second half of the cycle it contains a bidirectional data bus. The address bits appearing on Port D must be latched into an external holding register. The leading edge of EMS, which indicates that the bus function is active, may be used for this purpose.

Figures 4-1a thru 4-1d show the possible configurations of the four bus modes. Figure 4-2 shows a memory map of the port as a function of the Bus Mode and further shows which addresses are active or inactive on each of the three possible buses.

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Table 4-4. Port C Control & Usage

		Full Address Mode		I/O Mode		Abbreviated Mode		Multiplexed Mode	
		MCR7 = 0 MCR6 = 0		MCR7 = 0 MCR6 = 1		MCR7 = 1 MCR6 = 0		MCR7 = 1 MCR6 = 1	
		Signal		Signal		Signal		Signal	
Pin #	Pin Name	Name	Type	Name	Type (1)	Name	Type (2)	Name	Type (2)
54	PC0	PC0	I/O (1)	PC0	I/O	A0	OUTPUT	A0	OUTPUT
55	PC1	PC1	I/O (1)	PC1	I/O	A1	OUTPUT	A1	OUTPUT
56	PC2	PC2	I/O (1)	PC2	I/O	A2	OUTPUT	A2	OUTPUT
57	PC3	PC3	I/O (1)	PC3	I/O	A3	OUTPUT	A3	OUTPUT
58	PC4	PC4	I/O (1)	PC4	I/O	A12	OUTPUT	A12	OUTPUT
59	PC5	PC5	I/O (1)	PC5	I/O	RW	OUTPUT	RW	OUTPUT
60	PC6	A13	OUTPUT (2)	PC6	I/O	A13	OUTPUT	A13	OUTPUT
61	PC7	A14	OUTPUT (2)	PC7	I/O	EMS	OUTPUT	EMS	OUTPUT

(1) Resistive Pull-Up, Active Buffer Pull-Down
 (2) Active Buffer Pull-Up and Pull-Down

Table 4-5. Port D Control & Usage

		I/O Modes				Abbreviated Mode		Multiplexed Mode			
		MCR7 = 0 MCR6 = X MCR5 = 0		MCR7 = 0 MCR6 = X MCR5 = 1		MCR7 = 1 MCR6 = 0 MCR5 = 1		MCR7 = 1 MCR6 = 1 MCR5 = 1			
		Signal		Signal		Signal		Signal		Signal	
Pin #	Pin Name	Name	Type (1)	Name	Type (2)	Name	Type (3)	#2 Low		#2 High	
								Name	Type (2)	Name	Type (3)
62	PD0	PD0	INPUT	PD0	OUTPUT	DATA0	I/O	A4	OUTPUT	DATA0	I/O
63	PD1	PD1	INPUT	PD1	OUTPUT	DATA1	I/O	A5	OUTPUT	DATA1	I/O
64	PD2	PD2	INPUT	PD2	OUTPUT	DATA2	I/O	A6	OUTPUT	DATA2	I/O
1	PD3	PD3	INPUT	PD3	OUTPUT	DATA3	I/O	A7	OUTPUT	DATA3	I/O
2	PD4	PD4	INPUT	PD4	OUTPUT	DATA4	I/O	A8	OUTPUT	DATA4	I/O
3	PD5	PD5	INPUT	PD5	OUTPUT	DATA5	I/O	A9	OUTPUT	DATA5	I/O
4	PD6	PD6	INPUT	PD6	OUTPUT	DATA6	I/O	A10	OUTPUT	DATA6	I/O
5	PD7	PD7	INPUT	PD7	OUTPUT	DATA7	I/O	A11	OUTPUT	DATA7	I/O

(1) Tri-State Buffer is in High Impedance Mode
 (2) Tri-State Buffer is in Active Mode
 (3) Tri-State Buffer is in Active Mode only during the phase 2 portion of a Write Cycle

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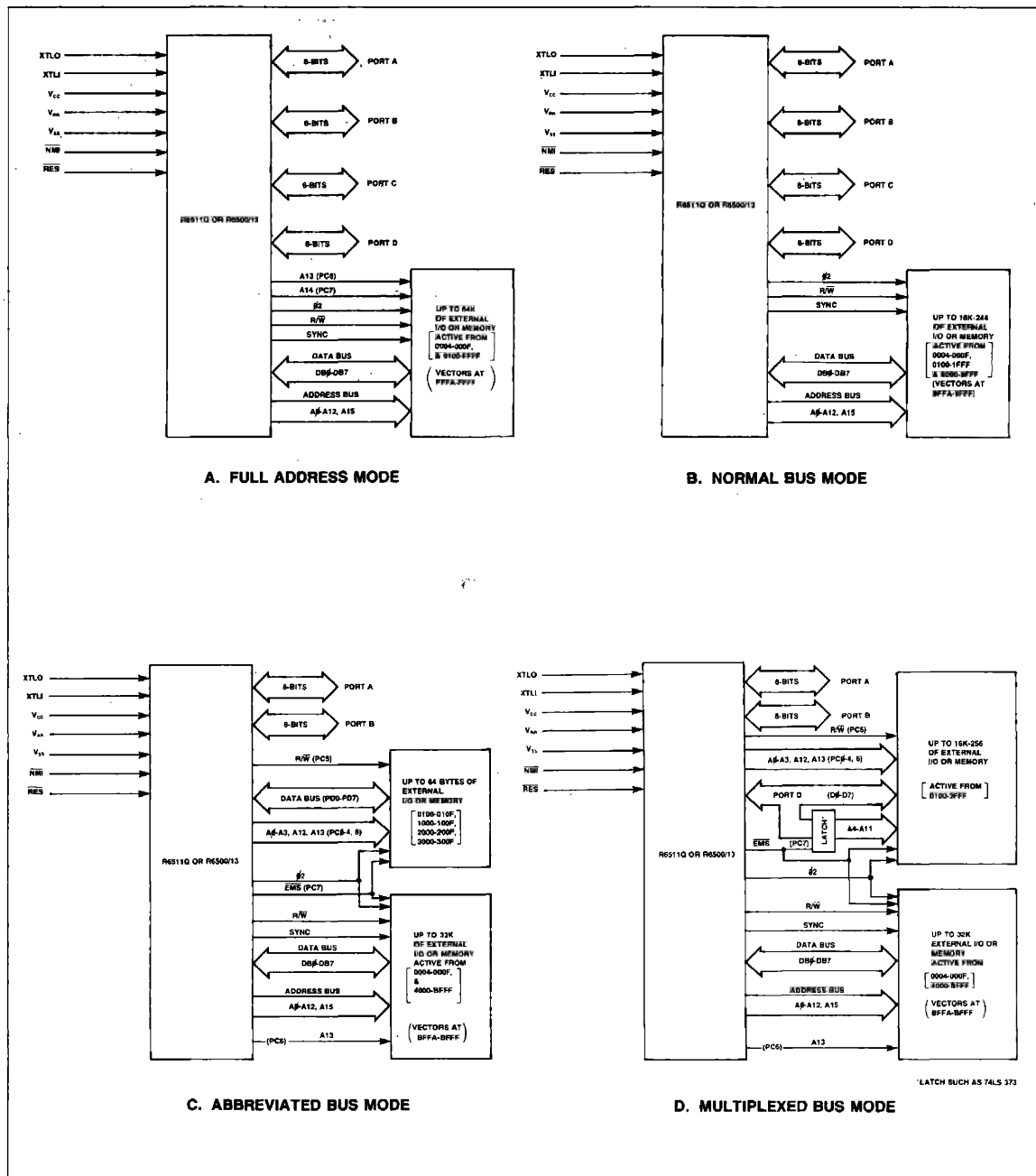


Figure 4-1. Bus Mode Configurations

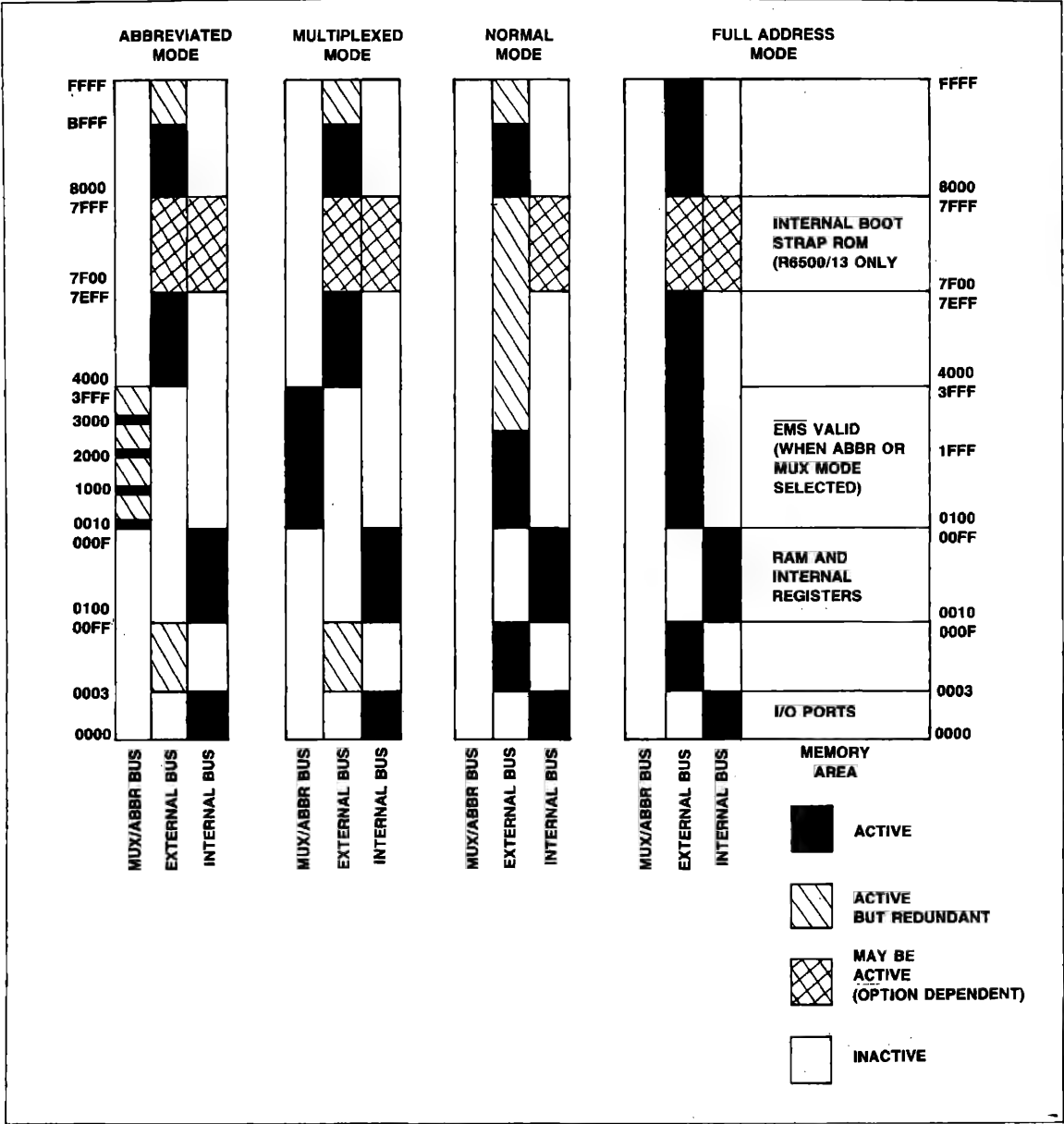


Figure 4-2. Memory Map

SECTION 5 SERIAL INPUT/OUTPUT CHANNEL

The device provides a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (at $f_{\text{clk}} = 1 \text{ MHz}$). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

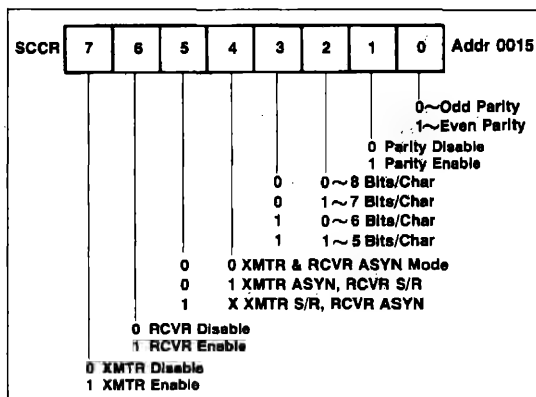


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are shown in Figure 5-2. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

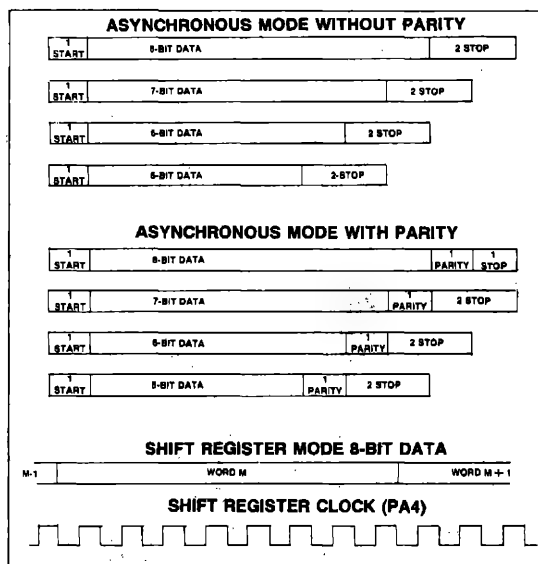


Figure 5-2. SIO Data Modes

In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter under-runs in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCSR5, SCSR6 and SCSR7.

$$\text{IFR7} = \text{SCSR6} \overline{(\text{SCSR5} + \text{SCSR7})}$$

5.2 RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, the appropriate number of data bits, a parity bit (if enabled), and one stop bit. Refer to paragraph 5.1 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits. Any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.

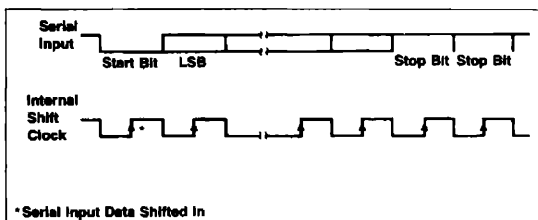


Figure 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.

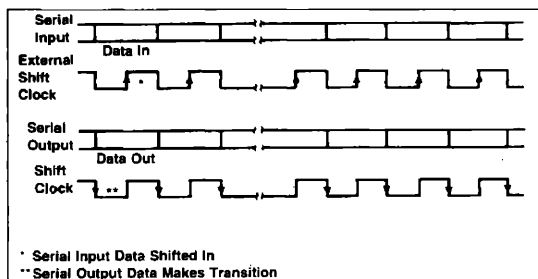


Figure 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR 0: Receiver Data Register Full—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by RES and is disabled if SCSR 6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition; instead, a corresponding error bit will be set to a logic 1.

SCSR 1: Over-Run Error—Set to a logic 1 when a new character is transferred from the Receiver Shift Register with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register or by RES.

SCSR 2: Parity Error—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the

received data has a parity error. This bit is cleared by reading the Receiver Data Register or by RES.

SCSR 3: Framing Error—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by RES (ASYN Mode only).

SCSR 4: Wake-Up—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by RES or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR 5: End of Transmission—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by RES or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6: Transmitter Data Register Empty—Set to a logic 1 when the contents of the Transmitter Data Register are transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmitter Data Register. This bit is initialized to a logic 1 by RES.

SCSR 7: Transmitter Under-Run—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register or by RES.

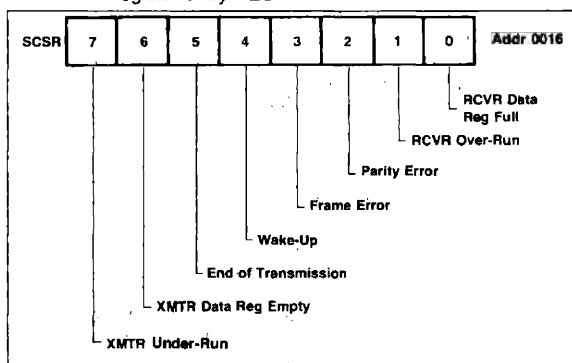


Figure 5-5. SCSR Bit Allocations

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of 11 consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6

COUNTER/TIMERS

The device contains two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A

- Pulse width measurement
- Pulse Generation
- Interval Timer
- Event Counter

Counter B

- Retriggerable Interval Counter
- Asymmetrical Pulse Generation
- Interval Timer
- Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either $\phi 2$ clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the

Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value—not FFFF—and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{\text{RES}}$.

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are $\phi 2$ clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a $\overline{\text{RES}}$ signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).
2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the $\phi 2$ clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore $1\mu\text{s}$ to 65.535 ms at the 1 MHz $\phi 2$ clock rate or $0.5\mu\text{s}$ to 32.767 ms at the 2 MHz $\phi 2$ clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting IRQ interrupt requests in the counter IRQ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an IRQ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the IRQ interrupt routine to determine that the IRQ was generated by the Counter A Underflow.

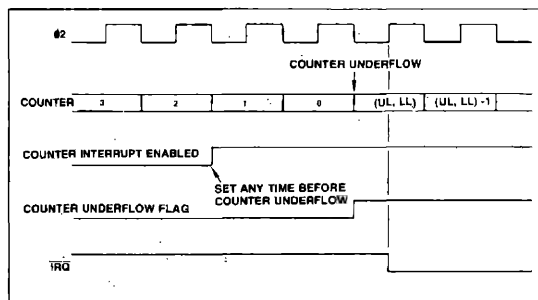


Figure 6-1. Interval Timer Timing Diagram

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While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

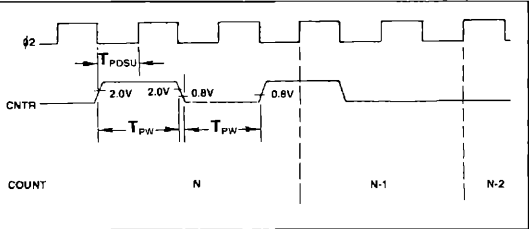


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the $\phi 2$ clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6.3.

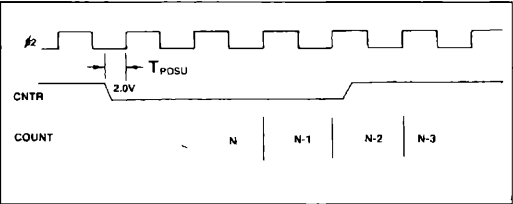


Figure 6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-1 identifies the values to be loaded in Counter A for selecting standard data rates with a $\phi 2$ clock rate of 1 MHz and 2 MHz. Although Table 6-1 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{16 \times \text{bps}} - 1$$

where

- N = decimal value to be loaded into Counter A using its hexadecimal equivalent.
- $\phi 2$ = the clock frequency (1 MHz or 2 MHz)
- bps = the desired data rate.

NOTE

In Table 6-1 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-1 for those baud rates which fall outside this limit.

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Table 6-1. Counter A Values for Baud Rate Selection

Standard Baud Rate	Hexadecimal Value		Actual Baud Rate At		Clock Rate Needed To Get Standard Baud Rate	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600.96	1.0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either $\emptyset 2$ clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a Read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A Read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value and can be loaded at any time by executing a Write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by RES.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode. Mode Control Register bits MCR2 and MCR3 select the four Counter B modes in a similar manner and coding as MCR0 and MCR1 select the modes of Counter A.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

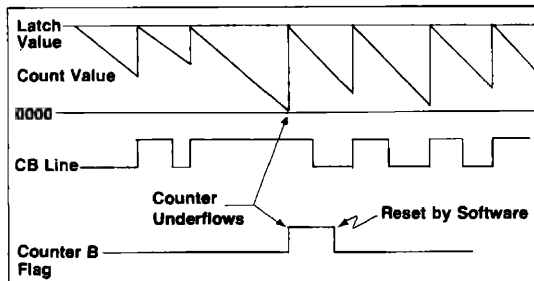


Figure 6-4. Counter B. Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value corresponding to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C; the upper 8 bits of P are loaded into ULB by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.
2. The lower 8 bits of D are loaded into LLB by writing to address 001C; the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and the CB output to go low as shown in Figure 6-5.
3. When Counter B underflow occurs the contents of the Latch C are loaded into the Counter B and the CB output toggles to a high level, staying high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER ON TIMING

After application of V_{CC} and V_{RR} power to the device, \overline{RES} must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at $\phi 2$ (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

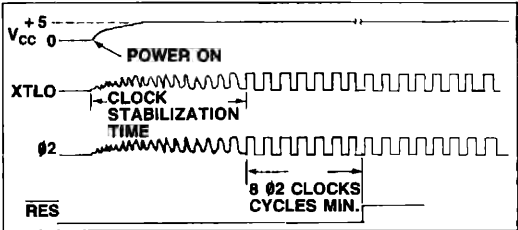


Figure 7-1. Power Turn-On Timing Detail

7.2 POWER-ON RESET

When \overline{RES} goes from low to high, the device sets the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiates a reset vector fetch at address FFFC and FFFD (or optionally 7FFE and 7FFF) to begin user program execution. All of the I/O ports (PA, PB, PC, PD) will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timers counter mode (mode 00) to be selected and all interrupt enabled bits to be reset.

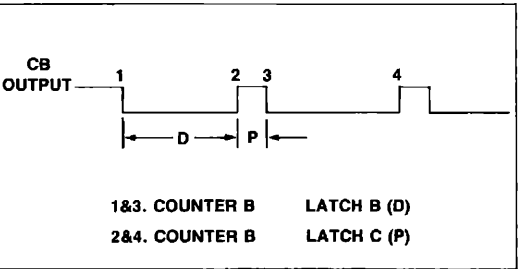


Figure 6-5. Counter B Pulse Generation

7.3 RESET (\overline{RES}) CONDITIONING

When \overline{RES} is driven from low to high the device is put in a reset state causing the registers and I/O ports to be configured as shown in Table 7-1.

Table 7-1. \overline{RES} Initialization of I/O Ports and Registers

Bit No.	7	6	5	4	3	2	1	0
REGISTERS								
Processor Status	—	—	—	—	—	1	—	—
Mode Control (MCR)	0	0	0	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	0	0	0	0	0	0	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1
PC Latch	1	1	1	1	1	1	1	1
PD Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

7.4 INITIALIZATION

Any initialization process for the device should include a \overline{RES} , as indicated in the preceding paragraphs. After stabilization of the internal clock (if a power on situation) an initialization subroutine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required
5. Clear Interrupts

A typical initialization subroutine could be as follows:

LDX Load stack pointer starting address into
 X Register
TXS Transfer X Register value to Stack Pointer
CLD Clear Decimal Mode
SEC Set Carry Flag
... Set-up Mode Control and
... special function registers
... and clear RAM as required
CLI Clear Interrupts

APPENDIX A

ENHANCED R6502 INSTRUCTION SET

This appendix contains a summary of the Enhanced R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Document 29650 N30. The four instructions notated with a * are added instructions to enhance the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

MNEMONIC	INSTRUCTION	MNEMONIC	INSTRUCTION
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative	NOP	No Operation
BCC	Branch on Carry Clear		
BCS	Branch on Carry Set	ORA	"OR" Memory with Accumulator
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator	PHA	Push Accumulator on Stack
BMI	Branch on Result Minus	PHP	Push Processor Status on Stack
BNE	Branch on Result not Zero	PLA	Pull Accumulator from Stack
BPL	Branch on Result Plus	PLP	Pull Processor Status from Stack
BRK	Force Break		
BVC	Branch on Overflow Clear	*RMB	Reset Memory Bit
BVS	Branch on Overflow Set	ROL	Rotate One Bit Left (Memory or Accumulator)
		ROR	Rotate One Bit Right (Memory or Accumulator)
CLC	Clear Carry Flag	RTI	Return from Interrupt
CLD	Clear Decimal Mode	RTS	Return from Subroutine
CLI	Clear Interrupt Disable Bit		
CLV	Clear Overflow Flag	SBC	Subtract Memory from Accumulator with Borrow
CMP	Compare Memory and Accumulator	SEC	Set Carry Flag
CPX	Compare Memory and Index X	SED	Set Decimal Mode
CPY	Compare Memory and Index Y	SEI	Set Interrupt Disable Status
		*SMB	Set Memory Bit
DEC	Decrement Memory by One	STA	Store Accumulator in Memory
DEX	Decrement Index X by One	STX	Store Index X in Memory
DEY	Decrement Index Y by One	STY	Store Index Y in Memory
EOR	"Exclusive-Or" Memory with Accumulator	TAX	Transfer Accumulator to Index X
		TAY	Transfer Accumulator to Index Y
INC	Increment Memory by One	TSX	Transfer Stack Pointer to Index X
INX	Increment Index X by One	TXA	Transfer Index X to Accumulator
INY	Increment Index Y by One	TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator
JMP	Jump to New Location		
JSR	Jump to New Location Saving Return Address		

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MNEUMONIC		OPERATION	ADDRESSING MODES																								PROCESSOR STATUS CODES																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
			IMMEDIATE		ABSOLUTE/ZERO PAGE		ACCUM.		IMPLIED		(IND. X)		(IND. Y)		Z PAGE X		ABS. X		RELATIVE		INDIRECT		Z PAGE Y		BIT ADDRESSING (OP BY BIT #)		7 6 5 4 3 2 1 0																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP

NOTES

1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
3. Carry not - Borrow
4. If in decimal mode Z flag is invalid
5. Effects 8-bit data field of the specified zero page address.

LEGEND

X = Index X
Y = Index Y
A = Accumulator
M = Memory per effective address
M₀ = Memory per stack pointer
M₁ = Selector zero page memory bit
N₁ = Memory Bit 7

M₆ = Memory Bit 6
+ = Add
- = Subtract
^ = And
v = Or
v = Exclusive Or
n = Number of cycles
= Number of Bytes

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A.3 INSTRUCTION CODE MATRIX

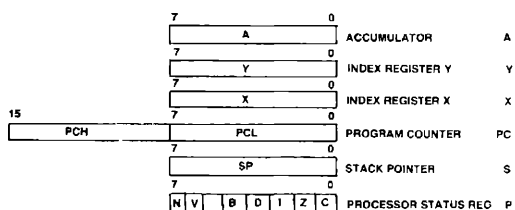
MSD	LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0		BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1		BPL Relative 2 2**	ORA (IND, Y) 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2		JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3		BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4		RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5		BVC Relative 2 2**	EOR (IND, Y) 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6		RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7		BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8			STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBR8 ZP 3 5**	8
9		BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBR9 ZP 3 5**	9
A		LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBR10 ZP 3 5**	A
B		BCS Relative 2 2**	LDA (IND, Y) 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBR11 ZP 3 5**	B
C		CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBR12 ZP 3 5**	C
D		BNE Relative 2 2**	CMP (IND, Y) 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBR13 ZP 3 5**	D
E		CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBR14 ZP 3 5**	E
F		BEQ Relative 2 2**	SBC (IND, Y) 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBR15 ZP 3 5**	F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

0	BRK Implied 1 7	—OP Code —Addressing Mode —Instruction Bytes; Machine Cycles
---	-----------------------	--------------------------------------------------------------------

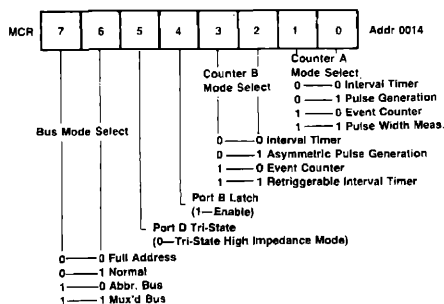
*Add 1 to N if page boundary is crossed.

**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

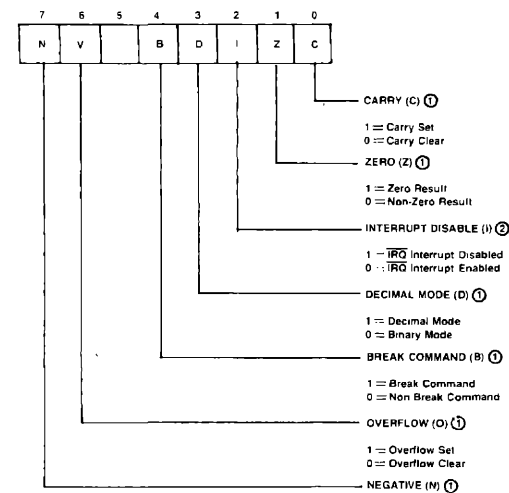
APPENDIX B KEY REGISTER SUMMARY



CPU Registers



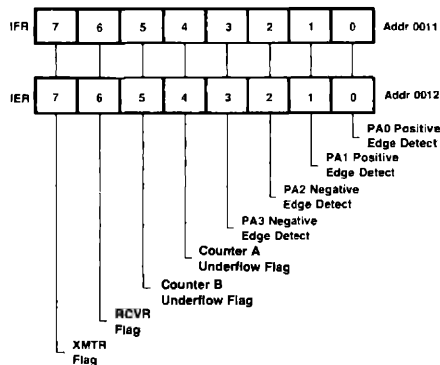
Mode Control Register



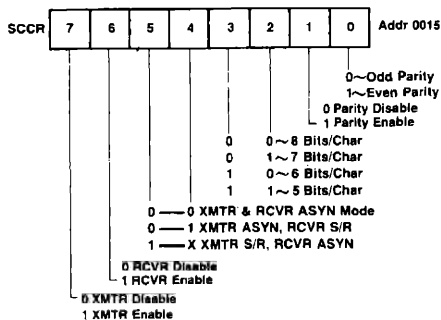
NOTES

- ① Not initialized by RES
② Set to Logic 1 by RES

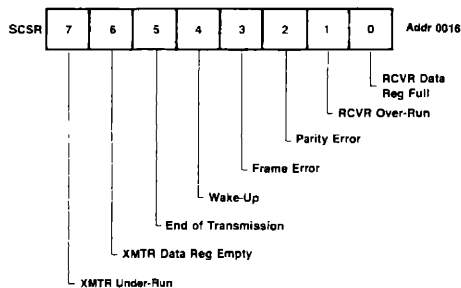
Processor Status Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



Serial Communications Status Register

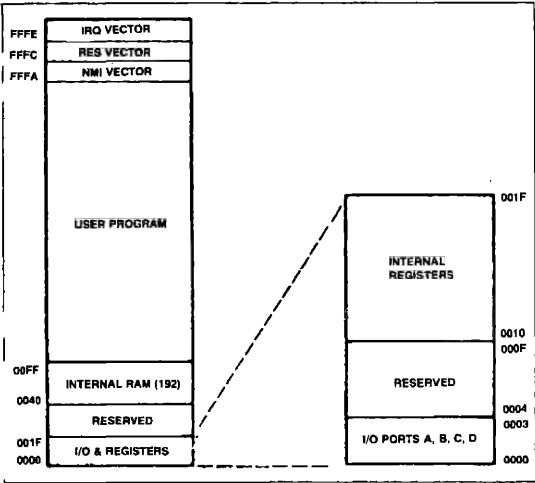
APPENDIX C **ADDRESS ASSIGNMENTS/MEMORY** **MAPS/PIN FUNCTIONS**

C.1 I/O AND INTERNAL REGISTER ADDRESSES

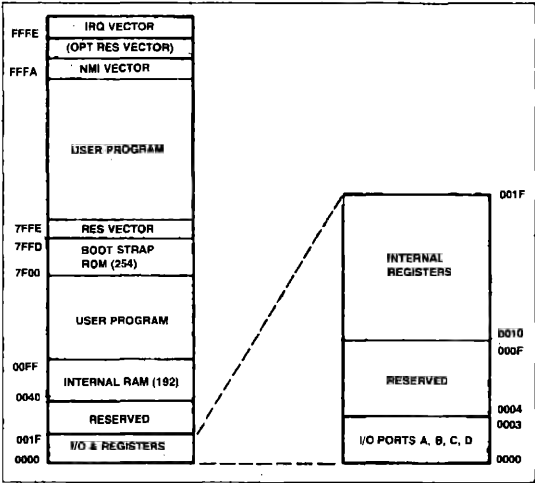
ADDRESS (HEX)	READ	WRITE
001F 1E 1D 1C	— — Lower Counter B Upper Counter B Lower Counter B, CLR Flag	— — Upper Latch B, Cntr B—Latch B, CLR Flag Upper Latch B, Latch C—Latch B Lower Latch B.
1B 1A 19 18	— — Lower Counter A Upper Counter A Lower Counter A, CLR Flag	— — Upper Latch A, Cntr A—Latch A, CLR Flag Upper Latch A Lower Latch A
17 16 15 14	Serial Receiver Data Register Serial Comm. Status Register Serial Comm. Control Register Mode Control Register	Serial Transmitter Data Register Serial Comm. Status Reg. Bits 4 & 5 only Serial Comm. Control Register Mode Control Register
13 12 11 0010	— — Interrupt Enable Register Interrupt Flag Register Read FF	— — Interrupt Enable Register — — Clear Int Flag (Bits 0-3 only, Write 0's only)
0F 0E 0D 0C	<p style="text-align: center;">RESERVED</p> <p style="text-align: center;">These addresses are reserved and are used by the CPU during Read and Write operation over the external Data Bus (D0-D7).</p>	
0B 0A 09 08		
07 06 05 04		
03 02 01 0000	Port D Port C Port B Port A	Port D Port C Port B Port A

R6511Q Microprocessor and R6500/13 Microcomputer

C.2 FULL ADDRESS MODE
MEMORY MAP
R6511Q OR R6500/13



C.3 FULL ADDRESS MODE
MEMORY MAP
R6500/13 ONLY



3

C.4 MULTIPLE FUNCTION PIN ASSIGNMENTS—PORT C AND PORT D

PIN NUMBER	FULL ADDRESS MODE	I/O PORT FUNCTION	ABBREVIATED PORT FUNCTION	MULTIPLEXED PORT FUNCTION
54	PC0	PC0	A0	A0
55	PC1	PC1	A1	A1
56	PC2	PC2	A2	A2
57	PC3	PC3	A3	A3
58	PC4	PC4	A12	A12
59	PC5	PC5	R/W	R/W
60	A13	PC6	A13	A13
61	A14	PC7	EMS	EMS
62	PD0	PD0	D0	A4/D0
63	PD1	PD1	D1	A5/D1
64	PD2	PD2	D2	A6/D2
1	PD3	PD3	D3	A7/D3
2	PD4	PD4	D4	A8/D4
3	PD5	PD5	D5	A9/D5
4	PD6	PD6	D6	A10/D6
5	PD7	PD7	D7	A11/D7

APPENDIX D

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{RR}	- 0.3 to + 7.0	Vdc
Input Voltage	V_{IN}	- 0.3 to + 7.0	Vdc
Operating Temperature Commercial Industrial	T_A	0 to +70 - 40 to +85	°C
Storage Temperature	T_{STG}	- 55 to + 150	°C

*NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

DC CHARACTERISTICS

($V_{CC} = 5V \pm 5\%$; $V_{RR} = V_{CC}$; $V_{SS} = 0$; $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High) Commercial @ 0°C Industrial @ -40°	P_D	—	750 ⁽¹⁾	1100 1200	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial @ 25°C Industrial @ 25°C	I_{RR}	—	4 5.2	—	mADC
Input High Voltage (Except XTLI and #2 in slave option)	V_{IH}	+ 2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI and #2 in slave option)	V_{IH}	+ 4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	- 0.3	—	+ 0.8	Vdc
Input Leakage Current (RES, NMI) $V_{in} = 0$ to 5.0 Vdc	I_{IN}	—	—	± 10.0	μAdc
Input Low Current PA, PB, PC, PD ($V_{IL} = 0.4$ Vdc)	I_{IL}	—	- 1.0	- 1.6	mAdc
Output High Voltage (Except XTLO) ($I_{LOAD} = .100 \mu\text{Adc}$)	V_{OH}	+ 2.4	—	V_{CC}	Vdc
Output Low Voltage ($I_{LOAD} = 1.6$ mAdc)	V_{OL}	—	—	+ 0.4	Vdc
Input Capacitance $V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz XTLI, XTLO All Others	C_{in}	— —	— —	50 10	pF
I/O Port Pull-Up Resistance PA0-PA7, PB0-PB7, PC0-PC7	R_L	3.0	6.0	11.5	K Ω
Output Leakage Current Tri-State I/O's while in	I_{OUT}	—	—	± 10	μAdc
Output Capacitance Tri-State I/O's while in High Impedance State $V_{IN} 0V$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz	C_{OUT}	—	—	10	pF
NOTE: Negative sign indicates outward current flow, positive indicates inward flow. (1) at 25°C					

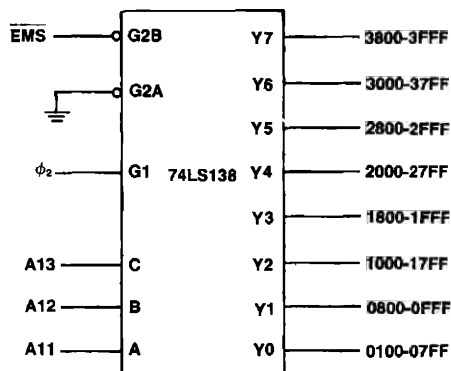
APPENDIX E TIMING REQUIREMENTS AND CHARACTERISTICS

E.1 GENERAL NOTES

1. $V_{CC} = 5V \pm 5\%$, $0^\circ C \leq T_A \leq 70^\circ C$
2. A valid $V_{CC} - \overline{RES}$ sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pf maximum, except as noted below:

PA, PB	—	50pf maximum
PC (I/O Modes Only)	—	50pf maximum
PC (ABB and Mux Mode)	—	130pf maximum
PC6, PC7 (Full Address Mode)	—	130pf maximum

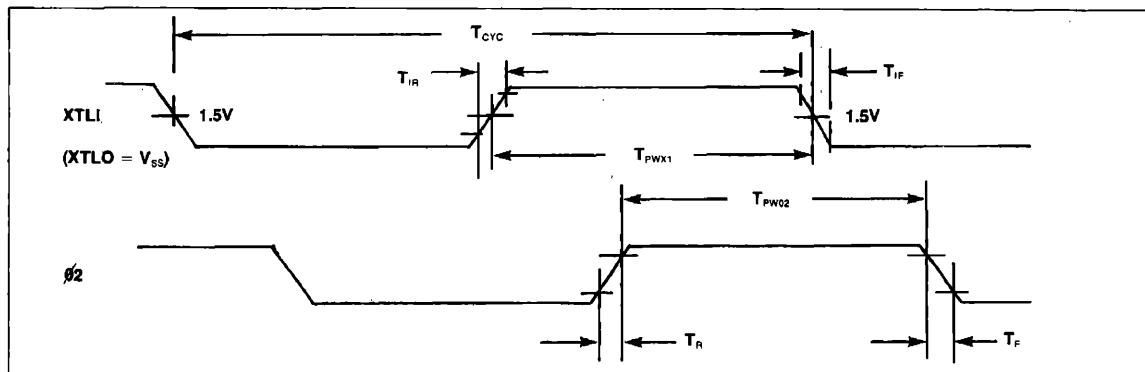
6. Example of External Chip Select (Multiplexed Bus)



Note that both \overline{EMS} and Phase 2 (ϕ_2) must be used to correctly enable the chip selects in the multiplexed or abbreviated bus modes.

E.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 ± 25	—	250 ± 10	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1}	$T_{PWX1} \pm 25$	T_{PWX1}	$T_{PWX1} \pm 20$
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10



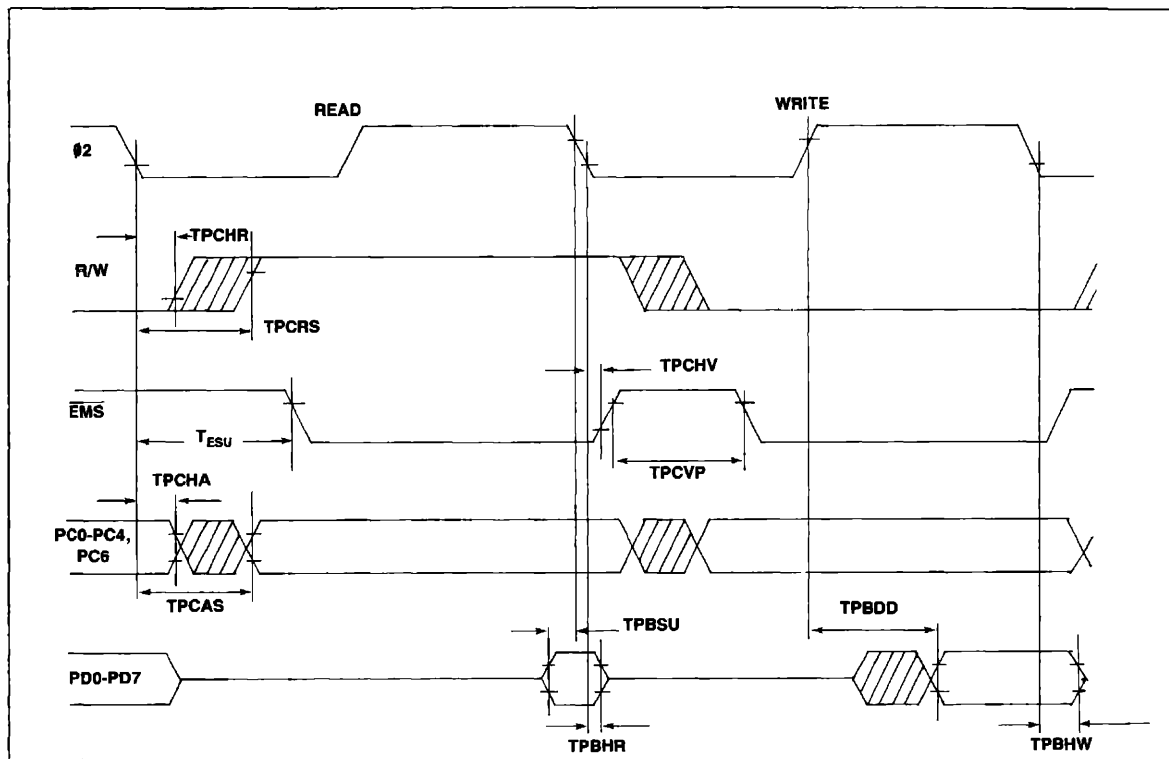
R6511Q Microprocessor and R6500/13 Microcomputer

E.3 ABBREVIATED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 0, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	200	—	100
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	130
T_{PCHA}	(PC0-PC4, PC6) Address Hold Time	30	—	30	—
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) EMS Hold Time	10	—	10	—
T_{PCVP}	(PC7) EMS Stabilization Time	30	—	30	—
T_{ESU}	EMS Setup Time	—	350	—	210

E.3.1 Abbreviated Mode Timing Diagram



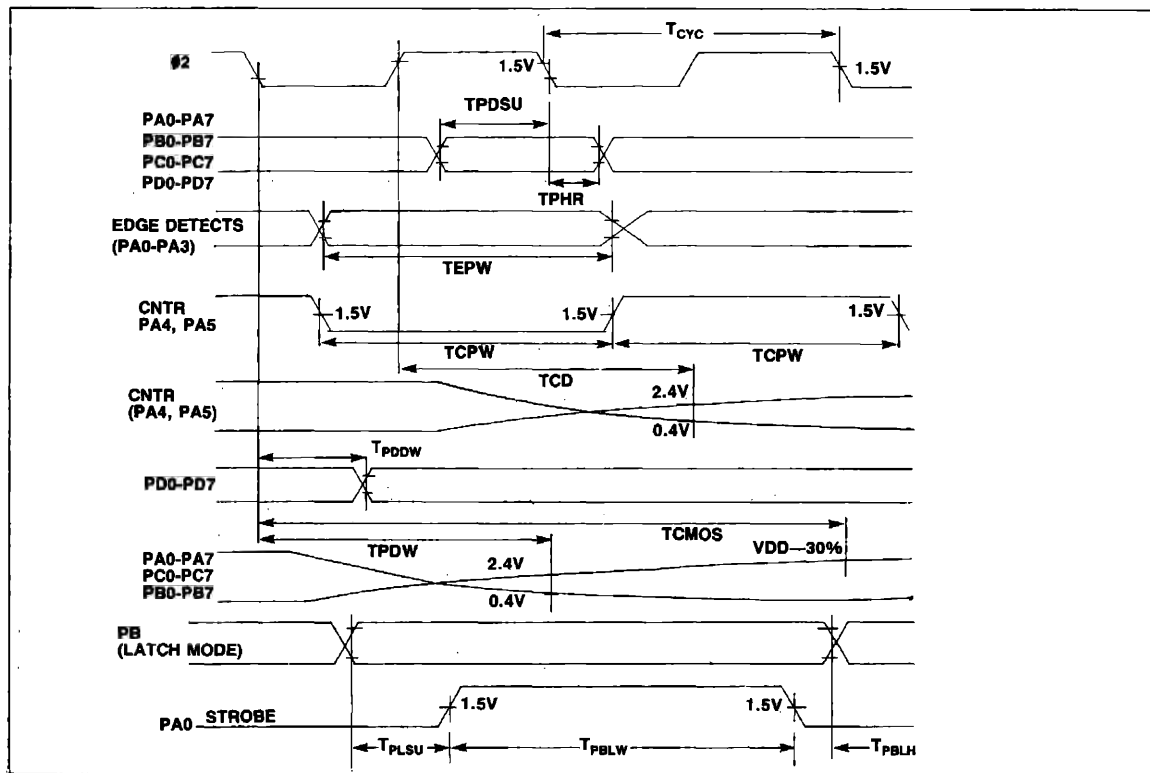
R6511Q Microprocessor and R6500/13 Microcomputer

E.5 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
$T_{PDW}^{(1)}$	Internal Write to Peripheral Data Valid PA, PB, PC TTL	—	500	—	500
$T_{CMOS}^{(1)}$	PA, PB, PC CMOS	—	1000	—	1000
T_{PDDW}	PD	—	175	—	150
T_{PDSU}	Peripheral Data Setup Time PA, PB, PC	200	—	200	—
T_{PHR}	PD	50	—	50	—
T_{PHR}	Peripheral Data Hold Time PA, PB, PC	75	—	75	—
T_{PHR}	PD	10	—	10	—
T_{EPW}	PA0-PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CPW}	Counters A and B PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
$T_{CD}^{(1)}$	PA4, PA5 Output Delay	—	500	—	500
T_{PBLW}	Port B Latch Mode PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PB Data Setup Time	175	—	150	—
T_{PBLH}	PB Data Hold Time	30	—	30	—
$T_{PDW}^{(1)}$	Serial I/O PA6 XMTR TTL	—	500	—	500
$T_{CMOS}^{(1)}$	PA6 XMTR CMOS	—	1000	—	1000
T_{CPW}	PA4 RCVR S/R Clock Width	$4 T_{CYC}$	—	$4 T_{CYC}$	—
$T_{PDW}^{(1)}$	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
$T_{CMOS}^{(1)}$	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

NOTE 1: Maximum Load Capacitance: 50pF
Passive Pull-Up Required

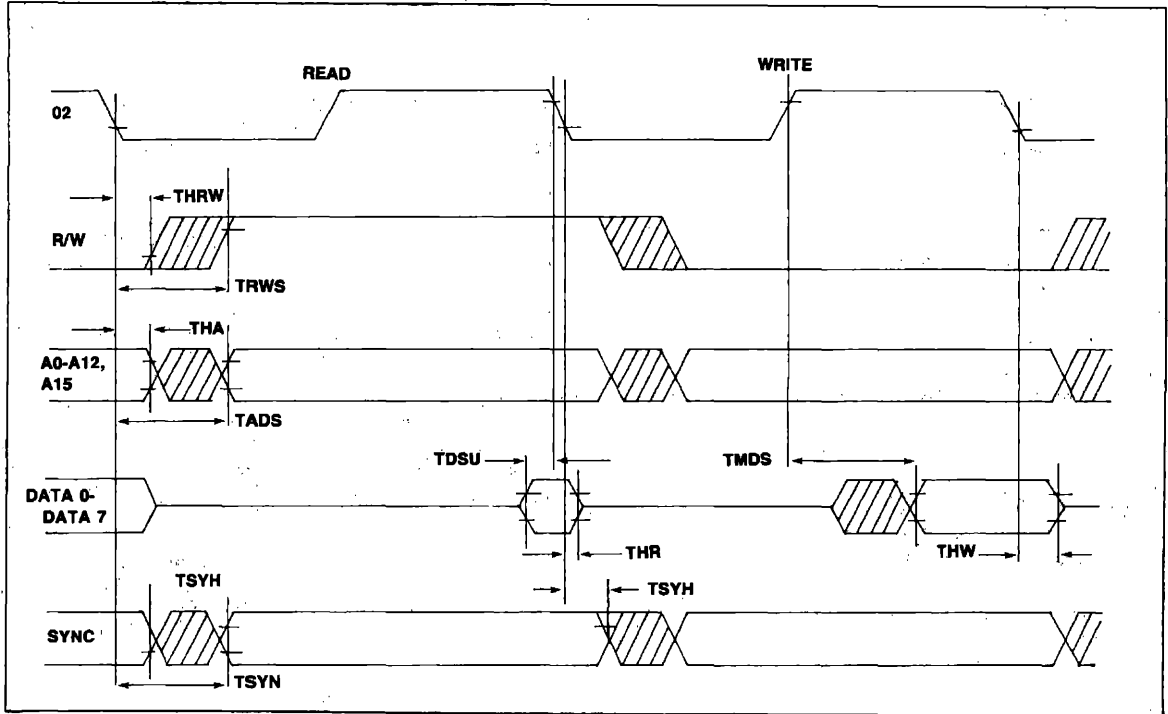
E.5.1 I/O, Edge Detect, Counter, and Serial I/O Timing



E.6 MICROPROCESSOR TIMING (D0-D7, A0-A12, A15, SYNC, R/W)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{RWS}	R/W Setup Time	—	225	—	140
T_{ADS}	A0-A12, A15 Setup Time	—	225	—	140
T_{DSU}	D0-D7 Data Setup Time	50	—	35	—
T_{HR}	D0-D7 Read Hold Time	10	—	10	—
T_{HW}	D0-D7 Write Hold Time	30	—	30	—
T_{MOS}	D0-D7 Write Output Delay	—	175	—	150
T_{SYN}	SYNC Setup	—	225	—	175
T_{HA}	A0-A12, A15 Hold Time	30	—	30	—
T_{HRW}	R/W Hold Time	30	—	30	—
T_{ACC}	External Memory Access Time $T_{ACC} = T_{CYC} - T_F - T_{ADS} - T_{DSU}$	—	T_{ACC}	—	T_{ACC}
T_{SYH}	SYNC Hold Time	30	—	30	—

E.6.1 Microprocessor Timing Diagram





R6500/41 AND R6500/42 ONE-CHIP INTELLIGENT PERIPHERAL CONTROLLERS

SECTION 1 INTRODUCTION

1.1 FEATURES

- Directly compatible with 6500, 6800, 8080, and Z80 bus families
- Asynchronous Host interface that allows independent clock operation
- Input, Output and Status Registers for CPU/Host data transfer
- Status register for CPU/Host data transfer operations
- Interrupt or polled data interchange with Host
- Enhanced 6502 CPU
 - Four new bit manipulation instructions:
 - Set Memory Bit (SMB)
 - Reset Memory Bit (RMB)
 - Branch on Bit Set (BBS)
 - Branch on Bit Reset (BBR)
 - Decimal and binary arithmetic modes
 - 13 addressing modes
 - True indexing
- 1536-byte mask-programmable ROM
- 64-byte static RAM
- 23 TTL-compatible I/O lines (R6500/41 only)
- 47 TTL-compatible I/O lines (R6500/42 only)
- A 16-bit programmable counter/timer, with latch
 - Pulse width measurement
 - Pulse generation
 - Interval timer
 - Event counter
- Seven interrupts
 - Two edge-sensitive lines; one positive, one negative
 - Reset
 - Counter Underflow
 - Host data received
 - Output Data Register full
 - Input Data Register empty
- Multiplexed bus expandable to 4K bytes of external memory
- Unmultiplexed bus for Peripheral I/O expansion
- 68% of the instructions are executed in less than $2\mu\text{s}$ @ 2 MHz

- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 40-pin DIP (R6500/41 only)
- 64-pin QUIP (R6500/42 only)

NOTE

This document describes both the R6500/41 and R6500/42. In the text, the terms IPC or device will be used when describing both parts. The few differences will be described in the text using the terms R6500/41 or R6500/42.

1.2 SUMMARY

The Rockwell R6500/41 and R6500/42 One-Chip Intelligent Peripheral Controllers (IPC) are general purpose, program-mable interface I/O devices designed for use with a variety of 8-bit and 16-bit microprocessor systems. The one-chip R6500/41 IPC has an enhanced R6502 CPU, 1.5K by 8-bit ROM, 64 by 8-bit RAM, three I/O ports with multiplexed special functions, and a multi-function timer all contained within a 40-pin package.

For systems requiring additional I/O ports, the device is also available in a 64-pin QUIP version, R6500/42, that provides three additional 8-bit ports. In both versions, special interface registers allow these IPC devices to function as peripheral controllers for the 6500, 6800, Z80, 8080, and other 8-bit or 16-bit host microcomputer systems.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the device a leading candidate for IPC computer applications.

To facilitate system and program development for the device Rockwell has developed the R6541Q which can be used as an Emulator. A description of the R6541Q is contained in the R6541Q Product Description (Document Order No. 2136).

Rockwell supports development of the R6500/41 and R6500/42 with the System 65 Microcomputer Development System and the R6500/★ Family of Personality Modules. Complete in-circuit emulation with the R6500/★ Family of Personality Modules allows total system test and evaluation.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Order Number 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order Number 202).

1.3 MASK OPTIONS

The R6500/41 has provision for internal pull-up resistors on PA and PC ports as a mask option. This option is available for port groups only, not for individual port lines.

The R6500/42 has provision for pull-up resistors on PA, PC, PF, and PG ports as a mask option. This option is available for port groups only, not for individual port lines.

SECTION 2

R6500/41 INTERFACE REQUIREMENTS

This section describes the interface requirements for the Intelligent Peripheral Controller. Figure 2-1 is the Interface Diagram for the devices. Figures 2-2 and 2-4 show the pin out configurations and Table 2-1 describes the function of each

pin of the devices. Figures 2-3 and 2-5 show the mechanical dimensions of the devices. Section 5 describes the Host computer interface protocol and timing requirements.

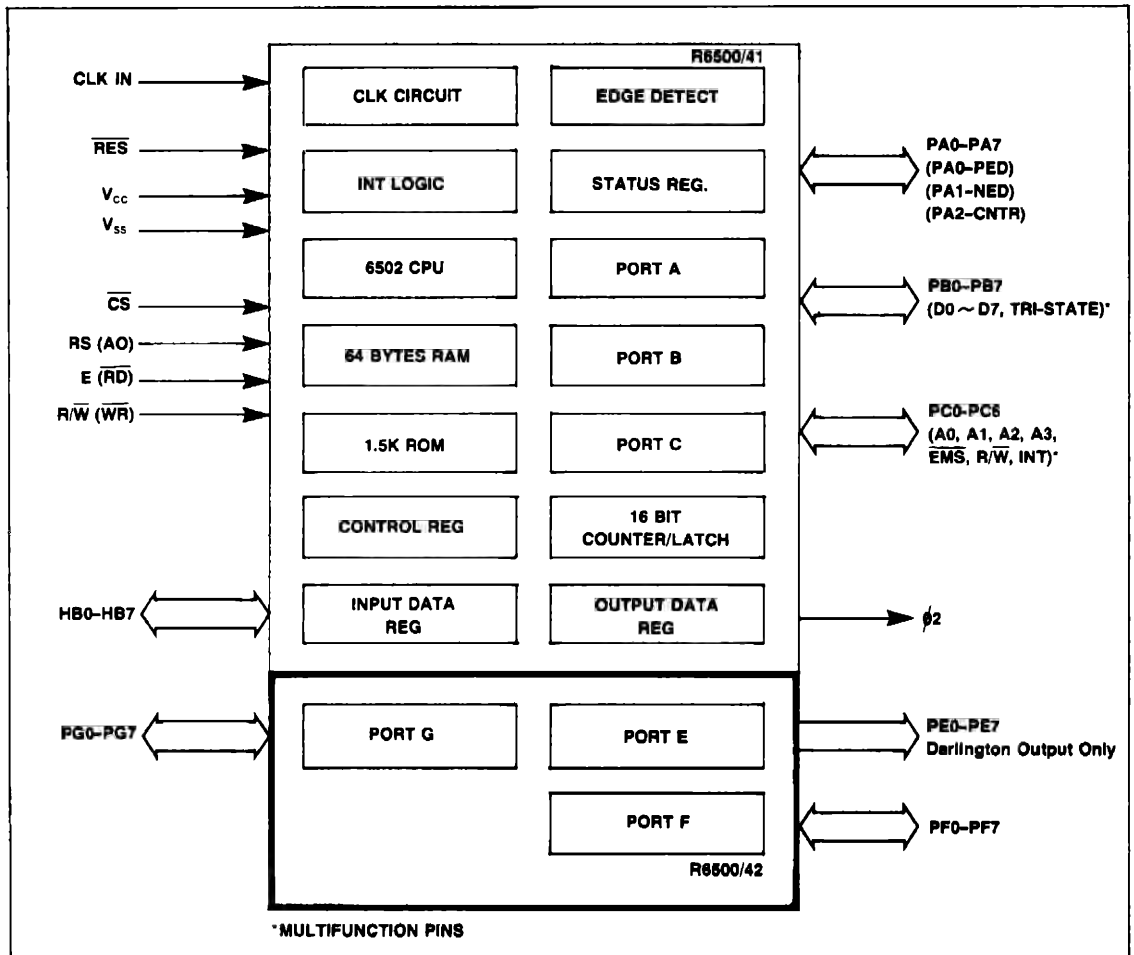


Figure 2-1. Interface Diagram

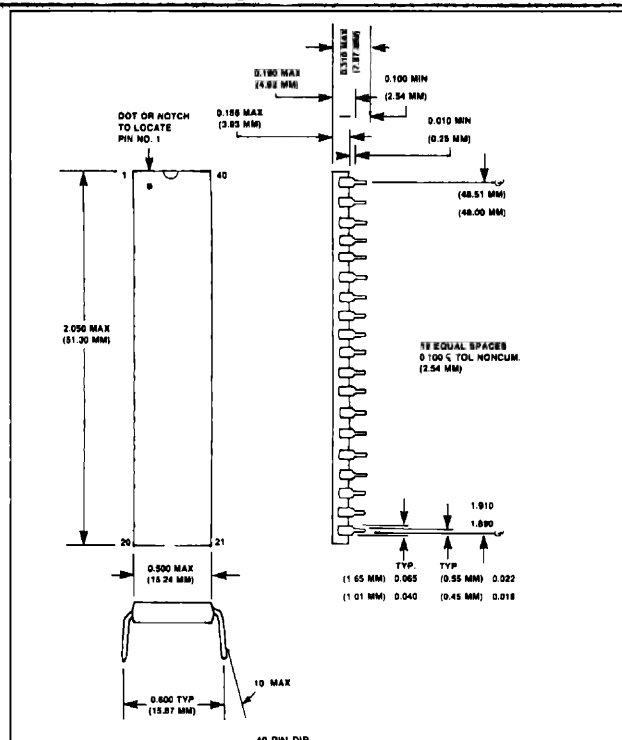


Figure 2-3. R6500/41 Dimensional Outline

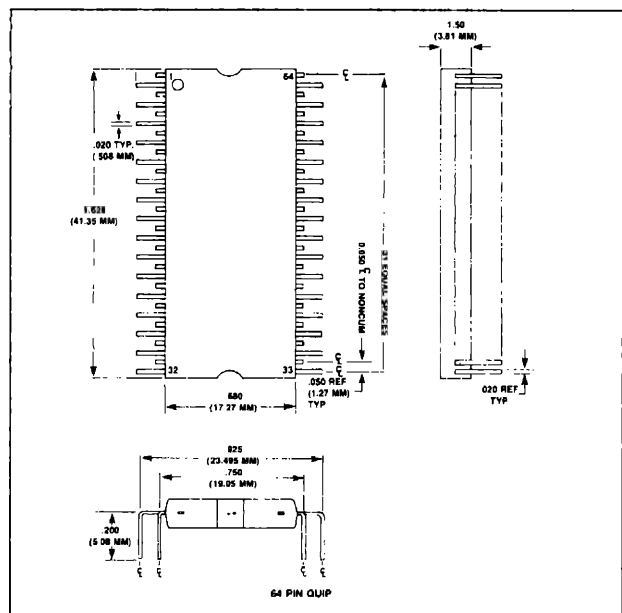


Figure 2-5. R6500/42 Dimensional Outline

Table 2-1. Pin Description

SIGNAL NAME	PIN NO.		DESCRIPTION	SIGNAL NAME	PIN NO.		DESCRIPTION
	R6500/41	R6500/42			R6500/41	R6500/42	
CLKIN	39	3	Symmetrical square wave 100 KHz to 2 MHz, TTL compatible input.	PA0-PA7	22-29	25-32	8 bit I/O port used for either input or output. Each line consists of an active transistor to V_{SS} and an optional passive pull-up to V_{CC} . The two lower bits PA0 and PA1 also serve as edge detect inputs. PA2 is time shared with the 16 bit Counter Input or output pin, CNTR, and is mode selected.
$\phi 2$	20	23	Output timing signal—This is an internally synchronized 1 × clock output suitable for external memory or peripheral interfacing.				
\overline{RES}	38	57	The reset input is used to initialize the device. Section 7 describes the process and conditions of the \overline{RES} procedure.	PB0-PB7	30-37	49-56	8 bit I/O port used for either input or output. Each line consists of an active transistor to V_{SS} and an active pull-up to V_{CC} . This port becomes a tri-state data bus, D0-D7, in the Abbreviated or Multiplexed Bus Mode. D0-D7 are multiplexed with address lines A4-A11 in the Multiplexed Bus Mode.
VCC	40	58	Power supply input (+5V)				
VSS	21	24	Signal and power ground (OV).				
\overline{CS}	1	4	Chip select pin.				
RS (A0)	4	7	Register select input pin used by the Host processor to indicate that information being written into the IPC is a data or command byte or to indicate that information being read from the IPC is a status or data byte.	PC0-PC6	13-19	16-22	7 bit I/O port used for either input or output. Each line consists of an active transistor to V_{SS} and an optional passive pull-up to V_{CC} . The pins PC0 to PC5 are multiplexed with address and control signals for use in abbreviated and multiplex modes. PC6 is multiplexed with INT and is program selectable. In these two modes PC0-PC5 have active pull-ups.
E (\overline{RD})	2	5	Host timing control signal for data register write and read.				
R/W (\overline{WR})	3	6	Host timing control signal for data register write and read.				
HB0-HB7	5-12	8-15	Data bus between Host and IPC data input and output registers.	PE0-PE7 PF0-PF7 PG0-PG7	N/A N/A N/A	1, 2, 64-59 33-40 41-48	For the R6500/42, the 64 pin QUIP version, three additional ports (24 lines) are provided. Each line consists of an active transistor to V_{SS} . PF0-PF7 and PG0-PG7 are bidirectional, and an optional passive pull-up to V_{CC} is provided. PE0-PE7 is outputs only with an active pullup. All ports will source 100 μ amps. at 2.4v except port E (PE0-PE7) which will source 1 ma. at 1.5v.

SECTION 3

SYSTEM ARCHITECTURE

This section provides a functional description of the IPC device. Functionally, the device consists of a CPU, both ROM and RAM memories, three parallel I/O ports (six in the 64-pin R6500/42), counter/latch circuit, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The internal CPU of the device is an enhanced R6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, or an internal IRQ interrupt. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time

data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 007F-0040. Normal usage calls for the initialization of the Stack Pointer at 007F.

3.1.4 Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is initialized each time an instruction fetch is executed and is advanced at the beginning of each low level of the Clock In pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

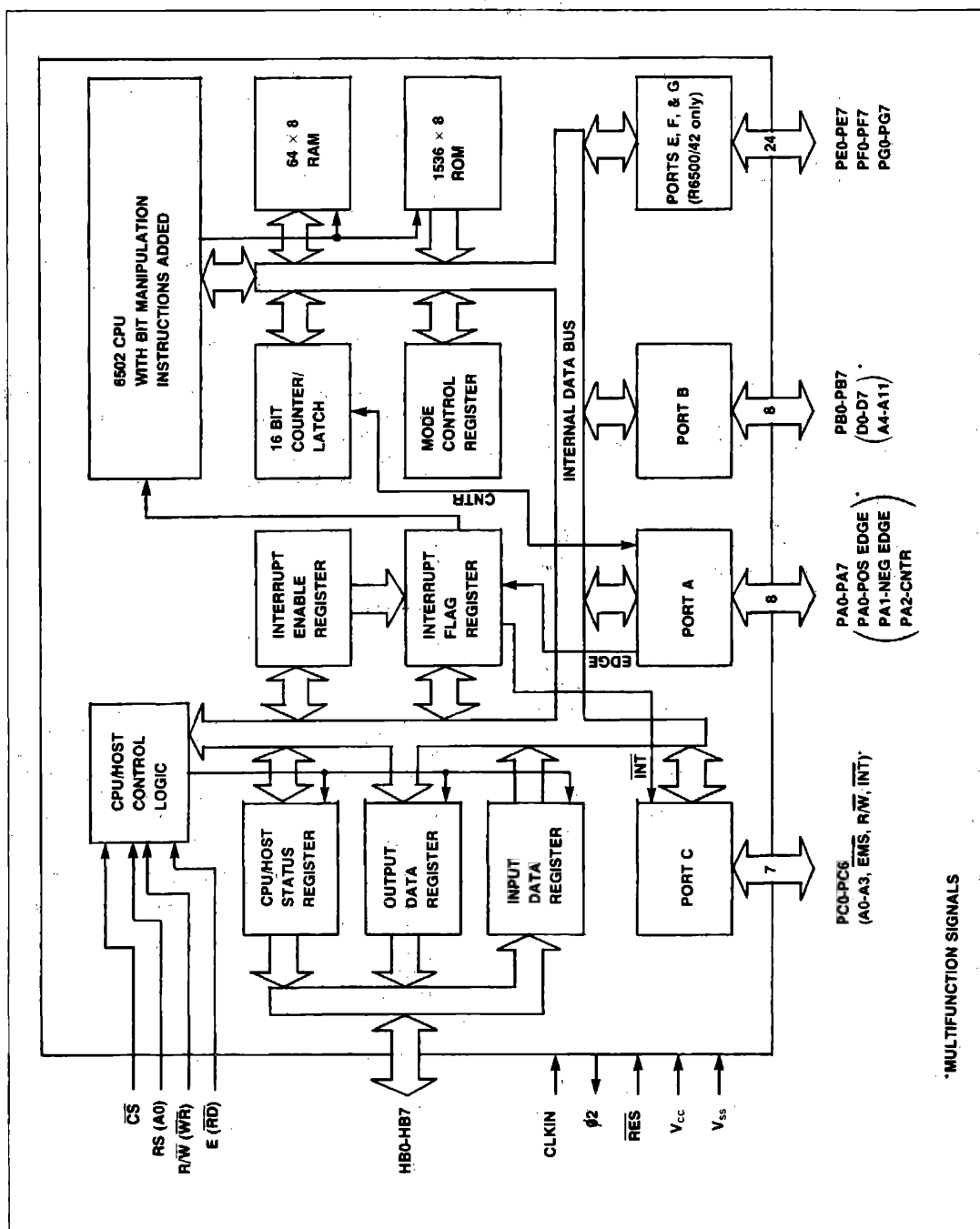


Figure 3-1. R6500/41 & R6500/42 Block Diagram

3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of two interrupts: \overline{RES} and \overline{IRQ} . \overline{IRQ} is generated by any one of four conditions: Counter Overflow, Positive Edge Detect, Negative Edge Detect, and Input Data Register Full.

3.2 NEW INSTRUCTIONS

In addition to the standard 6502 instruction set, four instructions have been added to the devices to simplify operations that previously required a read/modify/write operation. In order for these instructions to be equally applicable to any I/O ports, with or without mixed input and output functions, the I/O ports have been designed to read the contents of the specified port data register during the Read cycle of the read/modify/write operation, rather than I/O pins as in normal read cycles. The added instructions and their format are explained in the following subparagraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and 1 of 8 bits to be set. The second byte of the instruction designates address (00-FF) of the byte or I/O port to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch on Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of 8 bits designated by a three bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8 bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

3.3 READ-ONLY-MEMORY (ROM)

The ROM consists of 1536 bytes (1.5K) mask programmable memory with an address space from FA00 to FFFF. ROM locations FFFC through FFFF are assigned for interrupt and reset vectors.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 64 bytes of read/write memory with an assigned page zero address of 0040 through 007F.

3.5 SYSTEM CLOCK

The device functions with an external clock. It is fully asynchronous in reference to the Host computer timing. The device clock frequency equals the external clock frequency. It is also made available for any external device synchronization at pin 02.

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for the Counter, the 6500 or 8080 Bus Select, and the Interrupt (INT). Its setting determines the basic configuration of the device in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-2.

The use of Counter A Mode Select is shown in Section 6.

The use of the 6500/8080 Host Bus Select is shown in Section 6.

The use of Interrupt Select is shown in Section 4.5.

The use of Bus Mode Select is shown in Sections 4.4 and 4.5.

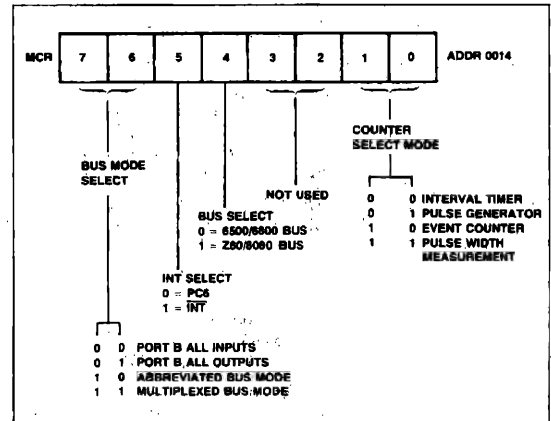


Figure 3-2. Mode Control Register Bit Allocations

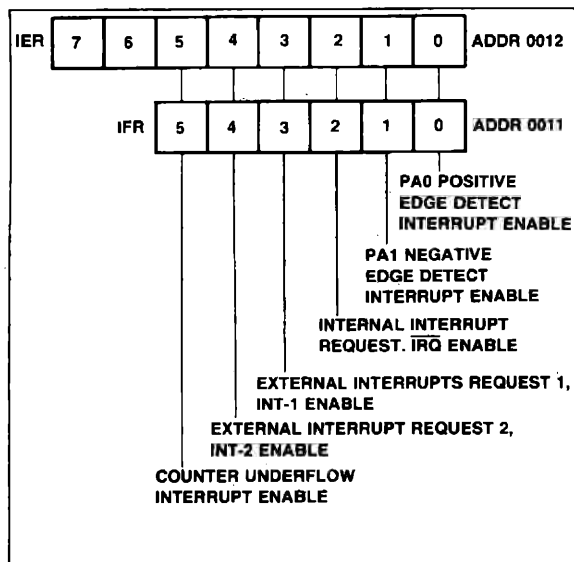


Figure 3-3. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Enable Signals

Control Signal	Description
IER 0	Positive Edge Detect, Interrupt Enable—when this bit is true, a positive going signal on PA0 will generate an IRQ and set the corresponding flag bit.
IER 1	Negative Edge Detect Interrupt Enable—when this bit is set to a "1" a negative going signal on PA1 will generate an IRQ and set the corresponding flag bit.
IER 2	Input Data Register Full Interrupt Enable—setting this bit to a "1" allows an IRQ to be generated each time the Host fills the IDR setting the IDFR bit.
IER 3	Output Data Register Full Interrupt Enable—when this bit is an interrupt request to the Host is generated each time the ODRF flag is set to a "1". (See External Interrupts, Paragraph 3.7.1). Reading the ODR clears INT-1 and ODRF flags.
IER 4	Input Data Register Empty Interrupt Enable—when this is set to a "1" an interrupt is generated to the Host each time the IDR is read by the CPU. The interrupt occurs when the IDRF flag is cleared. INT-2 is cleared when the Host reads the status flag register. (See External Interrupts, Paragraph 3.7.1).
IER 5	Counter Interrupt Enable—if enabled, an IRQ is generated whenever the Counter overflows.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{\text{IRQ}}$ interrupt request can be initiated by any or all of four possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the $\overline{\text{IRQ}}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. IFR bits 6 and 7 are indeterminate on a Read.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{\text{RES}}$. If set to a "1", an $\overline{\text{IRQ}}$ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-3 and the functions of each bit are explained in Table 3-1.

3.7.1 External Interrupts ($\overline{\text{INT}}$)

An external interrupt $\overline{\text{INT}}$ to the Host computer may be selected in two modes. (See Section 5 for information on the Host/Device interface).

OUTPUT DATA REGISTER (ODR) FULL

When IER 3 of the Interrupt Enable Register is set to a "1", the device will assert the $\overline{\text{INT}}$ (PC6) line each time it loads the ODR. The ODRF flag of the Status Flag Register and the IFR 3 of the IFR will be set to a "1" indicating the ODR is full. The ODRF and IFR 3 flags are cleared and $\overline{\text{INT}}$ is negated when the Host processor reads the ODR.

INPUT DATA REGISTER (IDR) EMPTY

When IER 4 of the Interrupt Enable Register is set to a "1", the device will assert the $\overline{\text{INT}}$ (PC6) line each time it reads the IDR. The IDRF flag of the Host Status Flag Register will be cleared and the IFR 4 flag of the IFR will be set to a "1" indicating the IDR has just been read by the device. The IFR 4 flag is cleared and $\overline{\text{INT}}$ is negated when the Host processor reads the Host Status Flag Register. $\overline{\text{RES}}$ clears the IDR and sets the IFR4 flag to indicate the register is empty.

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-4, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to

zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6502 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request (IRQ). If the I Bit is reset to logic 0, the IRQ signal will be serviced. If the bit is set to logic 1, the IRQ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET (RES) or Non-Maskable Interrupt (NMI) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit may also be set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

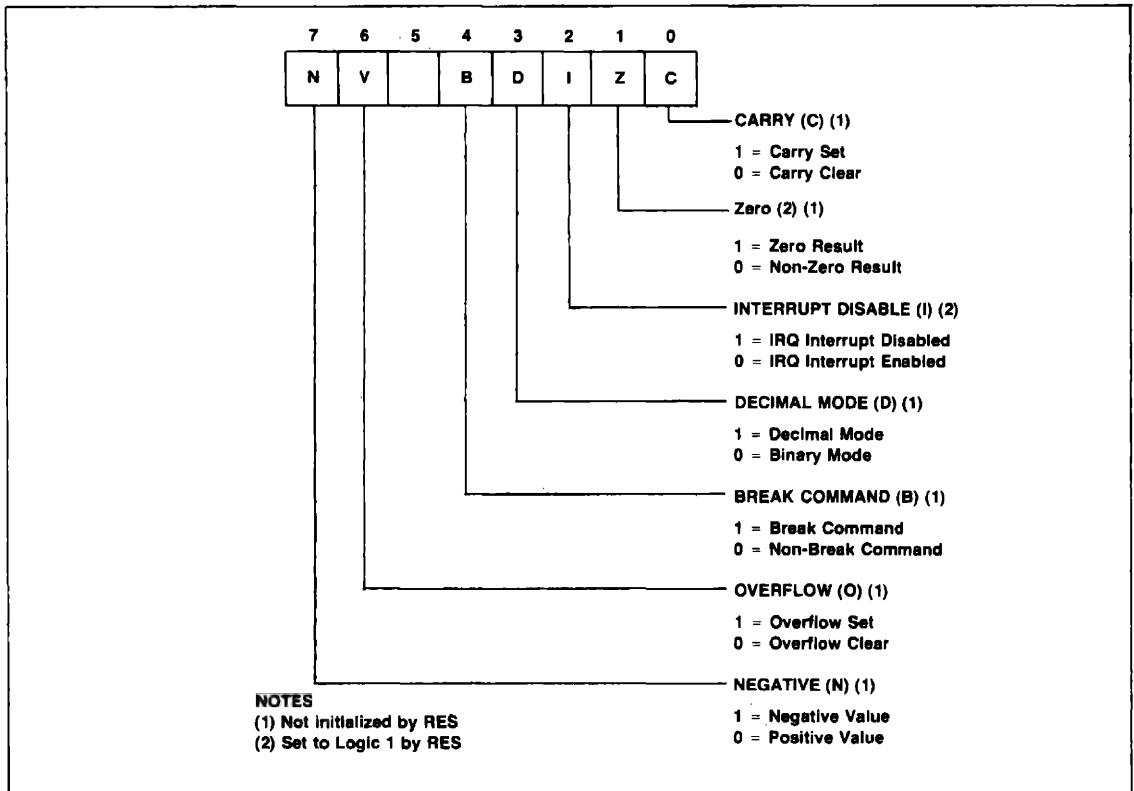


Figure 3-4. Processor Status Register

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application to the device. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{\text{IRQ}}$ service routine to be entered. If the $\overline{\text{IRQ}}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{\text{IRQ}}$ routine was entered as the result of an $\overline{\text{IRQ}}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$).

This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or -128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4

PARALLEL INPUT/OUTPUT PORTS

INPUT/OUTPUT PORTS

The IPC device provides three ports (PA, PB, and PC). The 15 lines of PA and PC are completely bidirectional, that is, there are no line grouping or port association restrictions. The eight lines of Port B may be programmed as all inputs or all outputs. Port PC, however, may be multiplexed under program control with seven other signals. Six of these signals form an address and control bus for extended addressing. The seventh signal is multiplexed with an external interrupt output, INT. All eight Port B lines are tri-state to permit their use as a data bus during extended addressing modes.

The R6500/42, a 64 pin QUIP device, has three additional ports: PE, PF, and PG. PE is outputs only. PF and PG are bidirectional.

Internal pull-up resistors (FET's with an impedance range of $3K \leq R_{pu} \leq 12K \text{ ohm}$) may be provided on ports PA and PC and ports PF & PG (R6500/42 only), as a mask option.

The direction of the I/O lines are controlled by 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 4-1. Section E.6 shows the I/O Port Timing.

Table 4-1. I/O Port Addresses

PORT	ADDRESS
A	0000
B	0001
C	0002
E	0004
F	0005
G	0006

4.1 INPUTS

Inputs for Ports A and C, and also Ports F and G of the R6500/42, are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A

low ($<0.8V$) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high ($>2.0V$) input will cause a logic 1 to be read. An RES signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port B may be all inputs or all outputs. All inputs is selected by setting bits MCR6 and MCR7 of the Mode Control Register to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, and also PF, & PG of the R6500/42. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, BBS, BBR, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru C, and Ports E thru G of the R6500/42, are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high ($>2.4V$) output while a logic 0 will force a low ($<0.4V$) output. Port B also requires that MCR6 be set to a "1" and MCR7 be set to a "0".

4.3 PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) as a standard parallel 8-bit, bit independent, I/O port, or a counter I/O line. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 can detect positive going edges, and PA1 can detect negative going edges. An edge transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the $\phi 2$ clock rate. Edge detection timing is shown in Section E.5.

Table 4-2. Port A Control & Usage

PA0-PA1 I/O		PA2 I/O		PA2 COUNTER				PA3-PA7 I/O	
		MCR0 = 0 MCR1 = 0		MCR0 = 1 MCR1 = 0		MCR0 = X MCR1 = 1			
SIGNAL		SIGNAL		SIGNAL		SIGNAL		SIGNAL	
NAME	TYPE	NAME	TYPE	NAME	TYPE	NAME	TYPE	NAME	TYPE
PA0 (1) PA1(2)	I/O I/O	PA2	I/O	CNTR	OUTPUT	CNTR	INPUT (3)	PA3-PA7	I/O

(1) POSITIVE EDGE DETECT (2) NEGATIVE EDGE DETECT (3) HARDWARE BUFFER FLOAT

4.4 PORT B (PB)

Port B can be programmed as an I/O Port, an 8-bit tri-state data bus, or as a multiplexed bus. Mode selection for Port B is made by the Mode Control Register (MCR). The Port B output drivers can be selected as tri-state output drivers by setting bit 7 of the MCR to 0 (zero) and bit 6 of the MCR to 1. An all inputs condition is created by setting both MCR6 and MCR7 to 0 (zero). Table 4-3 shows the necessary settings for the MCR to achieve the various modes for Port B. When Port B is selected to operate in the Abbreviated Mode PB0-PB7 serves as data register bits D0-D7. When Port B is selected to operate in the Multiplexed Mode data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix B) for Abbreviated and Multiplexed memory assignments. See Appendix E.3 through E.5 for Port B timing.

4.5 PORT C (PC)

Port C can be programmed as an I/O port and in conjunction with Port B, as an abbreviated bus, or as a multiplexed bus.

When used in the abbreviated or multiplexed bus modes, PC0-PC5 function as A0-A3, R/W, and EMS, respectively, as shown in Table 4-4. EMS (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0080 and 0FFF. (See Memory Map, Appendix C). The leading edge of EMS may be used to strobe the eight address lines multiplexed on Port B in the Multiplexed Bus Mode. See Appendix E.3 through E.5 for Port C timing.

4.6 PORT E, PORT F AND PORT G (PE, PF & PG) R6500/42 ONLY

Port E only operates in the Output mode. It provides a Darlington output that can source current at the high (1) level. Port F and Port G operate identically and can be programmed as bidirectional I/O ports. They have standard output capability. See Appendix E.3 through E.5 for Port E, F & Port G timing.

Table 4-3. Port B Control & Usage

R6500/41 R6500/42		I/O MODES				ABBREVIATED MODE		MULTIPLEXED MODE							
		MCR7 = 0 MCR6 = 0		MCR7 = 0 MCR6 = 1		MCR7 = 1 MCR6 = 0		MCR7 = 1 MCR6 = 1							
		SIGNAL		SIGNAL		SIGNAL		PHASE 1		PHASE 2					
		PIN #	PIN #	NAME	TYPE (1)	NAME	TYPE (2)	NAME	TYPE (3)	SIGNAL		SIGNAL			
30	49	PB0	INPUT	PB0	OUTPUT	D0	I/O	A4	OUTPUT	D0	I/O				
31	50	PB1	INPUT	PB1	OUTPUT	D1	I/O	A5	OUTPUT	D1	I/O				
32	51	PB2	INPUT	PB2	OUTPUT	D2	I/O	A6	OUTPUT	D2	I/O				
33	52	PB3	INPUT	PB3	OUTPUT	D3	I/O	A7	OUTPUT	D3	I/O				
34	53	PB4	INPUT	PB4	OUTPUT	D4	I/O	A8	OUTPUT	D4	I/O				
35	54	PB5	INPUT	PB5	OUTPUT	D5	I/O	A9	OUTPUT	D5	I/O				
36	55	PB6	INPUT	PB6	OUTPUT	D6	I/O	A10	OUTPUT	D6	I/O				
37	56	PB7	INPUT	PB7	OUTPUT	D7	I/O	A11	OUTPUT	D7	I/O				

- (1) TRI-STATE BUFFER IS IN HIGH IMPEDANCE MODE (2) TRI-STATE BUFFER IS IN ACTIVE MODE
(3) TRI-STATE BUFFER IS IN ACTIVE MODE ONLY DURING THE PHASE 2 PORTION OF A WRITE CYCLE

Table 4-4. Port C Control & Usage

R6500/41	R6500/42	I/O MODE		ABBREVIATED MODE		MULTIPLEXED MODE	
		MCR7 = 0 MCR6 = X		MCR7 = 1 MCR6 = 0		MCR7 = 1 MCR6 = 1	
		SIGNAL		SIGNAL		SIGNAL	
PIN #	PIN #	NAME	TYPE (1)	NAME	TYPE (2)	NAME	TYPE (2)
13	16	PC0	I/O	A0	OUTPUT	A0	OUTPUT
14	17	PC1	I/O	A1	OUTPUT	A1	OUTPUT
15	18	PC2	I/O	A2	OUTPUT	A2	OUTPUT
16	19	PC3	I/O	A3	OUTPUT	A3	OUTPUT
17	20	PC4	I/O	EMS	OUTPUT	EMS	OUTPUT
18	21	PC5	I/O	R/W	OUTPUT	R/W	OUTPUT
19	22	PC6*	I/O	INT*	OUTPUT	INT*	OUTPUT

- (1) RESISTIVE PULL-UP, ACTIVE BUFFER PULL-DOWN
(2) ACTIVE BUFFER PULL-UP AND PULL-DOWN

* PC6 if MCR5 = 0; INT* if MCR5 = 1

SECTION 5

HOST INTERFACE BUS

Two way data transfers are performed between the IPC and the Host microprocessor by means of the Output Data Register and the Input Data Register. The Host can also write a command to the IDR and read from the Host Status Flag Register. Table 5-1 shows the Host addressing matrix. A hardware interrupt procedure and a software polling procedure is available to control data traffic between the CPU and Host.

Table 5-1. Host Addressing Matrix

RS (A ₀)	READ	WRITE
1	HOST STATUS FLAG	COMMAND INPUT
0	DATA REG OUTPUT	DATA REG INPUT

5.1 DATA REGISTERS

The device has an 8-bit Input Data Register (IDR) and an 8-bit Output Data Register (ODR). The IDR serves as a temporary storage for commands and data from the Host to the device. When transferring data from the Host to the device, the following conditions are in effect:

- \overline{CS} is asserted
- RS (A₀) indicates command input or data input.
- The contents of the host data bus (HB0-HB7) are copied into the IDR when the appropriate Host bus write signals are asserted.

The ODR serves as a temporary storage for data from the device to the Host. When the Host is reading data from the device, the following conditions are in effect:

- \overline{CS} is asserted
- RS (A₀) input selects ODR or HSFR
- The contents of ODR or the Flag Register are placed on the host data bus (HB0-HB7) when the appropriate Host read signals are asserted.

5.2 HOST STATUS FLAG REGISTER

A Host Status Flag Register facilitates a software protocol that permits independent and uninterrupted flow of data asynchronously between the host computer and the device.

The Host Status Flag Register contains 8 flag bits that can be read at anytime by either the Host or the device. See Figure 5-1. General purpose flags F2 through F6 are serviced by the device in either read or write modes and monitored by the Host (Read Only).

Flag F1 can be read at anytime by either the host or the device. The F1 flag copies the A0 (RS) input signal during any

host write data exchange. The device can write to the F1 flag at any time.

The ODRF (Output Data Register Full) flag is set each time the device writes to the Output Data Register. The setting of the ODRF sets the device Interrupt Status Register IFR3 flag. An Output Interrupt (INT) may be generated under program control by setting IER3 in the interrupt enable register. The ODRF flag is reset only by a hardware reset or by the host performing a read on the output data register. The ODRF flag is reset following the conclusion of any host output data register read. The resetting of the ODRF causes the reset of the IFR3 flag and thus the reset of the external interrupt (INT).

The IDRF (Input Data Register Full) flag is set following the conclusion of any host write data exchange. The setting of the IDRF causes IFR2 of the device status register to be set. An internal interrupt may be generated under program control by setting IER2 in the Interrupt Enable Register. The setting of IDRF also causes IFR4 to be reset. The IDRF resets during device read of the input data register. IFR2 sets and IFR4 resets following the reset of IDRF. IFR4 may generate an external output interrupt (INT, input buffer empty), under program control by setting IER4 in the interrupt enable register.

The Host Status Flag Register is cleared by the \overline{RES} input.

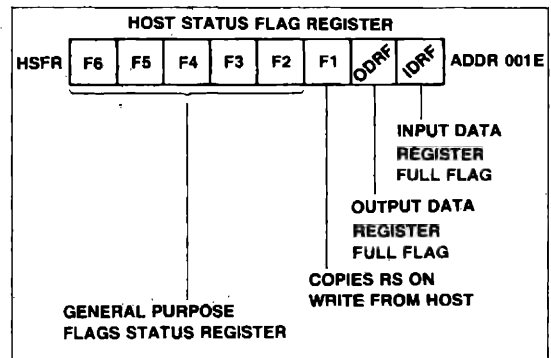


Figure 5-1. Host Status Flag Register Bit Allocation

5.3 HOST COMPUTER INTERFACE

The device will work with a variety of Host Computers. The HOST interface consists of a chip select, one address line, 2 control lines and an 8 bit three state data bus. Internal logic of the device, controlled by MCR4, configures, the address and two control lines to either a 6500 or 8080 operational methodology. The interface is completely asynchronous and will work with a Host Computer up to a 5 MHz bus transfer rate. The device clock input frequency need not be the same as the Host's. A mode control register is set to match the interface to that of the Host device as follows:

MCR4 = 0 When MCR4 is set to a logic zero, the IPC is configured to operate on a 6502/6800 type host bus. In this mode, the E input is connected to the host transfer strobe (VMA or 02 for 6800, 02 for 6500) and the R/W input is connected to the host microprocessor R/W output line. Figure 5-3 and Table 5-2, together, specify the relevant timing for read and write cycles on this type of host bus.

**Table 5-2. Host Interface
Timing Characteristics BSEL = 0 (6500)**

CHARACTERISTICS 1 AND 2 MHz	SYMBOL	MIN	MAX
CS, R/W, RS Setup Time	t_{CS}	10	—
Access Time	t_{OA}	—	90*
Data Hold Time	t_{DHR}	10	—
Control Hold Time	t_{HC}	10	—
Write Data Setup Time	t_{WDS}	75	—
Write Data Hold Time	t_{DHW}	10	—
Write Stroke Width	t_{WR}	75	—

***NOTE:**

90 ns when loading = 130 pf + 1 TTL LOAD and
75 ns when loading = 90 pf + 1 TTL LOAD.

MCR4 = 1 When MCR4 is set to a logic one, the IPC is configured for operation on an 8080/Z80 type bus. In this mode, the RD input is used as a read strobe and the WR input is connected to the write strobe of the host microprocessor bus. Figure 5-4 and Table 5-3 show the relevant timing characteristics for this mode of operation.

**Table 5-3. Host Interface
Timing Characteristics BSEL = 1 (8080)**

CHARACTERISTICS 1 AND 2 MH	SYMBOL	MIN	MAX
CS, A0 Setup Time	t_{CS}	10	—
Data Access Time on Read	t_{OA}	—	90*
Data Hold Time	t_{DHR}	10	—
Control Hold Time	t_{HC}	10	—
Write Data Setup Time	t_{WDS}	75	—
Write Data Hold Time	t_{DHW}	10	—
Write Stroke Width	t_{WR}	75	—

***NOTE:**

90 ns when loading = 130 pf + 1 TTL LOAD and
75 ns when loading = 90 pf + 1 TTL LOAD.

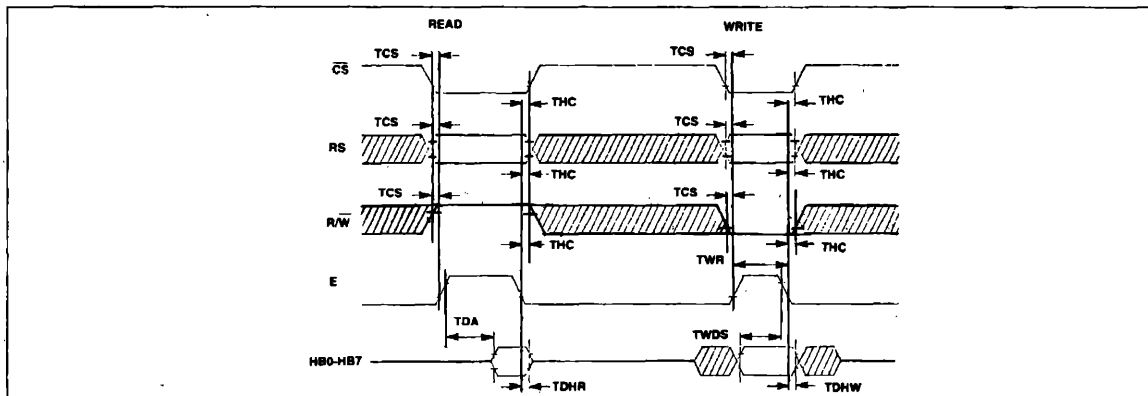


Figure 5-3. Timing Diagram—Host Interface (MCR4 = 0) (6500 Version)

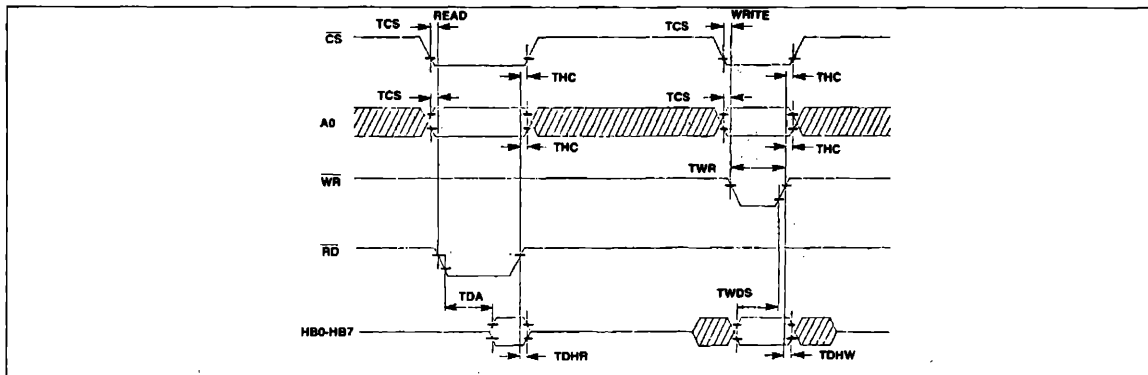


Figure 5-4. Timing Diagram—Host Interface (MCR4 = 1) (8080 Version)

SECTION 6

COUNTER/TIMERS

The device contains a 16-bit counter and a 16-bit latch associated with it. The counter can be independently programmed to operate in one of four modes:

Counter

- Pulse width measurement
- Pulse Generation
- Interval Timer
- Event Counter

Operating modes of the Counter are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA2 is selected for Counter I/O.

6.1 COUNTER

The Counter consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter (LC), Upper Counter (UC), Lower Latch (LL), and Upper Latch (UL). The counter contains the count of either $\phi 2$ clock pulses or external events, depending on the counter mode selected. The contents of the Counter may be read any time by executing a read at location 0018 for the Upper Counter and at location 001A or location 0019 for the Lower Counter. A read at location 0019 also clears the Counter Underflow Flag (IFR5).

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch at location 0018 and the Lower Latch at location 001A. In either case, the contents of the accumulator are copied into the applicable latch register.

The Counter can be started at any time by writing to address 0019. The contents of the accumulator will be copied into the Upper Latch before the contents of the 16-bit latch are transferred to the Counter. The counter is set to the latch value whenever the Counter underflows. When the Counter decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter Underflow Flag (IFR 5) will be set to "1". This bit may be cleared by reading the Lower Counter at location 0019, by writing to address location 0019, or by RES.

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are $\phi 2$ clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line (PA2).

The Counter is set to the Interval Timer Mode (00) when a RES signal is generated.

6.1.1 Interval Timer Mode

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).
2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 0019, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the $\phi 2$ clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore $1\mu\text{s}$ to 65.535 ms at the 1 MHz $\phi 2$ clock rate or $0.5\mu\text{s}$ to 32.767 ms at the 2 MHz $\phi 2$ clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting IRQ interrupt requests in the counter IRQ interrupt routine.

When the Counter decrements from 0000, the Counter Underflow (IFR5) is set to logic 1. If the Counter Interrupt Enable Bit (IER5) is also set, an IRQ interrupt request will be generated. The Counter Underflow bit in the Interrupt Flag Register can be examined in the IRQ interrupt routine to determine that the IRQ was generated by the Counter Underflow.

While the timer is operating in the Interval Timer Mode, PA2 operates as a PA I/O.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

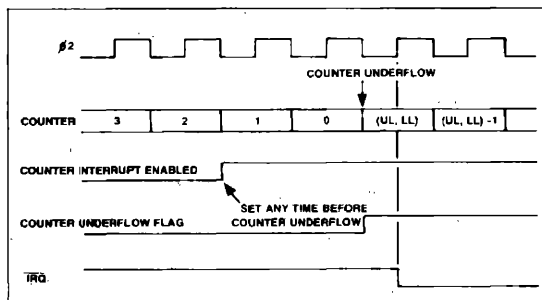


Figure 6-1. Interval Timer Timing Diagram

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the PA2 line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter Underflow occurs, or a write is performed to address 0019.

The normal output waveform is a symmetrical square-wave. The PA2 output is initialized high when entering the mode and transitions low when writing to 0019.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode PA2 is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter Underflow bit (IER5) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

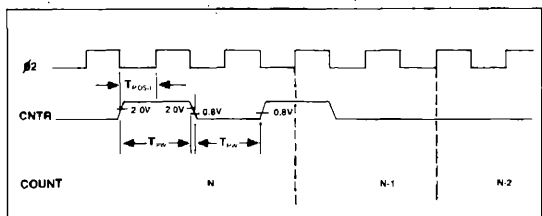
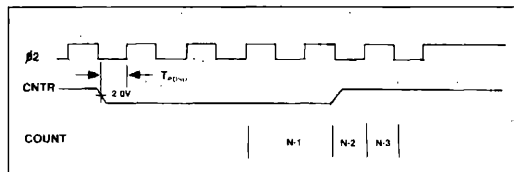


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the PA2 line. The Counter decrements by one count at the $\phi 2$ clock rate as long as the PA2 line is held in the low state. The Counter is stopped when PA2 is in the high state.

The Counter underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the PA2 pin is held low. After the counter is stopped by a high level on PA2, the count will hold as long as PA2 remains high. Any further low levels on PA2 will again cause the counter to count down from its present value. The state of the PA2 line can be determined by testing the state of PA2.



SECTION 7

POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER ON TIMING

After application of VCC power to the device, $\overline{\text{RES}}$ must be held low for at least eight stable $\phi/2$ clock cycles after VCC reaches operating range.

Figure 7-1 illustrates the power turn-on waveforms. External clock stabilization time is typically 20ms.

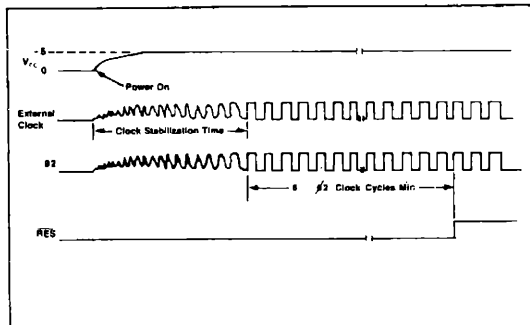


Figure 7-1. Power Turn-On Timing Detail

7.2 POWER-ON RESET

The occurrence of $\overline{\text{RES}}$ going from low to high will cause the device to set the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiate a reset vector fetch at address FFFC and FFFD to begin user program execution. All of the I/O ports will be initialized to the high (logic 1) state. All bits of the Control Register will be cleared causing the Interval Timer counter mode to be selected and causing all interrupt enabled bits to be reset.

7.3 RESET ($\overline{\text{RES}}$) CONDITIONS

When $\overline{\text{RES}}$ is driven from low to high the device is put in a reset state causing the registers and I/O ports to be set as shown in Table 7-1.

Table 7-1. $\overline{\text{RES}}$ Initialization of I/O Ports and Registers

BIT NO. →	7	6	5	4	3	2	1	0
REGISTERS								
Processor Status	—	—	—	—	—	1	—	—
Mode Control (MCR)	0	0	0	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	1	0	0	0	0
Host Status Flag	0	0	0	0	0	0	0	0
Input Data	0	0	0	0	0	0	0	0
Output Data	0	0	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1
PC Latch	1	1	1	1	1	1	1	1
PE Latch	1	1	1	1	1	1	1	1
PF Latch	1	1	1	1	1	1	1	1
PG Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

7.4 INITIALIZATION

Any initialization process for the device should include a $\overline{\text{RES}}$ as indicated in the preceding paragraphs. After stabilization of the external clock (if a power on situation) an initialization routine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls and Counter as required
5. Clear Interrupts.

A typical initialization routine could be as follows:

```
LDX    Load stack pointer starting address into
        X Register
TXS    Transfer X Register value to Stack Pointer
CLD    Clear Decimal Mode
SEC    Set Carry Flag
. . . . Set-up Mode Control,
. . . . Counter, special function
. . . . registers and Clear RAM as required
CLI    Clear Interrupts
```

APPENDIX A

EXPANDED R6502 INSTRUCTION SET

This appendix contains a summary of the R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Document 29650 N30.

The four instructions notated with a * are added instructions for the IPC devices which enhance the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

MNEMONIC	INSTRUCTION	MNEMONIC	INSTRUCTION
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative	NOP	No Operation
BCC	Branch on Carry Clear		
BCS	Branch on Carry Set	ORA	"OR" Memory with Accumulator
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator	PHA	Push Accumulator on Stack
BMI	Branch on Result Minus	PHP	Push Processor Status on Stack
BNE	Branch on Result not Zero	PLA	Pull Accumulator from Stack
BPL	Branch on Result Plus	PLP	Pull Processor Status from Stack
BRK	Force Break		
BVC	Branch on Overflow Clear		
BVS	Branch on Overflow Set		
CLC	Clear Carry Flag	*RMB	Reset Memory Bit
CLD	Clear Decimal Mode	ROL	Rotate One Bit Left (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit	ROR	Rotate One Bit Right (Memory or Accumulator)
CLV	Clear Overflow Flag	RTI	Return from Interrupt
CMP	Compare Memory and Accumulator	RTS	Return from Subroutine
CPX	Compare Memory and Index X		
CPY	Compare Memory and Index Y		
DEC	Decrement Memory by One	SBC	Subtract Memory from Accumulator with Borrow
DEX	Decrement Index X by One	SEC	Set Carry Flag
DEY	Decrement Index Y by One	SED	Set Decimal Mode
		SEI	Set Interrupt Disable Status
EOR	"Exclusive-Or" Memory with Accumulator	*SMB	Set Memory Bit
		STA	Store Accumulator in Memory
		STX	Store Index X in Memory
		STY	Store Index Y in Memory
INC	Increment Memory by One	TAX	Transfer Accumulator to Index X
INX	Increment Index X by One	TAY	Transfer Accumulator to Index Y
INY	Increment Index Y by One	TSX	Transfer Stack Pointer to Index X
		TXA	Transfer Index X to Accumulator
JMP	Jump to New Location	TXS	Transfer Index X to Stack Register
JSR	Jump to New Location Saving Return Address	TYA	Transfer Index Y to Accumulator

3

NOTES	LEGEND	
1. Add 1 to N if page boundary is crossed	X = Index X	M ₆ = Memory Bit 6
2. Add 1 to N if branch occurs to same page	Y = Index Y	A ₆ = Add
3. Add 2 to N if branch occurs to different page	A = Accumulator	S ₆ = Subtract
4. Carry not = Borrow	M ₆ = Memory per effective address	Λ = And
5. If in decimal mode Z flag is invalid	M ₇ = Memory per stack pointer	Or
6. accumulator must be checked on zero result	m = Selector zero page memory bit	Exclusive Or
7. Effects 8-bit data field of the specified zero page address.	M ₇ = Memory Bit 7	n = Number of bytes
		#

A.3 INSTRUCTION CODE MATRIX

0	BRK	—OP Code
0	Implied	—Addressing Mode
1	7	—Instruction Bytes; Machine Cycles

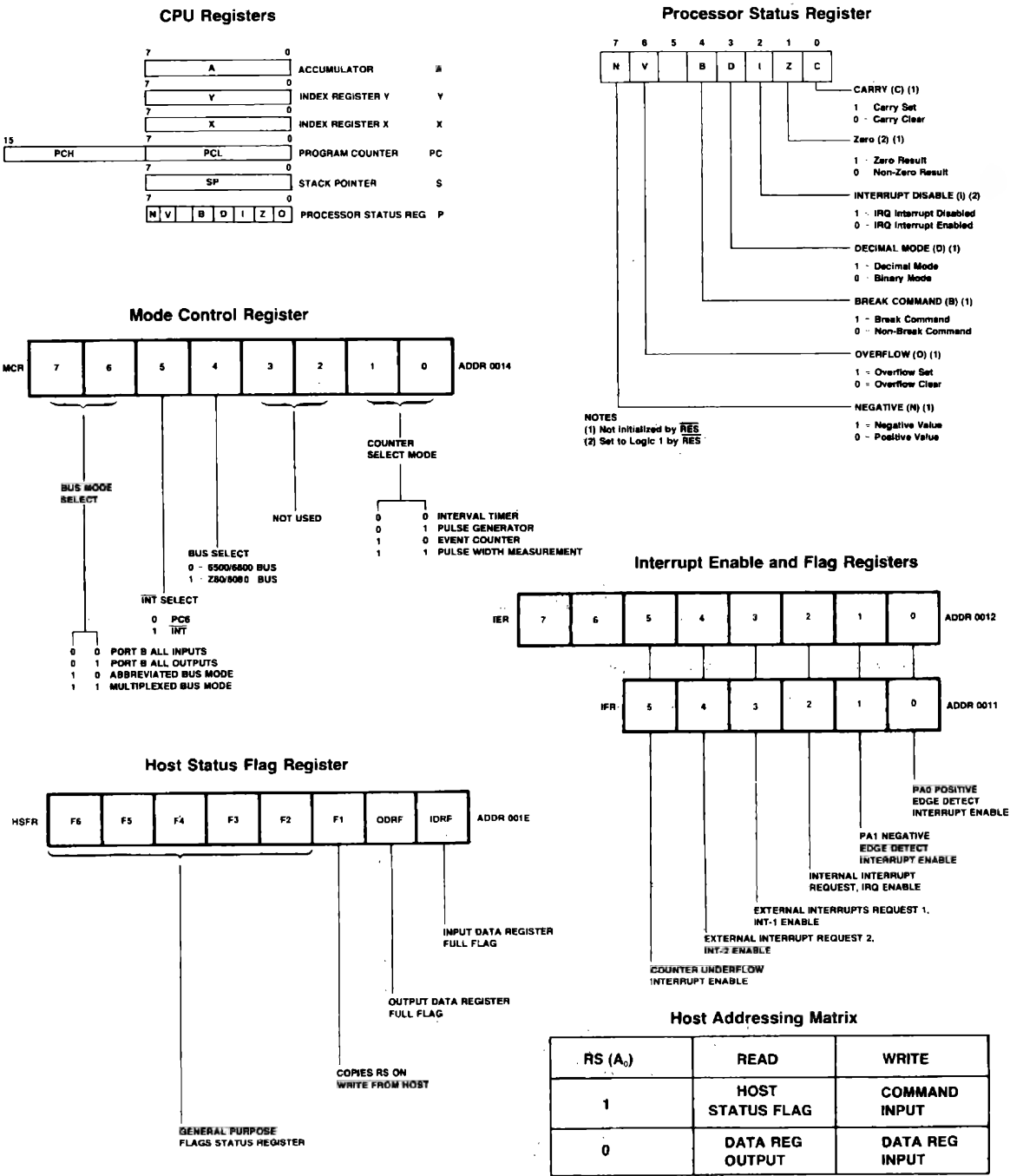
MSD	LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBS0 ZP 3 5**	0
1	1	BPL Relative 2 2**	ORA (IND, Y) 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBS1 ZP 3 5**	1
2	2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBS2 ZP 3 5**	2
3	3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBS3 ZP 3 5**	3
4	4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBS4 ZP 3 5**	4
5	5	BVC Relative 2 2**	EOR (IND, Y) 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBS5 ZP 3 5**	5
6	6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBS6 ZP 3 5**	6
7	7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBS7 ZP 3 5**	7
8	8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	B	BCS Relative 2 2**	LDA (IND, Y) 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	D	BNE Relative 2 2**	CMP (IND, Y) 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	F	BEQ Relative 2 2**	SBC (IND, Y) 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

*Add 1 to N if page boundary is crossed.

**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

APPENDIX B

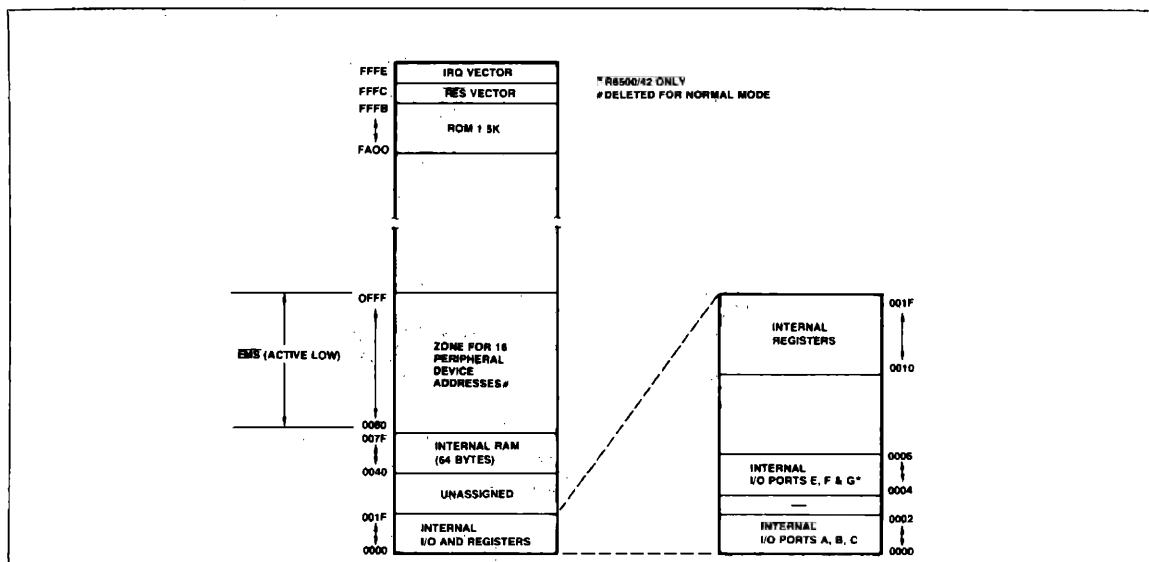
KEY REGISTER SUMMARY



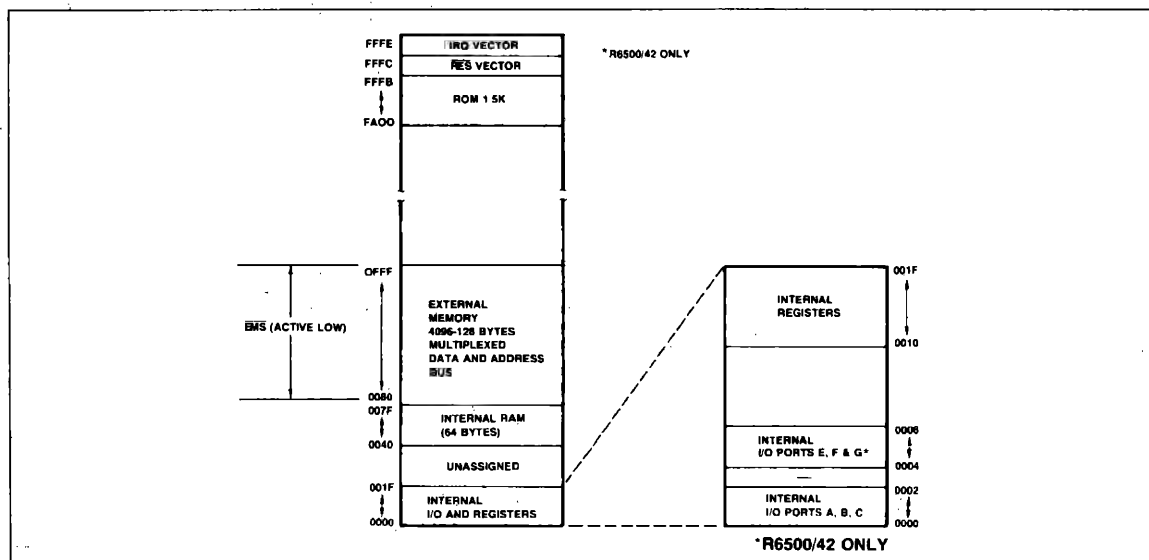
APPENDIX C

MEMORY MAPS AND ADDRESS AND PIN ASSIGNMENTS

C.1 ABBREVIATED BUS MODE MEMORY MAP



C.2 MULTIPLEXED BUS MODE MEMORY MAP



C.3 I/O AND INTERNAL REGISTER ADDRESSES

ADDRESS	READ	WRITE
001F	---	---
1E	Host Status Flag Register	Host Status Flag Register
1D	---	---
1C	Input Data Register (IDR)	Output Data Register (ODR)
1B	---	---
1A	Lower Counter	Lower Latch
19	Lower Counter & Clear Flag (IFR5)	Upper Latch/Transfer Latch to Counter & Clear Flag (IFR5)
18	Upper Counter	Upper Latch
17	---	---
16	---	---
15	---	---
14	Mode Control Register	Mode Control Register
13	---	---
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	---
10	Read "FF"	Clear Int Flag Bit
0F	---	---
0E	---	---
0D	---	---
0C	---	---
0B	---	---
0A	---	---
09	---	---
08	---	---
07	---	---
06	Port G (R6500/42 only)	Port G (R6500/42 only)
05	Port F (R6500/42 only)	Port F (R6500/42 only)
04	Port E (R6500/42 only)	Port E (R6500/42 only)
03	---	---
02	Port C	Port C
01	Port B	Port B
00	Port A	Port A

C.4 MULTIPLE FUNCTION PIN ASSIGNMENTS

PIN NUMBER R6500/41	PIN NUMBER R6500/42	I/O FUNCTION	ABBREVIATED PORT FUNCTION	MULTIPLEXED PORT FUNCTION
13	16	PC0	A0	A0
14	17	PC1	A1	A1
15	18	PC2	A2	A2
16	19	PC3	A3	A3
17	20	PC4	R/W	R/W
18	21	PC5	EMS	EMS
19	22	PC6/INT	PC6/INT	PC6/INT
30	49	PB0	D0	A4/D0
31	50	PB1	D1	A5/D1
32	51	PB2	D2	A6/D2
33	52	PB3	D3	A7/D3
34	53	PB4	D4	A8/D4
35	54	PB5	D5	A9/D5
36	55	PB6	D6	A10/D6
37	56	PB7	D7	A11/D7

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Commercial	T_A	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

($V_{CC} = 5V \pm 5\%$, $V_{SS} = 0$)

Parameter	Symbol	Min.	Typ.	Max.	Units
Power Dissipation (Outputs High) Commercial 0°C to +70°C	P_D	—	500	—	mW
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	—	+0.8	Vdc
Input Leakage Current $V_{in} = 0$ to 5.25 Vdc	I_{IN}	-10.0	—	+10.0	μ Adc
Input Low Current ($V_{IL} = 0.4$ Vdc)	I_{IL}	—	-1.0	-1.6	mAdc
Output High Voltage ($V_{CC} = \min$, $I_{LOAD} = -100 \mu$ Adc)	V_{OH}	+2.4	—	V_{CC}	Vdc
Output High Voltage ($V_{CC} = \min$)	V_{CMOS}	$V_{CC} - 30\%$	—	V_{CC}	Vdc
Output Low Voltage ($V_{CC} = \min$, $I_{LOAD} = 1.6$ mAdc)	V_{OL}	—	—	+0.4	Vdc
Output High Current (Sourcing) ($V_{OH} = 2.4$ Vdc)	I_{OH}	-100	—	—	μ Adc
Output Low Current (Sinking) ($V_{OL} = 0.4$ Vdc)	I_{OL}	1.6	—	—	mAdc
Darlington Current Drive, PE* ($V_{OH} = 1.5$ Vdc)	I_{OH}	-1.0	—	—	mAdc
Output Low Current, PE* ($V_{OL} = 0.4$ Vdc)	I_{OL}	1.6	—	—	mAdc
Input Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz) PA, PB, PC, PF*, PG*	C_{in}	—	—	10	pF
Output Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz)	C_{OUT}	—	—	10	pF
I/O Port Resistance PA0-PA7, PC0-PC6 PF0-PF7, PG0-PG7	R_L	3.0	6.0	11.5	K Ω

Note: Negative sign indicates outward current flow, positive indicates inward flow. $V_{CC} = 5V \pm 5\%$.

*R6500/42 only.

APPENDIX E

TIMING REQUIREMENTS AND CHARACTERISTICS

E.1 GENERAL NOTES

- 1 V_{CC} 5V \pm 5%, 0 C \leq TA \leq 70 C
2. A valid V_{CC} — RES sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pf maximum, except as noted below:

PA, PB

PB, PC (I/O Modes Only)

PB, PC (ABB and Mux Mode)

— 50pf maximum

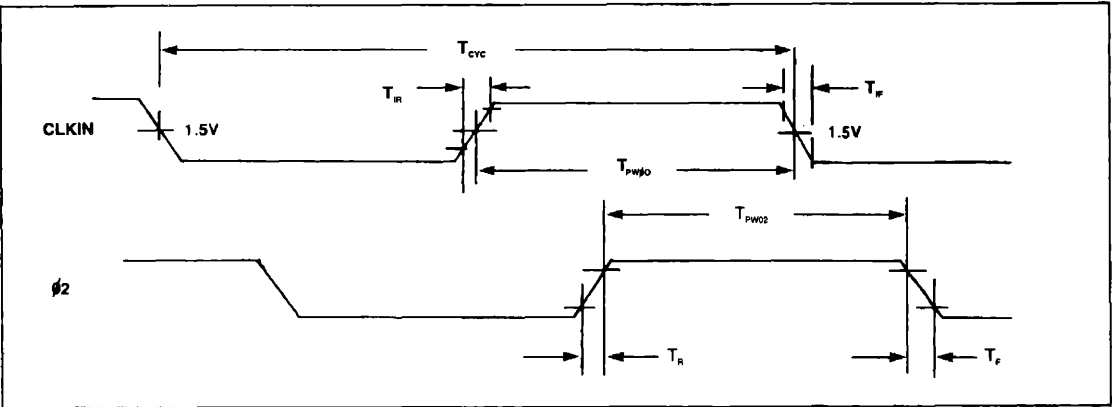
— 50pf maximum

— 130pf maximum

E.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{cyc}	Cycle Time	1000	10 μ s	500	10 μ s
T_{pwq0}	CLKIN Input Clock Pulse Width	475	—	240	—
T_{pw02}	Output Clock Pulse Width at Minimum T_{cyc}	T_{pwq0}	$T_{pwq0} + 25$	T_{pwq0}	$T_{pwq0} + 20$
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10

3



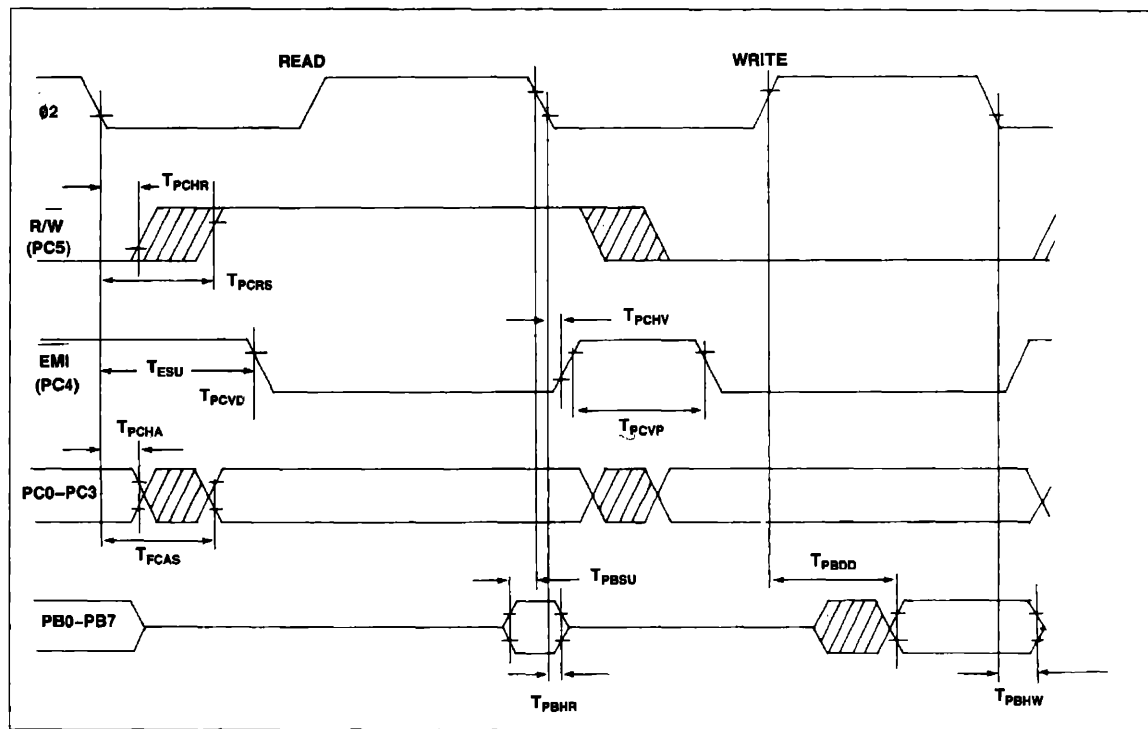
E.3 ABBREVIATED MODE TIMING—PB AND PC

(MCR 5 = 1, MCR 6 = 0, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC3) Address Setup Time	—	225	—	140
T_{PBSU}	(PB) Data Setup Time	50	—	35	—
T_{PBHR}	(PB) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PB) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PB) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC3) Address Hold Time	30	—	30	—
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC4) $\overline{EM\overline{S}}$ Hold Time	10	—	10	—
T_{PCVP}	(PC4) $\overline{EM\overline{S}}$ Stabilization Time	30	—	30	—
T_{ESV}	$\overline{EM\overline{S}}$ Setup Time	—	350	—	210

NOTE 1: Values assume PC0-PC5 have the same capacitive load.

E.3.1 Abbreviated Mode Timing Diagram



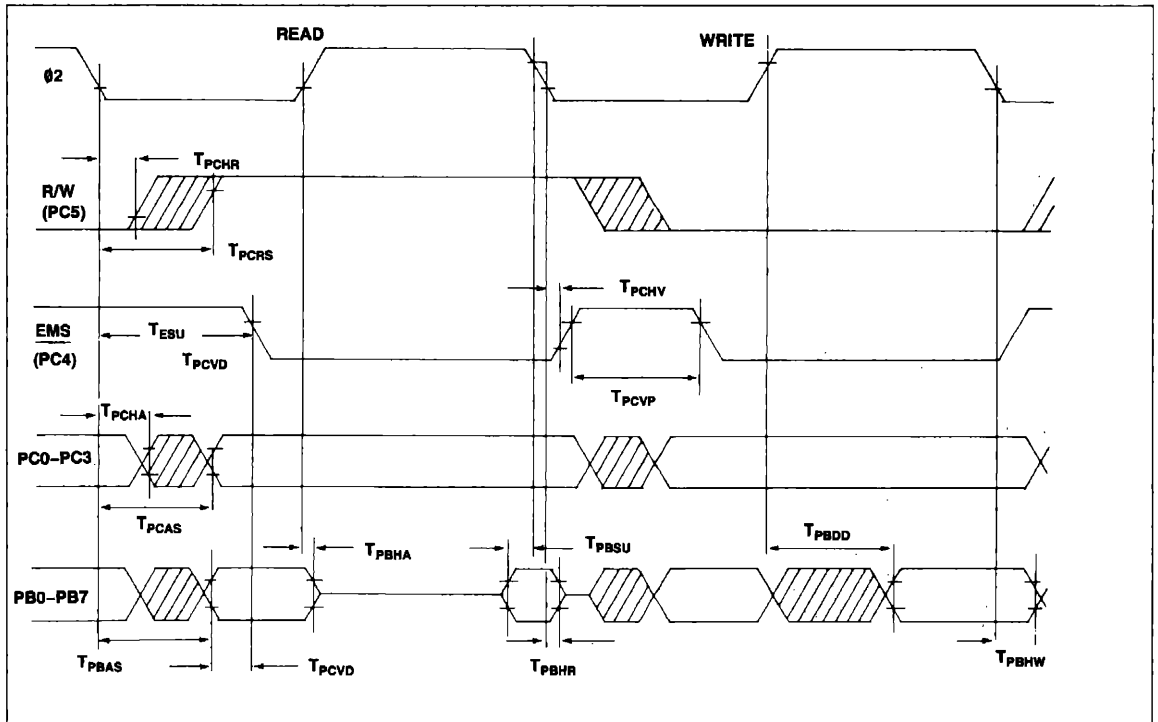
E.4 MULTIPLEXED MODE TIMING—PB AND PC

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC3) Address Setup Time	—	225	—	140
T_{PBAS}	(PB) Address Setup Time	—	225	—	140
T_{PBSU}	(PB) Data Setup Time	50	—	35	—
T_{PBHR}	(PB) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PB) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PB) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC3) Address Hold Time	30	—	30	—
T_{PBHA}	(PB) Address Hold Time	0	100	0	80
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC4) EMS Hold Time	10	—	10	—
$T_{PCVD}^{(1)}$	(PC4) Address to EMS Delay Time	30	—	30	—
T_{PCVP}	(PC4) EMS Stabilization Time	30	—	30	—
T_{ESU}	EMS Setup Time	—	350	—	210

NOTE 1: Values assume PC0-PC5 have the same capacitive load.

E.4.1 Multiplex Mode Timing Diagram

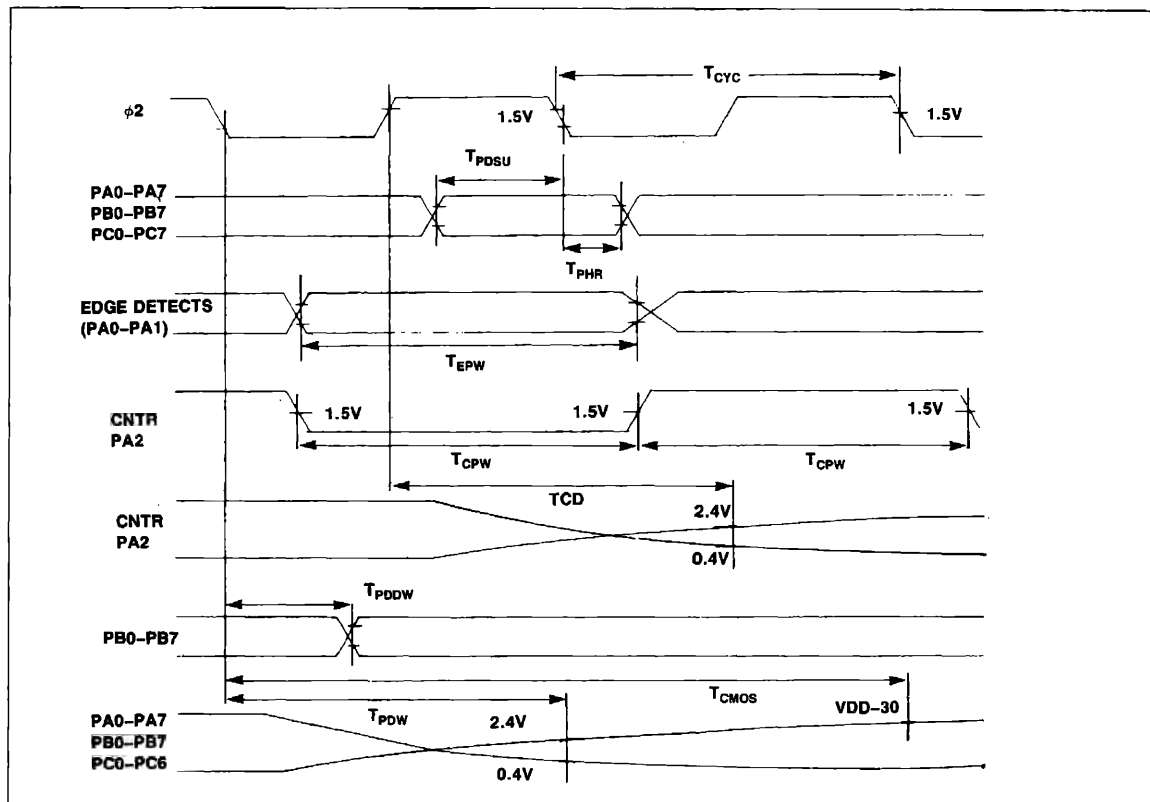


E.5 I/O, EDGE DETECT AND COUNTER TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
$T_{PDW}^{(1)}$	Internal Write to Peripheral Data Valid	—	500	—	500
$T_{CMOS}^{(1)}$	PA, PC CMOS	—	1000	—	1000
T_{PDOW}	PB	—	175	—	150
T_{PDSU}	Peripheral Data Setup Time				
	PA, PC	200	—	200	—
T_{PHR}	PB	50	—	50	—
T_{PHR}	Peripheral Data Hold Time				
	PA, PC	75	—	75	—
T_{EPW}	PB	10	—	10	—
T_{EPW}	PA0-PA1 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CPW}	Counter				
	PA2 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
$T_{CO}^{(1)}$	PA2 Output Delay	—	500	—	500

NOTE 1 Maximum Load Capacitance: 50pF Passive Pull-Up Required

E.5.1 I/O, Edge Detect, Counter





R65/41EB AND R65/41EAB BACKPACK EMULATORS

INTRODUCTION

The Rockwell R65/41EB and R65/41EAB Backpack Emulator is the PROM prototyping version of the 8-bit, masked-ROM R6500/41 one-chip microcomputer. Like the R6500/41, the backpack device is totally upward/downward compatible with all members of the R6500/41 family. It is designed to accept standard 5-volt, 24-pin EPROMs or ROMs directly, in a socket on top of the Emulator. This packaging concept allows a standard EPROM to be easily removed, re-programmed, then reinserted as often as desired.

The backpack devices have the same pinouts as the masked-ROM R6500/41 microcomputer. These 40 pins are functionally and operationally identical to the pins on the R6500/41. The R6500/41 Microcomputer Product Description (Rockwell Document No. 29651N38, Order No. 2135) includes a description of the interface signals and their functions. Whereas the masked-ROM R6500/41 provides 1.5K bytes of read-only memory, the R65/41EB will address 4.0K bytes of external program memory. This extra memory accommodates program patches, test programs or optional programs during breadboard and prototype development states.

ORDERING INFORMATION

Backpack Emulator

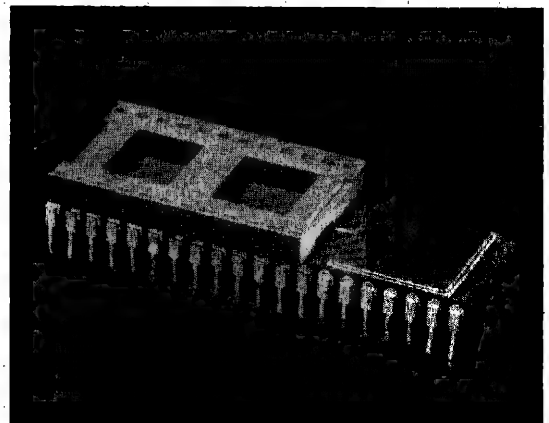
Part Number	Memory Capacity	Compatible Memories	Temperature Range and Speed
R65/41EB	4K × 8	2732	0°C to 70°C 1 MHz
R65/41EAB	4K × 8	2732A	0°C to 70°C .2 MHz

Support Products

Part Number	Description
S65-101	SYSTEM 65 Microcomputer Development System
M65-040	PROM Programmer Module
M65-131	1-MHz R6500/41 Personality Module
M65-132	2-MHz R6500/41 Personality Module
RDC-1001	Rockwell Development Center
RDC-131	1 MHz R6500/41 Personality Set (RDC)
RDC-132	2 MHz R6500/41 Personality Set (RDC)

FEATURES

- PROM version of the R6500/41
- All Host bus features of R6500/41
- Completely pin compatible with R6500/41 single-chip microcomputers
- Profile approaches 40-pin DIP of R6500/41
- Accepts 5 volt, 24-pin industry-standard EPROMs—4K memories—2732, 2732A
- Use as prototyping tool or for low volume production
- 4K bytes of memory capacity
- 64 × 8 static RAM
- Software compatibility with the R6500 family
- 23 bi-directional TTL compatible I/O lines
- 16 bit programmable counter/latch with four modes (interval timer, pulse generator, event counter, pulse width measurement)
- 7 interrupts (reset, two external edge sensitive, counter underflow, Host data received, Output data register full, Input data register empty).
- External time base
- Single +5V power supply



R65/41EB-R65/41EAB Backpack Emulator

CONFIGURATIONS

The Backpack Emulator is available in two different versions, to accommodate 1 MHz and 2 MHz speeds. Both versions provide 192 bytes of RAM and I/O, as well as 24 signals to support the external memory "backpack" socket.

External 4K memories with addresses of 000 to FFF, are upward translated to addresses F000 to FFFF when assembled to form the Backpack Emulator.

EXTERNAL FREQUENCY REFERENCE

The external frequency reference is an output timing signal $\phi 2$. This is an internally synchronized 1 x clock output suitable for external memory or peripheral interfacing.

I/O PORT PULLUPS

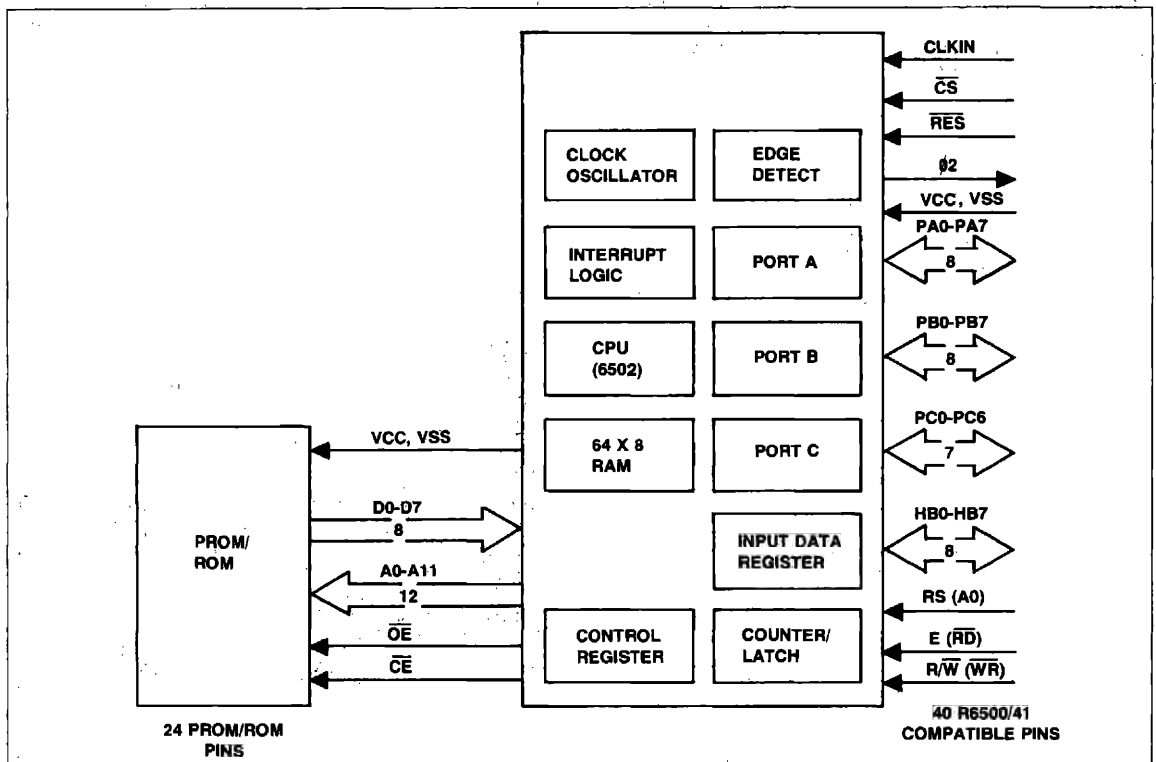
The emulator devices have internal I/O port pullup resistors on ports A and C. Port B has tri-state drivers.

PRODUCT SUPPORT

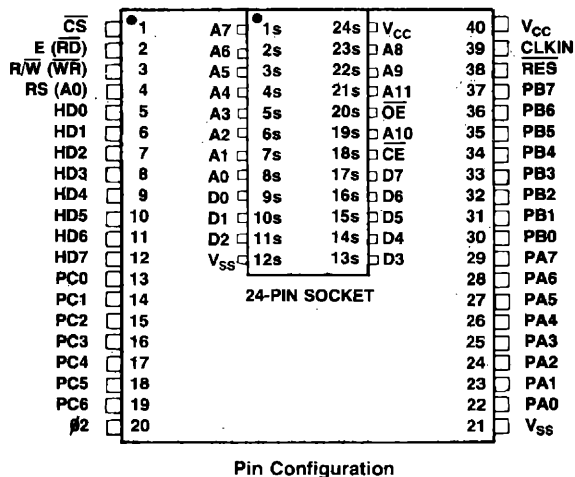
The Backpack Emulator is just one of the products that Rockwell offers to facilitate system and program development for the R6500/41.

The SYSTEM 65 Microcomputer Development System with R6500/41 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/41 Personality Module allows total system test and evaluation. With the optional PROM Programmer, SYSTEM 65 can also be used to program EPROMs for the development activity. When PROM programs have been finalized, the PROM device can be sent to Rockwell for masking into the 1.5K ROM of the R6500/41.

In addition to support products, Rockwell offers regularly-scheduled designer courses at regional centers.



R65/41EB Interface Diagram



(1) PIN 21 is V_{cc} for R65/41EB or A11 for R65/41EAB

BACKPACK MEMORY SIGNAL DESCRIPTION

Signal Name	Pin No.	Description
D0-D7	9S-11S, 13S-17S	Data Bus Lines. All instruction and data transfers take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.
A0-A9, A10, A11	1S-8S, 22S, 23S, 19S, 21S	Address Bus Lines. The address bus lines are buffered by push/pull type drivers that can drive one standard TTL load.
\overline{CE}	18S	Chip Enable.
\overline{OE}	20S	Memory Enable Line. This signal provides the output enable for the memory to place information on the data bus lines. This signal is driven by the R/W signal from the CPU and then inverted to form \overline{OE} . This signal is driven by the inverted address line A11. The \overline{OE} signal will be low for addresses greater than 0FFF.
V_{cc}	24S	Main Power Supply +5V. This pin is tied directly to pin 40 (V_{cc}).
V_{ss}	12S	Signal and Power Ground (zero volts). This pin is tied directly to pin 21 (V_{ss}).

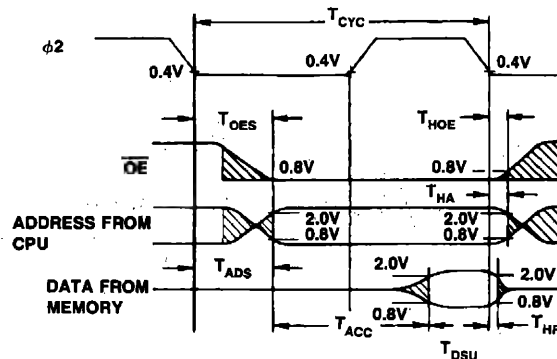
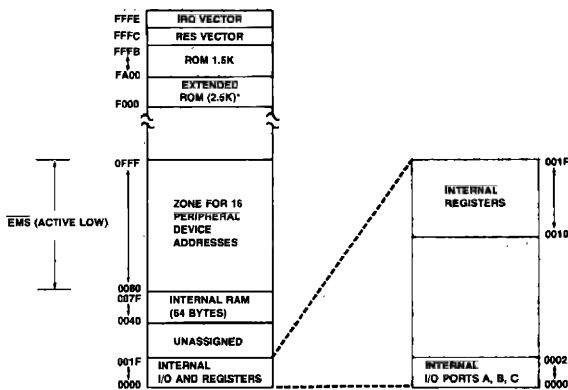
I/O AND INTERNAL REGISTER ADDRESSES

Address	Read	Write
001F	---	---
1E	Host Status Flag Register	Host Status Flag Register
1D	---	---
1C	Input Data Register (IDR)	Output Data Register (ODR)
1B	---	---
1A	Lower Counter	Lower Latch
19	Lower Counter & Clear Flag (IFR5)	Upper Latch/Transfer Latch to Counter & Clear Flag (IFR5)
18	Upper Counter	Upper Latch
17	---	---
16	---	---
15	---	---
14	Mode Control Register	Mode Control Register
13	---	---
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	---
10	Read "FF"	Clear Int Flag Bit
03 thru 0F	---	---
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

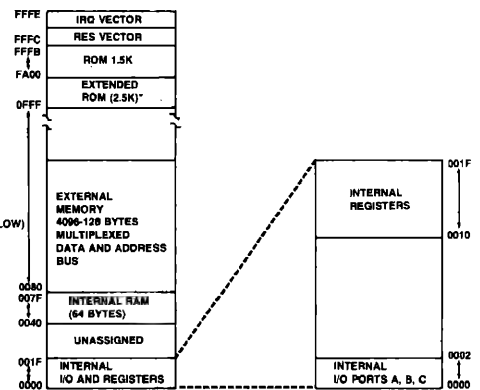
READ TIMING CHARACTERISTICS

Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
\overline{OE} and \overline{CE} setup time from CPU	T_{OES}	—	225	—	140	ns
Address setup time from CPU	T_{ADS}	—	225	—	140	ns
Memory read access time	T_{ACC}	—	700	—	315	ns
Data set up time	T_{DSU}	50	—	35	—	ns
Data hold time—Read	T_{HR}	10	—	10	—	ns
Address hold time	T_{HA}	30	—	30	—	ns
\overline{OE} and \overline{CE} hold time	T_{HOE}	30	—	30	—	ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μ s

READ TIMING WAVEFORMS

ABBREVIATED BUS
MODE MEMORY MAP

*Not available for masked ROM R6503/41.

MULTIPLEXED BUS
MODE MEMORY MAP

*Not available for masked ROM R6503/41.

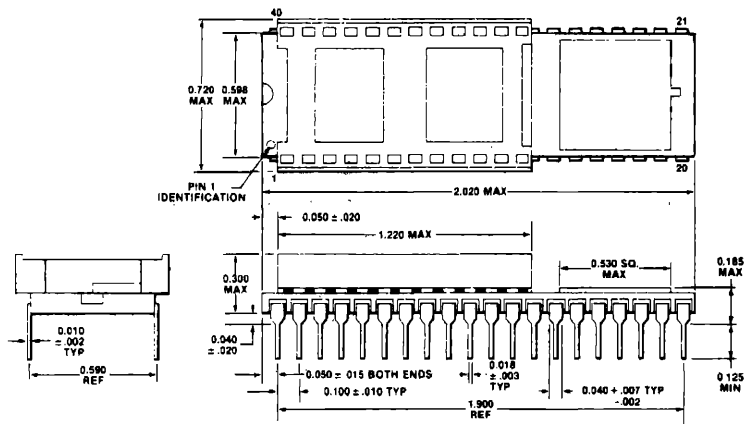
*R6500/42 ONLY

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ± 5%, V_{SS} = 0, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Threshold Voltage D0-D7	V _{IHT}	V _{SS} + 2.0	—	—	V _{dc}
Input Low Threshold Voltage D0-D7	V _{ILT}	—	—	V _{SS} + 0.8	V _{dc}
Three-State (Off State) Input Current (V = 0.4 to 2.4V, V _{CC} = 5.25V) D0-D7	I _{TSI}	—	—	± 10	μA
Output High Voltage (I _{LOAD} = 100μ Adc, V _{CC} = 4.75V) D0-D7, A0-A11, \overline{OE} , \overline{CE}	V _{OH}	V _{SS} + 2.4	—	—	V _{dc}
Output Low Voltage (I _{LOAD} = 1.6 mAdc, V _{CC} = 4.75V) D0-D7, A0-A11, \overline{OE} , \overline{CE}	V _{OL}	—	—	V _{SS} + 0.4	V _{dc}
Power Dissipation (less EPROM)	P _D	—	0.50	—	W
Capacitance (V _{in} = 0, T _A = 25°C, f = 1 MHz) D0-D7 (High Impedance State) Input Capacitance	C C _{out} C _{in}	— — —	— — —	10 10	pF
I/O Port Pull-up Resistance	R _L	3.0	6.0	11.5	kohm

3



40-Pin Backpack Package



R6541Q AND R6500/43

INTELLIGENT PERIPHERAL CONTROLLERS

SECTION 1

INTRODUCTION

1.1 FEATURES OF THE R6541Q & R6500/43

- Directly compatible with 6500, 6800, 8080, and Z80 bus families
- Asynchronous Host interface that allows independent clock operation
- Input, Output and Status Registers for CPU/Host data transfer
- Status register for CPU/Host data transfer operations
- Interrupt or polled data interchange with Host
- Enhanced 6502 CPU
 - Four new bit manipulation instructions
 - Set Memory Bit (SMB)
 - Reset Memory Bit (RMB)
 - Branch on Bit Set (BBS)
 - Branch on Bit Reset (BBR)
 - Decimal and binary arithmetic modes
 - 13 addressing modes
 - True indexing
- 256-byte mask-programmable ROM*
- 64-byte static RAM
- 23 TTL-compatible I/O lines
- A 16-bit programmable counter/timer, with latch
 - Pulse width measurement
 - Pulse generation
 - Interval timer
 - Event counter
- Eight interrupts
 - Two edge-sensitive lines; one positive, one negative
 - Reset
 - Counter Underflow
 - Host data received
 - Output Data Register full
 - Input Data Register empty
 - Non-maskable
- Multiplexed bus expandable to 4K bytes of external memory

* R6541Q has no ROM.

- Unmultiplexed Address and Data buses for 4K of Peripheral I/O expansion
- 68% of the instructions are executed in less than 2 μ s @ 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 64-pin QUIP

NOTE

This document describes both the R6541Q and R6500/43. In the text, the terms IPC or device will be used when describing both parts. See Section 1.3 for a description of the options available for the R6500/13 and the fixed features of the R6541Q.

1.2 SUMMARY

The Rockwell R6541Q and R6500/43 One-Chip Intelligent Peripheral Controllers (IPC) are general purpose, programmable interface I/O devices designed for use with a variety of 8-bit and 16-bit microprocessor systems. They have an enhanced R6502 CPU, an optional 256 by 8-bit ROM, 64 by 8-bit RAM, three I/O ports with multiplexed special functions, a multi-function timer, and a full 4K address and data buses all contained within a 64-pin Quad-in-line package.

In both versions, special interface registers allow these IPC devices to function as peripheral controllers for the 6500, 6800, Z80, 8080, and other 8-bit or 16-bit host microcomputer systems.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the device a leading candidate for IPC computer applications.

Rockwell supports development of the R6541Q and R6500/43 with the System 65 Microcomputer Development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This product description assumes that the reader is familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Order Number 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Document Order Number 202).

1.3 CUSTOMER OPTIONS

The R6500/43 microcomputer is available with the following customer specified mask options.

- Option 1 with or without a 256 byte ROM
- Option 2 Reset Vector at FFFC or 0FFC
- Option 3 Port A with or without internal pull-up resistors
- Option 4 Port C with or without internal pull-up resistors

All options should be specified on an R6500/43 order form.

The R6541Q has no customer specified mask options. It has the following characteristics.

- Without ROM
- Reset Vector at FFFC
- No internal pull-up resistors on any Port (PA or PC)

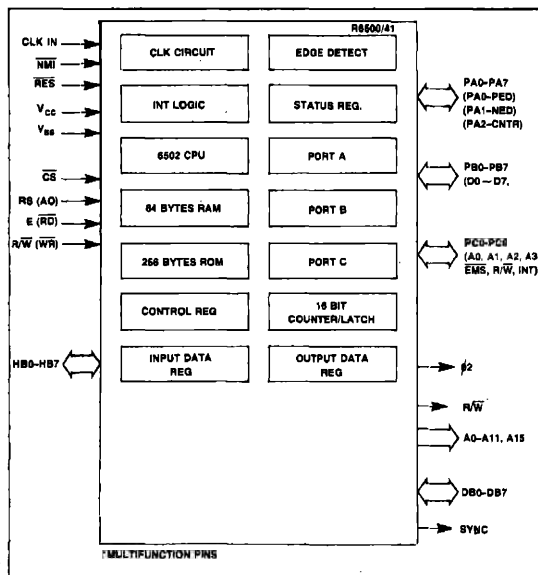


Figure 2-1. Interface Diagram

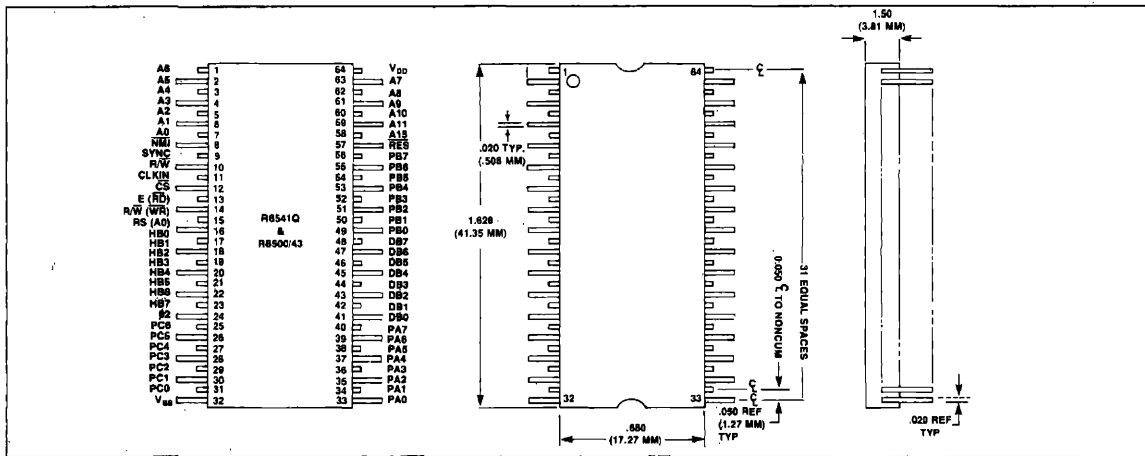


Figure 2-2. R6541Q & R6500/43 Pin Out Designation (64 PIN QUIP)

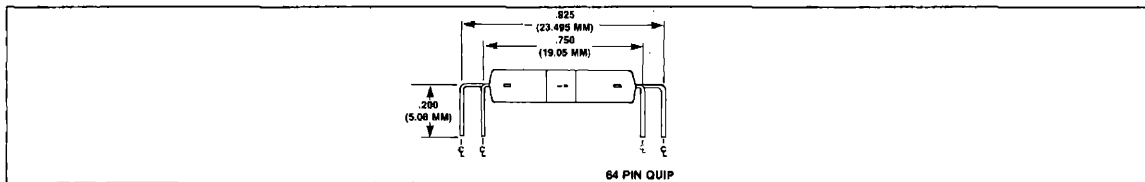


Figure 2-3. R6541Q & R6500/43 Dimensional Outline

SECTION 2

R6500/41 INTERFACE REQUIREMENTS

This section describes the interface requirements for the Intelligent Peripheral Controller. Figure 2-1 is the Interface Diagram for the devices. Figure 2-2 shows the pin out configuration and Table 2-1 describes the function of each pin of the

devices. Figure 2-3 shows the mechanical dimensions of the devices. Section 5 describes the Host computer interface protocol and timing requirements.

Table 2-1. Pin Description

SIGNAL NAME	PIN NO. R6541Q & R6500/43	DESCRIPTION	SIGNAL NAME	PIN NO. R6541Q & R6500/43	DESCRIPTION
CLKIN	11	Symmetrical square wave 100 KHz to 2 MHz, TTL compatible input.	PB0-PB7	49-56	8 bit I/O port used for either input or output. Each line consists of an active transistor to V_{SS} and an active pull-up to V_{CC} . This port becomes a tri-state data bus, D0-D7, in the Abbreviated or Multiplexed Bus Mode. D0-D7 are multiplexed with address lines A4-A11 in the Multiplexed Bus Mode.
$\phi 2$	24	Output timing signal—This is an internally synchronized $1 \times$ clock output suitable for external memory or peripheral interfacing.	PC0-PC6	31-25	7 bit I/O port used for either input or output. Each line consists of an active transistor to V_{SS} and an optional passive pull-up to V_{CC} . The pins PC0 to PC5 are multiplexed with address and control signals for use in abbreviated and multiplex modes. PC6 is multiplexed with INT and is program selectable. In these two modes PC0-PC5 have active pull-ups.
\overline{RES}	57	The reset input is used to initialize the device. Section 7 describes the process and conditions of the \overline{RES} procedure.	A0-A11, A15	7-1 63-58	Thirteen address lines used to address a complete 8K external address space.
VCC	64	Power supply input (+5V)	DB0-DB7	41-48	Eight bidirectional data bus lines used to transmit data to and from external memory.
VSS	32	Signal and power ground (0V).	SYNC	9	SYNC is a positive going signal for the full clock cycle whenever the CPU is performing an OP CODE fetch.
\overline{CS}	12	Chip select pin for host interface.	R/W	10	Controls the direction of data transfer between the CPU and the external 65K address space. The signal is high when reading and low when writing.
RS (A0)	15	Register select input pin used by the Host processor to indicate that information being written into the IPC is a data or command byte or to indicate that information being read from the IPC is a status or data byte.			
E (\overline{RD})	13	Host timing control signal for data register write and read.			
R/W (\overline{WR})	14	Host timing control signal for data register write and read.			
HB0-HB7	16-23	Data bus between Host and IPC data input and output registers.			
\overline{NMI}	8	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated with the CPU.			
PA0-PA7	33-40	8 bit I/O port used for either input or output. Each line consists of an active transistor to V_{SS} and an optional passive pull-up to V_{CC} . The two lower bits PA0 and PA1 also serve as edge detect inputs. PA2 is time shared with the 16 bit Counter Input or output pin, CNTR, and is mode selected.			

SECTION 3

SYSTEM ARCHITECTURE

This section provides a functional description of the IPC device. Functionally, the device consists of a CPU, RAM and optional ROM memories, three parallel I/O ports (actually 23 I/O lines), counter/latch circuit, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The internal CPU of the device is an enhanced R6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, or an internal IRQ interrupt. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time

data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 007F-0040. Normal usage calls for the initialization of the Stack Pointer at 007F.

3.1.4 Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is initialized each time an instruction fetch is executed and is advanced at the beginning of each low level of the Clock In pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

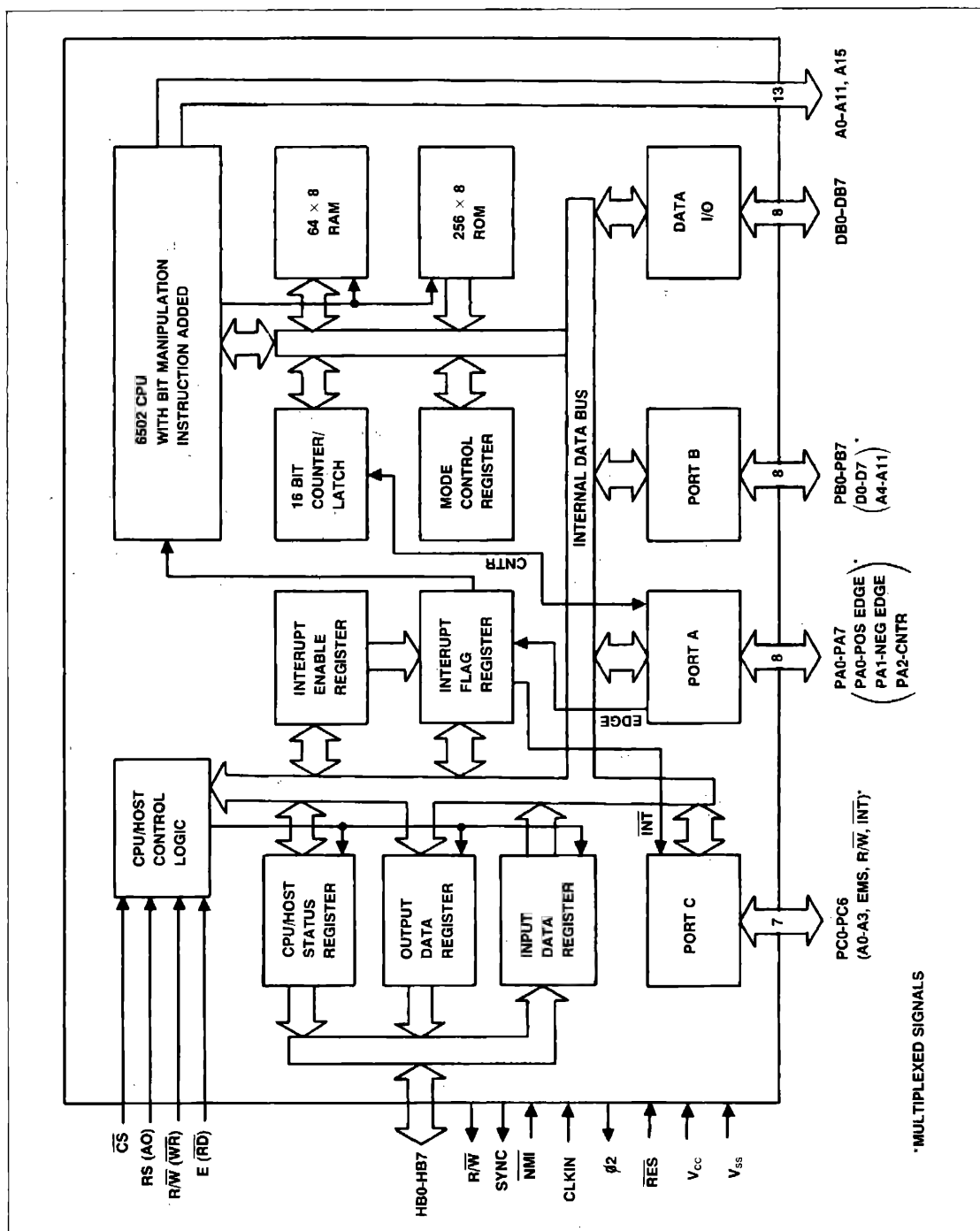


Figure 3-1. R6541Q & R6500/43 Block Diagram

3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts: RES, NMI, and IRQ. IRQ is generated by any one of four conditions: Counter Overflow, Positive Edge Detect, Negative Edge Detect, and Input Data Register Full.

3.2 NEW INSTRUCTIONS

In addition to the standard 6502 instruction set, four instructions have been added to the devices to simplify operations that previously required a read/modify/write operation. In order for these instructions to be equally applicable to any I/O ports, with or without mixed input and output functions, the I/O ports have been designed to read the contents of the specified port data register during the Read cycle of the read/modify/write operation, rather than I/O pins as in normal read cycles. The added instructions and their format are explained in the following subparagraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and 1 of 8 bits to be set. The second byte of the instruction designates address (00-FF) of the byte or I/O port to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch on Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of 8 bits designated by a three bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8 bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

3.3 READ-ONLY-MEMORY (ROM)

The optional ROM consists of 256 bytes mask programmable memory with an address space from 0F00 to 0FFF. ROM locations FFFA through FFFF are assigned for interrupt vectors. The Reset vector can be optionally at 0FFC or 0FFD.

The R6541Q has no ROM and its reset vector is at 0FFC.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 64 bytes of read/write memory with an assigned page zero address of 0040 through 007F.

3.5 SYSTEM CLOCK

The device functions with an external clock. It is fully asynchronous in reference to the Host computer timing. The device clock frequency equals the external clock frequency. It is also made available for any external device synchronization at pin 02.

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for the Counter, the 6500 or 8080 Bus Select, and the Interrupt (INT). Its setting determines the basic configuration of the device in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-2.

The use of Counter A Mode Select is shown in Section 6.

The use of the 6500/8080 Host Bus Select is shown in Section 6.

The use of Interrupt Select is shown in Section 4.5.

The use of Bus Mode Select is shown in Sections 4.4 and 4.5.

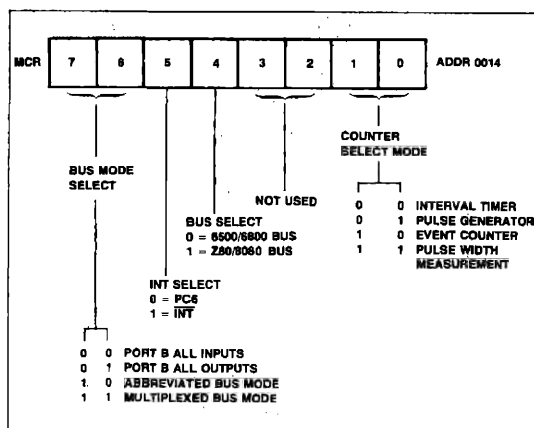


Figure 3-2. Mode Control Register Bit Allocations

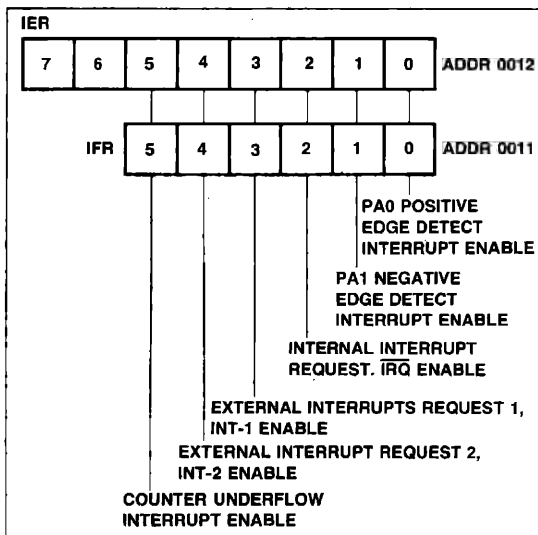


Figure 3-3. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Enable Signals

Control Signal	Description
IER 0	Positive Edge Detect, Interrupt Enable—when this bit is true, a positive going signal on PA0 will generate an IRQ and set the corresponding flag bit.
IER 1	Negative Edge Detect Interrupt Enable—when this bit is set to a "1" a negative going signal on PA1 will generate an IRQ and set the corresponding flag bit.
IER 2	Input Data Register Full Interrupt Enable—setting this bit to a "1" allows an IRQ to be generated each time the Host fills the IDR setting the IDFR bit.
IER 3	Output Data Register Full Interrupt Enable—when this bit is an interrupt request to the Host is generated each time the ODRF flag is set to a "1". (See External Interrupts, Paragraph 3.7.1). Reading the ODR clears INT-1 and ODRF flags.
IER 4	Input Data Register Empty interrupt Enable—when this is set to a "1" an interrupt is generated to the Host each time the IDR is read by the CPU. The interrupt occurs when the IDRF flag is cleared. INT-2 is cleared when the Host reads the status flag register. (See External Interrupts, Paragraph 3.7.1).
IER 5	Counter Interrupt Enable—if enabled, an IRQ is generated whenever the Counter overflows.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{\text{IRQ}}$ interrupt request can be initiated by any or all of four possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the $\overline{\text{IRQ}}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. IFR bits 6 and 7 are indeterminate on a Read.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{\text{RES}}$. If set to a "1", an $\overline{\text{IRQ}}$ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-3 and the functions of each bit are explained in Table 3-1.

3.7.1 External Interrupts ($\overline{\text{INT}}$)

An external interrupt $\overline{\text{INT}}$ to the Host computer may be selected in two modes. (See Section 5 for information on the Host/Device interface).

OUTPUT DATA REGISTER (ODR) FULL

When IER 3 of the Interrupt Enable Register is set to a "1", the device will assert the $\overline{\text{INT}}$ (PC6) line each time it loads the ODR. The ODRF flag of the Status Flag Register and the IFR 3 of the IFR will be set to a "1" indicating the ODR is full. The ODRF and IFR 3 flags are cleared and $\overline{\text{INT}}$ is negated when the Host processor reads the ODR.

INPUT DATA REGISTER (IDR) EMPTY

When IER 4 of the Interrupt Enable Register is set to a "1", the device will assert the $\overline{\text{INT}}$ (PC6) line each time it reads the IDR. The IDRF flag of the Host Status Flag Register will be cleared and the IFR 4 flag of the IFR will be set to a "1" indicating the IDR has just been read by the device. The IFR 4 flag is cleared and $\overline{\text{INT}}$ is negated when the Host processor reads the Host Status Flag Register. $\overline{\text{RES}}$ clears the IDR and sets the IFR4 flag to indicate the register is empty.

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-4, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to

zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6502 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request (IRQ). If the I Bit is reset to logic 0, the IRQ signal will be serviced. If the bit is set to logic 1, the IRQ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET (\overline{RES}) or Non-Maskable Interrupt (NMI) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit may also be set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

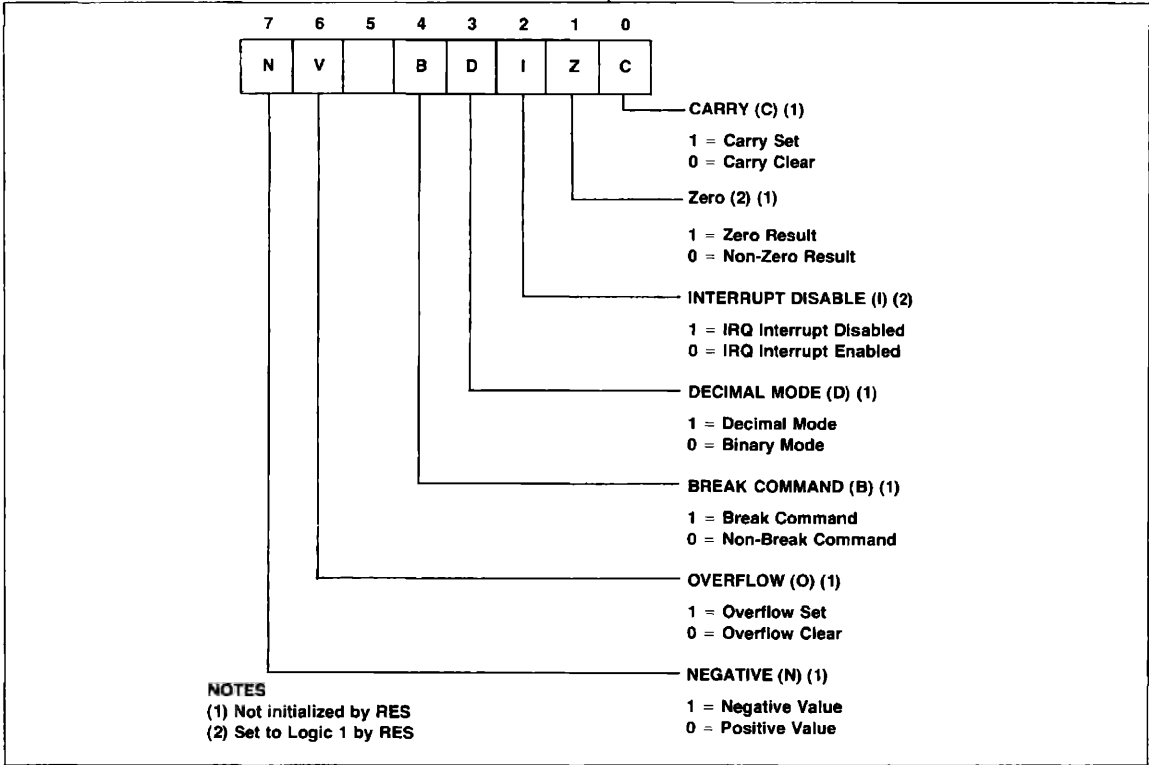


Figure 3-4. Processor Status Register

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application to the device. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{\text{IRQ}}$ service routine to be entered. If the $\overline{\text{IRQ}}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{\text{IRQ}}$ routine was entered as the result of an $\overline{\text{IRQ}}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$).

This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or -128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4

PARALLEL INPUT/OUTPUT PORTS

INPUT/OUTPUT PORTS

The IPC device provides three ports (PA, PB, and PC). The 15 lines of PA and PC are completely bidirectional, that is, there is no line grouping or port association restrictions. The eight lines of Port B may be programmed as all inputs or all outputs. Port PC, however, may be multiplexed under program control with seven other signals. Six of these signals form an address and control bus for extended addressing. The seventh signal is multiplexed with an external interrupt output, $\overline{\text{INT}}$. All eight Port B lines are tri-state to permit their use as a data bus during extended addressing modes.

Internal pull-up resistors (FET's with an impedance range of $3K \leq R_{pu} \leq 12K \text{ ohm}$) may be provided on ports PA and/or PC. The R6541Q does not have these resistors.

The direction of the I/O lines are controlled by 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 4-1. If a part is being used to emulate a R6500/42 the ports must be provided in external circuitry and addressed through locations 0004-0006.

Table 4-1. I/O Port Addresses

PORT	ADDRESS
A	0000
B	0001
C	0002
E	0004
F	0005
G	0006

} R6500/42 only

4.1 INPUTS

Inputs for Ports A and C, and also Ports F and G if emulating the R6500/42, are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low ($<0.8V$) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high

($>2.0V$) input will cause a logic 1 to be read. An $\overline{\text{RES}}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port B may be all inputs or all outputs. All inputs is selected by setting bits MCR6 and MCR7 of the Mode Control Register to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, and also PF, & PG of an emulated R6500/42. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, BBS, BBR, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru C, and emulated Ports E thru G of the R6500/42, are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high ($>2.4V$) output while a logic 0 will force a low ($<0.4V$) output. Port B also requires that MCR6 be set to a "1" and MCR7 be set to a "0".

4.3 PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) as a standard parallel 8-bit, bit independent, I/O port, or a counter I/O line. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 can detect positive going edges, and PA1 can detect negative going edges. An edge transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the $\phi 2$ clock rate. Edge detection timing is shown in Section E.5.

Table 4-2. Port A Control & Usage

PA0-PA1 I/O		PA2 I/O		PA2 COUNTER				PA3-PA7 I/O	
		MCR0 = 0 MCR1 = 0		MCR0 = 1 MCR1 = 0		MCR0 = X MCR1 = 1			
SIGNAL		SIGNAL		SIGNAL		SIGNAL		SIGNAL	
NAME	TYPE	NAME	TYPE	NAME	TYPE	NAME	TYPE	NAME	TYPE
PA0 (1)	I/O	PA2	I/O	CNTR	OUTPUT	CNTR	INPUT (3)	PA3-PA7	I/O
PA1(2)	I/O								

(1) POSITIVE EDGE DETECT (2) NEGATIVE EDGE DETECT (3) HARDWARE BUFFER FLOAT

4.4 PORT B (PB)

Port B can be programmed as an I/O Port, an 8-bit tri-state data bus, or as a multiplexed bus. Mode selection for Port B is made by the Mode Control Register (MCR). The Port B output drivers can be selected as tri-state output drivers by setting bit 7 of the MCR to 0 (zero) and bit 6 of the MCR to 1. An all inputs condition is created by setting both MCR6 and MCR7 to 0 (zero). Table 4-3 shows the necessary settings for the MCR to achieve the various modes for Port B. When Port B is selected to operate in the Abbreviated Mode PB0-PB7 serves as data register bits D0-D7. When Port B is selected to operate in the Multiplexed Mode data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix B) for Abbreviated and Multiplexed memory assignments. See Appendix E.3 through E.5 for Port B timing.

4.5 PORT C (PC)

Port C can be programmed as an I/O port and in conjunction with Port B, as an abbreviated bus, or as a multiplexed bus. When used in the abbreviated or multiplexed bus modes, PC0-PC5 function as A0-A3, R/W, and EMS, respectively, as shown in Table 4-4. EMS (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0080 and 0FFF. (See Memory Map, Appendix C). The leading edge of EMS may be used to strobe the eight address lines multiplexed on Port B in the Multiplexed Bus Mode. See Appendix E.3 through E.5 for Port C timing.

Table 4-3. Port B Control & Usage

R6541Q & R6500/43	I/O MODES				ABBREVIATED MODE		MULTIPLEXED MODE			
	MCR7 = 0 MCR6 = 0		MCR7 = 0 MCR6 = 1		MCR7 = 1 MCR6 = 0		MCR7 = 1 MCR6 = 1			
	SIGNAL		SIGNAL		SIGNAL		PHASE 1		PHASE 2	
	PIN #	NAME	TYPE (1)	NAME	TYPE (2)	NAME	TYPE (3)	SIGNAL		SIGNAL
NAME								TYPE (2)	NAME	TYPE (3)
49	PB0	INPUT	PB0	OUTPUT	D0	I/O	A4	OUTPUT	D0	I/O
50	PB1	INPUT	PB1	OUTPUT	D1	I/O	A5	OUTPUT	D1	I/O
51	PB2	INPUT	PB2	OUTPUT	D2	I/O	A6	OUTPUT	D2	I/O
52	PB3	INPUT	PB3	OUTPUT	D3	I/O	A7	OUTPUT	D3	I/O
53	PB4	INPUT	PB4	OUTPUT	D4	I/O	A8	OUTPUT	D4	I/O
54	PB5	INPUT	PB5	OUTPUT	D5	I/O	A9	OUTPUT	D5	I/O
55	PB6	INPUT	PB6	OUTPUT	D6	I/O	A10	OUTPUT	D6	I/O
56	PB7	INPUT	PB7	OUTPUT	D7	I/O	A11	OUTPUT	D7	I/O

- (1) TRI-STATE BUFFER IS IN HIGH IMPEDANCE MODE (2) TRI-STATE BUFFER IS IN ACTIVE MODE
(3) TRI-STATE BUFFER IS IN ACTIVE MODE ONLY DURING THE PHASE 2 PORTION OF A WRITE CYCLE

Table 4-4. Port C Control & Usage

R6541Q & R6500/43	I/O MODE		ABBREVIATED MODE		MULTIPLEXED MODE	
	MCR7 = 0 MCR6 = X		MCR7 = 1 MCR6 = 0		MCR7 = 1 MCR6 = 1	
	SIGNAL		SIGNAL		SIGNAL	
PIN #	NAME	TYPE (1)	NAME	TYPE (2)	NAME	TYPE (2)
31	PC0	I/O	A0	OUTPUT	A0	OUTPUT
30	PC1	I/O	A1	OUTPUT	A1	OUTPUT
29	PC2	I/O	A2	OUTPUT	A2	OUTPUT
28	PC3	I/O	A3	OUTPUT	A3	OUTPUT
27	PC4	I/O	EMS	OUTPUT	EMS	OUTPUT
26	PC5	I/O	R/W	OUTPUT	R/W	OUTPUT
25	PC6*	I/O	INT*	OUTPUT	INT*	OUTPUT

- (1) RESISTIVE PULL-UP, ACTIVE BUFFER PULL-DOWN
(2) ACTIVE BUFFER PULL-UP AND PULL-DOWN

*PC6 if MCR5 = 0; INT if MCR5 = 1

4.7 BUS MODES

A special attribute of Port B and Port C is their capability to be configured via the Mode Control Register (see Section 3.6) into four different modes.

In the Port B All Inputs and Port B All Outputs modes the separate address and data bus are used. The difference lies in the direction of Port B—all inputs or all outputs. The receiving ports perform the normal I/O function. A15 is usually used as a chip select for external memory.

In the Abbreviated Bus Mode, the address and data lines can be used as above to emulate the R6500/41. Port B and Port C are automatically transformed into an abbreviated address bus and control signals (Port C) and a bidirectional data bus (Port B). 16 Peripheral addresses can be selected. In general usage, these 16 addresses would be distributed to several external I/O devices such as R6522 and R6520, etc., each of which may contain more than one unique address.

In the Multiplexed Bus Mode, the operation is similar to the Abbreviated Mode except that a full 4K of external addresses are provided. Port C provides the lower addresses and control signals. Port B multiplexes functions. During the first half of the cycle it contains the remaining necessary 8 address bits for 4K; during the second half of the cycle it contains a bidirectional data bus. The address bits appearing on Port B must be latched into an external holding register. The leading edge of $\overline{\text{EMS}}$, which indicates that the bus function is active, may be used for this purpose.

Figures 4-1a thru 4-1d show the possible configurations of the four bus modes. Appendix C1 shows a memory map of the port as a function of the Bus Mode and further shows which addresses are active or inactive on each of the three possible buses.

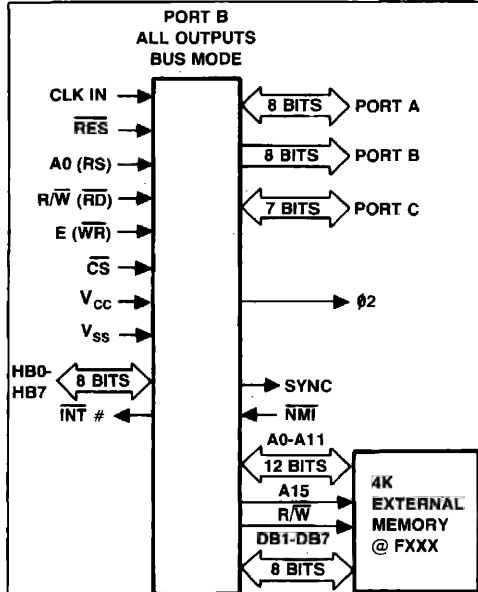


Figure 4-1a.

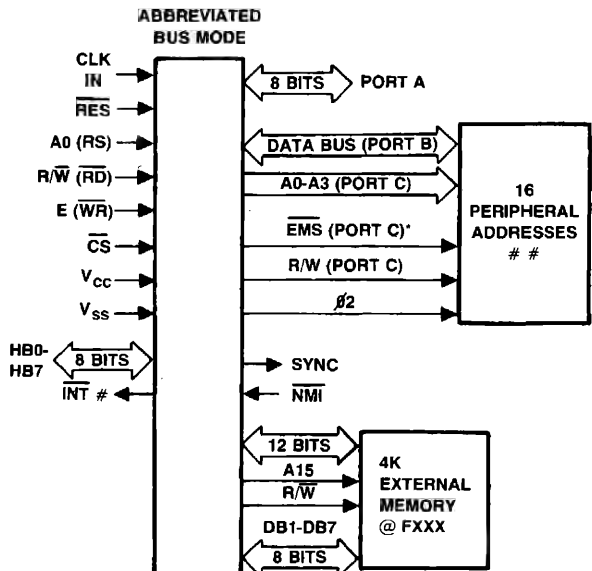


Figure 4-1c.

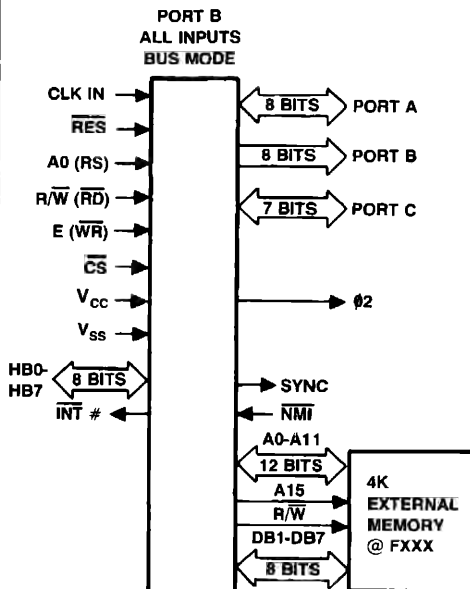


Figure 4-1b.

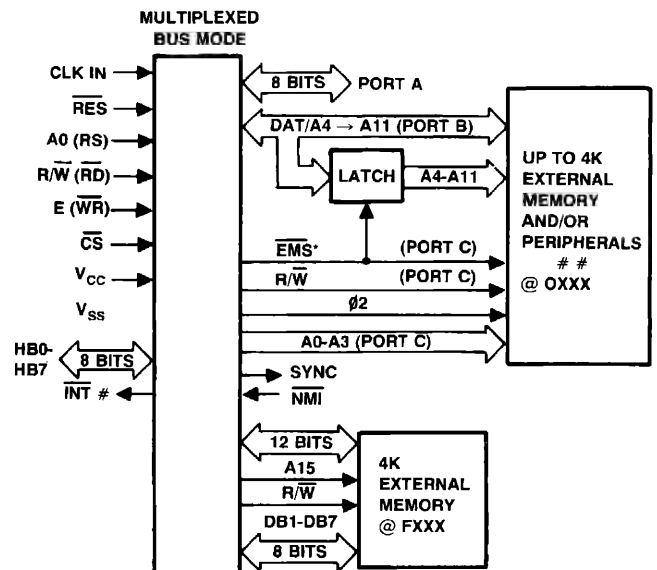


Figure 4-1d.

OPTIONAL PC6

NOT AVAILABLE WITH BOOTSTRAP ROM OPTION

* EMS VALID @ 0100 THRU OFF

SECTION 5

HOST INTERFACE BUS

Two way data transfers are performed between the IPC and the Host microprocessor by means of the Output Data Register and the Input Data Register. The Host can also write a command to the IDR and read from the Host Status Flag Register. Figure 5-1 shows the Host addressing matrix. A hardware interrupt procedure and a software polling procedure is available to control data traffic between the CPU and Host.

RS (A ₀)	READ	WRITE
1	HOST STATUS FLAG	COMMAND INPUT
0	DATA REG OUTPUT	DATA REG INPUT

Figure 5-1. Host Addressing Matrix

5.1 DATA REGISTERS

The device has an 8-bit Input Data Register (IDR) and an 8-bit Output Data Register (ODR). The IDR serves as a temporary storage for commands and data from the Host to the device. When transferring data from the Host to the device, the following conditions are in effect:

- \overline{CS} is asserted
- RS (A₀) indicates command input or data input.
- The contents of the host data bus (HB0-HB7) are copied into the IDR when the appropriate Host bus write signals are asserted.

The ODR serves as a temporary storage for data from the device to the Host. When the Host is reading data from the device, the following conditions are in effect:

- \overline{CS} is asserted
- RS (A₀) input selects ODR or HSFR
- The contents of ODR or the Flag Register are placed on the host data bus (HB0-HB7) when the appropriate Host read signals are asserted.

5.2 HOST STATUS FLAG REGISTER

A Host Status Flag Register facilitates a software protocol that permits independent and uninterrupted flow of data asynchronously between the host computer and the device.

The Host Status Flag Register contains 8 flag bits that can be read at anytime by either the Host or the device. See Figure 5-2. General purpose flags F2 through F6 are serviced by the device in either read or write modes and monitored by the Host (Read Only).

Flag F1 can be read at anytime by either the host or the device. The F1 flag copies the A0 (RS) input signal during any

host write data exchange. The device can write to the F1 flag at any time.

The ODRF (Output Data Register Full) flag is set each time the device writes to the Output Data Register. The setting of the ODRF sets the device Interrupt Status Register IFR3 flag. An Output Interrupt (INT) may be generated under program control by setting IER3 in the interrupt enable register. The ODRF flag is reset only by a hardware reset or by the host performing a read on the output data register. The ODRF flag is reset following the conclusion of any host output data register read. The resetting of the ODRF causes the reset of the IFR3 flag and thus the reset of the external interrupt (INT).

The IDRF (Input Data Register Full) flag is set following the conclusion of any host write data exchange. The setting of the IDRF causes IFR2 of the device status register to be set. An internal interrupt may be generated under program control by setting IER2 in the Interrupt Enable Register. The setting of IDRF also causes IFR4 to be reset. The IDRF resets during device read of the input data register. IFR2 sets and IFR4 resets following the reset of IDRF. IFR4 may generate an external output interrupt (INT, input buffer empty), under program control by setting IER4 in the interrupt-enable register.

The Host Status Flag Register is cleared by the \overline{RES} input.

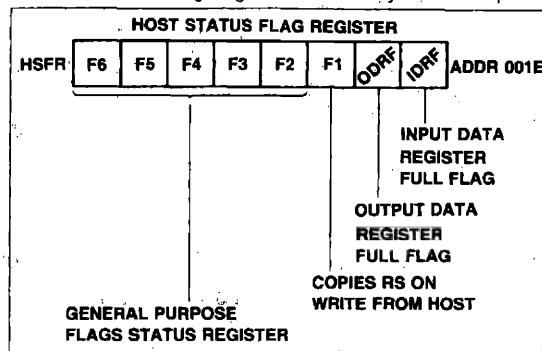


Figure 5-2. Host Status Flag Register Bit Allocation

5.3 HOST COMPUTER INTERFACE

The device will work with a variety of Host Computers. The HOST interface consists of a chip select, one address line, 2 control lines and an 8 bit three state data bus. Internal logic of the device, controlled by MCR4, configures the address and two control lines to either a 6500 or 8080 operational methodology. The interface is completely asynchronous and will work with a Host Computer up to a 5 MHz bus transfer rate. The device clock input frequency need not be the same as the Host's. A mode control register is set to match the interface to that of the Host device as follows:

MCR4 = 0 When MCR4 is set to a logic zero, the IPC is configured to operate on a 6502/6800 type host bus. In this mode, the E input is connected to the host transfer strobe (VMA or $\phi 2$ for 6800, $\phi 2$ for 6500) and the R/W input is connected to the host microprocessor R/W output line. Figure 5-3 and Table 5-1, together, specify the relevant timing for read and write cycles on this type of host bus.

Table 5-1. Host Interface
Timing Characteristics BSEL = 0 (6500)

CHARACTERISTICS 1 AND 2 MHz	SYMBOL	MIN	MAX
CS, R/W, RS Setup Time	t_{CS}	10	—
Access Time	t_{DA}	—	90*
Data Hold Time	t_{DHR}	10	—
Control Hold Time	t_{HC}	10	—
Write Data Setup Time	t_{WDS}	75	—
Write Data Hold Time	t_{DHW}	10	—
Write Stroke Width	t_{WR}	75	—

*NOTE:
90 ns when loading = 130 pf + 1 TTL LOAD and
75 ns when loading = 90 pf + 1 TTL LOAD.

MCR4 = 1 When MCR4 is set to a logic one, the IPC is configured for operation on an 8080/Z80 type bus. In this mode, the \overline{RD} input is used as a read strobe and the \overline{WR} input is connected to the write strobe of the host microprocessor bus. Figure 5-4 and Table 5-2 show the relevant timing characteristics for this mode of operation.

Table 5-2. Host Interface
Timing Characteristics BSEL = 1 (8080)

CHARACTERISTICS 1 AND 2 MH	SYMBOL	MIN	MAX
CS, A0 Setup Time	t_{CS}	10	—
Data Access Time on Read	t_{DA}	—	90*
Data Hold Time	t_{DHR}	10	—
Control Hold Time	t_{HC}	10	—
Write Data Setup Time	t_{WDS}	75	—
Write Data Hold Time	t_{DHW}	10	—
Write Stroke Width	t_{WR}	75	—

*NOTE:
90 ns when loading = 130 pf + 1 TTL LOAD and
75 ns when loading = 90 pf + 1 TTL LOAD.

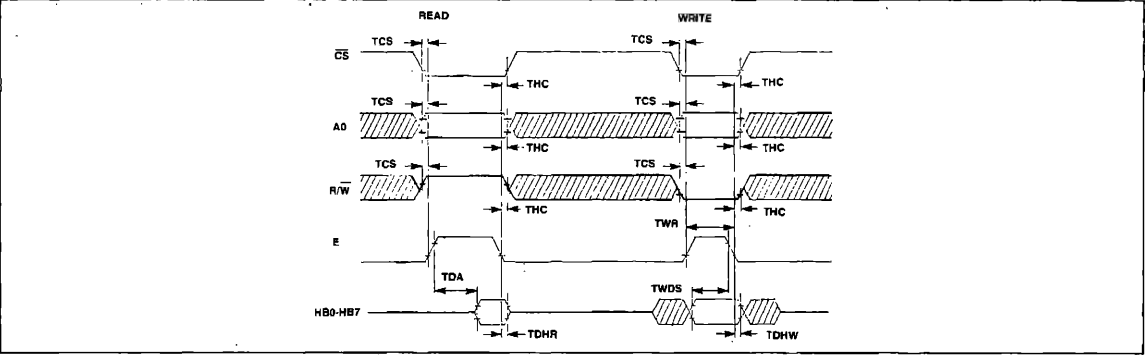


Figure 5-3. Timing Diagram—Host Interface (MCR4 = 0) (6500 Version)

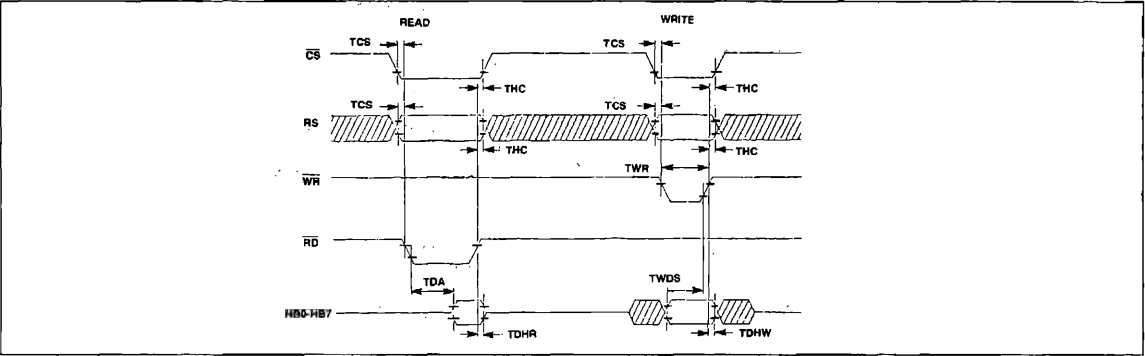


Figure 5-4. Timing Diagram—Host Interface (MCR4 = 1) (8080 Version)

SECTION 6

COUNTER/TIMERS

The device contains a 16-bit counter and a 16-bit latch associated with it. The counter can be independently programmed to operate in one of four modes:

Counter

- Pulse width measurement
- Pulse Generation
- Interval Timer
- Event Counter

Operating modes of the Counter are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA2 is selected for Counter I/O.

6.1 COUNTER

The Counter consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter (LC), Upper Counter (UC), Lower Latch (LL), and Upper Latch (UL). The counter contains the count of either $\phi 2$ clock pulses or external events, depending on the counter mode selected. The contents of the Counter may be read any time by executing a read at location 0018 for the Upper Counter and at location 001A or location 0019 for the Lower Counter. A read at location 0019 also clears the Counter Underflow Flag (IFR5).

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch at location 0018 and the Lower Latch at location 001A. In either case, the contents of the accumulator are copied into the applicable latch register.

The Counter can be started at any time by writing to address 0019. The contents of the accumulator will be copied into the Upper Latch before the contents of the 16-bit latch are transferred to the Counter. The counter is set to the latch value whenever the Counter underflows. When the Counter decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter Underflow Flag (IFR 5) will be set to "1". This bit may be cleared by reading the Lower Counter at location 0019, by writing to address location 0019, or by RES.

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are $\phi 2$ clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line (PA2).

The Counter is set to the Interval Timer Mode (00) when a RES signal is generated.

6.1.1 Interval Timer Mode

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).
2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 0019, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the $\phi 2$ clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore $1\mu\text{s}$ to 65.535 ms at the 1 MHz $\phi 2$ clock rate or $0.5\mu\text{s}$ to 32.767 ms at the 2 MHz $\phi 2$ clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{\text{IRQ}}$ interrupt requests in the counter IRQ interrupt routine.

When the Counter decrements from 0000, the Counter Underflow (IFR5) is set to logic 1. If the Counter Interrupt Enable Bit (IER5) is also set, an $\overline{\text{IRQ}}$ interrupt request will be generated. The Counter Underflow bit in the Interrupt Flag Register can be examined in the $\overline{\text{IRQ}}$ interrupt routine to determine that the $\overline{\text{IRQ}}$ was generated by the Counter Underflow.

While the timer is operating in the Interval Timer Mode, PA2 operates as a PA I/O.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

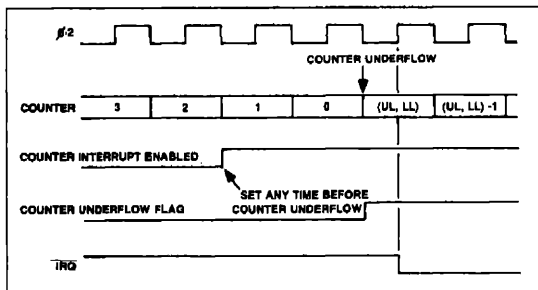


Figure 6-1. Interval Timer Timing Diagram

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the PA2 line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter Underflow occurs, or a write is performed to address 0019.

The normal output waveform is a symmetrical square-wave. The PA2 output is initialized high when entering the mode and transitions low when writing to 0019.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode PA2 is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter Underflow bit (IER5) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

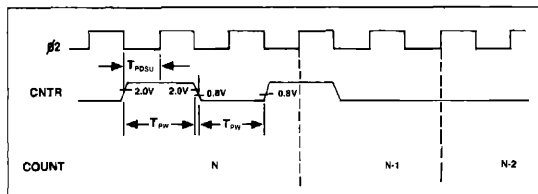
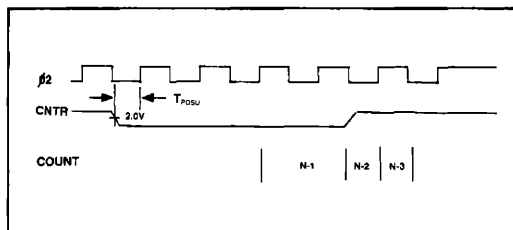


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the PA2 line. The Counter decrements by one count at the $\phi 2$ clock rate as long as the PA2 line is held in the low state. The Counter is stopped when PA2 is in the high state.

The Counter underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the PA2 pin is held low. After the counter is stopped by a high level on PA2, the count will hold as long as PA2 remains high. Any further low levels on PA2 will again cause the counter to count down from its present value. The state of the PA2 line can be determined by testing the state of PA2.



SECTION 7

POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER ON TIMING

After application of VCC power to the device, \overline{RES} must be held low for at least eight stable $\phi 2$ clock cycles after VCC reaches operating range.

Figure 7-1 illustrates the power turn-on waveforms. External clock stabilization time is typically 20ms.

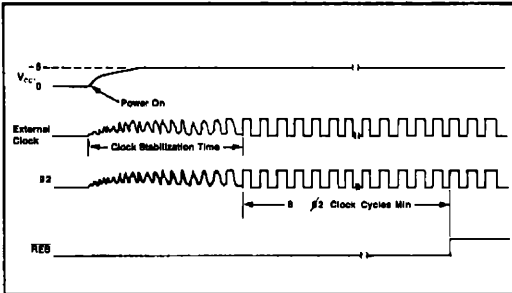


Figure 7-1. Power Turn-On Timing Detail

7.2 POWER-ON RESET

The occurrence of \overline{RES} going from low to high will cause the device to set the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiate a reset vector fetch at address FFFC and FFFD to begin user program execution. All of the I/O ports will be initialized to the high (logic 1) state. All bits of the Control Register will be cleared causing the Interval Timer counter mode to be selected and causing all interrupt enabled bits to be reset.

7.3 RESET (\overline{RES}) CONDITIONS

When \overline{RES} is driven from low to high the device is put in a reset state causing the registers and I/O ports to be set as shown in Table 7-1.

Table 7-1. \overline{RES} Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
REGISTERS								
Processor Status	—	—	—	—	—	1	—	—
Mode Control (MCR)	0	0	0	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	1	0	0	0	0
Host Status Flag	0	0	0	0	0	0	0	0
Input Data	0	0	0	0	0	0	0	0
Output Data	0	0	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1
PC Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

7.4 INITIALIZATION

Any initialization process for the device should include a \overline{RES} as indicated in the preceding paragraphs. After stabilization of the external clock (if a power on situation) an initialization routine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls and Counter as required
5. Clear Interrupts.

A typical initialization routine could be as follows:

```
LDX    Load stack pointer starting address into
        X Register
TXS    Transfer X Register value to Stack Pointer
CLD    Clear Decimal Mode
SEC    Set Carry Flag
...    Set-up Mode Control,
...    Counter, special function
...    registers and Clear RAM as required
CLI    Clear Interrupts
```

APPENDIX A

EXPANDED R6502 INSTRUCTION SET

This appendix contains a summary of the R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Document 29650 N30.

The four instructions notated with a * are added instructions for the IPC devices which are not part of the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

MNEMONIC	INSTRUCTION	MNEMONIC	INSTRUCTION
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative	NOP	No Operation
BCC	Branch on Carry Clear		
BCS	Branch on Carry Set	ORA	"OR" Memory with Accumulator
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator	PHA	Push Accumulator on Stack
BMI	Branch on Result Minus	PHP	Push Processor Status on Stack
BNE	Branch on Result not Zero	PLA	Pull Accumulator from Stack
BPL	Branch on Result Plus	PLP	Pull Processor Status from Stack
BRK	Force Break		
BVC	Branch on Overflow Clear		
BVS	Branch on Overflow Set		
CLC	Clear Carry Flag	*RMB	Reset Memory Bit
CLD	Clear Decimal Mode	ROL	Rotate One Bit Left (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit		
CLV	Clear Overflow Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CMP	Compare Memory and Accumulator	RTI	Return from Interrupt
CPX	Compare Memory and Index X	RTS	Return from Subroutine
CPY	Compare Memory and Index Y		
DEC	Decrement Memory by One	SBC	Subtract Memory from Accumulator with Borrow
DEX	Decrement Index X by One	SEC	Set Carry Flag
DEY	Decrement Index Y by One	SED	Set Decimal Mode
		SEI	Set Interrupt Disable Status
EOR	"Exclusive-Or" Memory with Accumulator	*SMB	Set Memory Bit
		STA	Store Accumulator in Memory
		STX	Store Index X in Memory
		STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index Y by One	TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
		TXA	Transfer Index X to Accumulator
JMP	Jump to New Location	TXS	Transfer Index X to Stack Register
JSR	Jump to New Location Saving Return Address	TYA	Transfer Index Y to Accumulator

3

NOTES	LEGEND	M_n
1. Add 1 to N if page boundary is crossed	X = Index X	= Memory Bit 6
2. Add 1 to N if branch occurs to same page	X = Instruction	
3. Carry not = Borrow	A = Accumulator	
4. If in decimal mode Z flag is invalid	M = Memory per effective address	
operator must be checked on zero result.	M = Memory per stack pointer	
Effects 8-bit data field of the specified zero page address.	m = Selector zero page memory bit	
	M ₇ = Memory Bit 7	
	# = Number of Bytes	

1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
3. Add 2 to N if branch occurs to different page
4. Carry not = Borrow
5. If in decimal mode Z flag is invalid accumulator must be checked on zero result.
6. Effects a-bit data field of the specified zero page address

A.3 INSTRUCTION CODE MATRIX

MSD	LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8	8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBR8 ZP 3 5**	8
9	9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBR9 ZP 3 5**	9
A	A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBR10 ZP 3 5**	A
B	B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBR11 ZP 3 5**	B
C	C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBR12 ZP 3 5**	C
D	D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBR13 ZP 3 5**	D
E	E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBR14 ZP 3 5**	E
F	F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBR15 ZP 3 5**	F

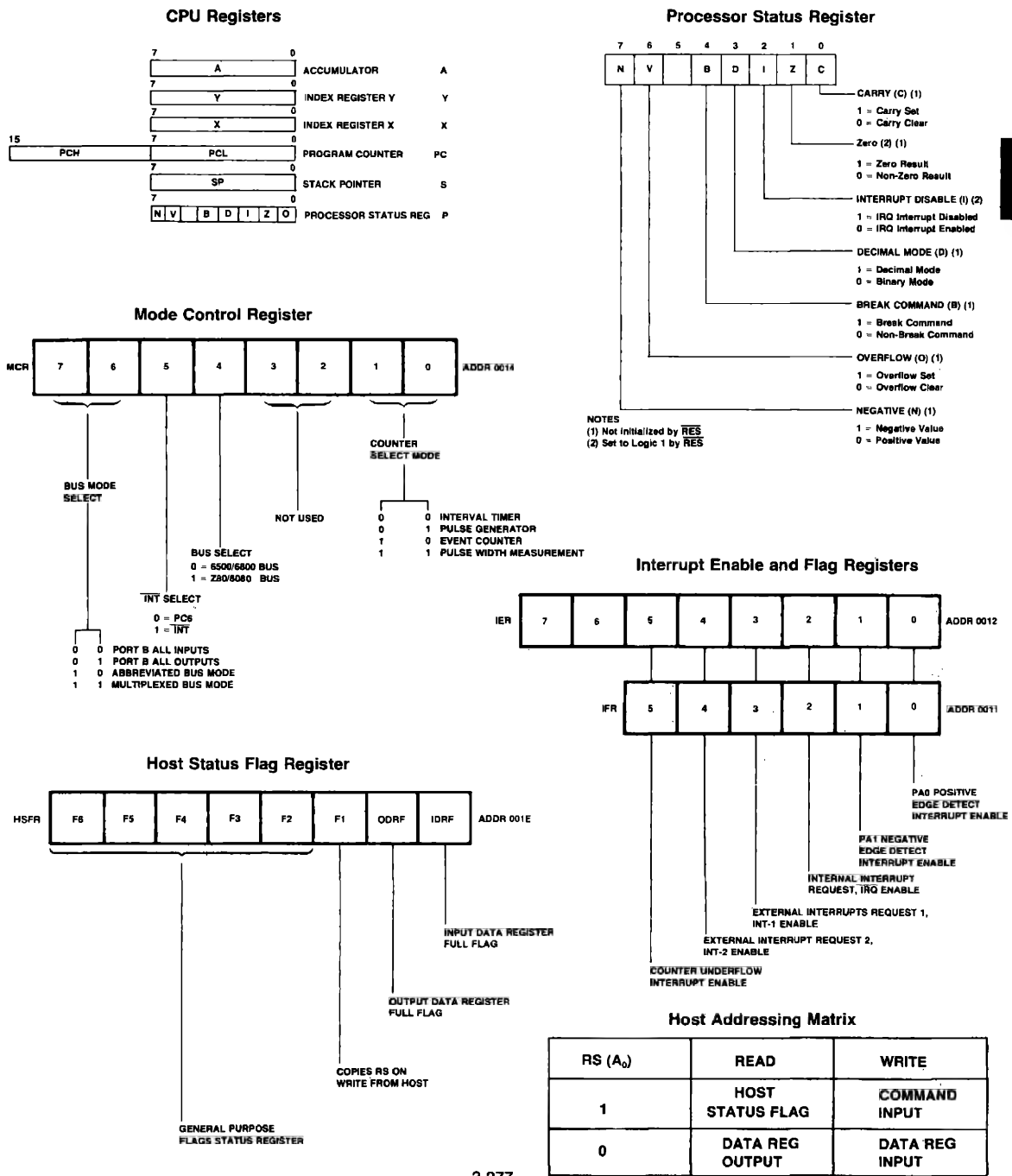
0
BRK
Implied
1 7

—OP Code
—Addressing Mode
—Instruction Bytes; Machine Cycles

*Add 1 to N if page boundary is crossed.

**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

APPENDIX B
KEY REGISTER SUMMARY



APPENDIX C

C.1 MEMORY MAPS AND ADDRESS AND PIN ASSIGNMENTS

PORT B ALL INPUTS

FFFF	IRQ VECTOR	FFFF	IRQ VECTOR	FFFF	IRQ VECTOR	FFFF	IRQ VECTOR
FFFC	RES VECTOR	FFFC	RES VECTOR	FFFC	RES VECTOR	FFFC	RES VECTOR
FFFA	NMI VECTOR	FFFA	NMI VECTOR	FFFA	NMI VECTOR	FFFA	NMI VECTOR
4K USER PROGRAM		4K USER PROGRAM		4K USER PROGRAM		4K USER PROGRAM	
F000		F000		F000		F000	

PORT B ALL OUTPUTS

FFFF	IRQ VECTOR	FFFF	IRQ VECTOR	FFFF	IRQ VECTOR	FFFF	IRQ VECTOR
FFFC	RES VECTOR	FFFC	RES VECTOR	FFFC	RES VECTOR	FFFC	RES VECTOR
FFFA	NMI VECTOR	FFFA	NMI VECTOR	FFFA	NMI VECTOR	FFFA	NMI VECTOR
4K USER PROGRAM		4K USER PROGRAM		4K USER PROGRAM		4K USER PROGRAM	
F000		F000		F000		F000	

ABBREVIATED BUS MODE

FFFF	IRQ VECTOR	FFFF	IRQ VECTOR	FFFF	IRQ VECTOR	FFFF	IRQ VECTOR
FFFC	RES VECTOR	FFFC	RES VECTOR	FFFC	RES VECTOR	FFFC	RES VECTOR
FFFA	NMI VECTOR	FFFA	NMI VECTOR	FFFA	NMI VECTOR	FFFA	NMI VECTOR
4K USER PROGRAM		4K USER PROGRAM		4K USER PROGRAM		4K USER PROGRAM	
F000		F000		F000		F000	

MULTI-PPLEKED BUS MODE

FFFF	IRQ VECTOR	FFFF	IRQ VECTOR	FFFF	IRQ VECTOR	FFFF	IRQ VECTOR
FFFC	RES VECTOR	FFFC	RES VECTOR	FFFC	RES VECTOR	FFFC	RES VECTOR
FFFA	NMI VECTOR	FFFA	NMI VECTOR	FFFA	NMI VECTOR	FFFA	NMI VECTOR
4K USER PROGRAM		4K USER PROGRAM		4K USER PROGRAM		4K USER PROGRAM	
F000		F000		F000		F000	

RES500/43 (W/BOOT STRAP ROM)

FFFF	IRQ VECTOR	FFFF	IRQ VECTOR	FFFF	IRQ VECTOR	FFFF	IRQ VECTOR
FFFC	RES VECTOR	FFFC	RES VECTOR	FFFC	RES VECTOR	FFFC	RES VECTOR
FFFA	NMI VECTOR	FFFA	NMI VECTOR	FFFA	NMI VECTOR	FFFA	NMI VECTOR
4K USER PROGRAM		4K USER PROGRAM		4K USER PROGRAM		4K USER PROGRAM	
F000		F000		F000		F000	

RES541 & RES600/43 (W/O BOOT STRAP ROM)

FFFF	IRQ VECTOR	FFFF	IRQ VECTOR	FFFF	IRQ VECTOR	FFFF	IRQ VECTOR
FFFC	RES VECTOR	FFFC	RES VECTOR	FFFC	RES VECTOR	FFFC	RES VECTOR
FFFA	NMI VECTOR	FFFA	NMI VECTOR	FFFA	NMI VECTOR	FFFA	NMI VECTOR
4K USER PROGRAM		4K USER PROGRAM		4K USER PROGRAM		4K USER PROGRAM	
F000		F000		F000		F000	

INTERNAL REGISTERS

ADDRESS	READ	WRITE
001F	HBB Status Register	---
001E	Register	---
001D	Input Host Bus Buffer	Output Host Bus Buffer
001C	Lower Counter A	Upper Latch A
001B	Lower Counter A	Upper Latch A
001A	Lower Counter A	Upper Latch A
0019	Lower Counter A	Upper Latch A
0018	Lower Counter A	Upper Latch A
0017	Mode Control Reg	Mode Control Reg
0016	Interrupt Enable Reg	Interrupt Enable Reg
0015	Interrupt Flag Reg	Interrupt Flag Reg
0014	Head FF	Ctr Interrupt Flag Reg
0013		
0012		
0011		
0010		
000F		

--- AND START COUNTER
CLEAR FLAG

C.2 I/O AND INTERNAL REGISTER ADDRESSES

ADDRESS	READ	WRITE
001F	— —	— —
1E	Host Status Flag Register	Host Status Flag Register
1D	— —	— —
1C	Input Data Register (IDR)	Output Data Register (ODR)
1B	— —	— —
1A	Lower Counter	Lower Latch
19	Lower Counter & Clear Flag (IFR5)	Upper Latch/Transfer Latch to Counter & Clear Flag (IFR5)
18	Upper Counter	Upper Latch
17	— —	— —
16	— —	— —
15	— —	— —
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
10	Read "FF"	Clear Int Flag Bit
0F	— —	— —
0E	— —	— —
0D	— —	— —
0C	— —	— —
0B	— —	— —
0A	— —	— —
09	— —	— —
08	— —	— —
07	— —	— —
06	— —	— —
05	— —	— —
04	— —	— —
03	— —	— —
02	Port C	Port C
01	Port B	Port B
00	Port A	Port A

C.3 MULTIPLE FUNCTION PIN ASSIGNMENTS

PIN NUMBER	I/O	ABBREVIATED PORT	MULTIPLEXED PORT
R6541Q	FUNCTION	FUNCTION	FUNCTION
31	PC0	A0	A0
30	PC1	A1	A1
29	PC2	A2	A2
28	PC3	A3	A3
27	PC4	R/W	R/W
26	PC5	EMS	EMS
25	PC6/INT	PC6/INT	PC6/INT
49	PB0	D0	A4/D0
50	PB1	D1	A5/D1
51	PB2	D2	A6/D2
52	PB3	D3	A7/D3
53	PB4	D4	A8/D4
54	PB5	D5	A9/D5
55	PB6	D6	A10/D6
56	PB7	D7	A11/D7

APPENDIX D

ELECTRICAL SPECIFICATIONS

Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range, Commercial	T	0 to +70	°C
Storage Temperature Range	T_{sto}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. Characteristics ($V_{CC} = 5V \pm 5\%$ $V_{SS} = 0$)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS
Power Dissipation (Outputs High) Commercial 0°C to +70°C	P_D	—	500	—	mW
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	—	+0.8	Vdc
Input Leakage Current $V_{in} = 0$ to 5.25 Vdc	I_{IN}	-10.0	—	+10.0	μ Adc
Input Low Current ($V_{IL} = 0.4$ Vdc)	I_{IL}	—	-1.0	-1.6	mAdc
Output High Voltage ($V_{CC} = \min$, $I_{Load} = -100$ μ Adc)	V_{OH}	+2.4	—	V_{CC}	Vdc
Output High Voltage ($V_{CC} = \min$)	V_{CMOS}	$V_{CC} - 30\%$	—	V_{CC}	Vdc
Output Low Voltage ($V_{CC} = \min$, $I_{Load} = 1.6$ mAdc)	V_{OL}	—	—	+0.4	Vdc
Output High Current (Sourcing) ($V_{OH} = 2.4$ Vdc)	I_{OH}	-100	—	—	μ Adc
Output Low Current (Sinking) ($V_{OL} = 0.4$ Vdc)	I_{OL}	1.6	—	—	mAdc
Darlington Current Drive, PE* ($V_{OH} = 1.5$ Vdc)	I_{OH}	-1.0	—	—	mAdc
Output Low Current, PE* ($V_{OL} = 0.4$ Vdc)	I_{OL}	1.6	—	—	mAdc
Input Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz) PA, PB, PC, PF*, PG*	C_{in}	—	—	10	pF
Output Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz)	C_{OUT}	—	—	10	pF
I/O Port Resistance PA0-PA7, PC0-PC6 PF0-PF7, PG0-PG7	R_L	3.0	6.0	11.5	K Ω

NOTE: Negative sign indicates outward current flow, positive indicates inward flow. $V_{CC} = 5V \pm 5\%$ *R6500/42 only

APPENDIX E
TIMING REQUIREMENTS AND CHARACTERISTICS

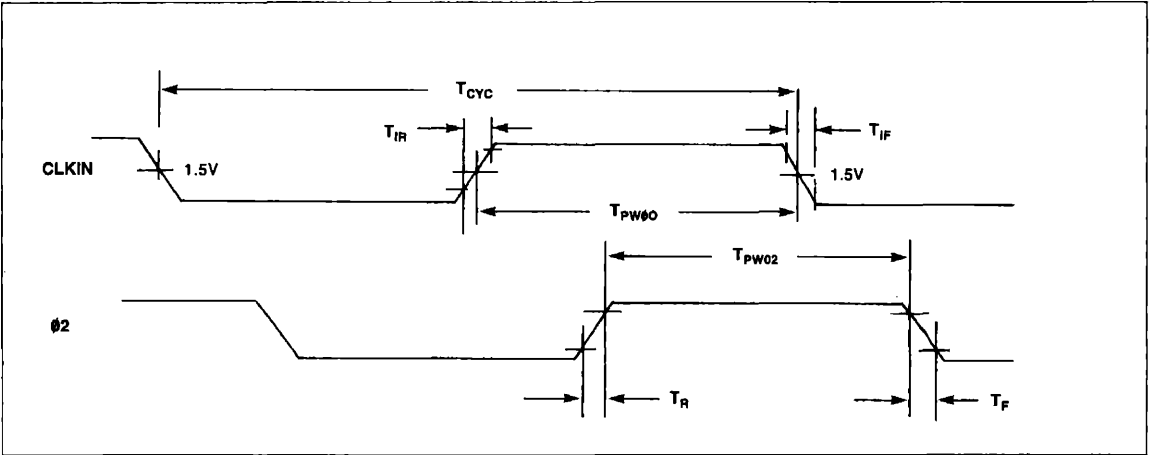
E.1 GENERAL NOTES

- 1. V_{CC} 5V $\pm 5\%$, $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$
- 2. A valid $V_{CC} - \overline{\text{RES}}$ sequence is required before proper operation is achieved.
- 3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
- 4. All time units are nanoseconds, unless otherwise specified.
- 5. All capacitive loading is 130 pF maximum, except as noted below:
 - PA, PB — 50 pF maximum
 - PB, PC (I/O Modes Only) — 50 pF maximum
 - PB, PC (ABB and Mux Mode) — 130 pF maximum

E.2 CLOCK TIMING

Symbol	Parameter	1 MHz		2 MHz	
		Min	Max	Min	Max
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
$T_{PW\phi 0}$	CLKIN Input Clock Pulse Width	475	—	240	—
$T_{PW\phi 2}$	Output Clock Pulse Width at Minimum T_{CYC}	$T_{PW\phi 0}$	$T_{PW\phi 0} + 25$	$T_{PW\phi 0}$	$T_{PW\phi 0} + 20$
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10

3



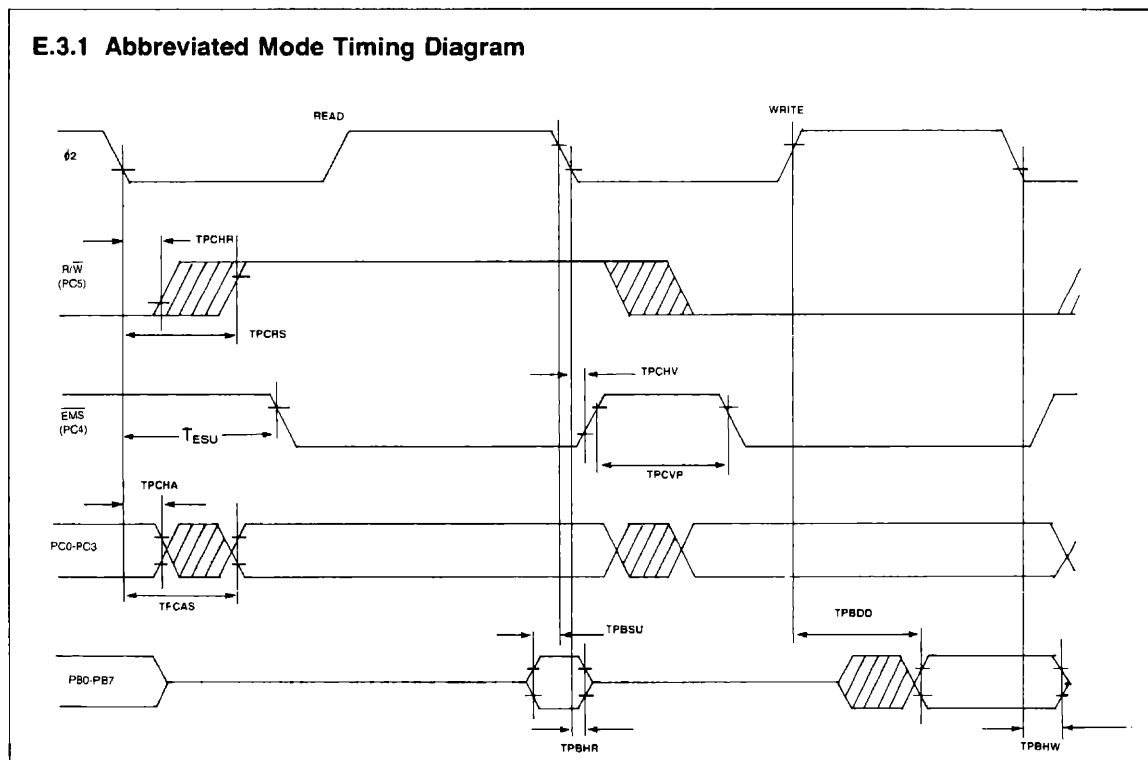
E.3 ABBREVIATED MODE TIMING—PB AND PC

(MCR 5 = 1, MCR 6 = 0, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC3) Address Setup Time	—	225	—	140
T_{PBSU}	(PB) Data Setup Time	50	—	35	—
T_{PBHR}	(PB) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PB) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PB) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC3) Address Hold Time	30	—	30	—
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC4) EMS Hold Time	10	—	10	—
T_{PCVP}	(PC4) EMS Stabilization Time	30	—	30	—
T_{ESU}	EMS Setup Time	—	350	—	210

NOTE 1: Values assume PC0-PC5 have the same capacitive load.

E.3.1 Abbreviated Mode Timing Diagram



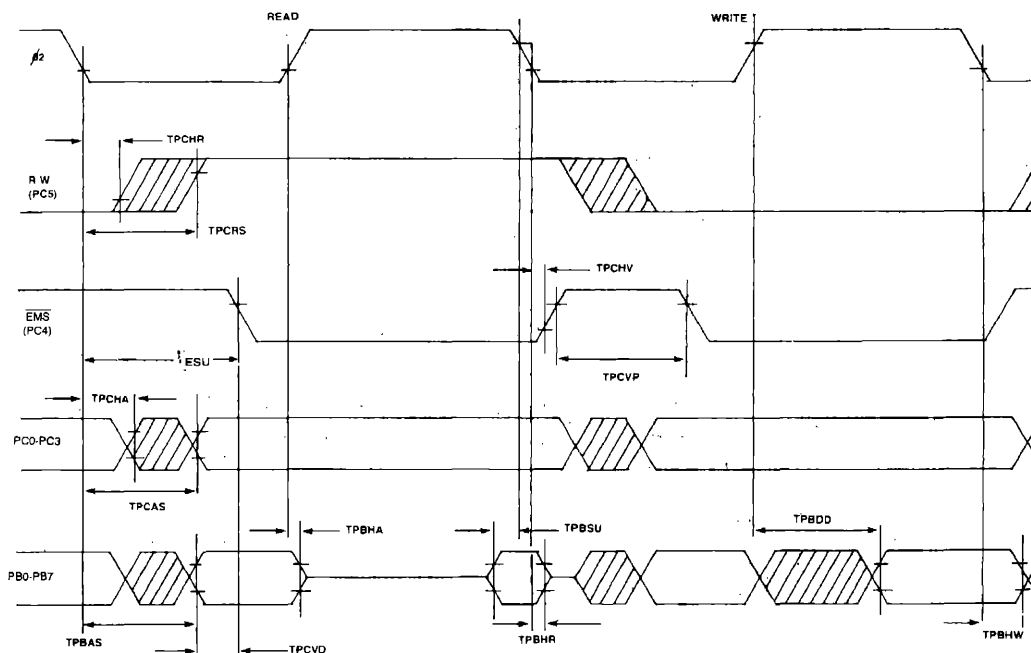
E.4 MULTIPLEXED MODE TIMING—PB AND PC

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC3) Address Setup Time	—	225	—	140
T_{PBAS}	(PB) Address Setup Time	—	225	—	140
T_{PBSU}	(PB) Data Setup Time	50	—	35	—
T_{PBHR}	(PB) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PB) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PB) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC3) Address Hold Time	30	—	30	—
T_{PBHA}	(PB) Address Hold Time	0	100	0	80
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC4) EMS Hold Time	10	—	10	—
$T_{PCVD}^{(1)}$	(PC4) Address to EMS Delay Time	30	—	30	—
T_{PCVP}	(PC4) EMS Stabilization Time	30	—	30	—
T_{ESU}	EMS Setup Time	—	350	—	210

NOTE 1: Values assume PC0-PC5 have the same capacitive load.

E.4.1 Multiplex Mode Timing Diagram

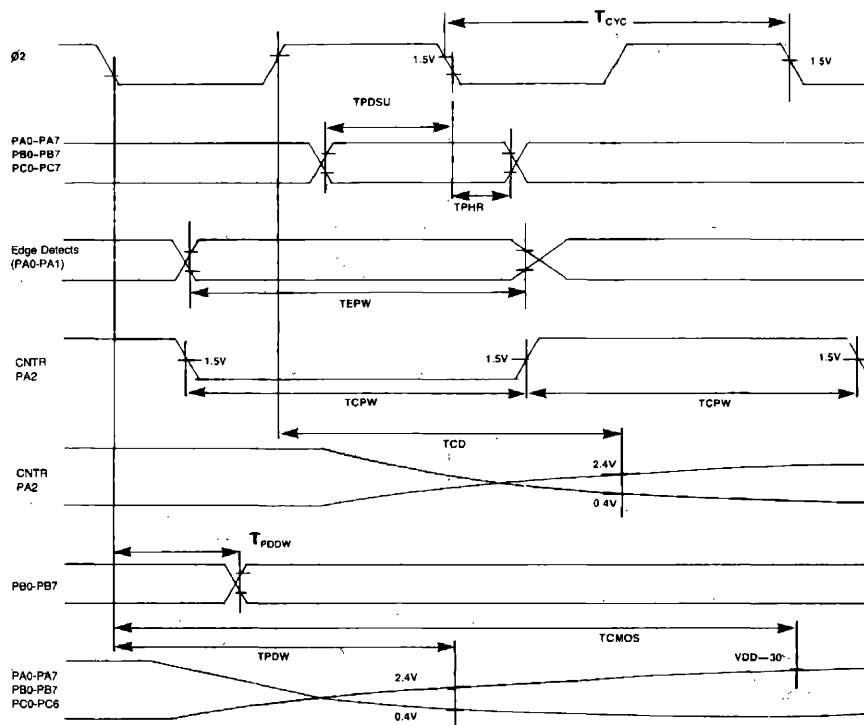


E.5 I/O, EDGE DETECT AND COUNTER TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
$T_{PDW}^{(1)}$	Internal Write to Peripheral Data Valid	—	500	—	500
$T_{CMOS}^{(1)}$	PA, PC CMOS	—	1000	—	1000
T_{PDDW}	PB	—	175	—	150
T_{PDSU}	Peripheral Data Setup Time				
	PA, PC	200	—	200	—
T_{PDSU}	PB	50	—	50	—
T_{PHR}	Peripheral Data Hold Time				
	PA, PC	75	—	75	—
T_{PHR}	PB	10	—	10	—
T_{EPW}	PA0-PA1 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CPW}	Counter				
	PA2 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
$T_{CD}^{(1)}$	PA2 Output Delay	—	500	—	500

NOTE 1: Maximum Load Capacitance: 50pF Passive Pull-Up Required

E.5.1 I/O, Edge Detect, Counter.

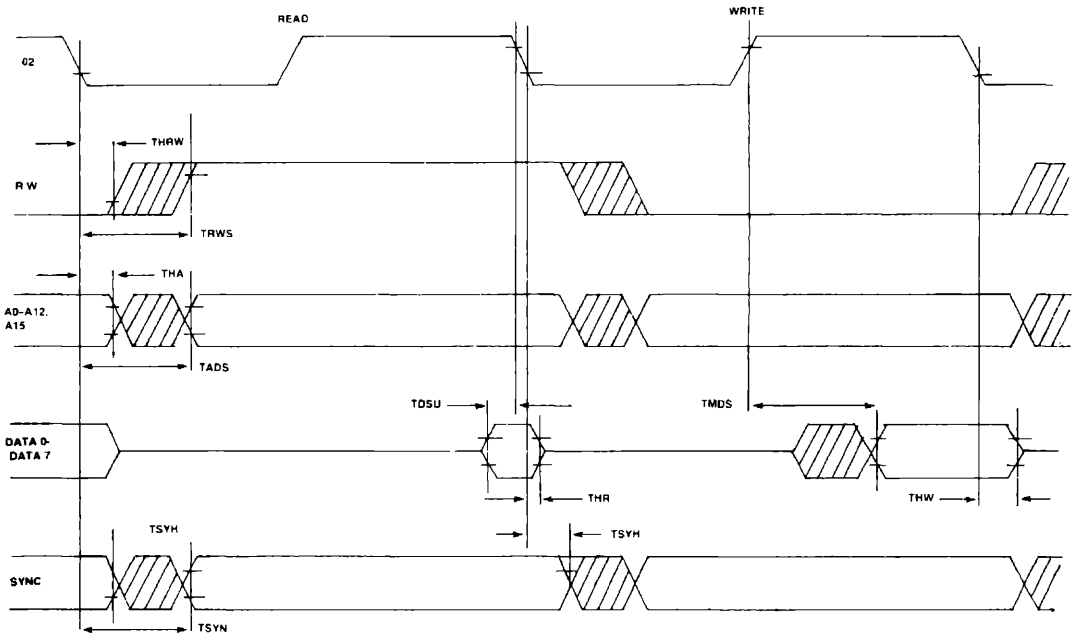


E.6 MICROPROCESSOR TIMING (D0-D7, A0-A12, A15, SYNC, R/W)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{RWS}	R/W Setup Time	—	225	—	140
T_{ADS}	A0-A12, A15 Setup Time	—	150	—	75
T_{DSU}	D0-D7 Data Setup Time	50	—	35	—
T_{HR}	D0-D7 Read Hold Time	10	—	10	—
T_{HW}	D0-D7 Write Hold Time	30	—	30	—
T_{MOS}	D0-D7 Write Output Delay	—	175	—	130
T_{SYN}	SYNC Setup	—	225	—	175
T_{HA}	A0-A12, A15 Hold Time	30	—	30	—
T_{HRW}	R/W Hold Time	30	—	30	—
T_{ACC}	External Memory Access Time $T_{ACC} = T_{CYC} - T_r - T_{ADS} - T_{DSU}$	—	T_{ACC}	—	T_{ACC}
T_{SYH}	SYNC Hold Time	30	—	30	—

3

E.6.1 Microprocessor Timing Diagram



100

100

100

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100

100

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MEMORY PRODUCTS

System ROM, Advanced CMOS and EEPROM

Multi-chip systems need memory. How much and what type is up to the designer. Some memory devices are high volume, low price products. Some are tougher to produce. Rockwell is as good as you can get at tough ROM, custom coded, made to order, 32K through 128K. So, when you're assembling a microprocessor based system, Rockwell can deliver it all, including ROM.

And, if you're working on a low power, high speed, system, Rockwell can supply CMOS ROM.

For systems needing low-power custom memory, we even offer CMOS UV EPROMs - ROM that can be electrically programmed and erased with ultraviolet light.

But Rockwell is also into some very new technology, with 5V EEPROMs. The new R5213 16K EEPROM has a

10 millisecond/byte erase/write time and unlimited read cycles. Each byte may be erased and written a minimum of 10,000 times, with a fast access time of less than 250 ns. And, there's more: the R2816A and R5516A, with on-chip timing and data latches. The R2816AH writes a byte in only 2 ms while the R5516A improves endurance to at least 1,000,000 write cycles/byte.

So, whatever your system need, Rockwell has the right ROM—NMOS, CMOS, UV EPROM and EEPROM.

Our multi- and single-chip microprocessor and micro-computers, 8 or 16 bit, are the most usable product line available today. And, to help make them even more usable, we also offer memory.

Rockwell Has The Right ROM For Your System

Memory	Part No.	Product Description	Access Time (Nanoseconds)	Package
NMOS EEPROM	R2816A -25 -3 -35	16K (2K x 8) 5V Latched EEPROM with On-Board Timer (10 ms Write Cycle)(2 ms Write Cycle ³) (10,000 Write Cycles/Byte)	-250 -300 -350	24-Pin CERDIP
	R5213 -25 -3 -35	16K (2K x 8) 5V EEPROM	-250 -300 -350	24-Pin CERDIP
	R5516A -25 -3 -35	16K (2K x 8) 5V Latched EEPROM with On-Board Timer (10 ms Write Cycle) (1,000,000 Write Cycles/Byte)	-250 -300 -350	24 Pin CERDIP
	R52B33 -2 -25 -3 -35	64K (8K x 8) 5V Latched EEPROM	-200 -250 -300 -350	24-Pin CERDIP
CMOS EPROM	R2716P -25 -350	64K (8K x 8) One-Time PROM	-250 -350	28-Pin Plastic DIP
	R87C32 -35 -45 -55	32K (4K x 8) 5V UV EPROM	-350 -450 -550	24-Pin CERDIP
	R87C64 -2 -25 -35	64K (8K x 8) 5V UV EPROM	-200 -250 -350	28-Pin CERDIP
CMOS ROM	R23C64 -15P -25P, -25PE -3P -35PE	64K (8K x 8) Static ROM	-150 -250 -300 -350	28-Pin Plastic DIP ¹
NMOS ROM	R2332A ² -2P -25P, -25SP, -25EP -3P, -3SP, -3EP -P, -SP, -EP	32K (4K x 8) Static ROM	-200 -250 -300 -450	24-Pin Plastic DIP ¹
	R2364A -2P -25P -3P, -3SP, -3EP	64K (8K x 8) Static ROM	-200 -250 -300	24-Pin Plastic DIP ¹
	R2364B -3P, -3SP, -3EP	64K (8K x 8) Static ROM	-300	28-Pin Plastic DIP ¹
	R23128 -25P, -25EP -3P, -3EP	128K (16K x 8) Static ROM	-250 -300	28-Pin Plastic DIP ¹

NOTES:

- Also available in ceramic DIP.
- Also available in alternate 24-pin pinout (R2332B — — —).
- R2816AH only.

LEGEND

- A = T.I./Motorola JEDEC
S = Standby power

E = Ext. Temp. (-40° to 85°C)



R2332A AND R2332B 32K (4K × 8) STATIC ROM

DESCRIPTION

The R2332A and R2332B ROMs are 32,768-bit static Read-Only Memories (ROMs), organized as 4,096 eight-bit bytes, that offer maximum access times of 200 to 450 nanoseconds, respectively. These ROMs are in industry-standard 24-pin, dual in-line packages, and are available in ceramic or low-cost plastic. These fully-static 32K-bit ROMs are compatible with 8-bit NMOS microprocessors, including the R6500 family of microprocessors.

All R2332A and R2332B ROMs operate totally asynchronously and require no clock input. These devices provide tri-state output buffers for memory expansion. These ROMs offer TTL input and output levels with a minimum noise immunity of 0.4 volts.

The mask-programmable chip enable input ($\overline{E}/\overline{E}'$) may be programmed to function as a chip select without power down standby mode or as a chip enable with power down standby mode. The active level of the enable input is also programmable.

FEATURES

- 4,096 × 8 organization
- Access time: 200 ns, 250 ns, 300 ns, and 450 ns (max.)
- Low power dissipation is 125 mW active, 37.5 mW standby
- Drives two TTL loads and 100 pF
- Single +5V $\pm 10\%$ power supply
- Totally static operation, no input clock required
- Completely TTL compatible
- Mask-programmable chip enable and chip select
- Tri-state outputs for memory expansion

ORDERING INFORMATION

Part Number: R2332-----

LPackage:

C = Ceramic

P = Plastic

Temperature Range:

No letter = 0°C to +70°C

E = -40°C to +85°C

Power Down Standby Mode:

S = Yes

No letter = No

Access Time (Max.):

2 = 200 ns

25 = 250 ns

3 = 300 ns

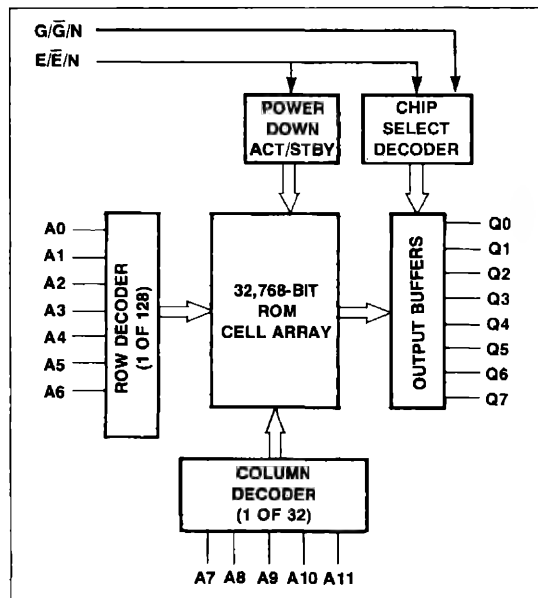
No number(s) = 450 ns

Model:

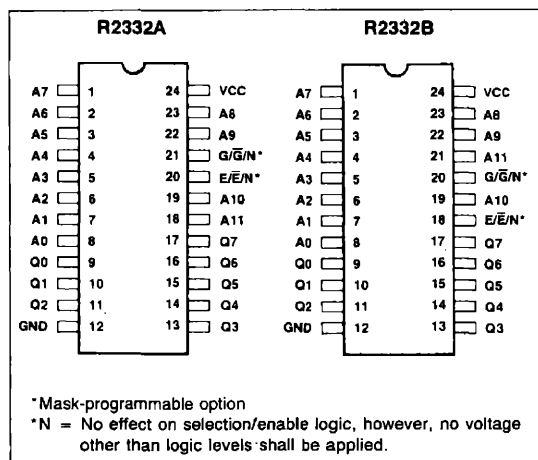
A = R2332A

B = R2332B

Note: Submit ROM codes using Rockwell ROM Code Order Form, Order No. 2137.



R2332A and R2332B Block Diagram



R2332A and R2332B Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.5 to +7.0	Vdc
Input Voltage	V _{IN}	-0.5 to +7.0	Vdc
Output Voltage	V _{OUT}	-0.5 to +7.0	Vdc
Temperature Under Bias Commercial Industrial	T _A	-10 to +80 -50 to +95	°C
Storage Temperature	T _{STG}	-65 to +150	°C
Power Dissipation	P	1.0	W

*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V _{OH}	Output High Voltage	2.4		V _{CC}	V	V _{CC} = 4.5V, I _{OH} = -400 μA
V _{OL}	Output Low Voltage			0.4	V	V _{CC} = 4.5V, I _{OL} = 3.3 mA
V _{IH}	Input High Voltage	2.0		V _{CC}	V	
V _{IL}	Input Low Voltage	-0.5		0.8	V	
I _{LI}	Input Load Current			10	μA	V _{CC} = 5.5V, 0V ≤ V _{IN} ≤ 5.5V
I _{LO}	Output Leakage Current			±10	μA	V _{CC} = 5.5V, chip deselected, V _{OUT} = +0.4V to V _{CC}
I _{CC}	Power Supply Current, Active		25	55	mA	V _{CC} = 5.5V
I _{SB}	Power Supply Current, Standby ¹		7.5	16	mA	
C _I	Input Capacitance ²			7	pF	V _{CC} = 5.0V, chip deselected, pin under test at 0V, T _A = 25°C, f = 1 MHz
C _O	Output Capacitance ²			10	pF	

Notes:

1. Applies only to chip enable with power down standby mode.
2. This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	R2332-2		R2332-25		R2332-3		R2332-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{AVAX}	Address Valid to Address Don't Care	200		250		300		450		ns
t _{ELEH}	Chip Enable Low to Chip Enable High ²	200		250		300		450		ns
t _{AVQV}	Address Valid to Output Valid (t _{ACC}) (Access)		200		250		300		450	ns
t _{ELQV}	Chip Enable Low to Output Valid (Access) ²		200		250		300		450	ns
t _{AVQX}	Address Valid to Output (t _{OH}) Invalid	10		10		10		10		ns
t _{ELQX}	Chip Enable Low to Output (t _{CO}) Invalid	10		10		10		10		ns
t _{EHQZ}	Chip Enable High to Output High Z (t _{DF})	10	70 ⁴	10	70 ⁴	10	70 ⁴	10	70 ⁴	ns
t _{PU}	Chip Selection to Power Up Time ²	0		0		0		0		ns
t _{PD}	Chip Deselection to Power Down Time ²		100 ⁴		100 ⁴		100 ⁴		100 ⁴	ns
t _{AEL}	Address Valid to Chip Enable Low	0		0		0		0		ns
t _{GLQV}	Chip Select Low to Output Valid ³	10	90 ⁴	10	90 ⁴	10	90 ⁴	10	90 ⁴	ns
t _{GQHZ}	Chip Select High to Output High Z ³	10	70 ⁴	10	70 ⁴	10	70 ⁴	10	70 ⁴	ns

Notes:

1. Test Conditions:

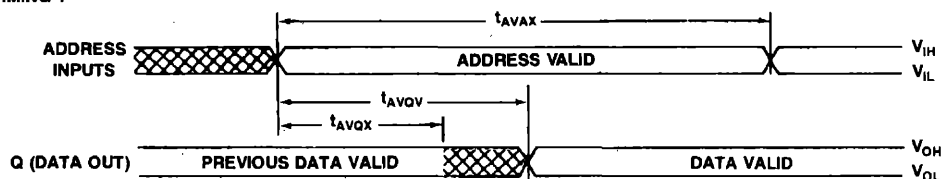
Output Load: 2 TTL Loads and 100 pF; Input Transition Time: 20 ns; Timing Reference Levels: Input: 1.5V; Output: 0.8V, 2.0V.

2. Mask-programmed for chip enable with power down standby mode.

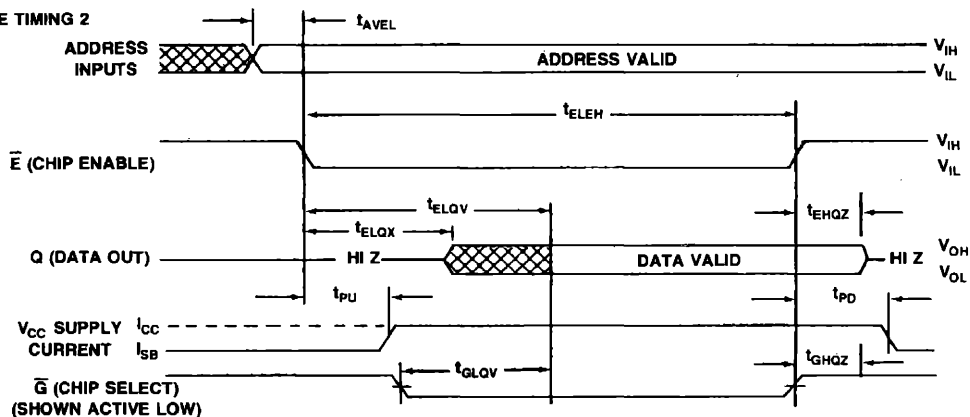
3. Mask-programmed for chip enable without power down standby mode.

4. Add 20 ns for extended temperature devices (-40°C to +85°C).

TIMING DIAGRAMS

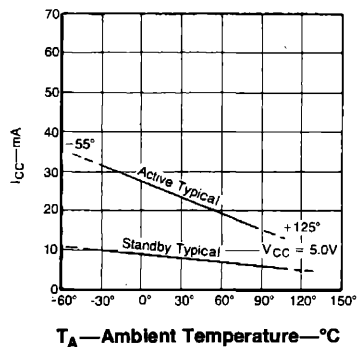
READ CYCLE TIMING 1
(\bar{E} HELD LOW)

READ CYCLE TIMING 2

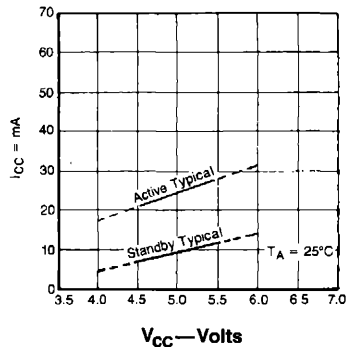
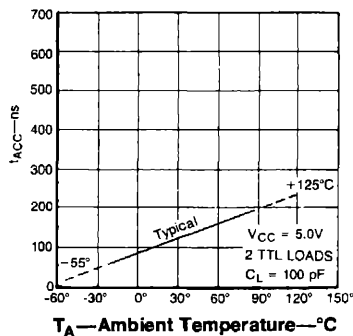


TYPICAL CHARACTERISTICS

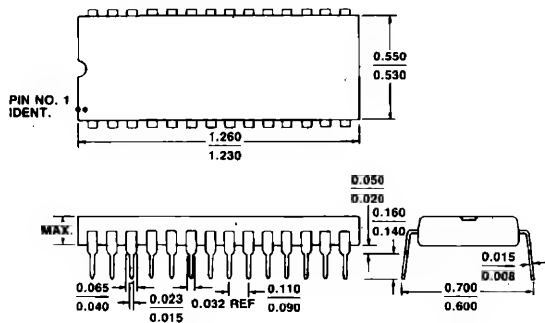
SUPPLY CURRENT VS AMBIENT TEMPERATURE



SUPPLY CURRENT VS SUPPLY VOLTAGE

ACCESS TIME
VS
AMBIENT TEMPERATURE

24-PIN CERAMIC DIP





R2364A

64K (8K × 8) STATIC ROM

DESCRIPTION

The R2364A2, R2364A25 and R2364A3 are 65,536-bit static Read-Only Memories (ROMs), organized as 8,192 eight-bit bytes, that offer maximum access times of 200, 250 and 300 nanoseconds, respectively. These ROMs are in industry-standard 24-pin, dual in-line packages, and are available in ceramic or low-cost plastic. These fully-static 64K-bit ROMs are compatible with all eight-bit N-channel microprocessors, including the R6500 family of microprocessors.

All three R2364A ROMs operate totally asynchronously, and require no clock input. These devices provide tri-state output buffers for memory expansion. The R2364A ROMs offer TTL input and output levels with a minimum noise immunity of 0.4 volts.

The mask-programmable chip enable input (E/\bar{E}) may be programmed to function as a chip select without power down standby mode or as a chip enable with power down standby mode. The active level of the enable input is also programmable.

FEATURES

- 8,192 × 8 organization
- Access time: 200 ns, 250 ns, and 300 ns (max.)
- Low power dissipation: 125 mW active, 37.5 mW standby
- Drives two TTL loads and 100 pF
- Single +5V ± 10% power supply
- Totally static operation, no input clock required
- Completely TTL compatible
- Mask-programmable chip enable
- Tri-state outputs for memory expansion

ORDERING INFORMATION

Part Number: R2364A

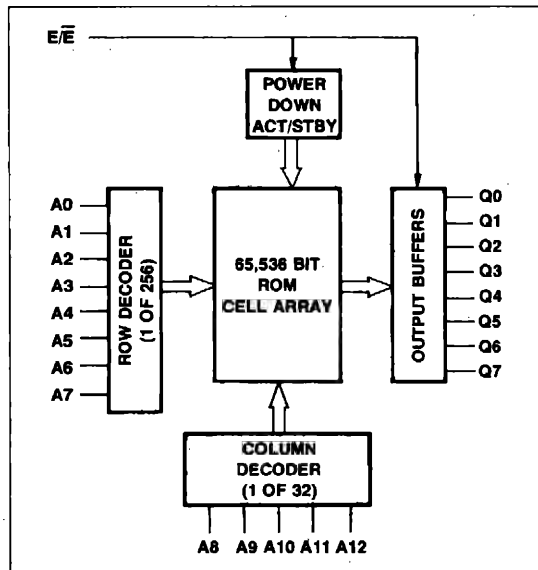
Package:
 C = Ceramic
 P = Plastic

Temperature Range:
 No letter = 0°C to +70°C
 E = -40°C to +85°C

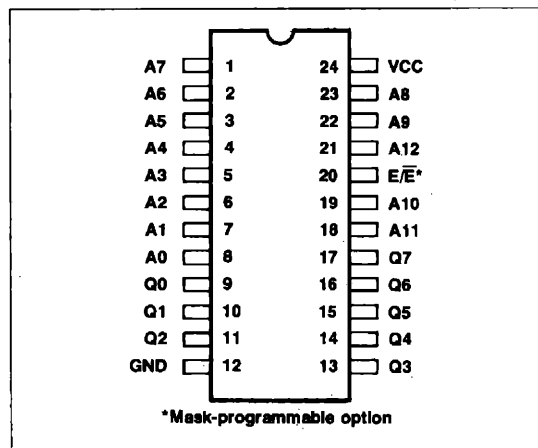
Power Down Standby Mode:
 S = Yes
 No letter = No

Access Time (Max):
 2 = 200 ns
 25 = 250 ns
 3 = 300 ns

Note: Submit ROM codes using the Rockwell ROM Code Order Form, Order No. 2137.



R2364A Block Diagram



R2364A Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.5 to +7.0	Vdc
Input Voltage	V _{IN}	-0.5 to +7.0	Vdc
Output Voltage	V _{OUT}	-0.5 to +7.0	Vdc
Temperature Under Bias Commercial Industrial	T _A	-10 to +80 -50 to +95	°C
Storage Temperature	T _{STG}	-65 to +150	°C
Power Dissipation	P	1.0	W

*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V _{OH}	Output High Voltage	2.4		V _{CC}	V	V _{CC} = 4.5V, I _{OH} = -400 μA
V _{OL}	Output Low Voltage			0.4	V	V _{CC} = 4.5V, I _{OL} = 3.3 mA
V _{IH}	Input High Voltage	2.0		V _{CC}	V	
V _{IL}	Input Low Voltage	-0.5		0.8	V	
I _{LI}	Input Load Current			10	μA	V _{CC} = 5.5V, 0V ≤ V _{in} ≤ 5.5V
I _{LO}	Output Leakage Current			±10	μA	V _{CC} = 5.5V, Chip Deselected, V _{OUT} = +0.4V to V _{CC}
I _{CC}	Power Supply Current, Active		25	55	mA	V _{CC} = 5.5V
I _{SB}	Power Supply Current, Standby ¹		7.5	16	mA	
C _I	Input Capacitance ²			7	pF	V _{CC} = 5.0V, chip deselected, pin under test at 0V, T _A = 25°C f = 1 MHz
C _O	Output Capacitance ²			10	pF	

Notes:

- Applies only to chip enable with power down standby mode.
- This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS

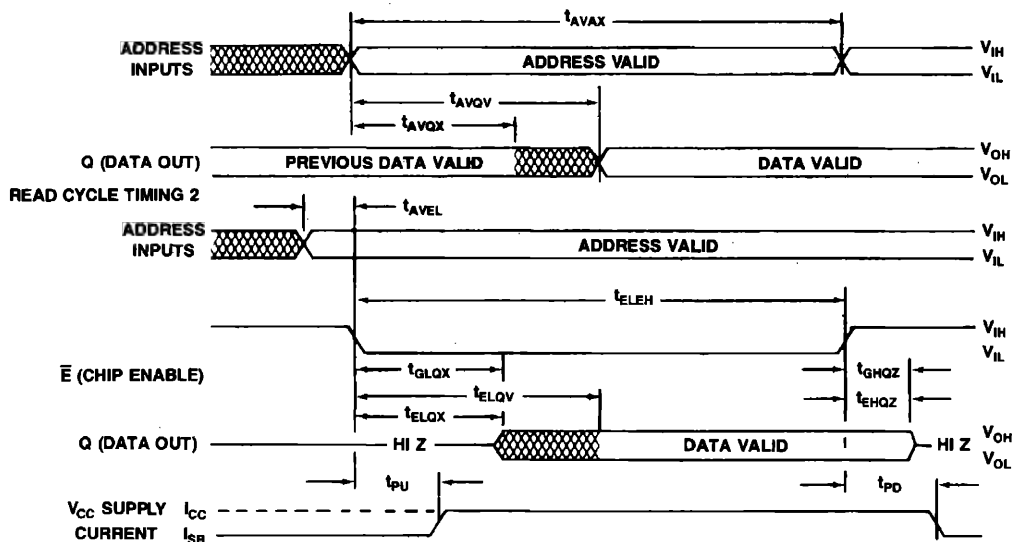
V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	R2364A2		R2364A25		R2364A3		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{AVAX}	Address Valid to Address Don't Care	200		250		300		ns
t _{ELEH}	Chip Enable Low to Chip Enable High ²	200		250		300		ns
t _{AVQV}	Address Valid to Output Valid (t _{ACC}) (Access)		200		250		300	ns
t _{ELQV}	Chip Enable Low to Output Valid (Access) ²		200		250		300	ns
t _{AVQX}	Address Valid to Output (t _{OH}) Invalid	10		10		10		ns
t _{ELQX}	Chip Enable Low to Output (t _{CO}) Invalid	10		10		10		ns
t _{EHQZ}	Chip Enable High to Output High Z (t _{DF})	10	70 ⁴	10	70 ⁴	10	70 ⁴	ns
t _{PU}	Chip Selection to Power Up Time ²	0		0		0		ns
t _{PD}	Chip Deselection to Power Down Time ²		100 ⁴		100 ⁴		100 ⁴	ns
t _{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t _{GLQX}	Chip Select Low to Output Invalid ³	10	90 ⁴	10	90 ⁴	10	90 ⁴	ns
t _{GHQZ}	Chip Select High to Output High Z	10	70 ⁴	10	70 ⁴	10	70 ⁴	ns

Notes:

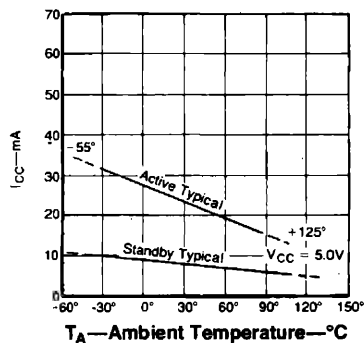
- Test Conditions:
Output Load: 2 TTL Loads and 100 pF; Input Transition Time: 20 ns; Timing Reference Levels: Input: 1.5V, Output: 0.8V, 2.0V.
- Mask-programmed for chip enable with power down standby mode.
- Mask-programmed for chip enable without power down standby mode.
- Add 20 ns for extended temperature devices (-40°C to +85°C).

TIMING DIAGRAMS

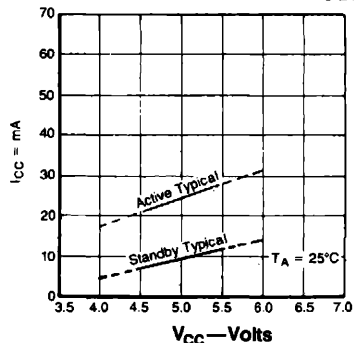
READ CYCLE TIMING 1 (\bar{E} HELD LOW)

TYPICAL CHARACTERISTICS

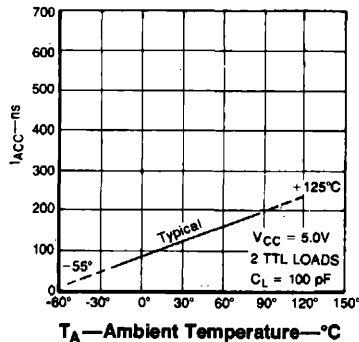
SUPPLY CURRENT VS AMBIENT TEMPERATURE



SUPPLY CURRENT VS SUPPLY VOLTAGE

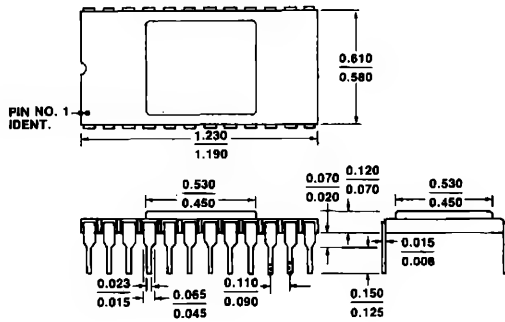


ACCESS TIME VS AMBIENT TEMPERATURE

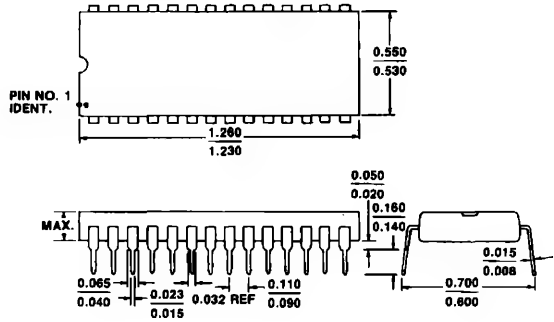


PACKAGE DIMENSIONS

24-PIN CERAMIC DIP



24-PIN PLASTIC DIP





R2364B

64K (8K × 8) STATIC ROM

DESCRIPTION

The R2364B2, R2364B25 and R2364B3 are 65,536-bit static Read-Only Memories (ROMs), organized as 8,192 eight-bit bytes, that offer maximum access times of 200, 250 and 300 nano-seconds, respectively. These ROMs are in industry-standard 28-pin, dual in-line packages, and are available in ceramic or low-cost plastic. These fully-static 64K-bit ROMs are compatible with all eight-bit N-channel microprocessors, including the R6500 family of microprocessors.

All three R2364B ROMs operate totally asynchronously, and require no clock input. Three mask-programmable chip select inputs allow up to eight 64K ROMs to be OR-tied without external decoding. These devices provide tri-state output buffers for memory expansion. The R2364B ROMs offer TTL input and output levels with a minimum noise immunity of 0.4 volts.

The mask-programmable chip enable input (E/\bar{E}) may be programmed to function as a chip select without power down standby mode or as a chip enable with power down standby mode. The active level of the enable input is also programmable.

FEATURES

- 8,192 × 8 organization
- Access time: 200 ns, 250 ns and 300 ns (max.)
- Low power dissipation: 125 mW active, 37.5 mW standby
- Drives two TTL loads and 100 pF
- Single +5V ± 10% power supply
- Totally static operation, no input clock required
- Completely TTL compatible
- Three tri-state mask-programmable chip select inputs
- Mask-programmable chip enable
- Tri-state outputs for memory expansion

ORDERING INFORMATION

Part Number: R2364B

Package:

C = Ceramic
P = Plastic

Temperature Range:

No letter = 0°C to +70°C
E = -40°C to +85°C

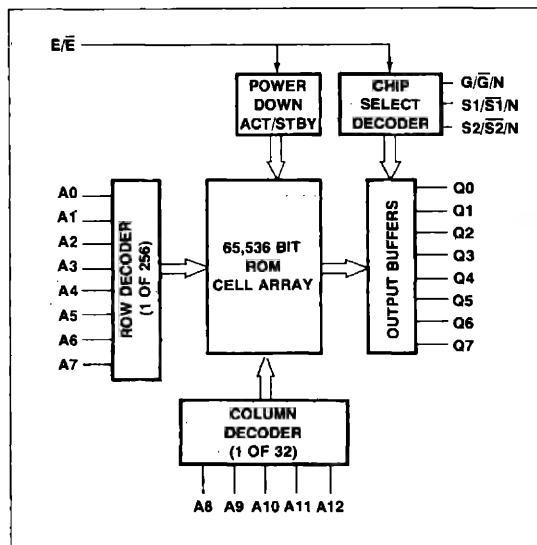
Power Down Standby Mode

S = Yes
No letter = No

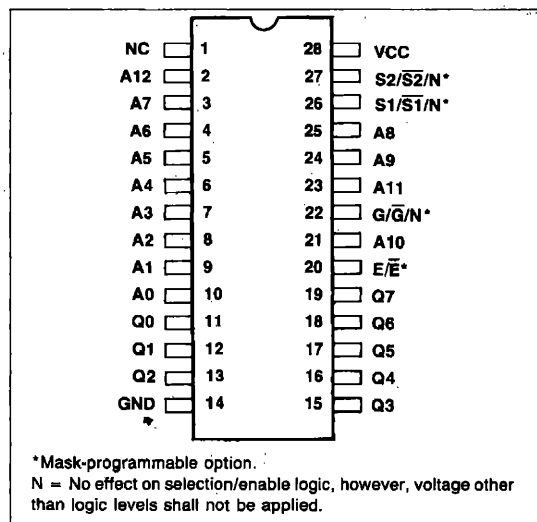
Access Time (Max):

2 = 200 ns
25 = 250 ns
3 = 300 ns

Note: Submit ROM codes using
Rockwell ROM Code Order
Form, Order No. 2137



R2364B Block Diagram



*Mask-programmable option.

N = No effect on selection/enable logic, however, voltage other than logic levels shall not be applied.

R2364B Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_{IN}	-0.5 to +7.0	Vdc
Output Voltage	V_{OUT}	-0.5 to +7.0	Vdc
Temperature Under Bias Commercial Industrial	T_A	-10 to +80 -50 to +95	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation	P	1.0	W

*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}	Output High Voltage	2.4		V_{CC}	V	$V_{CC} = 4.5V$, $I_{OH} = -400 \mu A$
V_{OL}	Output Low Voltage			0.4	V	$V_{CC} = 4.5V$, $I_{OL} = 3.3 mA$
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	-0.5		0.8	V	
I_{LI}	Input Load Current			10	μA	$V_{CC} = 5.5V$, $0V \leq V_{in} \leq 5.5V$
I_{LO}	Output Leakage Current			± 10	μA	$V_{CC} = 5.5V$, chip deselected, $V_{OUT} = +0.4V$ to V_{CC}
I_{CC}	Power Supply Current, Active		25	55	mA	$V_{CC} = 5.5V$
I_{SB}	Power Supply Current, Standby ¹		7.5	16	mA	
C_I	Input Capacitance ²			7	pF	$V_{CC} = 5.0V$, chip deselected, pin under test at 0V, $T_A = 25^\circ C$
C_O	Output Capacitance ²			10	pF	$f = 1 MHz$

Notes:

1. Applies only to chip enable with power down standby mode.
2. This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise specified)

Symbol	Parameter	R2364B2		R2364B25		R2364B3		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAX}	Address Valid to Address Don't Care	200		250		300		ns
t_{ELEH}	Chip Enable Low to Chip Enable High ²	200		250		300		ns
t_{AVQV}	Address Valid to Output Valid (t_{ACC}) (Access)		200		250		300	ns
t_{ELQV}	Chip Enable Low to Output Valid (Access) ²		200		250		300	ns
t_{AVQX}	Address Valid to Output (t_{OH}) Invalid	10		10		10		ns
t_{ELQX}	Chip Enable Low to Output (t_{CO}) Invalid	10		10		10		ns
t_{EHQZ}	Chip Enable High to Output High Z (t_{DF})	10	70 ⁴	10	70 ⁴	10	70 ⁴	ns
t_{PU}	Chip Selection to Power Up Time ²	0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time ²		100 ⁴		100 ⁴		100 ⁴	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{GLQV}	Chip Select Low to Output Valid ³	10	90 ⁴	10	90 ⁴	10	90 ⁴	ns
t_{GHQZ}	Chip Select High to Output High Z	10	70 ⁴	10	70 ⁴	10	70 ⁴	ns

Notes:

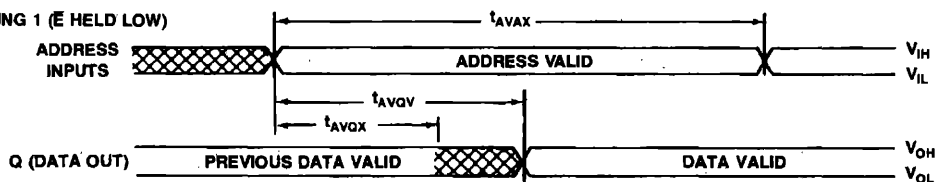
1. Test Conditions:

Output Load: 2 TTL Loads and 100 pF; Input Transition Time: 20 ns; Timing Reference Levels: Input: 1.5V; Output: 0.8V, 2.0V.

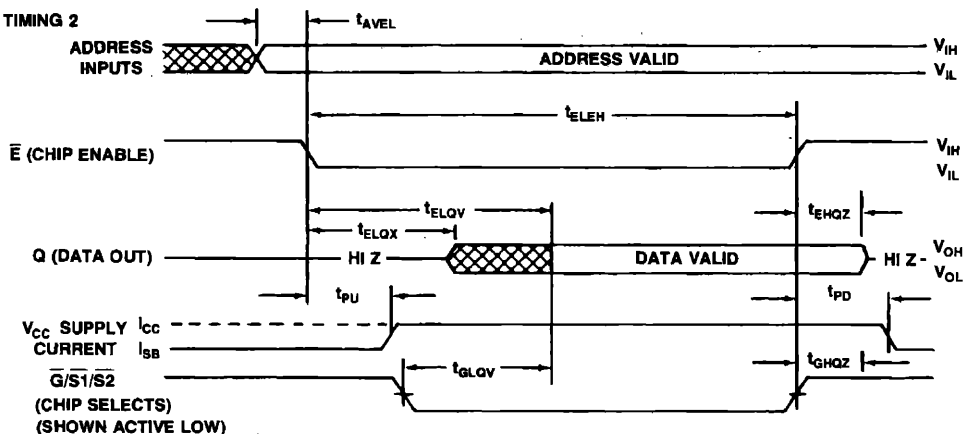
2. Mask programmed for chip enable with power down standby mode.
3. Mask programmed for chip enable without power down standby mode.

4. Add 20 ns for extended temperature devices ($-40^\circ C$ to $+85^\circ C$).
5. \bar{G} may be delayed up to $t_{AVQV} - t_{GLQV}$ after the falling edge of \bar{E} without impact on t_{AVQV} . Data is available at the Q outputs after a delay of t_{GLQV} from the falling edge of \bar{G} , provided that \bar{E} has been low (V_{IL}) and addresses have been valid for at least $t_{AVQV} - t_{GLQV}$.
6. t_{GHQZ} and t_{EHQZ} are specified from \bar{G} or \bar{E} , whichever occurs first.

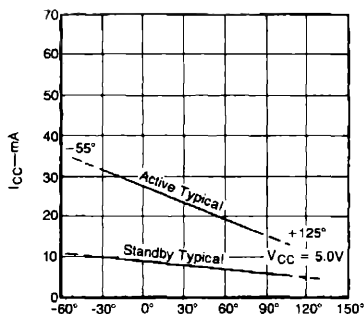
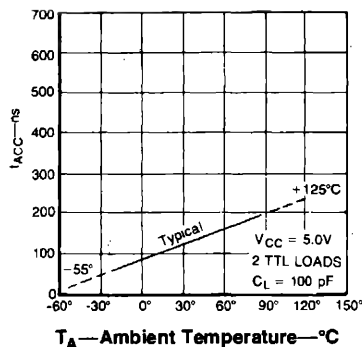
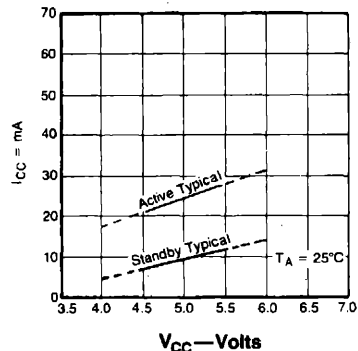
TIMING DIAGRAMS

READ CYCLE TIMING 1 (\bar{E} HELD LOW)

READ CYCLE TIMING 2

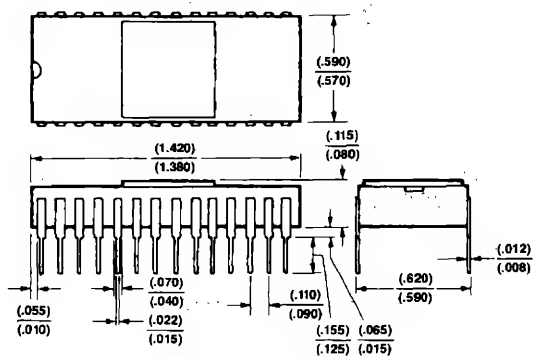


TYPICAL CHARACTERISTICS

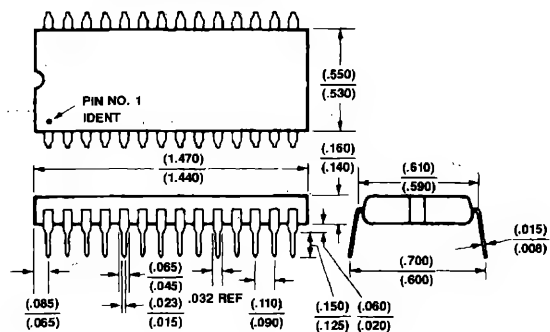
SUPPLY CURRENT VS
AMBIENT TEMPERATUREACCESS TIME VS
AMBIENT TEMPERATURESUPPLY CURRENT VS
SUPPLY VOLTAGE

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP





R23C64

64K (8K × 8) CMOS STATIC ROM

PRELIMINARY

DESCRIPTION

The Rockwell R23C64 is an 8K × 8 (65,536 bits) CMOS static read-only-memory (ROM) housed in a 28-pin JEDEC standard (B version) package. It is fabricated in CMOS technology to achieve high performance with extremely low power dissipation. This device is available with maximum access times of 150, 250, or 300 nanoseconds, optional extended temperature range, and packaged in ceramic or low-cost plastic.

The R23C64 is controlled via the chip enable (\bar{E}) and the mask programmable chip selects ($G/\bar{G}/N$, $S1/\bar{S1}/N$, $S2/\bar{S2}/N$). The addresses are latched on the falling edge of \bar{E} , allowing the R23C64 to operate on multiplexed busses as well as non-multiplexed busses. The chip selects control the output buffers, however, these buffers do not become active until valid data is present from the internal data latches. This prevents spurious, invalid outputs that increase power dissipation. When \bar{E} is high, the output buffers are in the high impedance state and the address and chip select pins are ignored. \bar{E} may also be held low indefinitely, keeping the address latched and the output buffers under chip select control.

FEATURES

- 8,192 × 8 organization
- JEDEC approved pinout
- Extremely low power
 - Active 10 mW (max.)
 - Active (quiescent) 50 μ W
 - Standby 50 μ W (max.)
- Fast access times: 150 ns, 250 ns and 300 ns (max.)
- Mask programmable chip selects
- Latched addresses and (optional) latched chip selects
- Drive two TTL loads and 130 pF
- Single 5V \pm 10% power supply
- Pin compatible with Rockwell R2364B NMOS ROMs and R87C64 and R2764 EPROMs

ORDERING INFORMATION

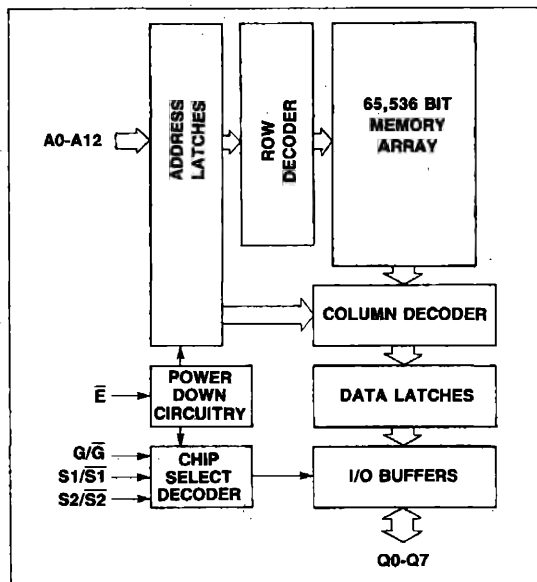
Part Number: R23C64

L Temperature Range:
No letter = 0°C to +70°C
E = -40°C to +85°C

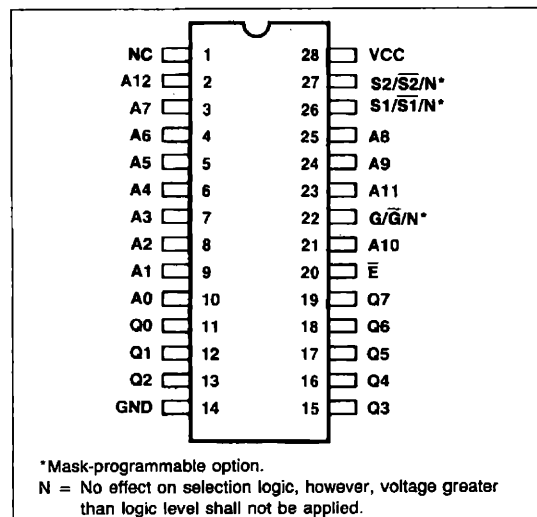
Package:
C = Ceramic
P = Plastic

Note: Submit ROM codes using Rockwell ROM Code Order Form, Order No. 2137.

Access Time (Max):
15 = 150 ns
25 = 250 ns
3 = 300 ns



R23C64 Block Diagram



R23C64 Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	Vdc
Output Voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	Vdc
Temperature Under Bias Commercial Industrial	T_A	-10 to +80 -50 to +95	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Power Dissipation	P	1.0	W

*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}	Output High Voltage	2.4		V_{CC}	V	$V_{CC} = 4.5V$, $I_{OH} = -200 \mu A + 130 pF$
V_{OL}	Output Low Voltage			0.4	V	$V_{CC} = 4.5V$, $I_{OL} = 3.2 mA + 130 pF$
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
I_{LI}	Input Load Current			± 1	μA	$V_{CC} = 5.5V$, $0V \leq V_{IN} \leq 5.5V$
I_{LO}	Output Leakage Current			± 10	μA	$V_{CC} = 5.5V$, chip deselected, $V_{OUT} = +0.4V$ to V_{CC}
I_{CC}	Power Supply Current, Active			2 1	mA mA	$T_{ELQV} = 150 ns^1$, $V_{CC} = 5.5V$ $T_{ELQV} = 300 ns^2$, $V_{CC} = 5.5V$
I_{SB}	Power Supply Current, Standby			10	μA	$\bar{E} = V_{CC} - 0.5V$; all other pins active
C_I	Input Capacitance (all but \bar{E}) (E)		5 10		pF pF	$V_{CC} = 5.0V$, chip deselected, pin under test at $0V$, $T_A = 25^\circ C$, $f = 1 MHz$
C_O	Output Capacitance ³		10		pF	

Notes:

- $T_{ELEH} = 150 ns$, all pins active, no loads, $1 \mu sec$ cycle time ($T_{ELEN} = 1 \mu s$).
- $T_{ELEH} = 300 ns$, all pins active, no loads, $2 \mu sec$ cycle time ($T_{ELEN} = 2 \mu s$).
- This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise specified)

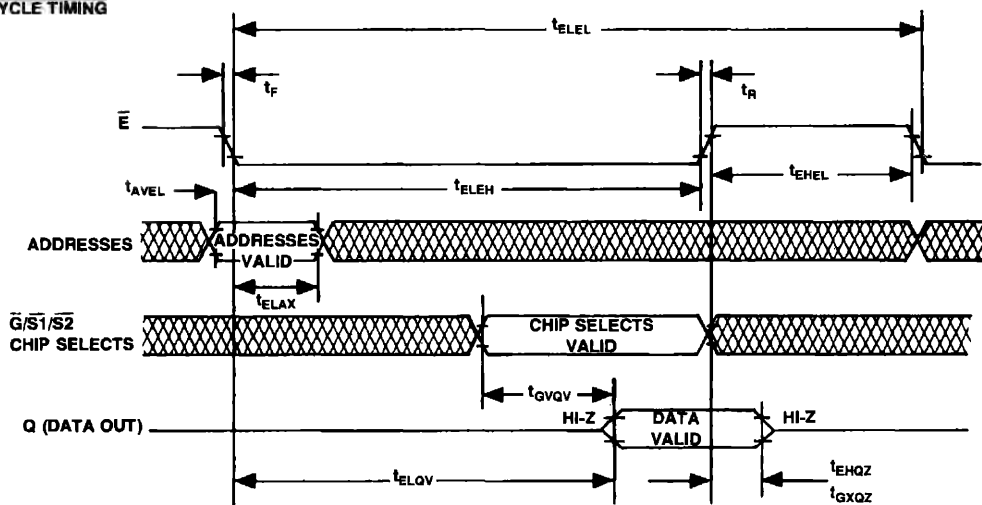
Symbol	Parameter	R23C64-15		R23C64-25		R23C64-3		Unit
		Min	Max	Min	Max	Min	Max	
t_{EEL}	Cycle Time	220		365		465		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	150		250		300		ns
t_{EHEL}	Chip Enable High to Chip Enable Low	60		100		150		ns
t_{ELQV}	Chip Enable Low to Output Valid (Access)		150		250		300	ns
t_{AVEL}	Address Setup Time	0		0		0		ns
t_{ELAX}	Address Hold Time	50		65		80		ns
t_{GVQV}	Chip Select Valid to Output Valid			100		150		ns
t_{EHQZ}^4	Chip Enable High to Output High Z		50		50	10	50	ns
t_{GXQZ}^4	Chip Selects Invalid to Output High Z	10	50	10	50	10		ns
t_F, t_R	Rise and Fall Times ⁽²⁾		10		15		20	ns

Notes:

1. Test Conditions: Output Load: 2 TTL Loads and 100 pF; Input Transition Time: 20 ns; Timing Reference Levels: Input: 1.5V; Output: 0.8V, 2.0V.
2. Rise and Fall times stated are required for these high performance parameters only and may be relaxed to 100 ns for slower operation, e.g., 100 kHz operation.
3. \bar{G} may be delayed up to $t_{AVQV} - t_{GLQV}$ after the falling edge of \bar{E} without impact on t_{AVQV} . Data is available at the Q outputs after a delay of t_{GLQV} from the falling edge of \bar{G} , provided that \bar{E} has been low (V_{IL}) and addresses have been valid for at least $t_{AVQV} - t_{GLQV}$.
4. t_{EHQZ} , t_{GXQZ} are specified from \bar{G} or \bar{E} whichever occurs first.

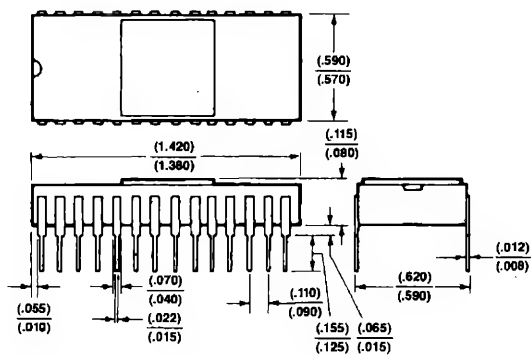
TIMING DIAGRAM

READ CYCLE TIMING

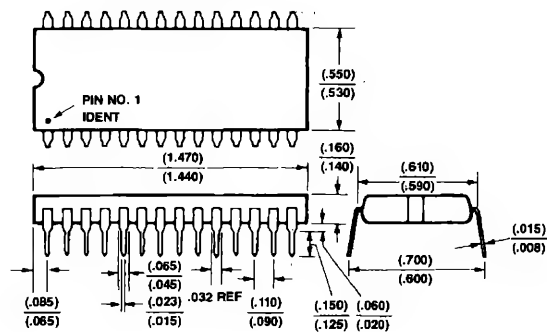


PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP





R23128

128K (16K × 8) STATIC ROM

DESCRIPTION

The R23128-25 and R23128-3 are 131,072-bit static Read-Only Memories (ROMs), organized as 16,384 eight-bit bytes, that offer maximum access times of 250 and 300 nanoseconds, respectively. These ROMs are in industry-standard 28-pin, dual in-line packages, and are available in ceramic or low-cost plastic. These fully-static 128K-bit ROMs are compatible with all N-channel microprocessors.

The R23128 ROMs operate totally asynchronously, and require no clock input. Three mask-programmable chip select inputs allow up to eight 128K ROMs to be OR-tied without external decoding. These devices provide tri-state output buffers for memory expansion. The R23128 ROMs offer TTL input and output levels with a minimum noise immunity of 0.4 volts.

The chip enable input (\bar{E}) functions as a chip enable with power down standby mode. When this line is high the chip is disabled and enters a low power standby state.

FEATURES

- 16,384 × 8 organization bytes
- Access time: 250 ns and 300 ns (max.)
- Low typical power dissipation is 100 mW active, 20 mW standby
- Drives two TTL loads and 100 pF
- Single +5V ± 10% power supply
- Totally static operation, no input clock required
- Completely TTL compatible
- Three mask-programmable chip select inputs
- Tri-state outputs for memory expansion

ORDERING INFORMATION

Part Number: R23128

Package:

C = Ceramic
P = Plastic

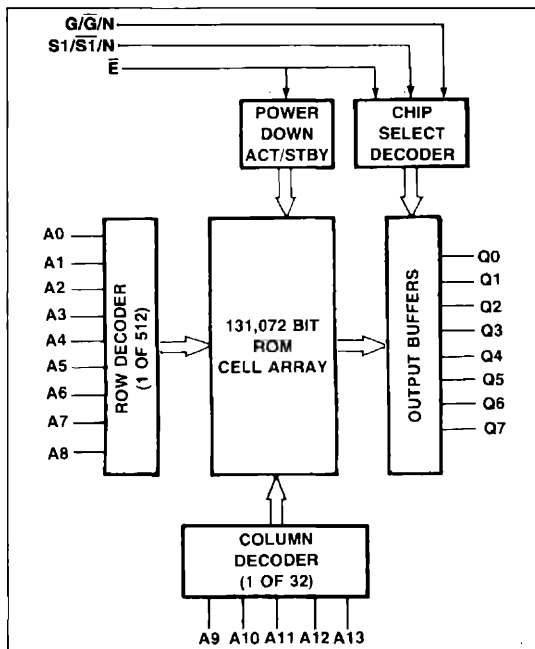
Temperature Range:

No letter = 0°C to +70°C
E = -40°C to +85°C

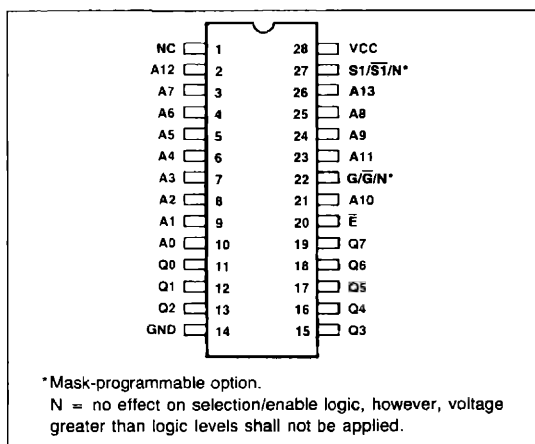
Note: Submit ROM codes using Rockwell ROM Code Order Form, Order No. 2137

Access Time (Max):

25 = 250 ns
3 = 300 ns



R23128 Block Diagram



R23128 Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_{in}	-0.5 to +7.0	Vdc
Output Voltage	V_{out}	-0.5 to +7.0	Vdc
Temperature under Bias Commercial Industrial	T_A	-10 to +80 -50 to +95	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation	P_D	1.0	W

*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	V	$V_{CC} = 4.5V$, $I_{OH} = -400 \mu A$
V_{OL}	Output LOW Voltage			0.4	V	$V_{CC} = 4.5V$, $I_{OL} = 3.3 mA$
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage	-0.5		0.8	V	
I_{LI}	Input Load Current			10	μA	$V_{CC} = 5.5V$, $0V \leq V_{in} \leq 5.5V$
I_{LO}	Output Leakage Current			± 10	μA	$V_{CC} = 5.5V$, chip deselected $V_{out} = +0.4V$ to V_{CC}
I_{CC}	Power Supply Current, Active		20	55	mA	$V_{CC} = 5.5V$
I_{SB}	Power Supply Current, Standby		7.5	16	mA	
C_I	Input Capacitance ¹			7	pF	$V_{CC} = 5.0V$, chip deselected, pin under test at $0V$, $T_A = 25^\circ C$ $f = 1 MHz$
C_O	Output Capacitance ¹			10	pF	

Note:
1. This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise specified)

Symbol	Parameter	R23128-25		R23128-3		Units
		Min	Max	Min	Max	
t_{AVAX}	Address Valid to Address Don't Care	250		300		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	250		300		ns
t_{AVQV}	Address Valid to Output Valid (t_{ACC}) (Access)		250		300	ns
t_{ELQV}	Chip Enable Low to Output Valid (Access)		250		300	ns
t_{AVQX}	Address Valid to Output (t_{OH}) Invalid	10		10		ns
t_{ELQX}	Chip Enable Low to Output (t_{CO}) Invalid	10		10		ns
t_{EHQZ}	Chip Enable High to Output High Z (t_{DF})	10	70	10	70	ns
t_{PU}	Chip Selection to Power Up Time	0		0		ns
t_{PD}	Chip Deselection to Power Down Time		100		100	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{GLQV}	Chip Select Low to Output Valid	10	90 ²	10	90 ²	ns
t_{GHQZ}	Chip Select High to Output High Z	10	70 ²	10	70 ²	ns

Notes:

1. Test Conditions:

Output load: 2 TTL loads and 100 pF

Input transition time: 20 ns

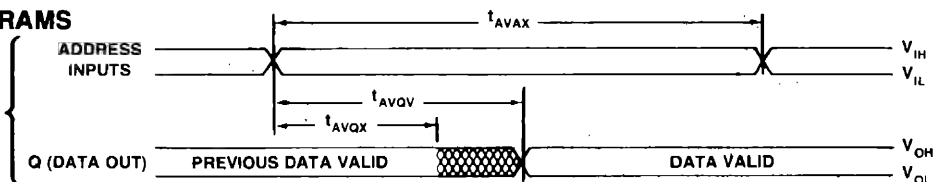
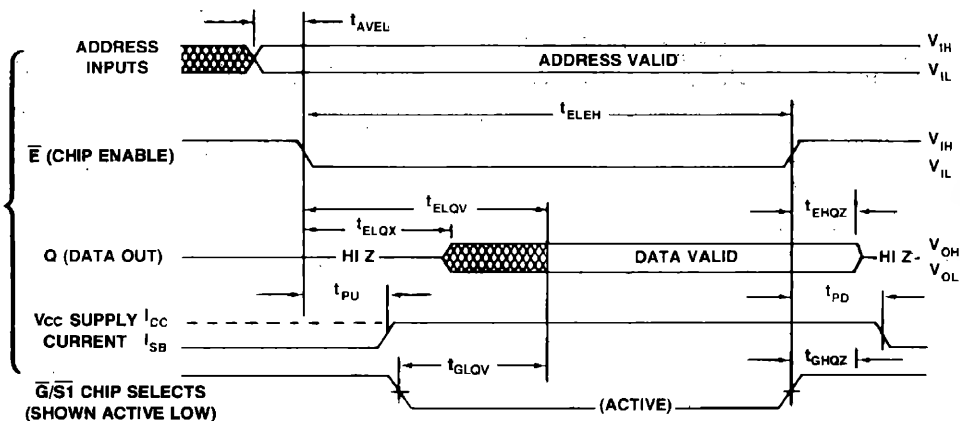
Timing reference levels: Input: 1.5V; Output: 0.8V, 2.0V

2. Add 20 ns for extended temperature devices ($-40^\circ C$ to $+85^\circ C$).

3. \bar{G} may be delayed up to $t_{AVQV} - t_{GLQV}$ after the falling edge of \bar{E} without impact on t_{AVQV} . Data is available at the Q outputs after a delay of t_{GLQV} from the falling edge of \bar{G} , provided that \bar{E} has been low (V_{IL}) and addresses have been valid for at least $t_{AVQV} - t_{GLQV}$.

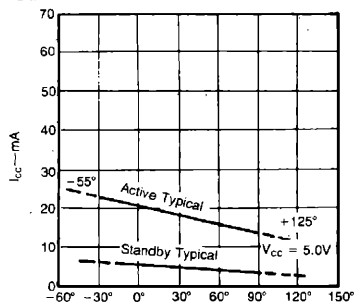
4. t_{GHQZ} and t_{EHQZ} are specified from \bar{G} or \bar{E} , whichever occurs first.

TIMING DIAGRAMS

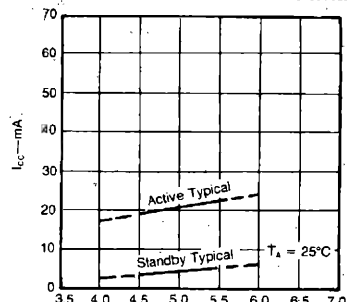
READ CYCLE
TIMING 1
(\bar{E} HELD LOW)READ CYCLE
TIMING 2

TYPICAL CHARACTERISTICS

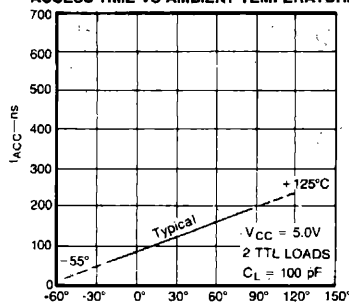
SUPPLY CURRENT VS AMBIENT TEMPERATURE

 T_A —Ambient Temperature—°C

SUPPLY CURRENT VS SUPPLY VOLTAGE

 V_{CC} —Volts

ACCESS TIME VS AMBIENT TEMPERATURE

 T_A —Ambient Temperature—°C

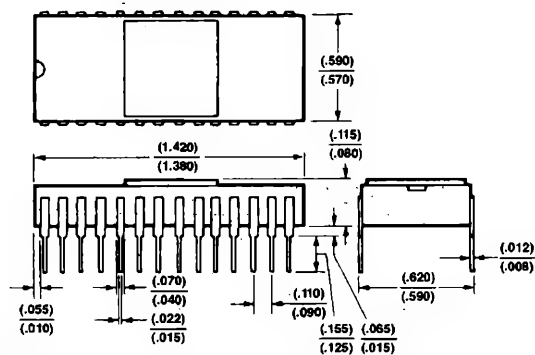
28-PIN CERAMIC DIP

Figure 1 is a mechanical drawing of the package, showing top, side, and detail views with dimensions in inches. The top view shows a rectangular package with a notch on the left side, labeled "PIN NO. 1 IDENT". Dimensions include a width of (1.470) and (1.440), and a height of (.550) and (.530). The side view shows a package with a height of (.160) and (.140), and a width of (.610) and (.590). The detail view shows a cross-section of the package with dimensions (.085), (.065), (.085), (.045), (.023), (.015), (.032 REF), (.110), (.090), (.150), (.060), (.125), (.020), (.015), and (.008).



R27C64P

64K (8K × 8) CMOS ONE-TIME PROM

PRELIMINARY

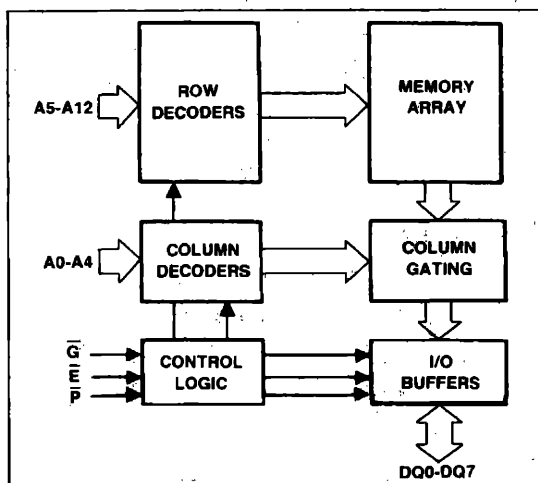
FEATURES

- 8,192 × 8 organization
- JEDEC approved pin-out
- Low Power
 - Active 80 mW (max.)
 - Standby 525 μ W (max.)
- Access times: 250 ns and 350 ns (max.)
- Single 5V power supply
- Static operation, no clocks required
- One-time programmable
- TTL compatible inputs and tri-state outputs during both read and program mode
- Pin compatible with INTEL 2764A EPROM, Rockwell R87C64 EPROM and R23C64 and R2364B ROMs.

ORDERING INFORMATION

Part Number: R27C64P

Access Time:
25 = 250 ns
35 = 350 ns



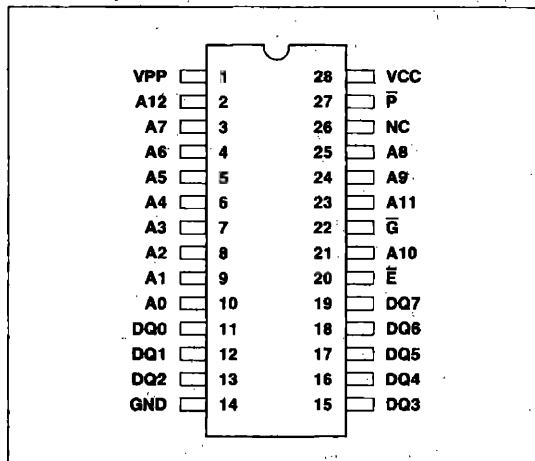
R27C64P Block Diagram

DESCRIPTION

The Rockwell R27C64P is an 8K × 8 (65,536 bits) one-time programmable read-only-memory (PROM). It is manufactured using CMOS technology for low power dissipation in both active and standby operating modes. Access times of 250 ns and 350 ns is performance compatible with most 8-bit and 16-bit microprocessors.

Initially, all bits are in the "1" state. Data is programmed by applying 21V to V_{PP} a TTL low to \bar{E} , and a 50 ms low pulse on \bar{P} while the desired data is stable on D_{Q0}-D_{Q7} lines and the address is stable on A₀-A₁₂ lines.

The R27C64P is ideal for low-cost permanent memory applications (program and/or data) in production runs requiring fast programming turn-around either at the factory, distributor/dealer or user's facility.



R27C64P Pin Configuration

A0-A12	ADDRESSES
\bar{E}	CHIP ENABLE
\bar{G}	OUTPUT ENABLE
DQ0-DQ7	DATA INPUT/OUTPUT
\bar{P}	PROGRAM ENABLE

R27C64P Pin Names

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage All, except V_{pp} during Programming V_{pp} during Programming	V_{IN}	-0.3 to $V_{CC} + 0.3$ -0.3 to +22.0	Vdc
Output Voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	Vdc
Temperature under Bias	T_A	-10 to +80	°C
Storage Temperature	T_{STG}	-40 to 125	°C
Power Dissipation @ 25°C	P	1.0	W

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Read Mode	Program Mode
V_{CC} Supply Voltage	5V ± 5%	5V ± 5%
V_{PP} Supply Voltage		21V ± 0.5V
Temperature Range	0 to 70°C	0 to 70°C

DC OPERATING CHARACTERISTICS DURING READ

$V_{CC} = 5.0V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{OH}	Output High Voltage	2.4		—	V	$I_{OH} = -400 \mu A$
V_{OL}	Output Low Voltage	—		0.45	V	$I_{OL} = 2.1 \text{ mA}$
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.1		0.8	V	
I_{CC1}	V_{CC} Standby Current			100	μA	$\bar{E} = V_{CC}$, $\bar{G} = V_{IL}$, $V_{IN} = 0V$ or V_{CC}
I_{CC2}	V_{CC} Active Current			15	mA	$\bar{E} = \bar{G} = V_{IL}$
I_{PP}	V_{PP} Current			100	μA	$V_{PP} = V_{CC} \text{ max.}$
I_{IN}	Input Leakage Current			± 10	μA	$V_{IN} = 0V$ to V_{CC}
I_O	Output Leakage Current			± 10	μA	$V_{OUT} = 0V$ to V_{CC}
C_I	Input Capacitance ²			7	pF	$V_{CC} = 5.0V$, chip deselected, pin under test at 0V, $T_A = 25^\circ C$ $f = 1 \text{ MHz}$
C_O	Output Capacitance ²			10	pF	

Notes:

1. Applies only to chip enable with power down standby mode.
2. This parameter is periodically sampled and is not 100% tested.

DC OPERATING CHARACTERISTICS DURING PROGRAMMING

$V_{CC} = 5.0V \pm 5\%$, $T_A = 20^\circ C$ to $30^\circ C$, $V_{PP} = 21.0V \pm 0.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.1		0.8	V	
I_{CC}	V_{CC} Active Current			0.5	mA	$\bar{E} = \bar{P} = V_{IL}$, $\bar{G} = V_{IH}$
I_{PP}	V_{PP} Active Current			30	mA	
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = 0V$ to V_{CC}



R27C64P

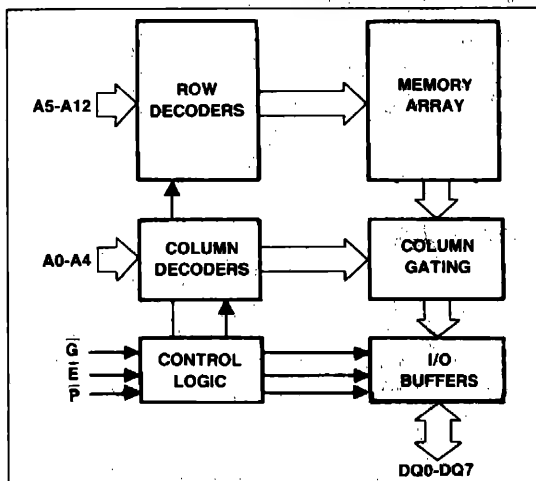
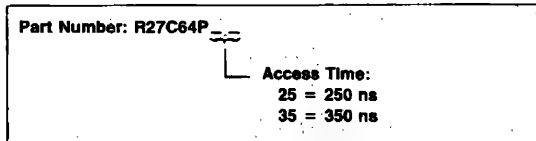
64K (8K × 8) CMOS ONE-TIME PROM

PRELIMINARY

FEATURES

- 8,192 × 8 organization
- JEDEC approved pin-out
- Low Power
 - Active 80 mW (max.)
 - Standby 525 μ W (max.)
- Access times: 250 ns and 350 ns (max.)
- Single 5V power supply
- Static operation, no clocks required
- One-time programmable
- TTL compatible inputs and tri-state outputs during both read and program mode
- Pin compatible with INTEL 2764A EPROM, Rockwell R87C64 EPROM and R23C64 and R2364B ROMs.

ORDERING INFORMATION



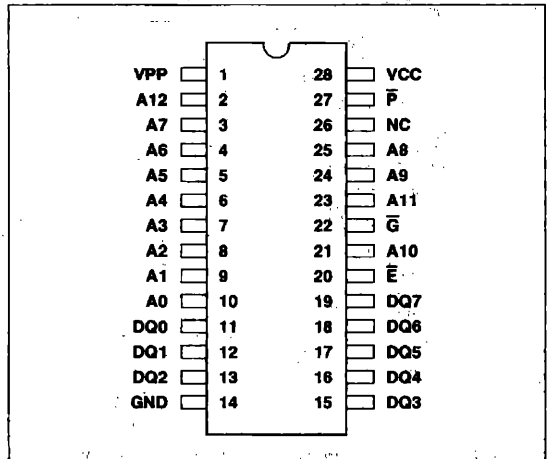
R27C64P Block Diagram

DESCRIPTION

The Rockwell R27C64P is an 8K × 8 (65,536 bits) one-time programmable read-only-memory (PROM). It is manufactured using CMOS technology for low power dissipation in both active and standby operating modes. Access times of 250 ns and 350 ns is performance compatible with most 8-bit and 16-bit microprocessors.

Initially, all bits are in the "1" state. Data is programmed by applying 21V to V_{PP} a TTL low to \bar{E} , and a 50 ms low pulse on \bar{P} while the desired data is stable on DQ0-DQ7 lines and the address is stable on A0-A12 lines.

The R27C64P is ideal for low-cost permanent memory applications (program and/or data) in production runs requiring fast programming turn-around either at the factory, distributor/dealer or user's facility.



R27C64P Pin Configuration

A0-A12	ADDRESSES
\bar{E}	CHIP ENABLE
G	OUTPUT ENABLE
DQ0-DQ7	DATA INPUT/OUTPUT
\bar{P}	PROGRAM ENABLE

R27C64P Pin Names

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage All, except V_{PP} during Programming V_{PP} during Programming	V_{IN}	-0.3 to $V_{CC} + 0.3$ -0.3 to +22.0	Vdc
Output Voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	Vdc
Temperature under Bias	T_A	-10 to +80	°C
Storage Temperature	T_{STG}	-40 to 125	°C
Power Dissipation @ 25°C	P	1.0	W

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Read Mode	Program Mode
V_{CC} Supply Voltage	5V ± 5%	5V ± 5%
V_{PP} Supply Voltage		21V ± 0.5V
Temperature Range	0 to 70°C	0 to 70°C

DC OPERATING CHARACTERISTICS DURING READ

$V_{CC} = 5.0V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{OH}	Output High Voltage	2.4		—	V	$I_{OH} = -400 \mu A$
V_{OL}	Output Low Voltage	—		0.45	V	$I_{OL} = 2.1 \text{ mA}$
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.1		0.8	V	
I_{CC1}	V_{CC} Standby Current			100	μA	$\bar{E} = V_{CC}$, $\bar{G} = V_{IL}$, $V_{IN} = 0V$ or V_{CC}
I_{CC2}	V_{CC} Active Current			15	mA	$\bar{E} = \bar{G} = V_{IL}$
I_{PP}	V_{PP} Current			100	μA	$V_{PP} = V_{CC} \text{ max.}$
I_{IN}	Input Leakage Current			± 10	μA	$V_{IN} = 0V$ to V_{CC}
I_O	Output Leakage Current			± 10	μA	$V_{OUT} = 0V$ to V_{CC}
C_I	Input Capacitance ²			7	pF	$V_{CC} = 5.0V$, chip deselected, pin under test at 0V, $T_A = 25^\circ C$
C_O	Output Capacitance ²			10	pF	$f = 1 \text{ MHz}$

Notes:

1. Applies only to chip enable with power down standby mode.
2. This parameter is periodically sampled and is not 100% tested.

DC OPERATING CHARACTERISTICS DURING PROGRAMMING

$V_{CC} = 5.0V \pm 5\%$, $T_A = 20^\circ C$ to $30^\circ C$, $V_{PP} = 21.0V \pm 0.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.1		0.8	V	
I_{CC}	V_{CC} Active Current			0.5	mA	$\bar{E} = \bar{P} = V_{IL}$, $\bar{G} = V_{IH}$
I_{PP}	V_{PP} Active Current			30	mA	
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = 0V$ to V_{CC}

AC CHARACTERISTICS DURING READ

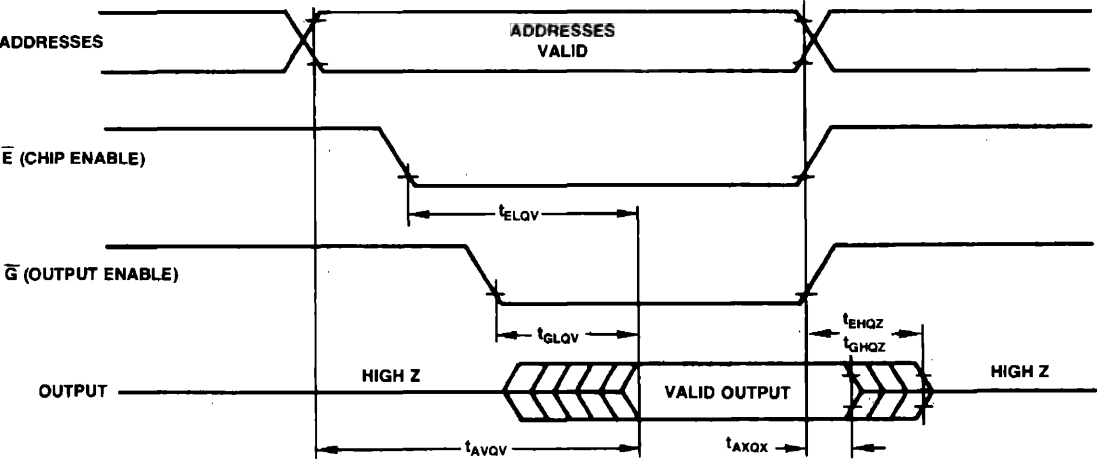
V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	R27C64P-25			R27C64P-35			Unit	Test Conditions ⁽³⁾
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{AVQV}	Address to Data Valid			250			350	ns	$\overline{E} = \overline{G} = V_{IL}$
t _{ELQV}	Chip Enable to Data Valid			250			350	ns	$\overline{G} = V_{IL}$
t _{GLQV} ¹	Output Enable to Data Valid	10		100	10		120	ns	$\overline{E} = V_{IL}$
t _{GHQZ} ²	Output Enable to High Impedance	0		90	0		100	ns	$\overline{E} = V_{IL}$
t _{AXQX}	Address to Output Hold	0			0			ns	$\overline{E} = \overline{G} = V_{IL}$
t _{EHQZ}	Chip Enable to High Impedance	0		90	0		100	ns	$\overline{G} = V_{IL}$

- Notes:
- 1. \overline{G} may be delayed up to t_{AVQV}–t_{GLQV} after the falling edge of \overline{E} without impact on t_{AVQV}. Data is available at the DQ outputs after a delay of t_{GLQV} from the falling edge of \overline{G} , provided that \overline{E} has been low (V_{IL}) and addresses have been valid for at least t_{AVQV}–t_{GLQV}.
 - 2. t_{GHQZ} and t_{EHQZ} are specified from \overline{G} or \overline{E} , whichever occurs first.
 - 3. Test Conditions:
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level: Inputs 1V and 2V
Outputs 0.8V and 2V

4

READ TIMING DIAGRAM



AC CHARACTERISTICS DURING PROGRAM

 $V_{CC} = 5.0V \pm 5\%$, $T_A = 20^\circ C$ to $30^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AVPL}	Address set-up time	2			μS
t_{DZGL}	\bar{G} set-up time	2			μS
t_{DVPL}	Data set-up time	2			μS
t_{ELPL}	\bar{E} set-up time	2			μS
t_{VHPL}	V_{PP} set-up time	2			μS
t_{PHDX}	Data hold time	2			μS
t_{GHAX}	Address hold time	0			μS
t_{GLQV}	Output enable to data valid			120	ns
t_{GHQZ}	Output disable to output high impedance	0		100	ns
t_{PLPH}	\bar{P} pulse width during programming	45	50	55	ms

Notes:

Test Conditions:

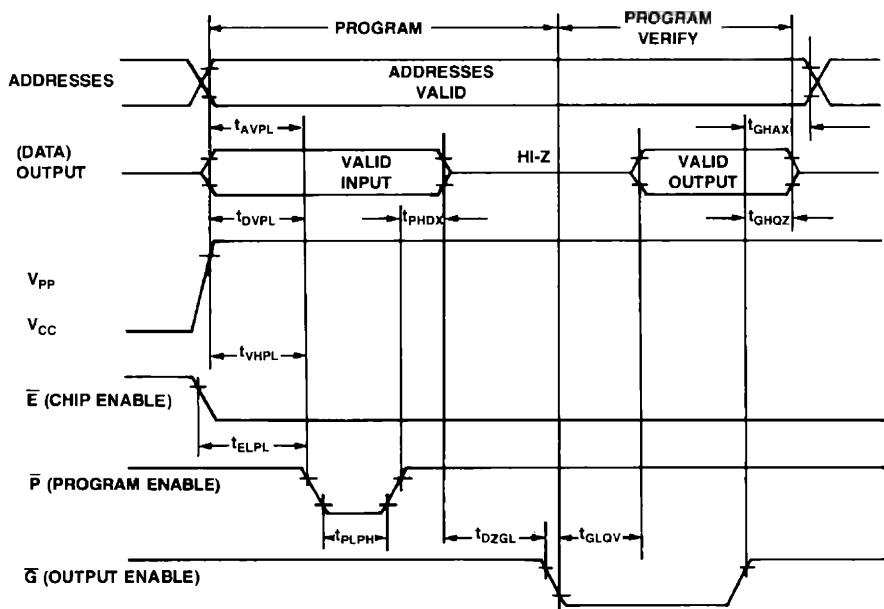
Output Load: 1 TTL gate and $C_L = 100$ pFInput Rise and Fall Times: ≤ 20 ns

Input Pulse Levels: 0.45V to 2.4V

Timing Measurement Reference Level: Inputs 1V and 2V

Outputs 0.8V and 2V

PROGRAM TIMING DIAGRAM



OPERATING MODES

The Rockwell R27C64P has five modes of operation (see table 1).

Read Mode

The read mode is governed by two control pins, \bar{E} and \bar{G} . In order to obtain data at the outputs, both \bar{E} and \bar{G} must be V_{IL} . \bar{E} is the power control and should be used for device selection. \bar{G} is the output control and should be used to gate data to the output pins. Valid data will appear on the output pins after T_{AVQV} , T_{ELQV} or T_{GLQV} times, depending on which is limiting.

Standby Mode

The standby mode of the R27C64P reduces power dissipation. The R27C64P is placed in the standby mode by making $\bar{E} = V_{IH}$. This is independent of \bar{G} and automatically puts the outputs in their high impedance (High-Z) state.

Program Mode

The R27C64P is in the program mode when V_{PP} is at 21V with \bar{E} input at V_{IL} . The data to be programmed is applied to the data output pins. When the address controls and data are stable, a 50 msec program pulse is applied to the \bar{P} input.

Program Verify Mode

A program verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 21V. Data should be verified to t_{GLQV} after the falling edge of \bar{G} .

Program Inhibit Mode

The program inhibit mode allows programming several R27C64P EPROMs simultaneously with different data for each by using \bar{E} to control which devices respond to the program pulse on \bar{P} .

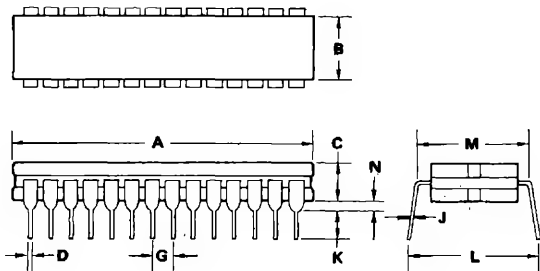
Table 1. Mode Selection

Pin Mode	\bar{E} (20)	\bar{G} (22)	\bar{P} (27)	V_{PP} (1)	V_{CC} (28)	DQ0-DQ7 (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	+5	+5	Q_{OUT}
Standby	V_{IH}	No Effect	No Effect	+5	+5	High-Z
Program	V_{IL}	No Effect	V_{IL}	+21	+5	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	+21	+5	Q_{OUT}
Program inhibit	V_{IH}	No Effect	No Effect	+21	+5	High-Z
Program inhibit	No Effect	No Effect	V_{IH}	+21	+5	High-Z

Note: No Effect = No effect on selection/enable logic, however, no voltage other than logic levels shall be applied.

PACKAGE DIMENSIONS

28-PIN CERDIP



NOTE: EITHER ROUND OR SQUARE UV WINDOW.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.32	37.34	1.430	1.470
B	12.95	13.46	0.510	0.530
C	3.68	4.19	0.145	0.165
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
J	0.20	0.30	0.008	0.012
K	3.18	4.19	0.125	0.165
L	16.13	17.41	0.635	0.685
M	15.24	15.75	0.600	0.620
N	0.89	1.14	0.035	0.045



R87C32 32K (4K × 8) CMOS UV EPROM

PRELIMINARY

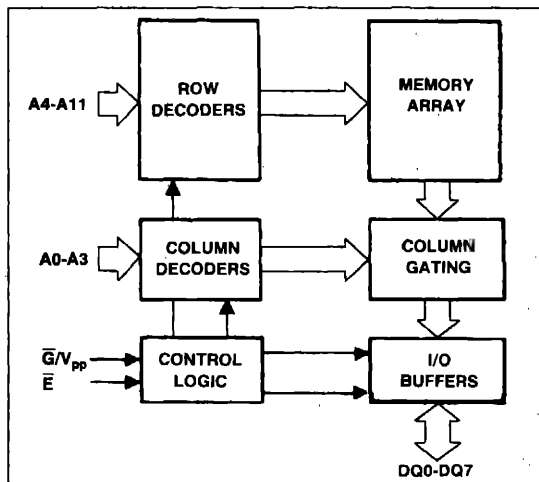
FEATURES

- 4096 × 8 organization
- JEDEC approved pin-out
- Low Power
 - Active: 132 mW (max.)
 - Standby: 525 μ W (max.)
- Access times: 350 ns, 450 ns and 550 ns (max.)
- Single 5V power supply
- Static operation, no clocks required
- Inputs and tri-state outputs TTL compatible during both read and program mode
- Pin compatible with INTEL 2732A EPROM and Rockwell R2332B ROM.

ORDERING INFORMATION

Part Number: R87C32

Access Time:
35 = 350 ns
45 = 450 ns
55 = 550 ns



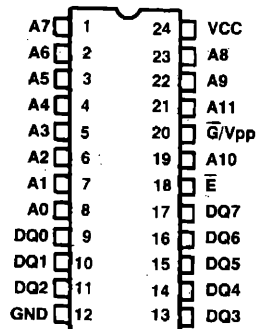
R87C32 Block Diagram

DESCRIPTION

The Rockwell R87C32 is a 4K × 8 (32,768 bits) ultraviolet (UV) light erasable programmable read-only-memory (EPROM). It is manufactured using CMOS technology for low power dissipation in both active and standby operating modes. Single 5V operation allows simple circuit design in runtime environments.

Initially, all bits are in the "1" state. Programming is performed by applying 21V to \bar{G}/V_{pp} and a 50 ms low level pulse to \bar{E} while the desired data is stable on DQ0-DQ7 lines and the address is stable on A0-A11 lines. All bits may be erased to the "1" state by exposure to a UV light source through the transparent window on the top of the device package.

The R87C32 EPROM is ideal for system development or low volume production applications requiring non-volatile memory in either multiple chip or single chip microcomputers with extended bus configurations. The low power requirements especially support applications using the R65C00 CMOS Microcomputer device family.



R87C32 Pin Configuration

A0-A11	ADDRESSES
\bar{E}	CHIP ENABLE
\bar{G}/V_{pp}	OUTPUT ENABLE/PROGRAM
DQ0-DQ7	DATA INPUT/OUTPUT

R87C32 Pin Names

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage All, except V_{pp} during Programming V_{pp} during Programming	V_{IN}	-0.3 to $V_{CC} + 0.3$ -0.3 to +22.0	Vdc
Output Voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	Vdc
Temperature under Bias	T_A	-10 to +80	°C
Storage Temperature	T_{STG}	-40 to 125	°C
Power Dissipation @ 25°C	P	1.0	W

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Read Mode	Program Mode
V_{CC} Supply Voltage	5V ± 5%	5V ± 5%
V_{PP} Supply Voltage		21V ± 0.5V
Temperature Range	0 to 70°C	0 to 70°C

DC OPERATING CHARACTERISTICS DURING READ

$V_{CC} = 5.0V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{OH}	Output High Voltage	2.4		—	V	$I_{OH} = -400 \mu A$
V_{OL}	Output Low Voltage	—		0.45	V	$I_{OL} = 2.1 \text{ mA}$
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.1		0.8	V	
I_{CC1}	V_{CC} Active Current TTL Level Address Inputs		2	10	mA	$\bar{E} = \bar{G} = V_{IL}$ $V_{IN} = V_{IH}$ or V_{IL} Frequency = 1 MHz, I/O = 0 mA
	CMOS Level Address Inputs		1	7	mA	$\bar{E} = \bar{G} = V_{IL}$ $V_{IN} = GND$ or V_{CC} Frequency = 1 MHz, I/O = 0 mA
I_{CC2}	V_{CC} Standby Current TTL Level Chip Enable		0.1	1	mA	$\bar{E} = V_{IH}$
	CMOS Level Chip Enable		10	100	μA	$\bar{E} = V_{CC}$
I_{PP}	V_{PP} Supply Current			30	mA	$\bar{E} = V_{IL}$, $\bar{G}/V_{PP} = V_{PP}$
I_{IN}	Input Leakage Current			±10	μA	$V_{IN} = 0V$ to V_{CC}
I_O	Output Leakage Current			±10	μA	$V_{OUT} = 0V$ to V_{CC}
C_I	Input Capacitance ¹			7	pF	$V_{CC} = 5.0V$, chip deselected, pin under test at 0V, $T_A = 25^\circ C$
C_O	Output Capacitance ¹			10	pF	$f = 1 \text{ MHz}$

Notes:

1. This parameter is periodically sampled and is not 100% tested.

DC OPERATING CHARACTERISTICS DURING PROGRAM

$V_{CC} = 5.0V \pm 5\%$, $T_A = -20^\circ C$ to $30^\circ C$, $V_{PP} = 21.0V \pm 0.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	-0.1		0.8	V	
I_{CC}	V_{CC} Active Current	—		25	mA	$\bar{E} = V_{IL}$, $\bar{G} = 21V$
I_{PP}	V_{PP} Active Current	—		30	mA	$\bar{E} = V_{IL}$, $\bar{G} = 21V$
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = 0V$ to V_{CC}

AC CHARACTERISTICS DURING READ

$V_{CC} = 5.0V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise specified)

Symbol	Parameter	R87C32-35		R87C32-45		R87C32-55		Unit	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVQV}	Address to Data Valid		350		450		550	ns	$\bar{E} = \bar{G} = V_{IL}$
t_{ELQV}	Chip Enable to Data Valid		350		450		550	ns	$\bar{G} = V_{IL}$
t_{GLQV}^2	Output Enable to Data Valid		120		120		120	ns	$\bar{E} = V_{IL}$
t_{GHQZ}^3	Output Enable to High Impedance	0	100	0	100	0	100	ns	$\bar{E} = V_{IL}$
t_{AXQX}	Address to Output Hold	0		0		0		ns	$\bar{E} = \bar{G} = V_{IL}$
t_{EHQZ}	Chip Enable to High Impedance	0	100	0	100	0	100	ns	$\bar{G} = V_{IL}$

Notes:

1. Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF

Input Rise and Fall Times: ≤ 20 ns

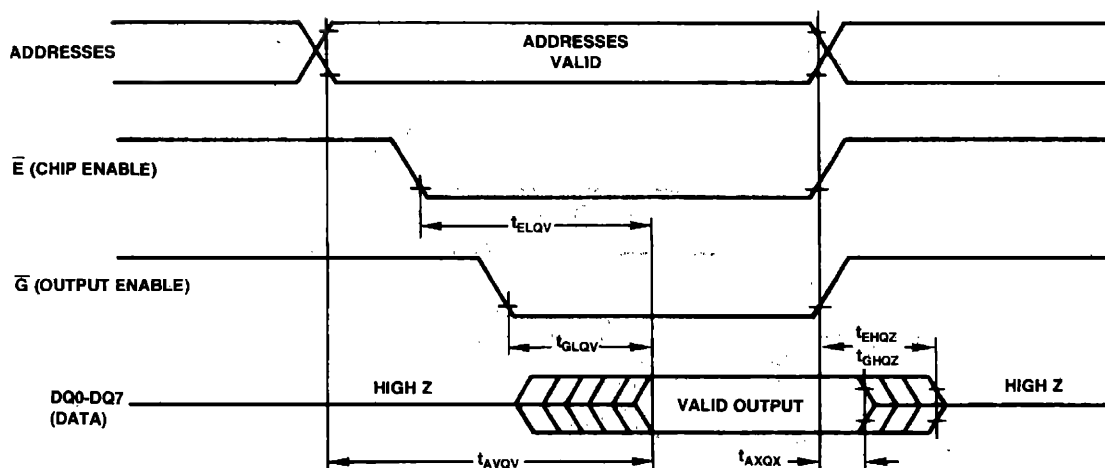
Input Pulse Levels: 0.45V to 2.4V

Timing Measurement Reference Level: Inputs 1V and 2V

Outputs 0.8V and 2V

2. \bar{G} may be delayed up to $t_{AVQV} - t_{GLQV}$ after the falling edge of \bar{E} without impact on t_{AVQV} . Data is available at the DQ outputs after a delay of t_{GLQV} from the falling edge of \bar{G} , provided that \bar{E} has been low (V_{IL}) and addresses have been valid for at least $t_{AVQV} - t_{GLQV}$.
3. t_{GHQZ} , t_{EHQZ} are specified from \bar{G} or \bar{E} , whichever occurs first.

READ TIMING DIAGRAM



AC CHARACTERISTICS DURING PROGRAM

$V_{CC} = 5.0V \pm 5\%$, $T_A = 20^\circ C$ to $30^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units
$t_{A\text{VEL}}$	Address set-up time	2			μs
$t_{G\text{HEL}}$	\bar{G} set-up time	2			μs
$t_{D\text{VEL}}$	Data set-up time	2			μs
$t_{E\text{HAX}}$	Address hold time	0			μs
$t_{E\text{HGL}}$	\bar{G} hold time	2			μs
$t_{E\text{HDX}}$	Data hold time	2			μs
$t_{E\text{HQZ}}$	Output disable to output Hi-Z delay	0		100	ns
$t_{E\text{LQV}}$	Data valid from \bar{E}			1	μs
$t_{E\text{LEH}}$	\bar{E} pulse width during programming	45	50	55	ms
t_{PR}	\bar{G} pulse rise time during programming	50			ns
$t_{G\text{LEL}}$	V_{PP} recovery time	2			μs

Notes:

Test Conditions:

Output Load: 1 TTL gate and $C_L = 100$ pF

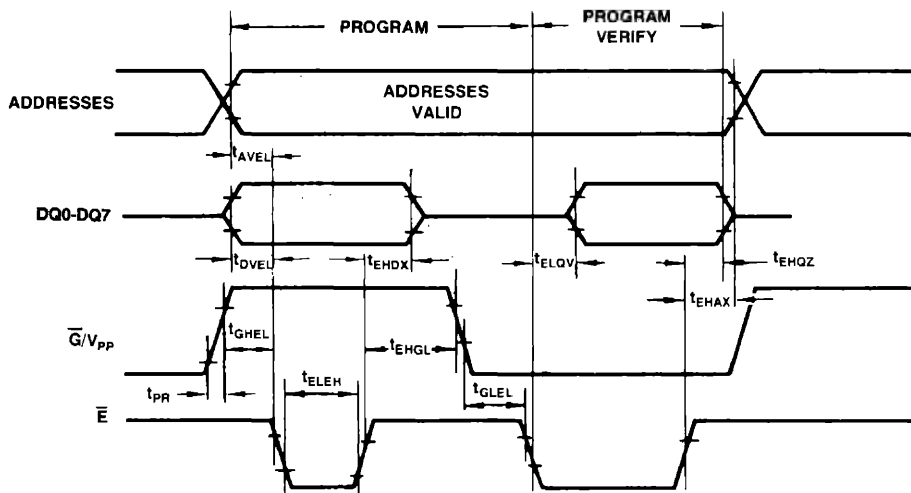
Input Rise and Fall Times: ≤ 20 ns

Input Pulse Levels: 0.45V to 2.4V

Timing Measurement Reference Level: Inputs 1V and 2V

Outputs 0.8V and 2V

PROGRAM TIMING DIAGRAM



OPERATING MODES

The Rockwell R87C32 has five modes of operation (see table 1) and is pin compatible with Intel's 2732A.

READ MODE

The read mode is governed by two control pins, \bar{E} and \bar{G} . In order to obtain data at the outputs, both \bar{E} and \bar{G} must be V_{IL} . \bar{E} is the power control and should be used for device selection. \bar{G} is the output control and should be used to gate data to the output pins. Valid data will appear on the output pins after T_{AVOQ} , T_{GLQV} or T_{ELQV} times, depending on which is limiting.

STANDBY MODE

The standby mode of the R87C32 reduces power dissipation. The R87C32 is placed in the standby mode by making $\bar{E} = V_{IH}$. This is independent of \bar{G} and automatically puts the outputs in their high impedance (High-Z) state.

PROGRAM MODE

The R87C32 is in the program mode when G/V_{PP} is at 21V. The data to be programmed is applied to the data output pins. When the address controls and data are stable, a 50 msec program pulse is applied to the \bar{E} input.

PROGRAM VERIFY MODE

A program verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with \bar{G}/V_{PP} and \bar{E} at V_{IL} . Data should be verified to t_{ELQV} after the falling edge of \bar{E} .

PROGRAM INHIBIT MODE

The program inhibit mode allows programming several R87C32 EPROMs simultaneously with different data for each by using \bar{E} to control which devices respond to the program pulse on \bar{E} .

Table 1. Mode Selection

Pin Mode	\bar{E} (18)	G/V_{PP} (20)	V_{CC} (24)	DQ0-DQ7 (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	No Effect	+5	High-Z
Program	Pulsed V_{IH} to V_{IL}	V_{PP}	+5	D_{IN}
Program verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program inhibit	V_{IH}	V_{PP}	+5	High-Z

Note: No Effect = No effect on selection/enable logic, however, no voltage other than logic levels shall be applied.

ERASURE PROCEDURE

Initially, and after each erasure by ultraviolet light, all bits of the R87C32 are in the "1" state. In Program Mode, "0"s are selectively programmed into the desired bit locations. The only way to change a "0" to a "1" is by ultra-violet light erasure.

The recommended erasure procedure for the R87C32 is exposure to ultra-violet light which has a wavelength of 2537 Angstroms.

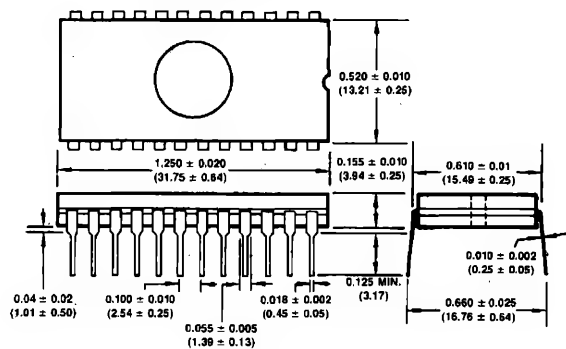
The integrated dose for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is 20 minutes using an ultraviolet lamp with a 12000 uW/cm² power rating.

Caution

The erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms. Sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Angstroms range.

PACKAGE DIMENSIONS

24-PIN CERDIP



DIMENSIONS IN INCHES AND (MILLIMETERS)



R87C64 64K (8K × 8) CMOS UV EPROM

PRELIMINARY

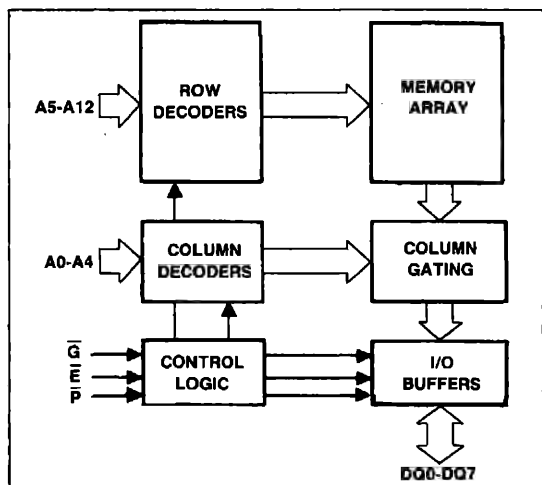
FEATURES

- 8,192 × 8 organization
- JEDEC approved pin-out
- Low Power
 - Active 80 mW (max.)
 - Standby 525 μ W (max.)
- Access times: 250 ns and 350 ns (max.)
- Single 5V power supply
- Static operation, no clocks required
- TTL compatible inputs and tri-state outputs during both read and program mode
- Pin compatible with INTEL 2764A EPROM and Rockwell R23C64 and R2364B ROMs.

ORDERING INFORMATION

Part Number: R87C64

Access Time:
25 = 250 ns
35 = 350 ns



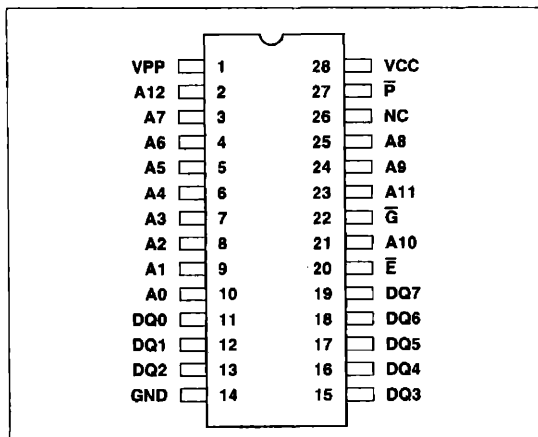
R87C64 Block Diagram

DESCRIPTION

The Rockwell R87C64 is an 8K × 8 (65,536 bits) ultraviolet (UV) light erasable programmable read-only-memory (EPROM). It is manufactured using CMOS technology for low power dissipation in both active and standby operating modes.

Initially, and also after erasure, all bits are in the "1" state. Data is programmed by applying 21V to V_{PP} a TTL low to \bar{E} , and a 50 ms low pulse on \bar{P} while the desired data is stable on DQ0-DQ7 lines and the address is stable on A0-A12 lines. All bits may be erased to the "1" state by exposure to a UV light source through the transparent window on the top of the device package.

The R87C64 EPROM is ideal for system development or production applications requiring non-volatile memory in either multiple chip or single chip microcomputers with extended bus configurations. The low power requirements especially support applications using the R65C00 CMOS Microcomputer device family.



R87C64 Pin Configuration

A0-A12	ADDRESSES
\bar{E}	CHIP ENABLE
\bar{G}	OUTPUT ENABLE
DQ0-DQ7	DATA INPUT/OUTPUT
\bar{P}	PROGRAM ENABLE

R87C64 Pin Names

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage All, except V_{PP} during Programming V_{PP} during Programming	V_{IN}	-0.3 to $V_{CC} + 0.3$ -0.3 to +22.0	Vdc
Output Voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	Vdc
Temperature under Bias	T_A	-10 to +80	°C
Storage Temperature	T_{STG}	-40 to 125	°C
Power Dissipation @ 25°C	P	1.0	W

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Read Mode	Program Mode
V_{CC} Supply Voltage	5V ± 5%	5V ± 5%
V_{PP} Supply Voltage		21V ± 0.5V
Temperature Range	0 to 70°C	0 to 70°C

DC OPERATING CHARACTERISTICS DURING READ

$V_{CC} = 5.0V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{OH}	Output High Voltage	2.4		—	V	$I_{OH} = -400 \mu A$
V_{OL}	Output Low Voltage	—		0.45	V	$I_{OL} = 2.1 mA$
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.1		0.8	V	
I_{CC1}	V_{CC} Standby Current			100	μA	$\bar{E} = V_{CC}$, $\bar{G} = V_{IL}$, $V_{IN} = 0V$ or V_{CC}
I_{CC2}	V_{CC} Active Current			15	mA	$\bar{E} = \bar{G} = V_{IL}$
I_{PP}	V_{PP} Current			100	μA	$V_{PP} = V_{CC} \text{ max.}$
I_{IN}	Input Leakage Current			± 10	μA	$V_{IN} = 0V$ to V_{CC}
I_O	Output Leakage Current			± 10	μA	$V_{OUT} = 0V$ to V_{CC}
C_I	Input Capacitance ²			7	pF	$V_{CC} = 5.0V$, chip deselected, pin under test at 0V, $T_A = 25^\circ C$ $f = 1 MHz$
C_O	Output Capacitance ²			10	pF	

Notes:

1. Applies only to chip enable with power down standby mode.
2. This parameter is periodically sampled and is not 100% tested.

DC OPERATING CHARACTERISTICS DURING PROGRAMMING

$V_{CC} = 5.0V \pm 5\%$, $T_A = 20^\circ C$ to $30^\circ C$, $V_{PP} = 21.0V \pm 0.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.1		0.8	V	
I_{CC}	V_{CC} Active Current			0.5	mA	$\bar{E} = \bar{P} = V_{IL}$, $\bar{G} = V_{IH}$
I_{PP}	V_{PP} Active Current			30	mA	
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = 0V$ to V_{CC}

AC CHARACTERISTICS DURING READ

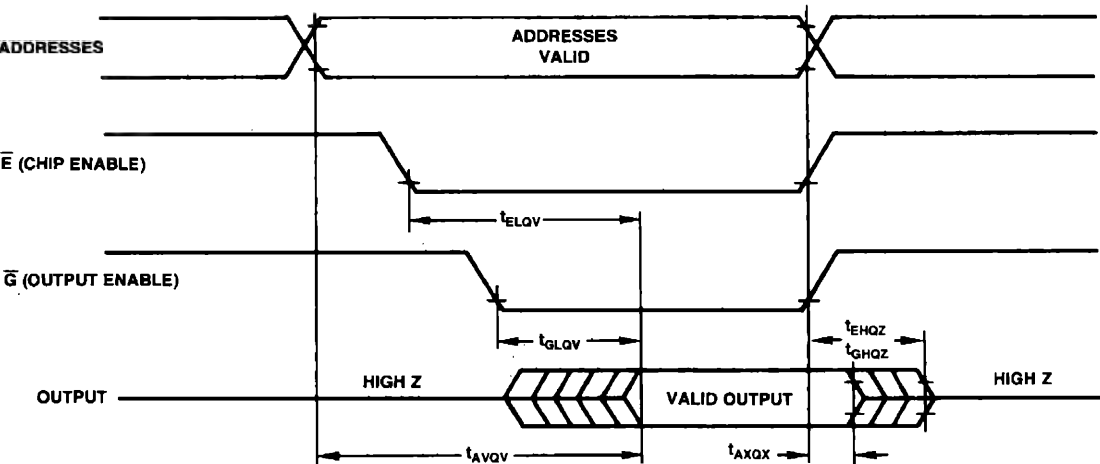
V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	R87C64-25			R87C64-35			Unit	Test Conditions ⁽²⁾
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{AVQV}	Address to Data Valid			250			350	ns	$\overline{E} = \overline{G} = V_{IL}$
t _{ELQV}	Chip Enable to Data Valid			250			350	ns	$\overline{G} = V_{IL}$
t _{GLQV} ¹	Output Enable to Data Valid	10		100	10		120	ns	$\overline{E} = V_{IL}$
t _{GHQZ} ²	Output Enable to High Impedance	0		90	0		100	ns	$\overline{E} = V_{IL}$
t _{AXQX}	Address to Output Hold	0			0			ns	$\overline{E} = \overline{G} = V_{IL}$
t _{EHQZ}	Chip Enable to High Impedance	0		90	0		100	ns	$\overline{G} = V_{IL}$

- Notes:
- \overline{G} may be delayed up to t_{AVQV}–t_{GLQV} after the falling edge of \overline{E} without impact on t_{AVQV}. Data is available at the DQ outputs after a delay of t_{GLQV} from the falling edge of \overline{G} , provided that \overline{E} has been low (V_{IL}) and addresses have been valid for at least t_{AVQV}–t_{GLQV}.
 - t_{GHQZ} and t_{EHQZ} are specified from \overline{G} or \overline{E} , whichever occurs first.
 - Test Conditions:
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level: Inputs 1V and 2V
Outputs 0.8V and 2V

4

READ TIMING DIAGRAM



AC CHARACTERISTICS DURING PROGRAM

$V_{CC} = 5.0V \pm 5\%$, $T_A = 20^\circ C$ to $30^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AVPL}	Address set-up time	2			μS
t_{DZGL}	\bar{G} set-up time	2			μS
t_{DVPL}	Data set-up time	2			μS
t_{ELPL}	\bar{E} set-up time	2			μS
t_{VHPL}	V_{PP} set-up time	2			μS
t_{PHDX}	Data hold time	2			μS
t_{GHAX}	Address hold time	0			μS
t_{GLQV}	Output enable to data valid			120	ns
t_{GHQZ}	Output disable to output high impedance	0		100	ns
t_{PLPH}	\bar{PE} pulse width during programming	45	50	55	ms

Notes:

Test Conditions:

Output Load: 1 TTL gate and $C_L = 100$ pF

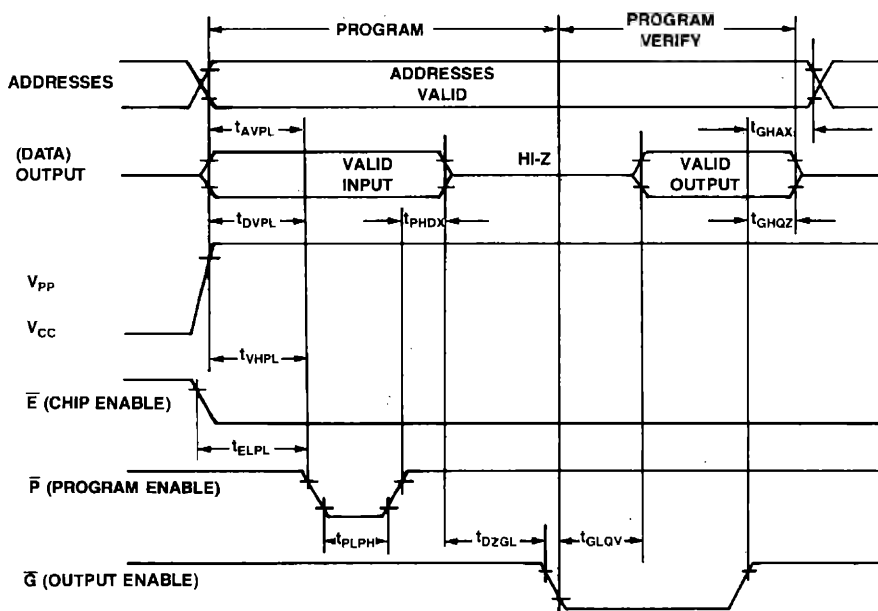
Input Rise and Fall Times: ≤ 20 ns

Input Pulse Levels: 0.45V to 2.4V

Timing Measurement Reference Level: Inputs 1V and 2V

Outputs 0.8V and 2V

PROGRAM TIMING DIAGRAM



OPERATING MODES

The Rockwell R87C64 has five modes of operation (see table 1).

Read Mode

The read mode is governed by two control pins, \bar{E} and \bar{G} . In order to obtain data at the outputs, both \bar{E} and \bar{G} must be V_{IL} . \bar{E} is the power control and should be used for device selection. \bar{G} is the output control and should be used to gate data to the output pins. Valid data will appear on the output pins after T_{AVQV} , T_{ELQV} or T_{GLQV} times, depending on which is limiting.

Standby Mode

The standby mode of the R87C64 reduces power dissipation. The R87C64 is placed in the standby mode by making $\bar{E} = V_{IH}$. This is independent of \bar{G} and automatically puts the outputs in their high impedance (High-Z) state.

Program Mode

The R87C64 is in the program mode when V_{PP} is at 21V with \bar{E} input at V_{IL} . The data to be programmed is applied to the data output pins. When the address controls and data are stable, a 50 msec program pulse is applied to the \bar{P} input.

Program Verify Mode

A program verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 21V. Data should be verified to t_{GLQV} after the falling edge of \bar{G} .

Program Inhibit Mode

The program inhibit mode allows programming several R87C64 EPROMs simultaneously with different data for each by using \bar{E} to control which devices respond to the program pulse on \bar{P} .

Table 1. Mode Selection

Pin Mode	\bar{E} (20)	\bar{G} (22)	\bar{P} (27)	V_{PP} (1)	V_{CC} (28)	DQ0-DQ7 (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	+5	+5	Q_{OUT}
Standby	V_{IH}	No Effect	No Effect	+5	+5	High-Z
Program	V_{IL}	No Effect	V_{IL}	+21	+5	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	+21	+5	Q_{OUT}
Program inhibit	V_{IH}	No Effect	No Effect	+21	+5	High-Z
Program inhibit	No Effect	No Effect	V_{IH}	+21	+5	High-Z
Note: No Effect = No effect on selection/enable logic, however, no voltage other than logic levels shall be applied.						

ERASURE PROCEDURE

Initially, and after each erasure by ultraviolet light, all bits of the R87C64 are in the "1" state. In Program Mode, "0"s are selectively programmed into the desired bit locations. The only way to change a "0" to a "1" is by ultra-violet light erasure.

The recommended erasure procedure for the R87C64 is exposure to ultra-violet light which has a wavelength of 2537 Angstroms.

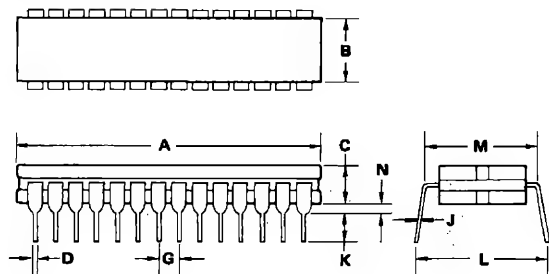
The integrated dose for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is 20 minutes using an ultraviolet lamp with a 12000 uW/cm² power rating.

Caution

The erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms. Sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Angstroms range.

PACKAGE DIMENSIONS

28-PIN CERDIP



NOTE: EITHER ROUND OR SQUARE UV WINDOW.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.32	37.34	1.430	1.470
B	12.95	13.46	0.510	0.530
C	3.68	4.19	0.145	0.165
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
J	0.20	0.30	0.008	0.012
K	3.18	4.19	0.125	0.165
L	16.13	17.41	0.635	0.685
M	15.24	15.75	0.600	0.620
N	0.89	1.14	0.035	0.045



R5213/2816 16K (2K × 8) ELECTRICALLY ERASABLE ROM

PRELIMINARY

FEATURES

- 2K × 8, 2048 × 8 organization
- Single 5V ± 10% supply
- TTL or high voltage byte erase/write
- 9 ms or 1 ms byte erase/write
- 10,000 erase/write cycles per byte
- Chip clear
- Access time: 350 ns (max.)
- Infinite number of read cycles
- JEDEC Approved pinout
- Pin and 2816A EEPROMs compatible with Seeq 5213, Intel 2816

ORDERING INFORMATION

Part Number:
R5213

Package:
CERDIP

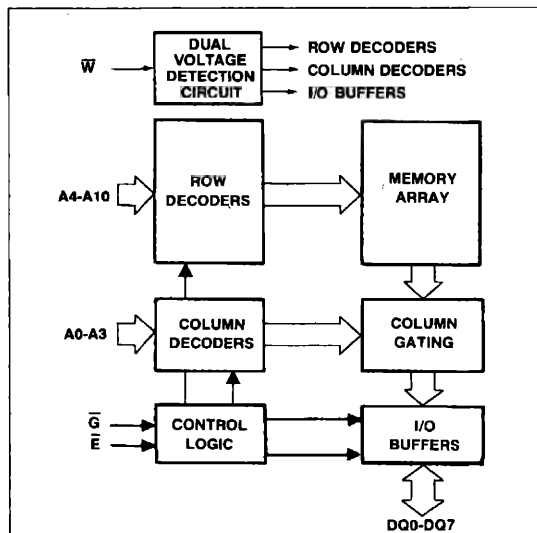
Access Time:
25 = 250 ns
35 = 350 ns

Model
No Letter = 9 ms Byte Write/Erase
H = 1 ms Byte Write/Erase

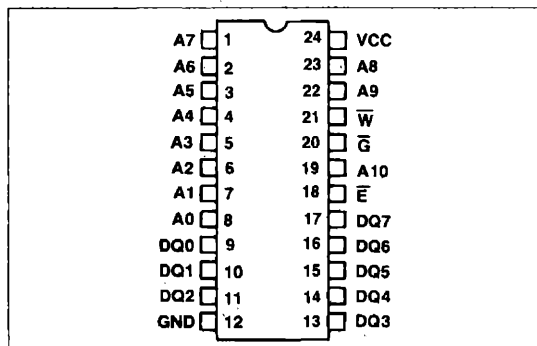
DESCRIPTION

The Rockwell R5213/2816 is a 2K × 8 (16,384 bits), 5V electrically erasable Read-Only Memory (EEROM). Data is electrically written either by a TTL pulse or a voltage between 15V and 22V on the Write Enable pin. Once written—this requires less than 10 milliseconds—there is no limit to the number of read cycles. A byte erase as well as a chip clear mode is available. Each byte may be erased and written 10,000 times. The erasure time, in either a byte erase or chip clear mode, is less than 10 milliseconds.

The R5213 is ideal for applications requiring a nonvolatile memory with in-system write and erase capability. These features make possible dynamic reconfiguration, i.e., operating software is altered in real time. Possible applications are instrument/machine self calibration, programmable character generators, table look-up updates over telephone lines, and controlling automotive fuel/air ratio. Designing the R5213 into 8- and 16-bit microprocessor systems is also simplified since the typical access time is less than 250 ns, allowing zero wait state operation.



R5213 Block Diagram



R5213 Pin Configuration

A0-A10	ADDRESSES
\bar{E}	CHIP ENABLE
\bar{G}	OUTPUT ENABLE
\bar{W} (VPP)	WRITE ENABLE
DQ0-DQ7	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.5 to +7.0	Vdc
Input Voltage	V _{IN}	-0.5 to +7.0	Vdc
Output Voltage	V _{OUT}	-0.5 to +7.0	Vdc
Temperature Under Bias	T _A	-10 to +80	°C
Storage Temperature	T _{STG}	-65 to +100	°C
\overline{W} Level During Writing/ Erasing	V _W	-0.5 to +22.0	Vdc
\overline{W} Max. Duration at 22V During W/E Inhibit	t _w	24	Hrs

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	All Modes
V _{CC} Supply Voltage	5V ± 10%
Temperature Range	0 to 70°C

DC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ. ⁽²⁾	Max.	Unit	Test Conditions ⁽¹⁾
I _{IN}	Input Leakage Current			10	μA	V _{IN} = V _{CC} Max.
I _O	Output Leakage Current			10	μA	V _{OUT} = V _{CC} Max.
I _W	Write Enable Leakage Read Mode		1.0	1.5	mA	\overline{W} = V _{IH}
	W/E Mode—TTL			-1.0	mA	\overline{W} = V _{IL}
	W/E Mode—High Voltage			1.5	mA	\overline{W} = 22V, E = V _{IL}
	W/E Inhibit Mode—High Voltage			1.5	mA	\overline{W} = 22V, E = V _{IH}
	Chip Clear Mode—TTL			-1.0	mA	\overline{W} = V _{IL}
	Chip Clear Mode—High Voltage			1.5	mA	\overline{W} = 22V
I _{CC1}	V _{CC} Standby Current		15	30	mA	\overline{E} = V _{IH}
I _{CC2}	V _{CC} Active Current		50	80	mA	\overline{E} = \overline{G} = V _{IL}
V _{IL} (DC)	Input Low Voltage (DC)	-0.1		0.8	V	
V _{IL} (AC)	Input Low Voltage (AC)	-0.4			V	Time = 10 ns
V _{IH}	Input High Voltage	2.0		V _{CC} + 1	V	
V _W	\overline{W} Read Voltage	2.0		V _{CC} + 1	V	
	\overline{W} Write/Erase Voltage -TTL Mode	-0.1		0.8	V	
	-High Voltage Mode	15	21	22	V	
V _{OL}	Output Low Voltage			0.45	V	I _{OL} = 2.1 mA
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -400 μA
V _G	\overline{G} Chip Clear Voltage	14		22	V	I _G = 10 μA
C _{IN}	Input Capacitance		5	10	pF	V _{CC} = 5.0V, chip deselected, pin under test at 0V, T _A = 25°C, f = 1 MHz
C _{OUT}	Output Capacitance ⁽³⁾			10	pF	
C _{VCC}	V _{CC} Capacitance ⁽³⁾			500	pF	\overline{G} = \overline{E} = V _{IH}
C _{VW}	V _W Capacitance ⁽³⁾			10	pF	\overline{G} = \overline{E} = V _{IH}

Notes:

- Test Conditions: Output Load: 1 TTL gate and C_L = 100 pF; Input Rise and Fall Times: ≤ 20 ns; Input Pulse Levels: 0.45V to 2.4V; Timing Measurement Reference Level: Inputs: 1V and 2V, Outputs: 0.8V and 2V
- Typical values are for T_A = 25°C and V_{CC} = 5.0V.
- This parameter is periodically sampled and is not 100% tested.

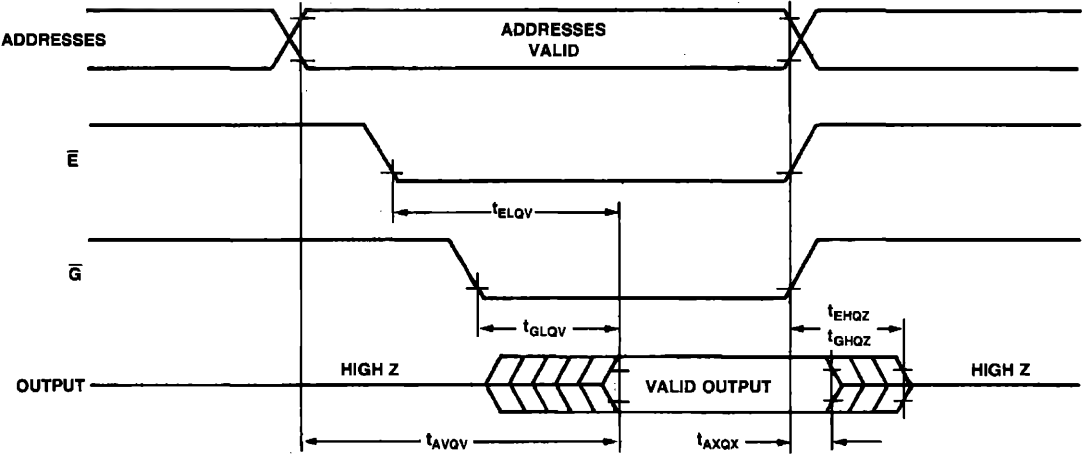
AC CHARACTERISTICS DURING READ

Symbol	Parameter	R5213-25 ⁽⁴⁾			R5213-35 ⁽⁴⁾			Test Conditions ⁽¹⁾
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t _{AVQV}	Address to Data Valid	10	200	250		300	350	$\bar{E} = \bar{G} = V_{IL}$
t _{ELQV}	Chip Enable to Data Valid	10	200	250		300	350	$\bar{G} = V_{IL}$
t _{GLQV}	Output Enable to Data Valid	10	50	90	10	50	100	$\bar{E} = V_{IL}$
t _{EHQZ} , t _{GHQZ} ⁽²⁾	Output Enable to High Impedance	0	50	70	0	50	80	$\bar{E} = V_{IL}$
t _{AXQX} ⁽³⁾	Output Hold from Address, Chip Enable, or Output Enable, whichever Transition Occurred First	0			0			$\bar{E} = \bar{G} = V_{IL}$

- Notes:
1. Test Conditions: Output Load: 1 TTL gate and C_L = 100 pF; Input Rise and Fall Times: ≤20 ns; Input Pulse Levels: 0.45V to 2.4V; Timing Measurement Reference Level: Inputs: 1V and 2V, Outputs: 0.8V and 2V
 2. \bar{G} may be delayed up to t_{AVQV}–t_{GLQV} after the falling edge of \bar{E} without impact on t_{AVQV}. Data is available at the DQ outputs after a delay of t_{GLQV} from the falling edge of \bar{G} , provided that \bar{E} has been low (V_{IL}) and addresses have been valid for at least t_{AVQV}–t_{GLQV}.
 3. t_{EHQZ}, t_{GHQZ} is specified from \bar{G} or \bar{E} whichever occurs first.
 4. All timing units in nanoseconds (ns).

4

READ TIMING DIAGRAM



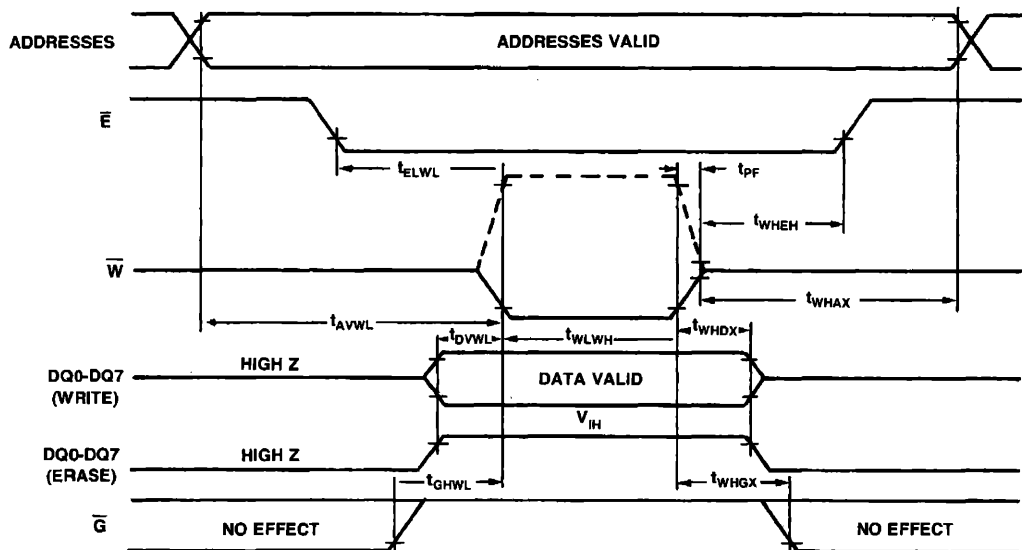
AC CHARACTERISTICS DURING WRITE/ERASE

Symbol	Parameter	Min. ⁽⁴⁾	Typ.	Max.	Units
$Q^{(1)}$	Maximum Endurance	10,000			cycles/byte
t_{AVWL}	Address to \bar{W} Set-Up Time	150			ns
t_{ELWL}	\bar{E} to \bar{W} Set-Up Time	150			ns
t_{DVWL}	Data to \bar{W} Set-Up Time	0			ns
t_{WHDx}	Write Enable Pulse Width	9	10	70	ms
	R5213	1		20	ms
$t_{WHEH}^{(2)}$	Write Recovery Time	50			ns
t_{GHWL}	\bar{G} Write/Erase Set-Up Time	0			ns
t_{WHGX}	\bar{G} Write/Erase Hold Time	0			ns
$t_{PF}^{(3)}$	V_W Fall Time	5			ns

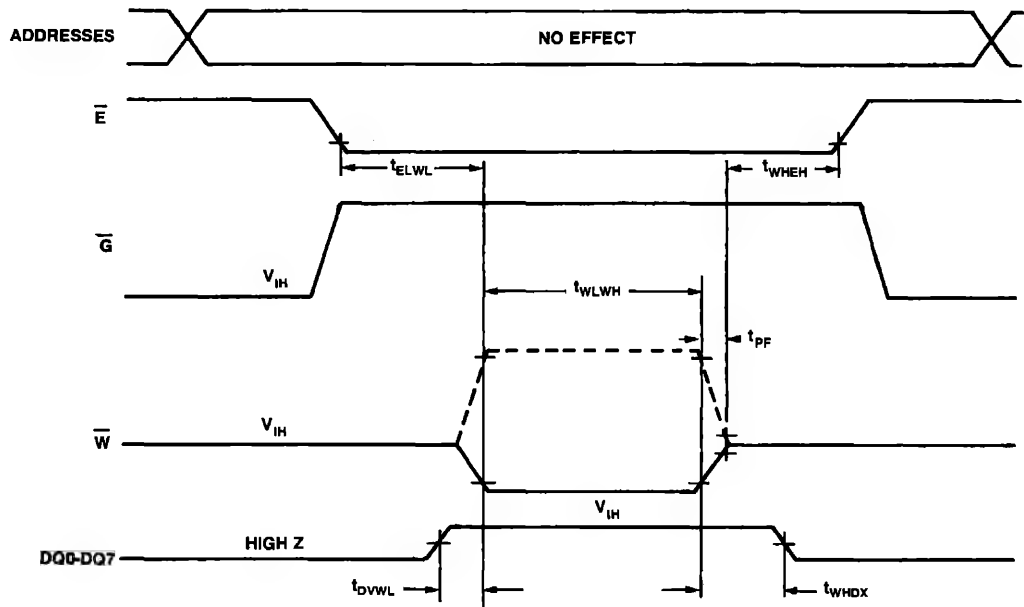
Notes:

- Maximum endurance, Q , is the number of write and erase cycles/byte.
- t_{WHEH} (min) = 50 ns when in the High Voltage W/E Mode only. When in the TTL W/E Mode, t_{WHEH} (min) = 700 ns.
- t_{PF} applies only when in the High Voltage W/E Mode.
- Test Conditions: Output Load: 1 TTL gate and $C_L = 100$ pF; Input Rise and Fall Times: ≤ 20 ns; Input Pulse Levels: 0.45V to 2.4V; Timing Measurement Reference Level: Inputs: 1V and 2V, Outputs: 0.8V and 2V

BYTE ERASE OR BYTE WRITE TIMING DIAGRAM



CHIP ERASE TIMING



4

DEVICE OPERATION

The Rockwell R5213/2816 has six modes of operation (see Table 1) and except for the chip clear mode it requires only TTL inputs to operate these modes.

To write a particular location of the R5213, that byte must first be erased. A memory location is erased by enabling the R5213 with Chip Enable at a TTL low, bringing Write Enable to a TTL low while Output Enable is a TTL high, and TTL highs (logical 1's) are being presented to all the I/O lines. The erase operation requires 9 ms. A write operation is the same as an erase except true data is presented to the I/O lines.

The R5213 is compatible to prior generation EEROMs which required a high voltage V_{PP} for writing and erasing. In the R5213 there is an internal dual level detection circuit which allows either a TTL low or 21V V_{PP} to be applied to \bar{W} to execute an erase or write operation. The R5213 specifies no restriction on the rising edge of V_{PP} .

For certain applications, the user may wish to erase the entire memory. A chip clear is performed in the same manner as a byte erase except that Output Enable is between 14V and 22V. All 2K bytes are erased in less than 10 ms.

A characteristic of all EEROMs is that the total number of write and erase cycles is not unlimited. The R5213 has been designed for applications requiring up to 10,000 write and erase cycles per byte. The write and erase cycling characteristic is completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to \bar{W} , enabling the chip, and enabling the outputs. Data is available t_{EVQV} time after Chip Enable is applied or t_{AVQV} time from the addresses. System power may be reduced by placing the R5213 into a standby mode. Raising Chip Enable to a TTL high will reduce the active power by over 60%.

COMPATIBILITY

The R5213/2816 is 100% compatible with the Seeq 5213 and the Intel 2816A and, except for the V_G (G Chip Erase Voltage), is also 100% backward compatible to the Intel 2816 which requires high voltage for byte erase/write.

Table 1. Mode Selection ($V_{CC} = 5V \pm 10\%$)

Table 1. Mode Selection

Mode \ Pin	\bar{E} (18)	\bar{G} (20)	\bar{W} (V_{PP}) (21)	DQ0-DQ7 (9-11, 13-17)
Read ⁽¹⁾	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby ⁽¹⁾	V_{IH}	No Effect	V_{IH}	High Z
Byte Erase ⁽²⁾	V_{IL}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write ⁽²⁾	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Chip Clear ⁽²⁾	V_{IL}	V_G	V_{IL}	$D_{IN} = V_{IH}$
Write/Erase Inhibit	V_{IH}	No Effect	No Effect	High Z

Note:

1. \bar{W} may be from V_{IH} to 6V in the read and standby mode.
2. \bar{W} may be at V_{IL} (TTL W/E Mode) or from 15V to 22V (High Voltage W/E Mode) in the byte erase, byte write, or chip clear mode.
3. No Effect = No effect on selection/enable logic, however, no voltage greater than logic levels shall be applied.

POWER UP/DOWN CONSIDERATIONS

Care must be taken to prevent an unintentional write (or erase) cycle during power-up or power-down. These cycles can be prevented by applying a signal level of V_{IH} to \overline{W} (pin 21) whenever V_{CC} is greater than 2.75 volts. When V_{CC} is 2.75 volts or less, the device cannot perform a write (or erase) cycle.

Figure 1 shows a suggested circuit which can be used for power-up or power-down conditions. The power supply used for the 470 ohm pull-up resistor should be the same supply used for

the R5213 V_{CC} . When this V_{CC} is outside the normal operating range (4.5 to 5.5 volts), the system power status signal (shown in Figure 1) should be low. Under these conditions, the open collector NAND gate and the 470 ohm resistor protect against an unintentional write (or erase).

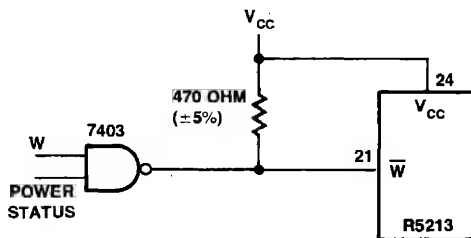
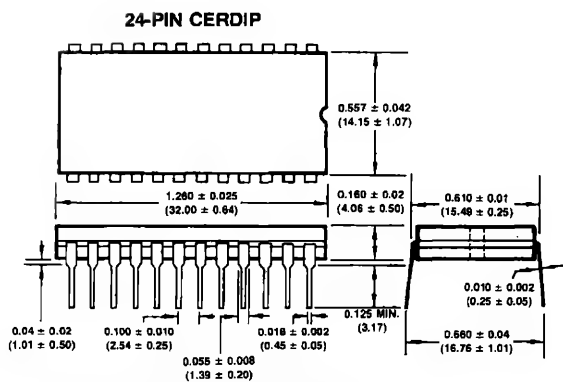


Figure 1. Typical Power Monitor Circuit

PACKAGE DIMENSIONS



DIMENSIONS IN INCHES AND (MILLIMETERS)



R52B33 64K (8K × 8) ELECTRICALLY ERASABLE ROM

FEATURES

- Input latches
- 8192 × 8 organization
- Single 5V ± 10% supply
- TTL byte erase/byte write
- 9 ms byte erase/byte write
- 10,000 erase/write cycles per byte
- Chip clear
- Fast access times: 200 ns, 250 ns, 300 ns and 350 ns (max.)
- Infinite number of read cycles
- JEDEC approved pinout
- Pin compatible With Seeq 52B33 EEPROM

ORDERING INFORMATION

Part Number:
R52B33

Package:
CERDIP

Access Time:
2 = 200 ns
25 = 250 ns
3 = 300 ns
35 = 350 ns

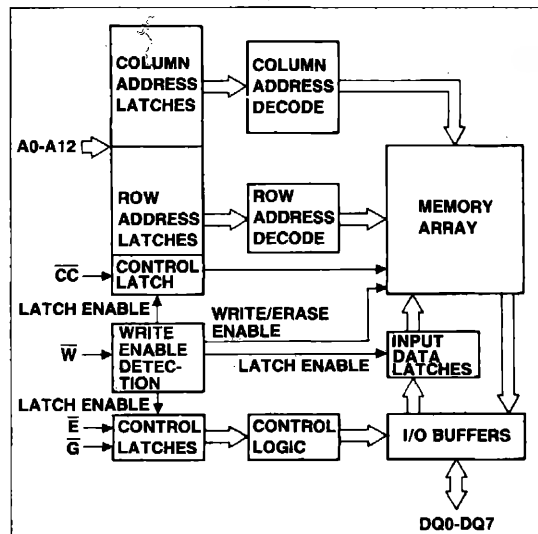
Model
No Letter = 9 ms Byte Write/Erase
H = 1 ms Byte Write/Erase

DESCRIPTION

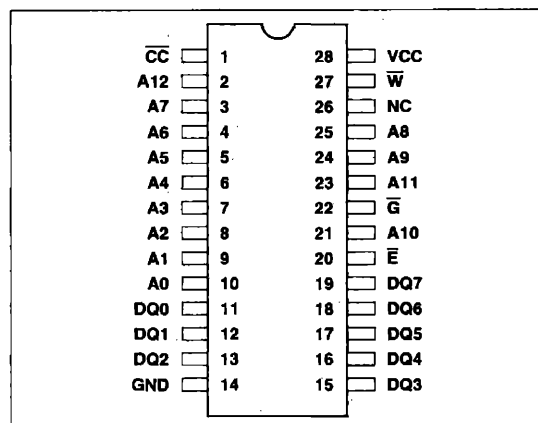
The Rockwell R52B33 is a 64K (8192 × 8 bits) 5 volt electrically erasable read-only-memory (EEROM). The device operates on 5 volt TTL levels in the read, write and erase modes. The R52B33 also has a chip clear mode in which the entire memory is erased in a single erase cycle. The device performs chip clear with a TTL high level signal applied to \bar{G} and a TTL low level applied to \bar{CC} . The erasure time for both chip clear and byte erase is under 10 ms.

Data, addresses, \bar{E} , \bar{CC} , and \bar{G} are latched on the leading edge of \bar{W} . The system controller needs only to maintain the \bar{W} signal during the erase/write cycle after the latches are activated. Once written, which requires under 10 ms, there is no limit to the number of times that the data may be read. Each byte may be erased and written at least 10,000 times.

The R52B33 is ideal for applications requiring a nonvolatile memory with in-system write and erase capability. These features make possible dynamic reconfiguration, i.e., operating software is altered in real time. Possible applications are instrument/machine self calibration, programmable character generators, table look-up updates over telephone lines, and controlling automotive fuel/air ratio.



R52B33 Block Diagram



R52B33 Pin Configuration

A0-A12	ADDRESSES
\bar{E}	CHIP ENABLE
\bar{G}	OUTPUT ENABLE
\bar{W}	WRITE ENABLE
DQ0-DQ7	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)
\bar{CC}	CHIP CLEAR
N/C	NO CONNECT

R52B33 Pin Names

OPERATING CONDITIONS

Parameter	All Modes
V _{CC} Supply Voltage	5V ± 10%
Temperature Range	0 to 70°C

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.5 to +7.0	Vdc
Input Voltage	V _{IN}	-0.5 to +7.0	Vdc
Output Voltage	V _{OUT}	-0.5 to +7.0	Vdc
Temperature Under Bias	T _A	-10 to +80	°C
Storage Temperature	T _{STG}	-65 to +100	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ. ⁽²⁾	Max.	Unit	Test Conditions ⁽¹⁾
I _{IN}	Input Leakage Current			± 10	μA	V _{IN} = V _{CC} Max.
I _O	Output Leakage Current			± 10	μA	V _{OUT} = V _{CC} Max.
I _{WE}	Write Enable Leakage Read Mode			10	μA	$\bar{W} = V_{IH}$
	W/E Mode			10	μA	$\bar{W} = V_{IL}$
	Chip Erase Mode			10	μA	$\bar{W} = V_{IL}$
I _{CC1}	V _{CC} Standby Current		18	40	mA	$\bar{E} = V_{IH}$
I _{CC2}	V _{CC} Active Current		60	110	mA	$\bar{E} = \bar{G} = V_{IL}$
V _{IL} (DC)	Input Low Voltage (DC)	-0.1		0.8	V	
V _{IL} (AC)	Input Low Voltage (AC)	-0.4			V	Time = 10 ns
V _{IH}	Input High Voltage	2.0		V _{CC} + 1	V	
V _W	\bar{W} Read Voltage	2.0		V _{CC} + 1	V	
	\bar{W} Write/Erase Voltage	-0.1		0.8	V	
V _{OL}	Output Low Voltage			0.45	V	I _{OL} = 2.1 mA
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -400 μA
C _{IN}	Input Capacitance		5	10	pF	V _{CC} = 5.0V, chip deselected, pin under test at 0V, T _A = 25°C, f = 1 MHz
C _{OUT}	Output Capacitance ⁽³⁾			10	pF	
C _{VCC}	V _{CC} Capacitance ⁽³⁾			500	pF	
C _{VW}	V _W Capacitance ⁽³⁾			10	pF	$\bar{G} = \bar{E} = V_{IH}$

Notes:

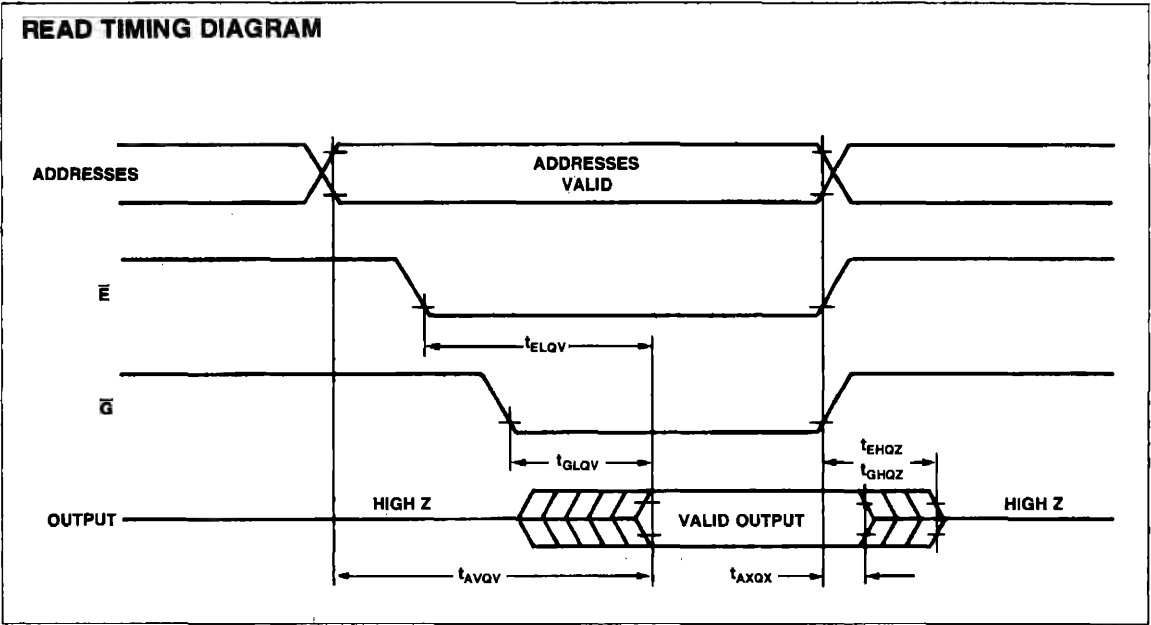
- Test Conditions: Output Load: 1 TTL gate and C_L = 100 pF; Input Rise and Fall Times: ≤ 20 ns; Input Pulse Levels: 0.45V to 2.4V; Timing Measurement Reference Level: Inputs: 1V and 2V, Outputs: 0.8V and 2V
- Typical values are for T_A = 25°C and nominal supply voltages
- This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS DURING READ

Symbol	Parameter	R52B33-20		R52B33-25		R52B33-30		R52B33-35		Unit	Test Conditions ⁽¹⁾
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t _{AVQV}	Address to Data Valid		200		250		300		350	ns	$\overline{E} = \overline{G} = V_{IL}$
t _{ELQV}	Chip Enable to Data Valid		200		250		300		350	ns	$\overline{G} = V_{IL}$
t _{GLQV} ⁽²⁾	Output Enable to Data Valid	10	80	10	90	10	100	10	100	ns	$\overline{E} = V_{IL}$
t _{EHQZ} , t _{GHQZ} ⁽³⁾	Output Enable to High Impedance	0	80	0	70	0	80	0	80	ns	$\overline{E} = V_{IL}$
t _{AXQX}	Output Hold from Address, Chip Enable, or Output Enable, whichever Transition Occurred First		0		0		0		0	ns	$\overline{E} = \overline{G} = V_{IL}$

- Notes:
1. Test Conditions: Output Load: 1 TTL gate and C_L = 100 pF; Input Rise and Fall times: ≤20 ns; Input Pulse Levels: 0.45V to 2.4V; Timing Measurement Reference Level: Inputs: 1V and 2V, Outputs: 0.8V and 2V
 2. \overline{G} may be delayed up to t_{AVQV}–t_{GLQV} after the falling edge of \overline{E} without impact on t_{AVQV}. Data is available at the DQ outputs after a delay of t_{GLQV} from the falling edge of \overline{G} , provided that \overline{E} has been low (V_{IL}) and addresses have been valid for at least t_{AVQV}–t_{GLQV}.
 3. t_{EHQZ}, t_{GHQZ} is specified from \overline{G} or \overline{E} whichever occurs first.

4



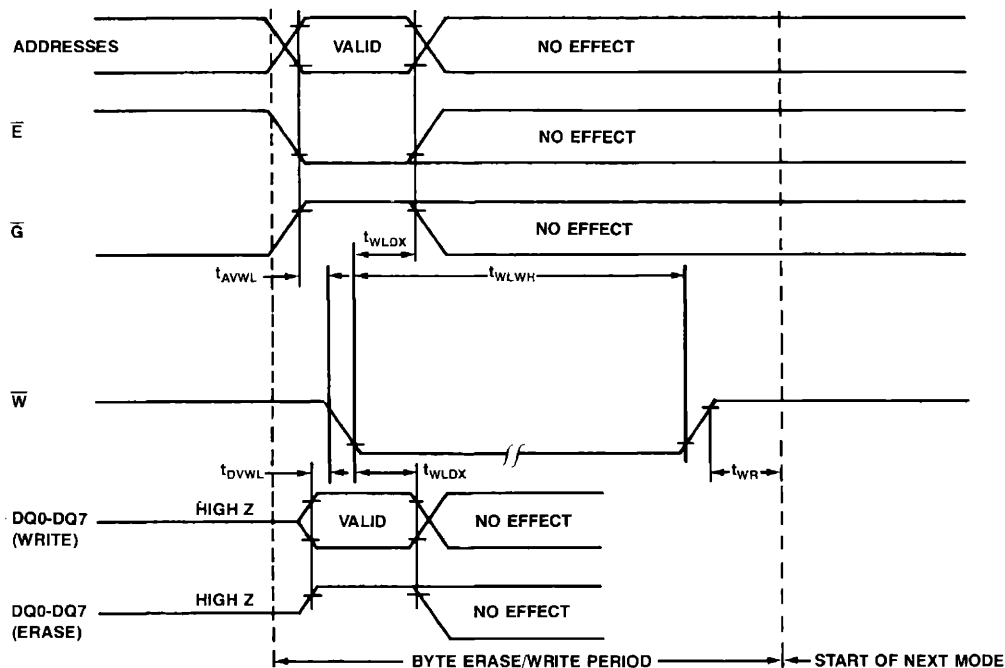
AC CHARACTERISTICS DURING WRITE/ERASE

Symbol	Parameter	R52B33-35			Unit
		Min.	Typ.	Max.	
Q ⁽¹⁾	Maximum Endurance	10,000			cycles/byte
t _{AVWL}	\overline{E} , \overline{G} or Address Setup to \overline{W}	50			ns
t _{DVWL}	Data Setup to \overline{W}	0			ns
t _{WLDX} ⁽²⁾	\overline{W} to \overline{E} , \overline{G} , Address or Data Change	50			ns
t _{WLWH}	Write Enable, \overline{W} , Pulse Width R52B33	9	10	70	ms
	R52B33H	1		20	ms
t _{WR} ⁽³⁾	\overline{W} to Mode Change (Write Recovery Time)	50			ns

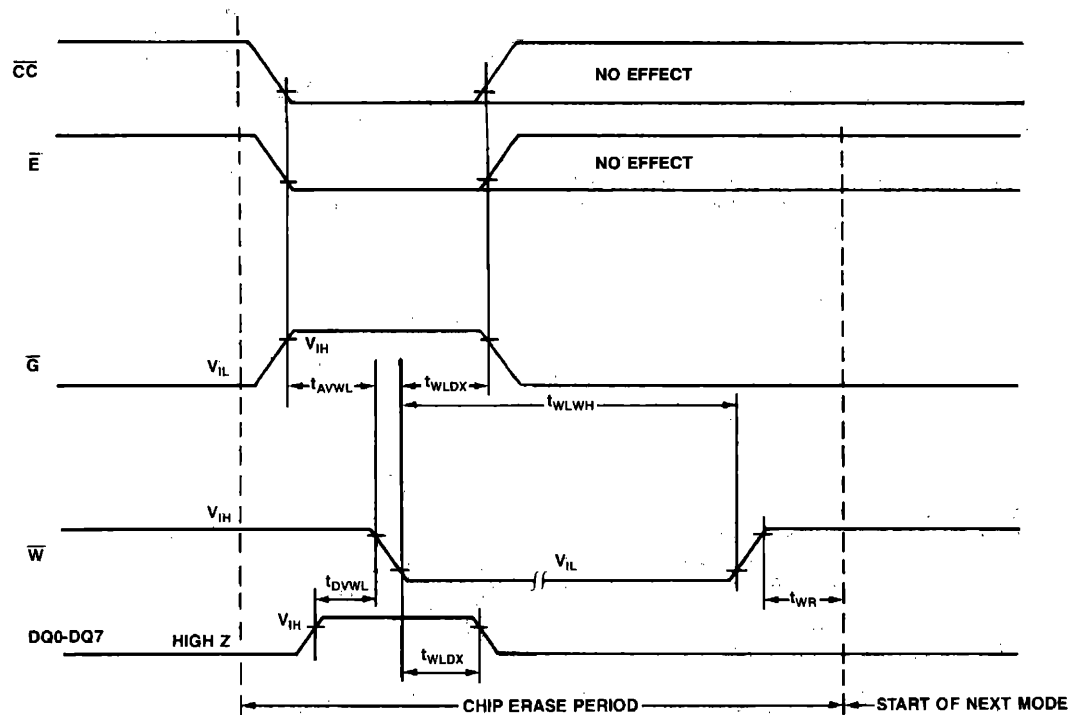
Notes:

1. Maximum endurance, Q, is the number of write and erase cycles/byte. The endurance of the R52B33 is guaranteed to be at least 10,000 cycles/byte.
2. After t_{WLDX} hold time, from \overline{W} , the inputs \overline{E} , \overline{G} , Address and Data are latched and are "No Effect" until t_{WR}, Write Recovery Time, after the trailing edge of \overline{W} .
3. The Write Recovery Time, t_{WR}, is the time after the trailing edge of \overline{W} that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 6) for mode control conditions.

BYTE ERASE OR BYTE WRITE TIMING



CHIP ERASE TIMING



DEVICE OPERATION

The Rockwell R52B33 has six modes of operation (see Table 1). The control signals that determine these modes are TTL compatible.

The chip clear and byte erase time is 10 ms.

READ

A read is accomplished by presenting the address of the desired byte to the Column and Row Address inputs with A0 as the LSB. Once the address is stable, \overline{E} is brought low in order to enable the chip (\overline{W} must be at a TTL high during the entire read cycle). The output drivers are made active by bringing \overline{G} to a TTL low. Data is valid t_{ELQV} after \overline{E} or t_{GLQV} after \overline{G} is low. The latches are transparent in the read mode.

STANDBY

The power dissipation of the chip may be reduced by taking \overline{E} to a TTL high between operations. This lowers P_D by over 60%.

BYTE ERASE/BYTE WRITE

Each byte of the memory may be individually erased or written with TTL level pulses. The two operations have the same timing and specifications since the byte erase is performed by writing all highs (HEX FF) to the selected byte. This restores the byte to its clear state of logical one. The byte erase is performed by presenting the device with \overline{E} at a logical low and \overline{G} at a logical high after the address is stable. These controls must be stable for t_{AVWL} before \overline{W} is taken active. The data must be stable for

t_{DWWL} . All of these control inputs together with the address and data lines are latched on the falling edge of \overline{W} . After t_{WLDX} they may be removed and the next condition established while the byte is being erased or written. This effectively increases the write speed. After t_{WLWH} , \overline{W} may be returned to the TTL high level and the next operation begun t_{WR} after the rising edge of the pulse.

CHIP CLEAR

The chip clear is performed by taking \overline{CC} and \overline{E} to a TTL low level and \overline{G} to a TTL high voltage level. The order in which the controls are set does not matter, only that they are stable for t_{AVWL} before \overline{W} goes low. The I/O and the address inputs are No Effect. After the control and data inputs are stable, take \overline{W} low. This latches all control and data inputs and, after t_{WLDX} all inputs with the exception of \overline{W} become No Effect. \overline{W} must be maintained at a low level for the duration of the chip clear cycle and then return it to a high level. Another mode of operation may be started t_{WR} after \overline{W} is stable. The memory has now been returned to its clear state and contains all 1's.

POWER UP/DOWN CONSIDERATIONS

Internal circuitry on all devices guard against inadvertent programming of bits during times when V_{CC} is below the normal operating voltage. The device outputs will remain in high impedance and the write/erase circuitry disabled as long as \overline{W} is kept at V_{IL} . Normal operation, as outlined in Table 1, can begin only after \overline{W} has been taken to V_{IH} .

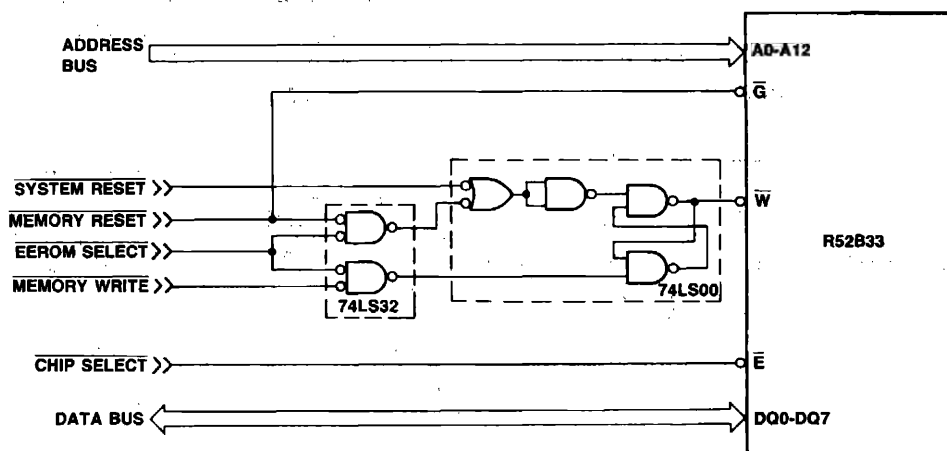
Table 1. Mode Selection ($V_{CC} = 5V \pm 10\%$)

Mode \ Pin	\overline{E} (20)	\overline{CC} (1)	\overline{G} (22)	\overline{W} (27)	DQ0-DQ7 (11-13, 15-19)
Read ⁽¹⁾	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}
Standby ⁽¹⁾	V_{IH}	No Effect	No Effect	No Effect	High Z
Byte Erase	V_{IL}	V_{IH}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write	V_{IL}	V_{IH}	V_{IH}	V_{IL}	D_{IN}
Chip Clear	V_{IL}	V_{IL}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Write/Erase Inhibit	V_{IH}	No Effect	No Effect	No Effect	High Z

Note:

1. \overline{W} may be from V_{IH} to 6V in the read and standby mode.
2. No Effect = No effect on selection/enable logic, however, no voltage greater than logic levels shall be applied.

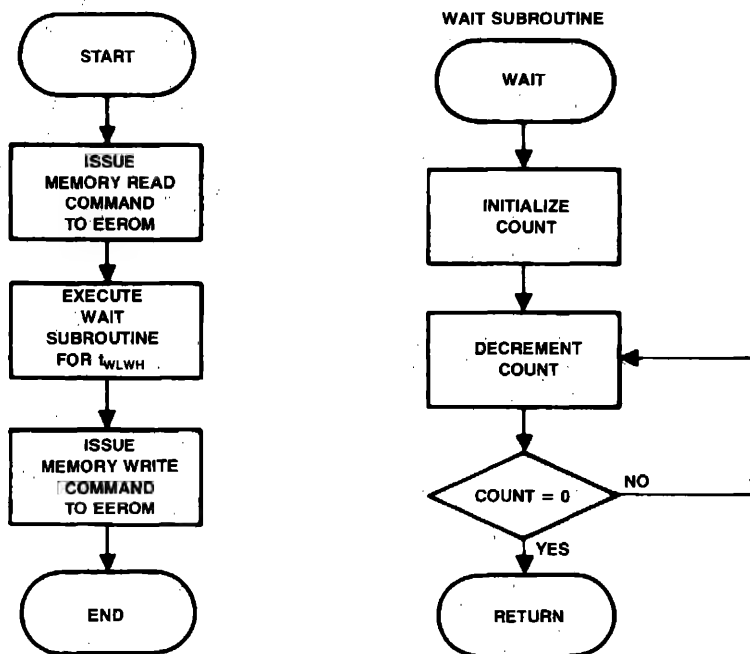
MICROPROCESSOR INTERFACE CIRCUIT EXAMPLE FOR BYTE WRITE/ERASE



NOTE:

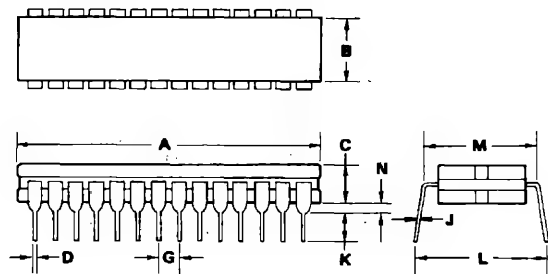
ALL SIGNALS MUST SATISFY THE RELATIONSHIPS INDICATED BY THE TIMING DIAGRAMS SHOWN ON PAGES 3, 4 AND 5. EEROM SELECT IS DERIVED FROM THE CHIP SELECT SIGNALS OF ALL DEVICES FOR WHICH THIS CIRCUIT GATES W. THIS MAY ENTAIL A SIMPLE OR FUNCTION. IN CASE OF A SINGLE EEROM, THE TWO SIGNALS WOULD BE COMMON.

TYPICAL EEROM WRITE/ERASE ROUTINE



PACKAGE DIMENSIONS

28-PIN CERDIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.32	37.34	1.430	1.470
B	12.95	13.46	0.510	0.530
C	3.68	4.19	0.145	0.165
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
J	0.20	0.30	0.008	0.012
K	3.18	4.19	0.125	0.165
L	16.13	17.41	0.635	0.685
M	15.24	15.75	0.600	0.620
N	0.89	1.14	0.035	0.045



R2816A and R5516A

16K (2K × 8) LATCHED EEPROM WITH TIMER

FEATURES

- High endurance erase/write cycles
 - 1,000,000 cycles per byte (R5516A)
 - 10,000 cycles per byte (R2816A and R2816AH)
- 5 volt-only operation
- On-chip latches for direct microprocessor bus interface
- On-chip timer for self-completed byte erase and write
- Fast byte write cycle
 - 2 ms write (R2816AH)
 - 10 ms write (R2816A and R5516A)
- Fast access time: 250 ns, 300 ns, 350 ns (max.)
- TTL voltage level controlled modes
 - Byte read
 - Byte write with automatic byte erase
 - Read/write inhibit
- Optional high voltage controlled modes
 - Byte erase
 - Byte write
 - 9 ms chip clear
- Power up/down protection circuitry
- Low power operation
 - 110 mA (max.) active current
 - 40 mA (max.) standby current
- JEDEC approved 24-pin byte-wide pinout
- Direct replacement for 2K × 8 EEPROMs
 - 21V 2816
 - 5V 2816A and 5516A

ORDERING INFORMATION

Part Number: R2816A ---
R5516A ---

Access Time

25 = 250 ns

3 = 300 ns

35 = 350 ns

Byte Write time

H = 2 ms (R2816AH only)

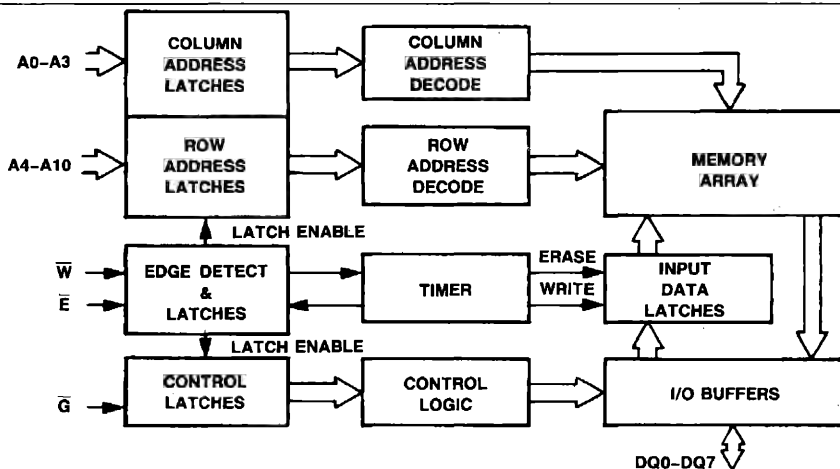
No letter = 10 ms

DESCRIPTION

The Rockwell R2816A and R5516A are 16K (2K × 8) electrically erasable programmable read-only memory (EEPROM) devices with on-chip latches and write timer. EEPROMs allow non-volatile storage of data when power is off and in-circuit reading and writing of data when power is on.

The R2816A and R5516A both operate with TTL level signals and a 5-volt power supply. The endurance, the number of times that a byte may be written to a particular location, is 1 million for the R5516A and 10 thousand for the R2816A. Once written, there is no limit to the number of times that the data may be read.

Both EEPROMs have an internal timer that automatically times out the write time. The on-chip timer, along with the latching of address and data lines, allows the EEPROM to complete write operation independently of the MPU. After executing a write



R2816A and R5516A Block Diagram

instruction to the EEPROM, the MPU is thus free to continue other computational tasks without delay or interruption required by earlier generation EEPROMs. The write operation is completed automatically, taking only 10 ms for the R2816A and R5516A, or only 2 ms for the faster R2816AH. A separate erase cycle is not required and the Write Enable (\bar{W}) pulse width requirement is only 150 ns (max.).

The R2816A EEPROM is the cost-effective choice for applications requiring infrequent updating of non-volatile data, i.e., no more than 10,000 updates/byte. The R5516A is ideal for designs employing frequent update of data.

A0 – A10	ADDRESS
\bar{E}	CHIP ENABLE
\bar{G}	OUTPUT ENABLE
\bar{W}	WRITE ENABLE
DQ0 – DQ7	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

R2816A and R5516A Pin Names

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_{IN}	-0.5 to +7.0	Vdc
Output Voltage	V_{OUT}	-0.5 to +7.0	Vdc
Temperature Under Bias	T_{STG}	-10 to +80	°C
Storage Temperature	T_{STG}	-65 to +100	°C
\bar{W} Level in Optional High Voltage Byte Erase/Write and Chip Clear Modes	V_W	-0.5 to +22.5	Vdc
\bar{W} or \bar{G} Max. Duration at 22V	t_W, t_G	24	Hrs
\bar{G} Level in Optional HV Chip Clear Mode	V_G	-0.5 to 22.5	Vdc

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise noted))

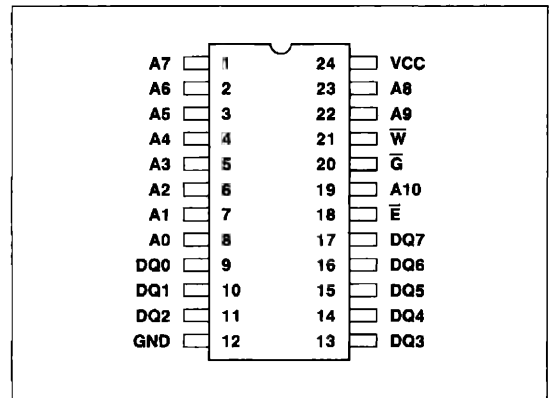
Symbol	Parameter	Min.	Typ. ²	Max.	Unit	Test Conditions ¹
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = 5.5V$
I_{OUT}	Output Leakage Current			10	μA	$V_{OUT} = 5.5V$
I_W	Write Enable Leakage Current			10	μA	$\bar{W} = V_W$
I_G	Output Enable Leakage Current			10	μA	$\bar{G} = V_G$
I_{CC1}	V_{CC} Standby Current		18	40	mA	$\bar{E} = V_{IH}, \bar{G} = V_{IL}$ All I/O lines open, other inputs = 5.5V
I_{CC2}	V_{CC} Active Current		60	110	mA	$\bar{E} = \bar{G} = V_{IL}$ All I/O lines open, other inputs = 5.5V
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC} + 1$	V	
V_W	\bar{W} Input High Voltage in Optional HV Byte Erase/Write and HV Chip Clear Modes	12		22	V	
V_G	\bar{G} Input High Voltage in Optional HV Chip Clear Mode	12		22	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1 \text{ mA}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400 \mu A$
C_{IN}	Input Capacitance ³			7	pF	$V_{CC} = 5.0 \text{ V}$, chip deselected, pin under test at 0V, $T_A = 25^\circ C$, $f = 1 \text{ MHz}$
C_{OUT}	Output Capacitance ³			10	pF	

Notes:

1. Test Conditions: Output Load: 1 TTL gate and $C_L = 100 \text{ pF}$; Input Rise and Fall Times: $\leq 20 \text{ ns}$; Input Pulse Levels: 0.45V to 2.4V; Timing Measurement Reference Level: Inputs: 1V and 2V, Outputs: 0.8V and 2V

2. Typical values are for $T_A = 25^\circ C$ and $V_{CC} = 5.0V$.

3. This parameter is periodically sampled and is not 100% tested.



R2816A and R5516A Pin Configuration

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	All Modes
V_{CC} Supply Voltage	5V $\pm 10\%$
Temperature Range	0 to $70^\circ C$

EEPROM OPERATION

The Rockwell R2816A and R5516A EEPROMs have four modes of TTL level controlled operation (Table 1) and three optional high voltage level controlled modes (Table 2). The standby, byte read, byte write, and write/read inhibit modes are controlled by TTL levels on the Chip Enable (\bar{E}), Output Enable (\bar{G}) and Write Enable (\bar{W}) inputs. These modes support operations in cost-sensitive designs where minimal supporting circuitry is required.

The optional high voltage controlled modes allow R2816A/R5516A operation in circuits designed for earlier generation EEPROMs. A high voltage (12–22V) on \bar{W} supports separate byte erase and byte write operations required by prior EEPROM designs. The chip clear mode requires high voltage inputs on two control pins (\bar{W} and \bar{G}).

TTL LEVEL CONTROLLED MODES

BYTE READ

The byte read mode drives the data line outputs (DQ0–DQ7) with the contents of the EEPROM byte located by input address lines A0–A10. Read access time is 250 ns or less (R2816A-25/R5516A-25).

A byte is read by stabilizing address lines A0–A10, applying a TTL low to \bar{E} to enable the device, and applying TTL low to \bar{G} to enable the data output drivers. Output data is valid on DQ0–DQ7 after t_{AVDV} , t_{ELDV} , or t_{QLDV} time, whichever is limiting. \bar{W} is held at TTL high throughout the cycle.

STANDBY

The standby mode reduces R2816A/R5516A power dissipation by over 60% (maximum ICC drops from 110 mA to 40 mA).

A TTL high on \bar{E} places the R2816A/R5516A in the standby mode regardless of the \bar{G} or \bar{W} input levels. The data output lines are in a high impedance state in this mode.

BYTE WRITE

The TTL controlled byte write cycle performs both a byte erase (all bits are written to the 1 state) and a byte write (all bits are written to the input data line states) in the same write cycle. A separate, preceding byte erase cycle is not required.

Table 1. TTL Modes Selection

Mode	Control Pins			I/O Data Lines (DQ0–DQ7)
	Chip Select (\bar{E})	Output Enable (\bar{G})	Write Enable (\bar{W})	
Byte Read	V _{IL}	V _{IL}	V _{IH}	D _{OUT}
Standby	V _{IH}	No Effect	No Effect	High Z
Byte Write	V _{IL}	V _{IH}	V _{IL}	D _{IN}
Write/Read Inhibit	V _{IL}	V _{IH}	V _{IH}	High Z
Note: No Effect = No effect on logic selection, however, no voltage level other than TTL levels shall be applied.				

Applying a TTL low to the \bar{W} input of the selected EEPROM (\bar{E} low) with the outputs disabled (\bar{G} high) initiates the byte write cycle. The address is latched on the falling edge of \bar{W} (or \bar{E} , whichever occurs later) and the data is latched on the rising edge of \bar{W} (or \bar{E} , whichever occurs first). The EEPROM uses the internal timer to automatically complete the byte erase and write operation without intervention from the MPU.

WRITE OR READ INHIBIT

Applying a TTL low to \bar{E} with both \bar{G} and \bar{W} held at TTL high enables the EEPROM but inhibits both reading from, and writing to, the device.

OPTIONAL HIGH VOLTAGE CONTROLLED MODES

HV BYTE ERASE OR BYTE WRITE

The high voltage byte erase or write mode operates the same as the TTL level controlled byte write mode with the following exceptions:

1. The active \bar{W} voltage level is 12–22V rather than TTL low.
2. A separate byte erase cycle must be performed with all data bits set to 1 (data lines are TTL high) prior to the byte write cycle.

HV CHIP CLEAR

The chip clear mode erases all data in the R2816A/R5516A to the 1 state (TTL high) in 10 ms.

When the device is enabled, raising \bar{W} and \bar{G} to a high voltage level (12–22V) initiates the chip clear mode. Dropping \bar{W} below the high voltage minimum level terminates the mode. The data lines must be held at TTL high.

POWER UP/DOWN WRITE PROTECTION

Internal circuitry protects the R2816A/R5516A against a false write during VCC power application or removal. This circuitry prevents writing under any of the following conditions:

1. VCC is less than 3V.
2. A negative transition on \bar{W} does not occur when VCC is between 3V and 5V.

Table 2. Optional High Voltage (HV) Modes Selection

Mode	Control Pins			I/O Data Lines (DQ0–DQ7)
	Chip Select (\bar{E})	Output Enable (\bar{G})	Write Enable (\bar{W})	
HV Byte Erase	V _{IL}	V _{IH}	V _W	V _{IH}
HV Byte Write	V _{IL}	V _{IH}	V _W	D _{IN}
HV Chip Clear	V _{IL}	V _G	V _W	V _{IH}

AC CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$ (unless otherwise specified)

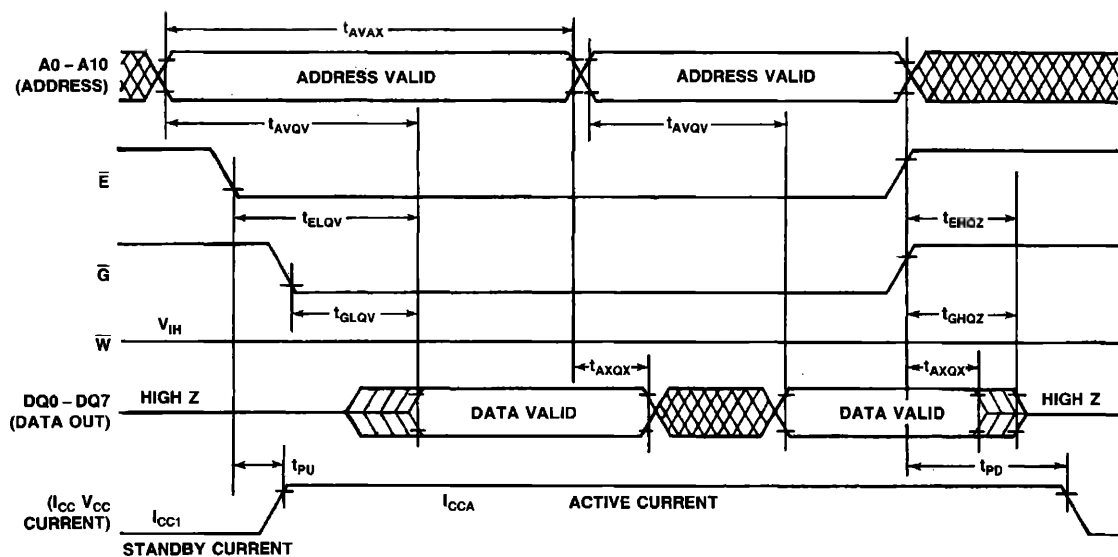
BYTE READ

Symbol	Parameter	Limits (ns)						Units
		R5516A-25 R2816A-25		R5516A-3 R2816A-3		R2816A-35		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{AVAX}	Read Cycle Time	250		300		350		ns
t _{ELQV}	Chip Enable (\bar{E}) Access Time (t _{CE})		250		300		350	ns
t _{AVQV}	Address Access Time (t _{ACC})		250		300		350	ns
t _{GLQV}	Output Enable (\bar{G}) Access Time (t _{OE})		90		100		100	ns
t _{EHQZ}	\bar{E} to Output in High Z	10	100	10	100	10	100	ns
t _{GHQZ}	\bar{G} to Output in High Z (t _{DF})	10	100	10	100	10	100	ns
t _{AXQX}	Output Hold from Address Change (t _{OH})	50		50		50		ns
t _{PU}	\bar{E} Low to Power-Up Time	0		0		0		ns
t _{PD}	\bar{E} High to Power Down Time		50		50		50	ns

Notes:

1. Test Conditions: Output Load: 1 TTL gate and $C_L = 100$ pF; Input Rise and Fall Times: ≤ 20 ns; Input Pulse Levels: 0.45V to 2.4V; Timing Measurement Reference Level: Inputs: 1V and 2V, Outputs: 0.8V and 2V.
2. \bar{G} low may be delayed up to t_{GLQV} after the falling edge of \bar{E} without impact on t_{AVQV} .
3. t_{EHQZ} and t_{GHQZ} are specified from \bar{G} or \bar{E} high whichever occurs first.

BYTE READ WAVEFORMS

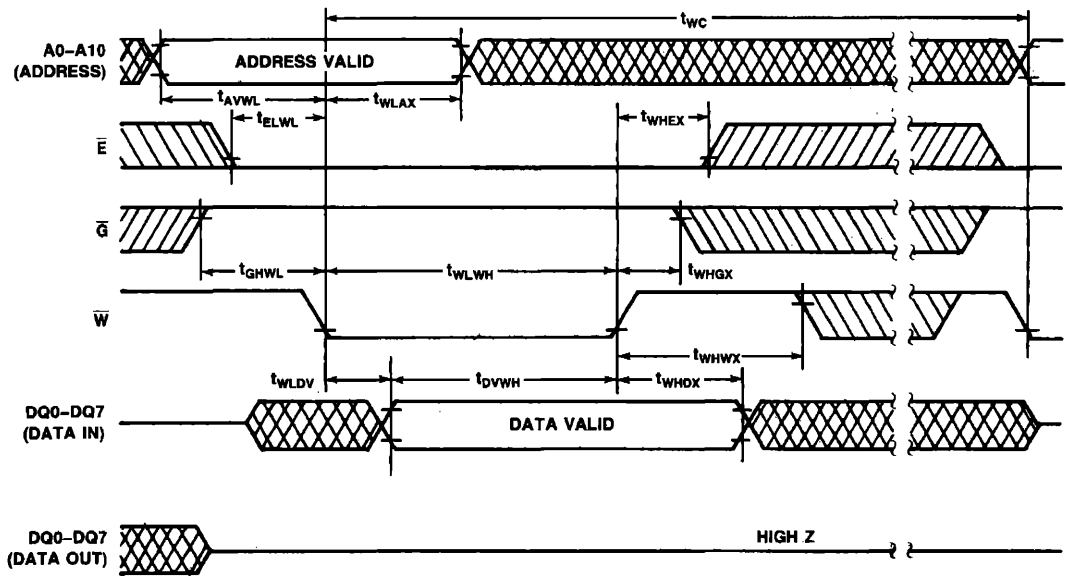


BYTE WRITE TIMING

Symbol	Parameter	R5516A-25 R2816A-25		R5516A-3 R2816A-3		R2816A-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Q	Maximum Endurance	R5516A	1,000,000		1,000,000	—		cycles/ bytes
		R2816A, R2816AH	10,000		10,000	10,000		
t _{WC}	Write Cycle Time	R2816AH	2		2	—		ms
		R5516A, R2816A	10		10	10		
t _{AVWL}	Address Setup Time		10		10		10	ns
t _{WLAX}	Address Hold Time		50		70		70	ns
t _{ELWL}	Write Setup Time		0		0		0	ns
t _{WHEX}	Write Hold Time		0		0		0	ns
t _{GHWL}	\overline{G} Setup Time		10		10		10	ns
t _{WHGX}	\overline{G} Hold Time		10		10		10	ns
t _{WLWH}	\overline{W} Write Pulse Width ¹		150		150		50	ns
t _{WHWX}	Data Latch Time		50		50		50	ns
t _{WLOV}	Data Valid Time ²			1		1		μs
t _{DVWH}	Data Setup Time		20		50		50	ns
t _{WHDX}	Data Hold Time		20		20		20	ns

Notes:
1. \overline{W} is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
2. Data must be valid within 1 μs maximum after the initiation of a write cycle.

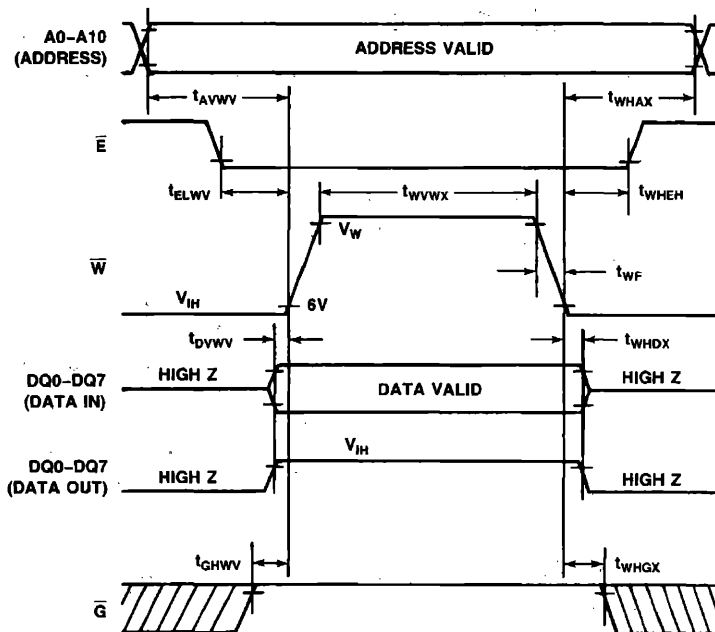
BYTE WRITE WAVEFORMS



HIGH VOLTAGE BYTE ERASE/WRITE TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{AVWV}	Address Valid to \bar{W} HV Setup Time (t_{AS})	150			ns	
t_{ELWV}	\bar{E} Low to \bar{W} HV Setup Time (t_{CS})	150			ns	
t_{GHWV}	G High to \bar{W} HV Setup Time	0			ns	$\bar{W} = 6V$
t_{DVWV}	Data Valid to \bar{W} HV Setup Time (t_{DS})	0			ns	
t_{WVWX}	\bar{W} HV Pulse Width	9	10	70	ms	
t_{WF}	\bar{W} Fall Time	5			μs	$\bar{W} = 6V$
t_{WHGX}	G Hold Time	0			ns	
t_{WHDX}	Data Hold Time (t_{DH})	50			ns	$\bar{W} = 6V$
t_{WHEH}	\bar{W} Recovery Time (t_{WR})	50			ns	$\bar{W} = 6V$
t_{WHAX}	Address Hold Time	50			ns	$\bar{W} = 6V$

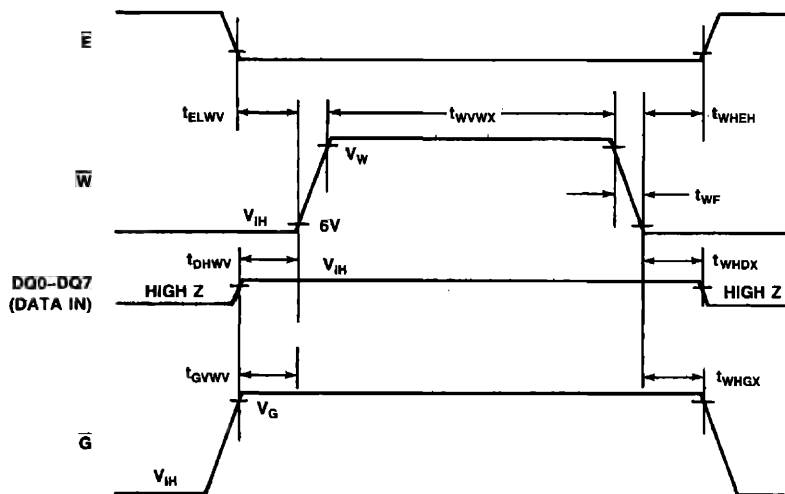
HIGH VOLTAGE BYTE ERASE/WRITE WAVEFORMS



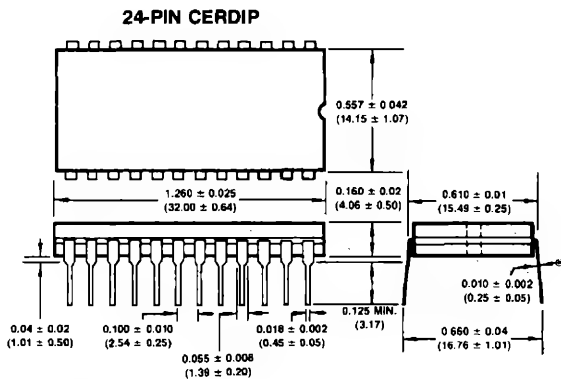
HIGH VOLTAGE CHIP CLEAR TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{ELWV}	\bar{E} Low to \bar{W} HV Setup Time (t_{CS})	10			ns	
t_{GVWV}	\bar{G} HV to \bar{W} HV Setup Time	10			ns	
t_{DHWV}	Data High to \bar{W} HV Setup Time (t_{DS})	0			ns	
t_{WVWX}	\bar{W} HV Pulse Width	9	10	70	ms	
t_{WF}	\bar{W} Fall Time	5			μ s	$\bar{W} = 6V$
t_{WHGX}	\bar{G} Hold Time	10			ns	$\bar{W} = 6V, \bar{G} = 12V$
t_{WHDX}	Data Hold Time (t_{DH})	50			ns	$\bar{W} = 6V$
t_{WHEH}	\bar{W} Recovery Time (t_{WR})	50			ns	$\bar{W} = 6V$

HIGH VOLTAGE CHIP CLEAR WAVEFORMS



PACKAGE DIMENSIONS



DIMENSIONS IN INCHES AND (MILLIMETERS)



R2000 64 × 8 NON-VOLATILE RAM

Product Preview

DESCRIPTION

The Rockwell R2000 Non-Volatile Random Access Memory (NVRAM) is a conventional 64 × 8 static random access memory (RAM) overlaid bit-for-bit with a 64 × 8 non-volatile electrically erasable programmable read only memory (EEPROM). The NVRAM combines the fast access read/write functions of static RAM with the permanent storage capability of EEPROM. STORE and RECALL commands, implemented as addresses to provide maximum user flexibility, initiate RAM to EEPROM and EEPROM to RAM data transfers. In response to the STORE command, the contents of the RAM are written into the EEPROM within 12 ms. In response to the RECALL command, the contents of the EEPROM are transferred to the RAM within 7.5 μs. These commands require no additional control lines or external circuitry to support bus operation during power loss, thus greatly simplifying R2000 system design-in.

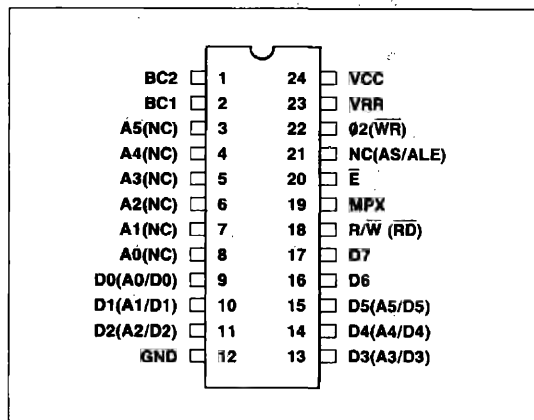
Three inputs can be variously strapped to cause the R2000's byte-wide parallel bus interface to operate in one of five different bus configurations. This enables the R2000 to operate with most industry standard microprocessors and single-chip microcomputers with extended buses.

R2000 applications include (1) saving of critical system data upon power failure, (2) permanent storage of instrument/machine self-recalibration or transmitted parameters, (3) password storage, (4) replacement of DIP switches used for system configuration, and (5) automotive applications ranging from entry-codes to engine performance adjustments.

FEATURES

- Byte-wide 64 × 8 organization
- Single 5V power supply
- Low power dissipation
 - 50 mA active current
 - 10 mA STORE current
 - 25 mA standby current
- 10-Year data retention for each STORE
- Minimum 10,000 non-volatile STORE cycle endurance
- Microprocessor and microcontroller bus compatible
- Five strappable, directly compatible, bus interface configurations:
 - R6500, R65C00, 6800 non-multiplexed bus
 - Z80 non-multiplexed bus
 - R65C00/21, 6801 multiplexed bus
 - R6500/11, R6500/41 multiplexed bus
 - 8051 multiplexed bus
- Software control of non-volatile functions
 - Storage protection
 - STORE and RECALL operation
 - No additional control lines
 - Only a single external capacitor required
- Fast static RAM access time:
 - 125 ns (max.) for non-multiplexed bus
 - 250 ns (max.) for multiplexed bus
- Reliable N-channel floating gate technology
- TTL compatible
- Self-timed STORE with power-down retention pin

4



R2000 Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +12.0	Vdc
Input Voltage	V_{IN}	-0.3 to +12.0	Vdc
Output Voltage	V_{OUT}	-0.3 to +7.0	Vdc
Temperature Under Bias	T_A	-10 to +80	°C
Storage Temperature	T_{STG}	-65 to +100	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	All Modes
V_{CC} Supply Voltage	5V \pm 5%
Temperature Range	0 to 70°C

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$, unless otherwise specified)

Symbol	Parameter	Min.	Typ. ²	Max.	Unit	Test Conditions ¹
I_{IN}	Input Leakage Current			10	μA	$V_{CC} = 5.25V$ $V_{IN} = GND$ to $5.25V$
I_{OUT}	Output Leakage Current			10	μA	$V_{OUT} = GND$ to V_{CC} Max.
I_{RR}	V_{RR} Store Current			10	mA	$V_{RR} = V_{CC} + 0V, -0.25V,$ $V_{CC} = 0V$
I_{CC1}	V_{CC} Standby Current			25	mA	$\bar{E} = V_{IH}, V_{CC} = 5.25V$
I_{CC2}	V_{CC} Active Current			50	mA	$\bar{E} = V_{IL}, V_{CC} = 5.25V$
V_{RR}	V_{RR} Supply Voltage	4.0		5.25	V	STORE Cycle, $V_{CC} = 0V$
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 3.2$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -0.3$ mA
C_{IN}	Input Capacitance			5	pF	$V_{CC} = 5.0V$, chip deselected, pin under test at $0V$,
C_{OUT}	Output Capacitance ³			150	pF	$T_A = 25^\circ C$, $f = 1$ MHz

Notes:

1. Test Conditions: Output Load: 1 TTL gate and $C_L = 100$ pF; Input Rise and Fall Times: ≤ 20 ns; Input Pulse Levels: 0.45V to 2.4V; Timing Measurement Reference Level: Inputs: 1V and 2V, Outputs: 0.8V and 2V.
2. Typical values are for $T_A = 25^\circ C$ and $V_{CC} = 5.0V$.
3. This parameter is periodically sampled and is not 100% tested.
4. All units are direct current (DC) except capacitance.

SIGNAL DESCRIPTION

A0-A5—Address Lines. The six address inputs select memory locations in RAM and initiate the STORE and RECALL commands. In a non-multiplexed bus configuration, these lines are assigned to the A0-A5 pins. In a multiplexed bus configuration, some, or all, of the address inputs are shared with the D0-D5 data lines.

D0-D7—Data Lines. When \bar{E} is LOW, the eight bidirectional, three-state, data lines transfer data from the R2000 RAM to the data bus during a read operation, or from the data bus to the R2000 during a write operation. When \bar{E} is HIGH, the data lines are in a high impedance state. In a multiplexed bus configuration, some of the data lines double as address lines.

\bar{E} —Chip Enable. \bar{E} LOW input enables RAM read and write operation, as well as STORE and RECALL initiation. When \bar{E} is HIGH, the R2000 is disabled and operates in a low-power standby mode. In the standby mode the R2000 consumes almost 50% less power than in the active mode. The data output lines are in a high impedance state during standby mode.

$\phi 2$ (WR)—Clock/(Write). This pin acts as either the Clock ($\phi 2$) or Write Enable (WR) input depending on bus interface configuration. When configured for an 6500/6800 bus, $\phi 2$ clocks data in or out of the R2000 depending on the level of R/W. When configured for an Z80/8051 bus, WR LOW (and RD HIGH) enables data to be written from the data lines into the R2000.

R/W (\bar{RD})—Read/Write (Read). This input pin serves as either Read/Write (R/W) or Read Enable (\bar{RD}) depending upon the bus interface configuration. When configured for an 6500/6800 bus, R/W HIGH enables data to be read from R2000 RAM to the data lines, whereas R/W LOW enables data to be written from the data lines into the R2000. When configured for an Z80/8051 bus, \bar{RD} LOW (and WR HIGH) enables data to be written from the R2000 RAM to the data bus.

NC(AS/ALE)—No Connect (Address Strobe/Address Latch Enable). This pin is used only with a multiplexed bus. A HIGH on this pin—AS for an R6500/* bus, or ALE for the 8051 bus—indicates that a valid address exists on the data/address lines.

MPX—Multiplex. The MPX, BC1 and BC2 inputs determine the bus interface configuration. MPX HIGH selects a multiplexed bus, whereas MPX LOW selects a non-multiplexed bus.

BC1, BC2—Bus Configuration 1 and 2. The BC1 and BC2 inputs, in conjunction with the MPX input, determine the bus interface configuration. Table 2 defines the specific bus selected by strapping each of these three inputs to either V_{CC} or GND.

V_{RR} —STORE Power Supply. This power down retention pin is normally connected to an external 470 μF capacitor. The capacitor retains enough power to write the data from RAM into EEPROM when STORE is commanded upon loss of V_{CC} .

V_{CC} —Power. +5 Vdc.

GND—Ground. Ground.

FUNCTIONAL DESCRIPTION

The major functions in the R2000 NVRAM are (1) the volatile static RAM with its associated address decode, sense and read circuitry, write control circuitry, and input receivers/output drivers; (2) the non-volatile EEPROM with its associated STORE and RECALL control circuit, and high voltage generator; and (3) the bus interface configuration logic. A block diagram of the R2000 NVRAM is shown in Figure 1.

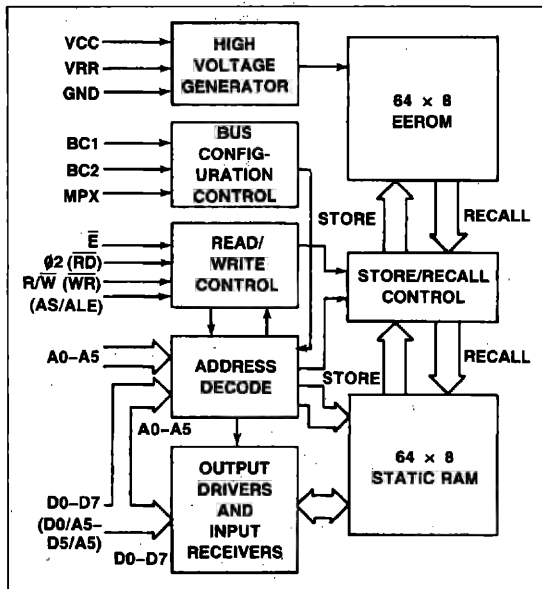


Figure 1. R2000 Block Diagram

RAM

The 64 bytes of volatile RAM are located at addresses 0 to 3F (hexadecimal) as decoded from address lines A0-A5. Locations 0 and 1 in RAM are not accessible since addresses 0 and 1 correspond to the STORE and RECALL commands, respectively. The remaining bytes are available for general read/write access. Table 1 summarizes the memory map and the command operations.

During normal operation, the RAM operates at bus speed without affecting the contents of the EEPROM. RAM accesses are controlled by \bar{E} , $\phi 2$ (WR), R/W(RD), and (AS/ALE) inputs depending on the strapped bus configuration.

EEPROM

The 64 bytes of non-volatile EEPROM shadow the static RAM cell-for-cell. Shadowing means that the RAM array is overlaid bit-for-bit with the EEPROM array. The EEPROM operates in parallel with the static RAM during a STORE or RECALL thus providing immediate storage and retrieval. The first two bytes are not used because the corresponding addresses are used for the STORE and RECALL commands.

STORE SECURITY KEY

The STORE and RECALL circuit controls the transfer of data between the RAM and the EEPROM. When a STORE command is received, i.e., address 0 is written with the value B5 (hexadecimal) on the data lines, data is copied from RAM to the EEPROM. The B5 value, called the STORE security key, is saved in an internal register during the STORE process. Once initiated, the STORE process completes under internal control and cannot be interrupted by an external signal. Access to the RAM from the data bus is inhibited during this time (indeterminate data will be output to the data bus if a read is attempted) and is re-enabled at the completion of the STORE. After STORE is complete—less than 12 ms after receipt of the STORE command—the B5 value is erased to prevent an inadvertent STORE from occurring due to an unintentional generation of address 0. Internal R2000 circuitry also prevents alteration of EEPROM contents during V_{CC} and V_{RR} decay following power loss, and during V_{CC} and V_{RR} rise after power application.

When a RECALL command is received, i.e., any data is written to address 1, data in the EEPROM is copied to the RAM. The RECALL time takes less than 7.5 μ s.

Table 1. R2000 NVRAM Memory Map

Address (Hex.)	Read/ Write	Data Value	Function
00	Write	B5	STORE RAM to EEPROM. The RAM byte at this location is not accessible. The B5 data value is required to initiate the STORE sequence.
	Read	—	No operation.
01	Write	Any	RECALL RAM from EEPROM. RAM data at this location is not accessible.
	Read	—	No operation
02–3F	Write	Any	Write data to RAM locations 02–3F.
	Read	Any	Read data from RAM locations 02–3F.

STORE AND RECALL EXECUTION

Read and write instructions can be executed in the application program to STORE and RECALL data either during normal operation or upon detection of power loss or turn-on. If performed as a part of normal operation, the STORE and RECALL instructions can be executed either periodically or upon demand. If performed as a part of power on/off processing, the STORE instruction should be executed as part of the power loss detect interrupt handling routine, and the RECALL instruction executed as part of the power turn-on processing.

V_{BB} CONNECTION

The V_{RR} pin is normally connected to an external $470\ \mu\text{F}$ (min.), 15V capacitor. The capacitor, charged through internal circuitry to a value of $V_{CC} - 0.25\text{V}$, contains enough energy to complete a STORE operation upon loss of V_{CC} . An internal current limiting switch prevents a large inrush current to the capacitor upon power turn-on. An internal power switch connected to V_{CC} opens during a STORE operation and when V_{CC} drops below V_{RR} to inhibit current drain from the capacitor into the V_{CC} power arid.

If the V_{CC} power grid has enough stored energy to support R2000 operation for at least 12 ms after the processor detects power loss and initiates a STORE, the V_{RR} pin can be connected to V_{CC} rather than the capacitor.

SYSTEM CONNECTION

Figure 2 shows a typical system connection using an R6502 CPU, 4K x 8 static RAM, system decode logic, on an R2000 NVRAM.

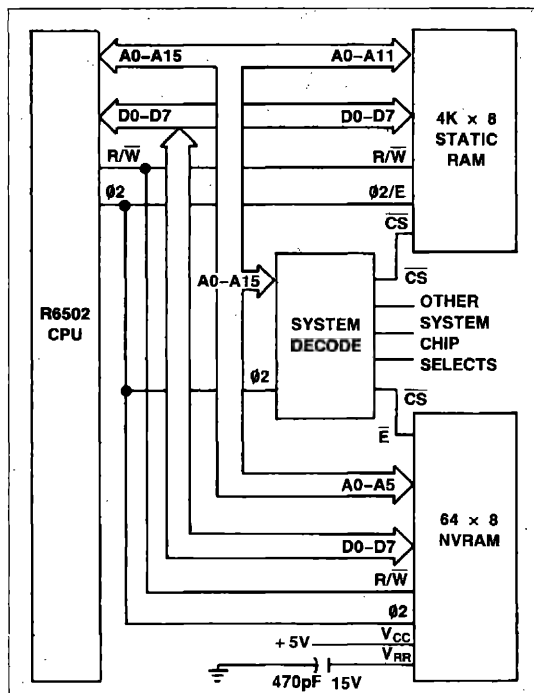


Figure 2. Typical System Interface

BUS CONFIGURATIONS

Strapping MPX, BC1, BC2 inputs high (V_{CC} or low (GND)) configures the R2000 bus interface to operate with one of five different busses as specified in Table 2. Figure 3 shows the five possible configurations.

Table 2. Bus Configuration Strapping

Pin Connections			Bus Interface
MPX	BC2	BC1	
LOW	LOW	LOW	R6500, R65C00, 6800 Non-multiplexed
LOW	LOW	HIGH	Z80 Non-multiplexed
HIGH	LOW	LOW	R65C00/21, 6801 Multiplexed
HIGH	HIGH	LOW	R6500/11, R6500/41 Multiplexed
HIGH	LOW	HIGH	8085/8051 Multiplexed

Note: Low = GND, High = V_{CC}

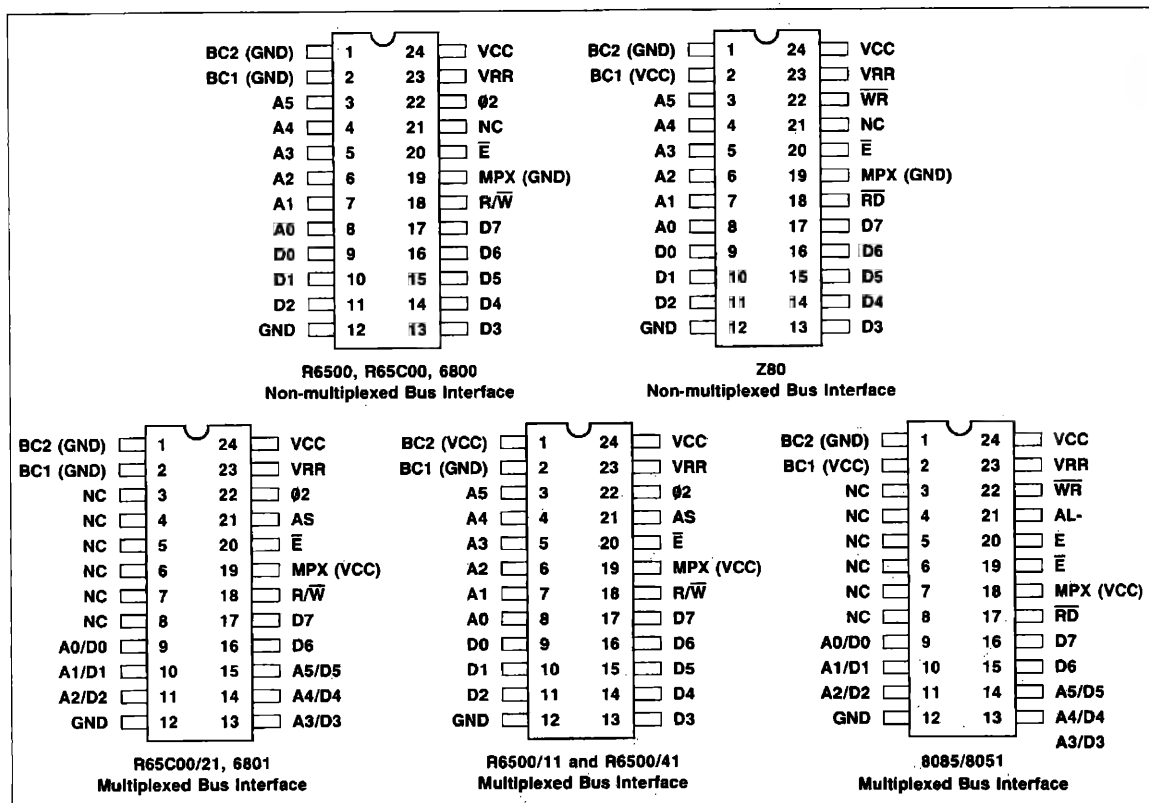
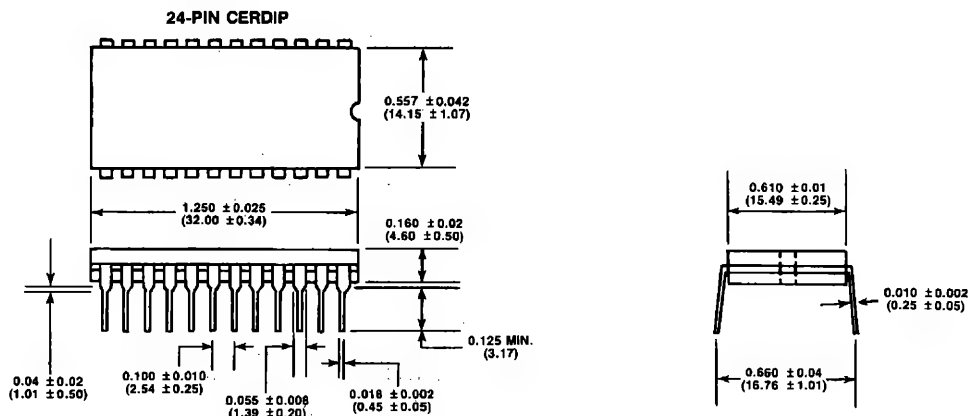


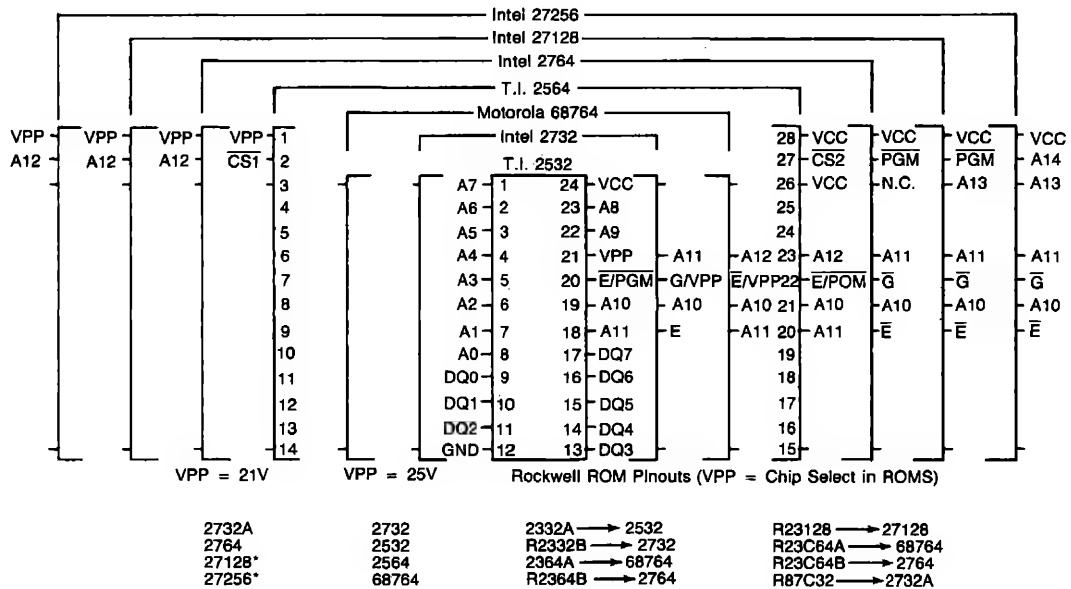
Figure 3. Five Possible Strapping Configurations

PACKAGE DIMENSIONS



DIMENSIONS IN INCHES AND (MILLIMETERS)

EPROM PINOUTS GUIDE



NOTE: Pins Without Their Function Designated Are the Same as the Corresponding Pin on the 2532
*12V for Intelligent Programming



SECTION 5

INTELLIGENT DISPLAY CONTROLLERS

	Page
Product Family Overview	5-2
10937 Alphanumeric Display Controller	5-3
10938 and 10939 Dot Matrix Display Controller	5-11
10939, 10942 and 10943 Dot Matrix Display Controller	5-20
10941 and 10939 Alphanumeric and Bargraph Display Controller	5-32
10951 Bargraph and Numeric Display Controller	5-41

INTELLIGENT DISPLAY CONTROLLERS

Cut Costs 30¢/digit, Replace Up To 11 TTL Devices, Interface With Any Host μ C

Rockwell display controllers drastically cut the cost and complexity of designing vacuum fluorescent (VF) displays into systems, can actually save up to 30 cents per digit. One 10937 can replace up to eleven TTL devices and can interface with any host microcomputer. VF Display manufacturers Futaba, NEC, and Noritake have all specified these controllers.

The 10937 is a single-chip alphanumeric display controller which directly drives 14 to 18 segment VF displays of up to 16 characters. It includes brightness and refresh controls and logic, its own RAM buffer, PLA segment decoder, and output driver.

The 10951 single-chip display controller is similar to the 10937 except the PLA segment decoder has been reprogrammed to drive a bar graph display and numerics.

If neither the 10937 nor the 10951 PLA segment codes satisfy the user's requirements, a custom code may be specified for the single-chip display controller.

The 10938 segment decoder/driver and the 10939 digit controller/driver operate as a set to drive dot matrix displays. A single set controls 5 x 7 dot matrix displays of up to 20 characters or cascaded to control up to

80 characters. Operating at 50V, the sets can drive VF displays and, with external drivers, LED, CCD, gas discharge and incandescent displays.

The 10941 can team with the 10939 to drive alphanumeric 14-18 segment VF displays of 20 to 40 characters and bar graphs. The 10942 and 10943 can team with the 10939 to drive 40 to 80 character 5 x 12 dot matrix displays.

The Rockwell display controllers are finding wide application in printers, photo copiers, typewriters, FAX machines and in various automotive and white goods uses. If the user has special requirements, a custom code may be specified for the segment decoder/driver device which can be packaged in a 40, 28, or 24 pin DIP according to the device type selected.

A new single-chip controller is under development which will be similar to the 10937/10951 devices except the user will have some control over the number of display outputs allocated as strobes or segments, the PLA will be doubled in size to allow 128 characters and the PLA may be bypassed to allow direct control of segments.

VACUUM FLUORESCENT CONTROLLER APPLICATIONS

Display Type	Single Chip	Multi-Chip Display Controller	
	Display Controller (See Part No.)	Anode Driver Type (See Part No.)	Grid Driver (10939)
<ul style="list-style-type: none"> • 8 Char. 14-18 Seg. • 10 Char. 14-18 Seg. • 16 Char. 14-18 Seg. • 20 Char. 14-18 Seg. • 32 Char. 14-18 Seg. • 40 Char. 14-18 Seg. 	1 (10937) 1 (10937) 1 (10937)	1 (10941)* 1 (10941)* 1 (10941)*	1 2 2
<ul style="list-style-type: none"> • 20 Char. 5 x 7 MTX • 32 Char. 5 x 7 MTX • 40 Char. 5 x 7 MTX • 40 Char. 5 x 12 MTX • 80 Char. 5 x 7 MTX • 80 Char. 5 x 12 MTX 		1 (10938) 1 (10938) 1 (10938) 1 EA (10942) (10943) 1 (10938) 1 EA (10942) (10943)	1 2 2 2 4 4
• Numeric + Bar Graph	1 (10951)		

*Also Controls Bar Graph Displays



10937 ALPHANUMERIC DISPLAY CONTROLLER

PRELIMINARY

DESCRIPTION

The 10937 Alphabetic Display Controller, one of the Rockwell Intelligent Display Controller products, is a MOS/LSI general purpose display controller designed to interface to segmented displays (gas discharge, vacuum fluorescent, or LED).

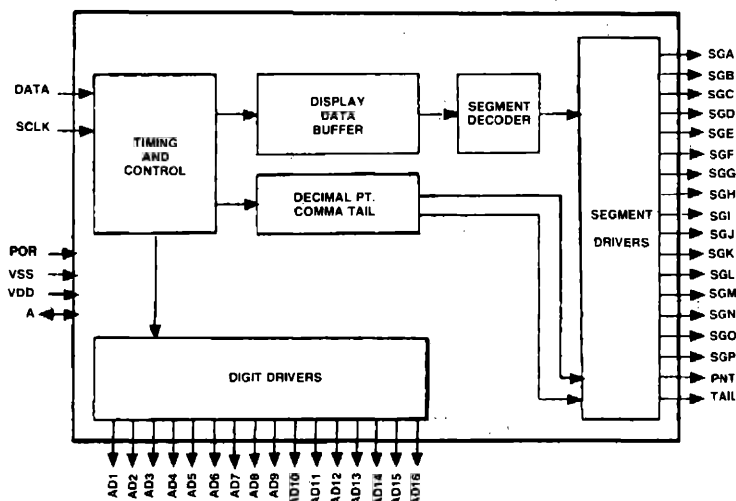
The 10937 will drive displays with up to 16 characters with 14 or 16 segments plus a decimal point and comma tail. Segment decoding within the device provides for the ASCII character set (upper case only). No external drive circuitry is required for displays that operate on 10 ma of drive current up to 40 volts. A 16 × 64-bit segment decoder provides internal ASCII character set decoding for the display.

FEATURES

- 16 character display driver with decimal point and comma tail
- 14 or 16 segment drivers
- Average data rate: 66 KHz
- Single character burst rate: 500 KHz
- TTL compatible
- Direct digit drive of 10 ma for 30, 35, and 40 volt displays
- Supports gas-discharge, vacuum fluorescent, or LED displays
- 64 × 16-bit PLA provides segment decoding for ASCII character set (all caps only)
- Serial data input for 8-bit display and control data words.
- 40-Pin DIP

ORDERING INFORMATION

Part Number	Package Type	Drive Voltage	Temperature Range
10937P-30	Plastic	30V	0°C to +70°C
10937P-35	Plastic	35V	0°C to +70°C
10937P-40	Plastic	40V	0°C to +70°C
10937PE-30	Plastic	30V	-40°C to +85°C
10937PE-35	Plastic	35V	-40°C to +85°C
10937PE-40	Plastic	40V	-40°C to +85°C



10937 Block Diagram

INTERFACE DESCRIPTION

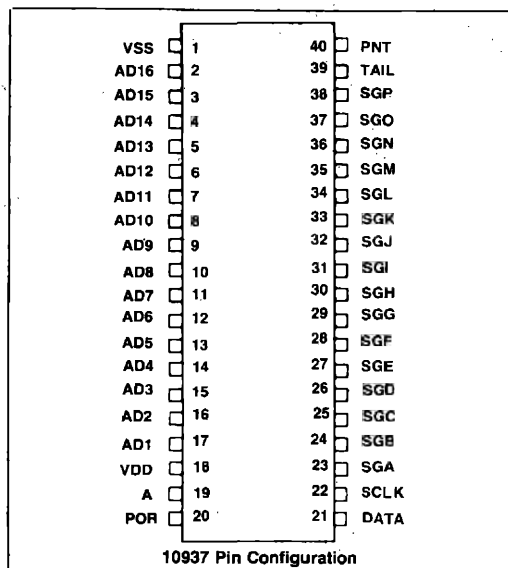
10937 Pin Functions

Signal Name	Pin No.	Function
VSS	1	Power and signal ground
AD16-AD1	2-17	Digits 16 through 1 driver outputs
VDD	18	DC power connection
A	19	A clock used only for device testing
POR	20	Power-on reset input
DATA	21	Serial data input
SCLK	22	Serial data clock input
SGA-SGP	23-38	Segments A through P driver outputs
TAIL	39	Comma tail driver output
PNT	40	Decimal point driver output

SPECIFICATIONS

Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	+0.3		-20	V
Power Dissipation	P_D		40	100	mW
Input Voltage	V_{IN}	+0.3		-20	V
Output Voltage	V_{OUT}	+0.3		-40	V
Operating Temperature					
Commercial	T_C	0		+70	°C
Industrial	T_I	-40		+85	°C
Storage Temperature	T_{STG}	-55		+125	°C
Input Capacitance	C_{IN}			5	pf
Output Capacitance	C_{OUT}			10	pf



10937 Pin Configuration

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated to this circuit.

All voltages are specified relative to V_{SS} .

D.C. Characteristics

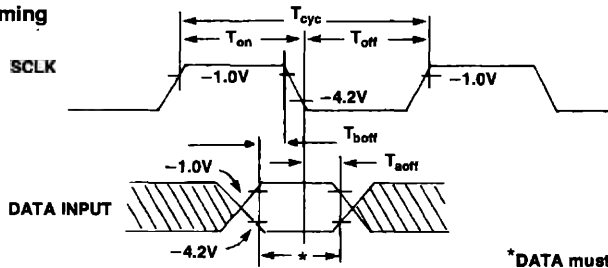
Parameter	Limits ($V_{SS} = 0$)			Limits ($V_{SS} = +5V$)			Conditions	Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.		
Supply Voltage (V_{DD})	-16.5	-15.0	-13.5	-11.5	-10.0	-8.5		V
Input DATA, SCLK, Logic "1"	-1.0		+0.3	+4.0		+5.3		V
Logic "0"	V_{DD}		-4.2	V_{DD}		+0.8		V
Input POR								
Logic "1"	-3.0		+0.3	+2.0		+5.3		
Logic "0"	V_{DD}		-10.0	V_{DD}		+5.0		
Output Digit and Segment Strokes Driver On								
Commercial			-1.5			+3.5	At 10mA	V
Industrial			-1.7			+3.3		V
Driver Off 10937-30			-30			-25		V
Driver Off 10937-35			-35			-30	Actual value determined by external circuit	V
Driver Off 10937-40			-40			-35		V
Output Leakage			10			10	Per driver at driver off	μA
Input Leakage			10			10		μA

NOTES: All outputs require Pulldown Resistors.

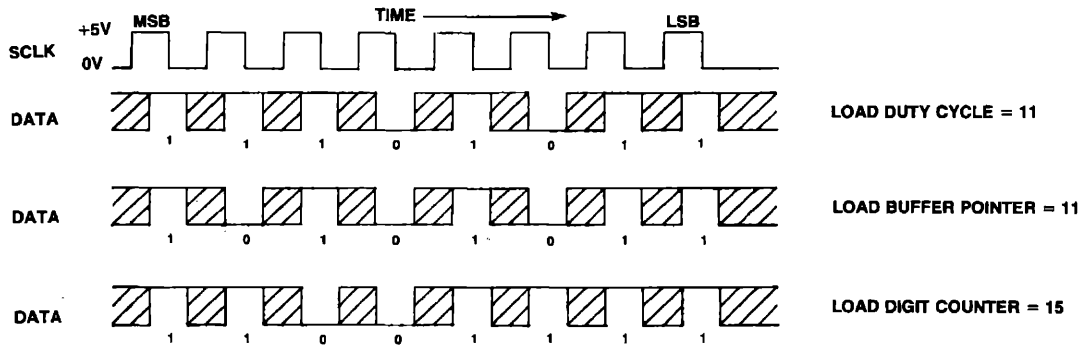
A.C. Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Clock (1 Bit Time)	T_{cyc}				
Commercial		6.67	10.0	20.0	μs
Industrial		5.88	10.0	22.2	μs
Segment or Digit Strobe Output	T_{out}	200			ns
SCLK Clock					
On Time	T_{on}	1.0		20.0	μs
Off Time	T_{off}	1.0			μs
Data Input Sample Time					
Before SCLK Clock Off	T_{boff}	200			ns
After SCLK Clock Off	T_{aoff}	100			ns

SCLK and Serial Data Timing

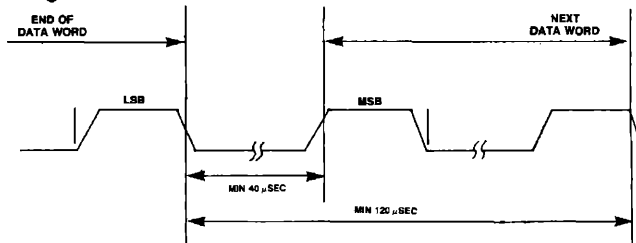


SCLK and Serial Data (Control Word) Examples

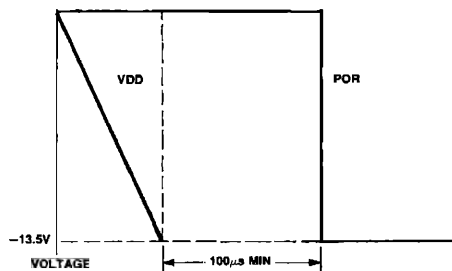


NOTE: Crosshatch = don't care

Data Word LSB/MSB Timing



Power-On Reset Voltage Limits



FUNCTIONAL DESCRIPTION

The 10937 is a general purpose display controller for multiplexed, segmented displays with up to 16 character positions and 14 or 16 segments, plus decimal point and comma tail. No external drive circuitry is needed for displays requiring up to 10 ma of drive current up to 40 volts. All timing signals required to control the display are generated in the 10937 device without any refresh input from the host processor.

Input data is loaded into the Display Data Buffer via the Serial Data Input (Data) channel. Internal timing and control blocks synchronize the segment and digit output signals to provide the proper timing for the multiplexing operation. A 16×64 -bit PLA is provided for segment decoding for the full ASCII character set (upper case only).

Input data is loaded into the 10937 ADC as a series of 8-bit words with the most significant bit (MSB), bit 7, first. If bit 7 of any word loaded is a logical 1 (this bit is referred to as the control bit C), the loaded word is a control data word. If the C bit of any word is a logical 0, the loaded word is a display data word. The following paragraphs describe the format and functions of these control and display data words.

INPUT CONTROL DATA WORDS

When the C-Bit (bit 7) of the 8-bit input word is a logical 1, bits 5 and 6 are decoded into one of four control commands while data associated with the command are extracted from bits 0-4 (see Table 1). There are three control codes which perform the following display functions:

- Load the Display Data Buffer pointer,
- Load the Digit Counter,
- Load the Duty Cycle register.

A fourth control code is defined but is not intended as a user function (see note associated with Table 1). Table 1 lists the control codes and their functions.

Load Buffer Pointer

The LOAD BUFFER POINTER code allows the Display Data Buffer pointer to be set to any digit position so that individual characters may be modified. The LOAD BUFFER PTR is loaded with a decimal equivalent value 2 less than the desired value (i.e., to point to character 6 of the display, a value of 4 is entered).

Load Digit Counter

The LOAD DIGIT COUNTER code is normally used only during initialization routines to define the number of character positions to be controlled. This code maximizes the duty cycle for any display. If 16 characters are to be controlled, enter a value of 0 (zero). Otherwise, enter the value desired.

Load Duty Cycle

The LOAD DUTY CYCLE code is used to turn the display on and off, to adjust display brightness, or to modify display timing for gas discharge displays. As shown in the block diagram, the time slot for each character is 32 clock cycles. The Segment and Digit Drivers for each character are on for a maximum of 31 cycles with a 1 cycle inter-digit off-time. The LOAD DUTY CYCLE code contains a 5-bit numeric field which modifies the on-time for segment Driver Outputs from 0 to 31 cycles. A duty cycle of 0 puts both the segment and digit drivers into the off state.

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit ASCII format codes. The 64 codes available (with the C-bit set to 0 to indicate a display data word) are shown in Table 2 with their corresponding ASCII characters.

Sixteen display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer is automatically incremented before each data word is stored in the Display Buffer except for decimal point and comma words. These do not cause the Buffer Pointer to increment and thus are always associated with the previous character entered. To select the next character position to be loaded out of the normal sequence, use the LOAD BUFFER POINTER command before entering the display data word. It is not necessary to use the LOAD BUFFER POINTER command to cycle back to position 1 when less than 16 character positions are being used (DIGIT COUNTER = 0).

Table 1. Control Data Words

8-Bit Control Word		Function
C-Bit (Bit 7)	7-Bit Code (Bits 6-0)	
1	010NNNN ⁽¹⁾	LOAD BUFFER POINTER (Position of character to be changed)
1	100NNNN ⁽¹⁾	LOAD DIGIT COUNTER (Number of characters to be output)
1	11NNNNN ⁽²⁾	LOAD DUTY CYCLE (On/off and brightness control)
1	00NNNNN ⁽³⁾	TEST MODE ONLY (Not a user function)
Notes: 1. NNNN is a 4-bit binary value representing the digit number to be loaded 2. NNNNN is a 5-bit binary value representing the number of clock cycles each digit is on.		3. This code is a device test function only. If executed it will lock the device in the test mode which can be removed only by performing a power-on reset.

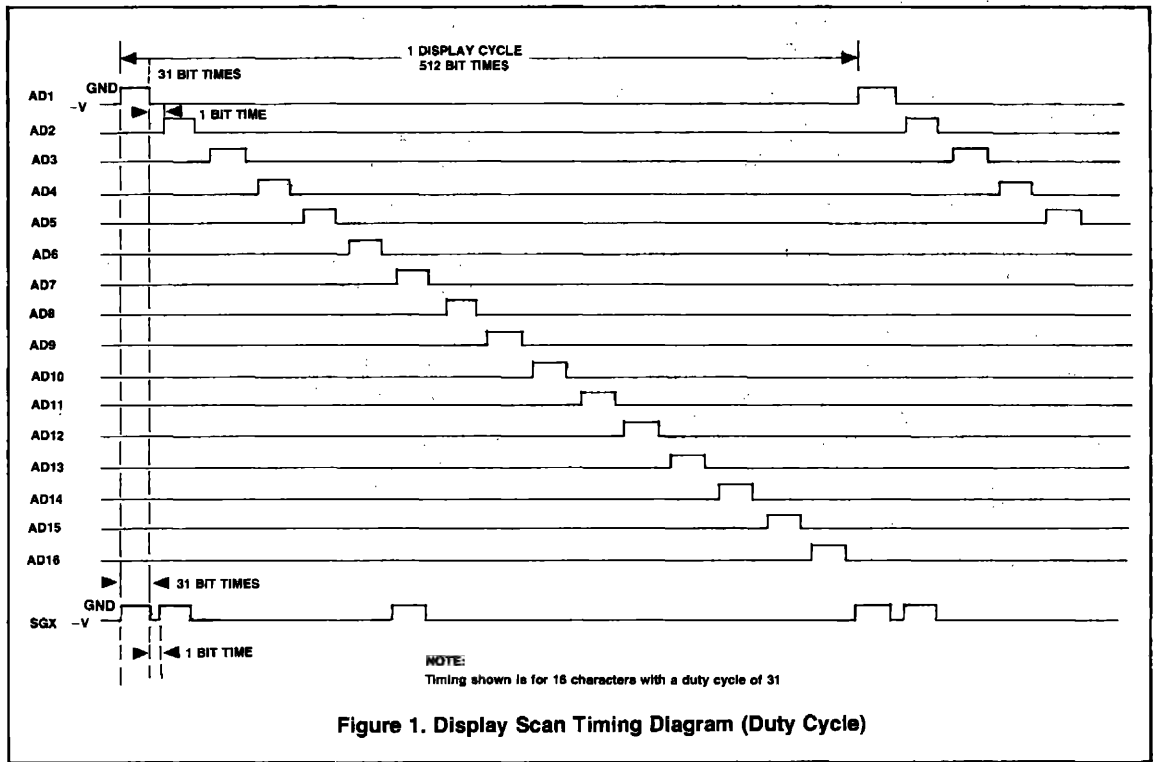


Table 2. Character Assignments for Display Data Words

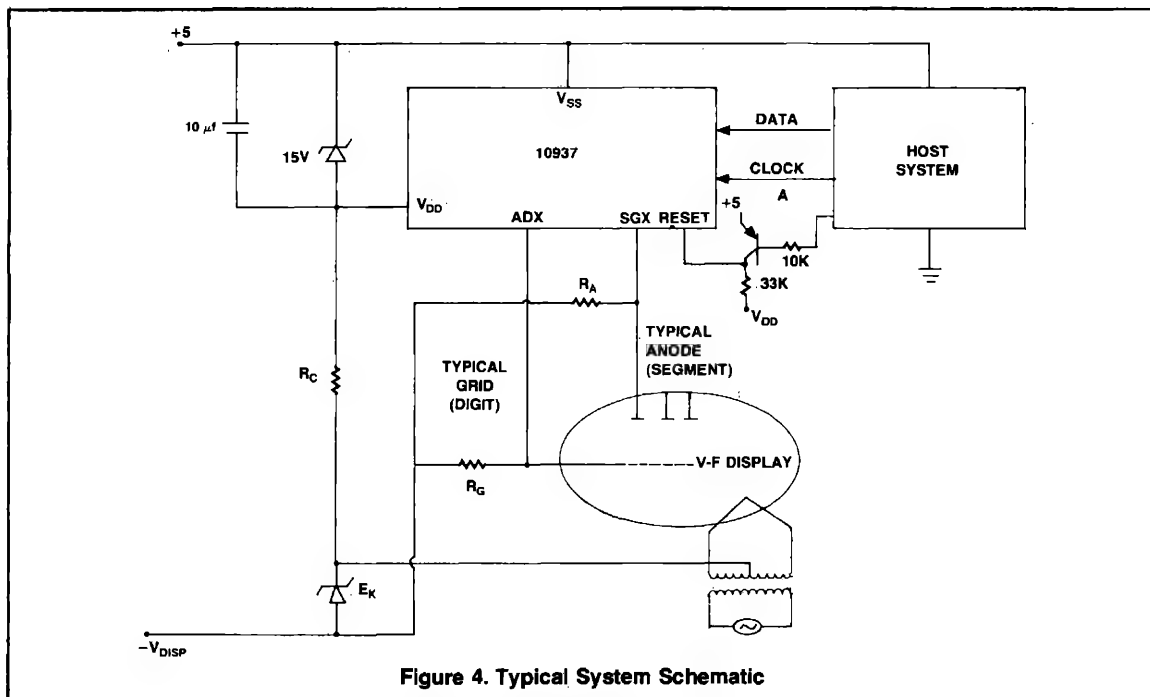
DATA WORD	CHARACTER	DATA WORD	CHARACTER	DATA WORD	CHARACTER	DATA WORD	CHARACTER
0X000000	@	0X010000	P	0X100000	!	0X110000	0
0X000001	A	0X010001	Q	0X100001	"	0X110001	1
0X000010	B	0X010010	R	0X100010	#	0X110010	2
0X000011	C	0X010011	S	0X100011	\$	0X110011	3
0X000100	D	0X010100	T	0X100100	%	0X110100	4
0X000101	E	0X010101	U	0X100101	&	0X110101	5
0X000110	F	0X010110	V	0X100110	'	0X110110	6
0X000111	G	0X010111	W	0X100111	(0X110111	7
0X001000	H	0X011000	X	0X101000)	0X111000	8
0X001001	I	0X011001	Y	0X101001	*	0X111001	9
0X001010	J	0X011010	Z	0X101010	+	0X111010	:
0X001011	K	0X011011	[0X101011	,	0X111011	;
0X001100	L	0X011100	/	0X101100	—	0X111100	<
0X001101	M	0X011101]	0X101101	.	0X111101	=
0X001110	N	0X011110	^	0X101110	\	0X111110	>
0X001111	O	0X011111	-	0X101111		0X111111	?

MSD LSD	0X000	0X001	0X010	0X011	0X100	0X101	0X110	0X111
000					SPACE			
001								
010								
011								
100						DECIMAL POINT + TAIL		
101								
110						DECIMAL POINT		
111								

NOTES: 1. Indicates characters that will not look the same as shown on a 14 segment display.

2. The LSD corresponds to the three least significant bits (0-2) and the MSD corresponds to the next three bits (3-5) in Table 2.

Figure 3. Display Segment Driver Character Patterns





10938 AND 10939 DOT MATRIX DISPLAY CONTROLLER

DESCRIPTION

The Rockwell 10938 and 10939 Dot Matrix Display Controller is a two-chip MOS/LSI general purpose display controller system designed to interface to dot matrix displays (gas discharge, vacuum-fluorescent or LED).

The two-chip set will drive displays with up to 35 anodes (dots) and up to 20 grids (characters) plus a cursor. The chips can be cascaded to drive larger displays of 80 characters or more with any number of segments. An internal PLA-type segment decoder provides character decoding and dot pattern generation for the full 96-character ASCII set.

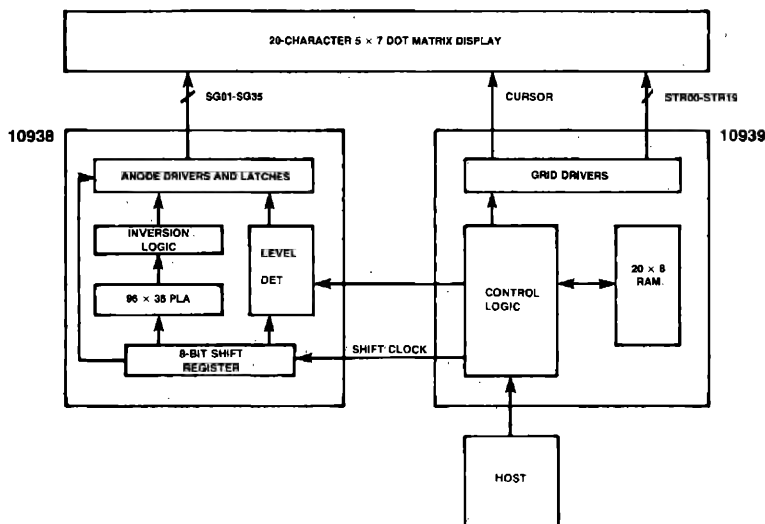
ORDERING INFORMATION

Part Number	Package Type	Temperature Range
10938P	Plastic	0°C to +70°C
10938PE	Plastic	-40°C to +85°C
10939P	Plastic	0°C to +70°C
10939PE	Plastic	-40°C to +85°C

FEATURES

- 20-character display driver cascable to 80 or more characters
- Standard 5 × 7 character font. Custom fonts available by special order
- Separate cursor driver output
- Direct drive capability for vacuum-fluorescent displays
- 96 × 35 PLA provides segment decoding for full 96-character ASCII set
- Serial or parallel data input for 8-bit display and control characters
- Brightness, refresh rate, and display mode controls
- 40-pin DIP

5



Block Diagram of 10938 and 10939

INTERFACE DESCRIPTION

10938 Pin Functions

Signal Name	Pin No.	Function
V _{SS}	2	Power and signal ground
SG01-SG35	3-25, 27-38	Segment driver outputs
SCLK-DIS	39	Serial data shift
DATA-LOAD	40	Serial data output/latch control
V _{DD}	1	DC Power
V _{GG}	26	Pull down driver voltage

10939 Pin Functions

Signal Name	Pin No.	Function
V _{SS}	36	Power and signal ground
V _{DD}	37	DC Power
CLOCK	38	Synchronization Clock
CURSOR	14	Cursor drive output
MASTER	39	Master/Slave Mode control
SIP	3	Sync Input
SOP	2	Sync Output
D0-D7	6-13	Serial or parallel data input
LD	5	Input data strobe
POR	4	Power-on reset
SCLK-DIS	1	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
STR00-STR19	15-34	Anode Drive Outputs
V _{GG}	35	Pull down driver voltage

V _{DD}	1	40	DATA-LOAD
V _{SS}	2	39	SCLK-DIS
SG35	3	38	SG01
SG34	4	37	SG02
SG33	5	36	SG03
SG32	6	35	SG04
SG31	7	34	SG05
SG30	8	33	SG06
SG29	9	32	SG07
SG28	10	31	SG08
SG27	11	30	SG09
SG26	12	29	SG10
SG25	13	28	SG11
SG24	14	27	SG12
SG23	15	26	V _{GG}
SG22	16	25	SG13
SG21	17	24	SG14
SG20	18	23	SG15
SG19	19	22	SG16
SG18	20	21	SG17

10938 Pin Configuration

SCLK-DIS	1	40	DATA-LOAD
SOP	2	39	MASTER
SIP	3	38	CLOCK
POR	4	37	V _{DD}
LD	5	36	V _{SS}
D0	6	35	V _{GG}
D1	7	34	STR00
D2	8	33	STR01
D3	9	32	STR02
D4	10	31	STR03
D5	11	30	STR04
D6	12	29	STR05
D7	13	28	STR06
CURSOR	14	27	STR07
STR19	15	26	STR08
STR18	16	25	STR09
STR17	17	24	STR10
STR16	18	23	STR11
STR15	19	22	STR12
STR14	20	21	STR13

10939 Pin Configuration

SPECIFICATIONS

Maximum Ratings

Parameters	Notes	Symbol	Min	Typ	Max	Unit
Operating Temperature	1					
Commercial		T _c	0		+70	°C
Industrial			-40		+85	°C
Storage Temperature		T _i	-55		+125	°C
Operating Voltage	1	V _{DD}	-22	-20	-18	Volts
Operating Display Voltage	1	V _{GG}	-50		-30	Volts
Power Dissipation (total)	2					
I _{load} = 0 mA per driver		PDO		40	100	mW
I _{load} = 2 mA per driver		PDL		200	750	mW
Power Dissipation	3	PD		200	400	mW

NOTES: 1. Designates characteristics for both 10938 and 10939.

2. Designates characteristics for 10938.

3. Designates characteristics for 10939.

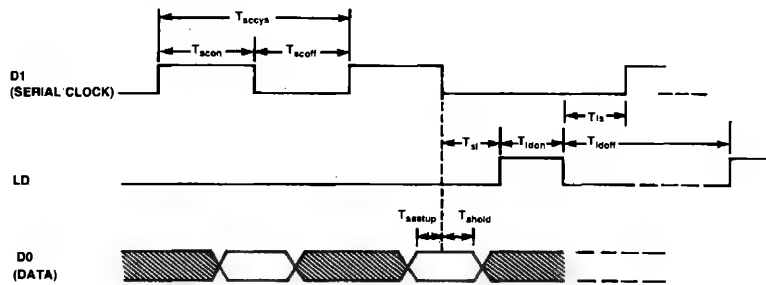
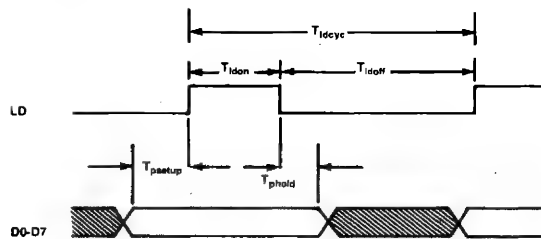
D.C. Characteristics

Parameters	Notes	Symbol	Min	Typ	Max	Unit
Input D0-D7, LD, SIP Logic "1" Logic "0"	3	V_{IH} V_{IL}	-1.2 V_{CC}		+0.3 -4.2	V V
Input POR Logic "1" Logic "0"	3	V_{IHPO} V_{ILPO}	-3.0 V_{DD}		+0.3 -10.0	V V
Output SOP Logic "1" Logic "0"	3	V_{OHsy} V_{OLsy}	-1.2 V_{DD}		+0.3 -4.2	V V
Output Digits, Cursor, and Segments Logic "1" ($I_{load} = 10\text{ mA}$) Logic "0" ($I_{load} = 0\text{ mA}$)	1	V_{OH} V_{OL}	-1.5 V_{GG}		.95 V_{CC}	V V
NOTES: 1. Designates characteristics for both 10938 and 10939. 2. Designates characteristics for 10938. 3. Designates characteristics for 10939.						

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
CLOCK Cycle Time Commercial Industrial	T_{cyc}	6.66 5.88		20.0 22.2	μs μs
Display Outputs (STR00-STR19 and CURSOR)	T_{stoft} T_{ston}			7.5* 1.54*	μs μs
SERIAL INTERFACE TIMING					
Serial Clock (D1) On Time Off Time Cycle Time	T_{scon} T_{scoff} T_{sccyc}	0.4 0.4 1.0		20.0	μs μs μs
Serial Data (D0) Set-up Time Hold Time	T_{ssetup} T_{shold}	400 400			ns ns
Serial Clock to LD Time LD to Serial Clock	T_{sl} T_{ls}	600 400			ns ns
PARALLEL INTERFACE TIMING					
Parallel Data (D0-D7) Set-up Time Hold Time	T_{psetup} T_{phold}	0 200			ns ns
Data Load (LD) On Time Off Time Commercial Industrial Cycle Time Commercial Industrial	T_{ldon} T_{ldoff} T_{ldcyc}	250 40.0 44.5 60.0 66.7			ns μs μs μs μs

* 40 pf. maximum load capacitance.

SERIAL INTERFACE TIMING WAVEFORMS**PARALLEL INTERFACE TIMING WAVEFORMS**

FUNCTIONAL DESCRIPTION

Once the display buffer has been loaded from the host processor, the 10938/10939 system generates all timing signals required to control the display.

Input data is loaded into the Display Data Buffer via the Serial or Parallel Data Input channel on the 10939. Internal timing and control logic synchronize the digit output signals with the Serial Data and Load signals to the 10938 to provide the proper timing for the multiplexing operation. A 96×35 bit PLA is provided for decoding the full 96 character ASCII set.

Input data is loaded into the 10939 as a series of 8-bit words. If the Serial Mode is selected, Input Data lines D2-D7 should be tied down to V_{DD} externally. Raising any one of these lines to the V_{SS} level automatically shifts the 10939 into the Parallel Mode. Input data may be Control or Display data. The following paragraphs describe the format and functions of these control and display data words.

CONTROL DATA WORDS

Control data words are distinguished from Display Data words by the fact that they must be preceded by a Control Prefix word (0000 0001 or 01_{16}). Control words and their functions are defined in Table 1.

Table 1. Control Word Assignments

Hex Value	Function
00	Not used
01	Load 01 into Data Buffer
02	Not used
03	Not used
04	Not used
05	Set digit time to 16 cycles per grid
06	Set digit time to 32 cycles per grid
07	Set digit time to 64 cycles per grid
08	Enable Normal Display Mode (MSB in data words is ignored)
09	Enable Blank Mode (data words with MSB = 1 will be blanked)
0A	Enable Inverse Mode (data words with MSB = 1 will be "inversed")
0B	Not used
0C	Not used
0D	Not used
0E	Start Display Refresh Cycle (use only once after reset)
0F	Not used
10-3F	Not used
40-7F	Load Duty Cycle Register with lower 6 bits (0-63)
80-9F	Load Digit Counter (80=32, 81=1, 82=2, etc.)
A0-BF	Not used
C0-DF	Load Buffer Pointer Register with lower 5 bits
E0-FF	Not used

Load Buffer Pointer

The Load Buffer Pointer code sets the Display Data Buffer pointer. The lower 5 bits of the code are loaded into the buffer pointer (see Table 2).

Table 2. Load Buffer Pointer Codes

Code Value	Pointer Value	Character Position
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15
D0	10	16
D1	11	17
D2	12	18
D3	13	19
D4	14	20
D5	15	21
D6	16	22
D7	17	23
D8	18	24
D9	19	25
DA	1A	26
DB	1B	27
DC	1C	28
DD	1D	29
DE	1E	30
DF	1F	31

NOTE: DO NOT USE CHARACTER POSITIONS 20-31.

Load Digit Counter

The Load Digit Counter defines the number of character positions (grids) to be controlled. This code is normally used only during initialization routines, but it may also be used in conjunction with the Load Duty Cycle control code to extend the range of brightness control (see Table 3).

Load Duty Cycle

The Load Duty Cycle code is used to turn the display on and off, to adjust display brightness, or to modify display timing. The time slot for each character is 16, 32, or 64 cycles as selected by the Load Digit Time codes (see Table 3). The segment and digit drivers for each character are on for a maximum of 13, 29, or 61 cycles with a 3.0 cycle inter-digit off-time. The lower 6 bits of the Load Duty Cycle code are loaded into the Duty Cycle Register. Resultant duty cycles are shown in Table 4.

Table 3. Load Digit Counter Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Load Digit Time

The Load Digit Time codes set the total time for each character during the refresh cycle. Three values can be set using the three codes shown in Table 1. The default value set at power-on is 64 cycles per grid. For displays with 40 or more characters, or under conditions where the display can be subjected to quick movements during viewing (e.g. portable or vehicle-mounted applications), it may be necessary to increase the refresh rate by selecting 16 or 32 cycles per grid with the appropriate control code.

Enable Display Mode

Each ASCII character is represented by the lower seven bits of the 8-bit value loaded into the 10939. The eighth (most significant) bit is ignored in Normal display mode. If either Blank or Inverse mode is selected, however, a "0" in this bit selects Normal display mode, while a "1" selects either Blank or Inverse mode, depending on which mode is enabled. Three control codes are provided (see Table 1) to enable blank mode, enable inverse mode, or enable normal mode.

Table 4. Duty Cycle Control Codes

Code	Digit Time=16		Digit Time=32		Digit Time=64	
	On	Off	On	Off	On	Off
40	—	16	—	32	—	64
41	—	16	—	32	—	64
42	—	16	—	32	—	64
43	1	15	1	31	1	63
44	2	14	2	30	2	62
45	3	13	3	29	3	61
46	4	12	4	28	4	60
47	5	11	5	27	5	59
48	6	10	6	26	6	58
49	7	9	7	25	7	57
4A	8	8	8	24	8	56
4B	9	7	9	23	9	55
4C	10	6	10	22	10	54
4D	11	5	11	21	11	53
4E	12	4	12	20	12	52
4F	13	3	13	19	13	51
50	13	3	14	18	14	50
51	13	3	15	17	15	49
52	13	3	16	16	16	48
.	"	"	17	15	17	47
.	"	"
.	"	"
.	"	"
5B	"	"	25	7	25	39
5C	"	"	26	6	26	38
5D	"	"	27	5	27	37
5E	"	"	28	4	28	36
5F	"	"	29	3	29	35
60	"	"	29	3	30	34
.	"	"	29	3	31	33
.	"	"	"	"	32	32
.	"	"
.	"	"
7C	"	"	"	"	58	6
7D	"	"	"	"	59	5
7E	"	"	"	"	60	4
7F	"	"	"	"	61	3

In the Blank mode, any character with the MSB="1" will be blanked. In the Inverse mode, it will be displayed with all segment driver outputs inverted. On video displays, this is referred to as "Inverse Video" format. These controls allow individual characters or groups of characters to be blinked or blanked by simply changing the mode without changing the data in the Display Buffer.

Start Refresh

At power on, the 10939 is held in an internal Halt mode. The normal display refresh sequence starts upon receipt of a Start Refresh control code. This is particularly useful for synchronizing systems using more than one 10939. Only the Master 10939 in a multi-chip system will recognize the Start Refresh code. The Master starts the Slave(s) at the appropriate time, using the SYNC0 signal.

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit codes. The eighth (most significant) bit specifies normal (0) or blank/inverse (1) display mode, depending on the blank/inverse mode selection (see Control data words 09 and 0A in Table 1). Figure 1 shows the ASCII codes for the segment patterns for a bargraph display.

Twenty display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer automatically increments after each data word is stored in the buffer. To select the next character position to be loaded out of sequence, use the Load Buffer Pointer command. The Buffer Pointer will automatically reset to character position 0 when its value is equal to the Digit Counter programmed value.

POWER-ON RESET

The Power-On Reset (POR) initializes the internal circuits of the 10939. This is normally accomplished when power (V_{DD}) is applied. The following conditions are established by application of POR:

- The Grid Drivers (STR00-STR19) on the 10939 are in the off state.
- The Anode Drivers (SG01-SG35) on the 10938 are in the off state.
- The Duty Cycle is set to 0.
- The Digit Counter is set to 32.
- The Buffer Pointer is set to 0.
- The Digit time is set to 64.
- The Normal display mode is set.
- DATA-LOAD is set to high impedance state.
- SCLK-DIS is set to V_{OL} to disable the segment drivers in the 10938.
- SOP is set to V_{OL} to disable the sync pulse.

NOTES:

- When the POR signal is removed, SCLK-DIS is set to the high impedance state.
- During the initial rise time of V_{DD} at power turn-on, the magnitude of V_{GG} should not exceed the magnitude of V_{DD} .

DIGIT DRIVERS (STR00-STR19) PLUS CURSOR

The 20 Digit Drivers select each of the display character positions sequentially during a refresh scan. Display segments will be illuminated when both the Digit Drivers and Segment Drivers for a particular character are energized simultaneously. The Cursor segment is generated by the 10939, but its timing characteristics are identical to the 16 segments generated by the 10938.

SEGMENT DRIVERS (SG01-SG35)

Sixteen Segment Drivers are provided in the 10938. The output states for each ASCII character pattern and each bargraph pattern are internally decoded from the 8-bit characters received from the 10939 by means of a 96×16 -bit PLA. Data codes and the corresponding of the ASCII patterns are shown in Figure 1. Data codes and the corresponding bargraph patterns are shown in Figure 2.

M	2	3	4	5	6	7
0		0	a	P	^	P
1	!	1	A	Q	a	q
2	"	2	B	R	b	r
3	#	3	C	S	c	s
4	\$	4	D	T	d	t
5	%	5	E	U	e	u
6	&	6	F	V	f	v
7	'	7	G	W	g	w
8	(8	H	X	h	x
9)	9	I	Y	i	y
A	*	.	J	Z	j	z
B	+	,	K	[k	[
C	-	<	L	\	l	Y
D	~	=	M]	m	*
E	:	>	N	^	n	~
F	/	?	O	_	o	■

The four least significant bits of the seven bit ASCII code are shown in hex notation down the left side of the table. The three most significant bits are shown across the top of the table.

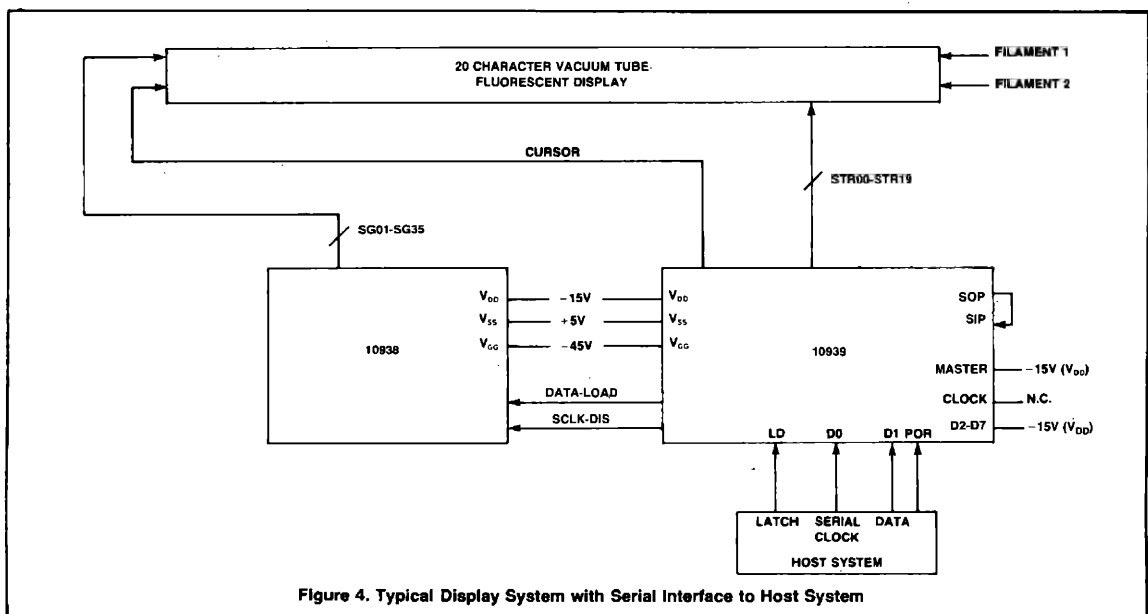
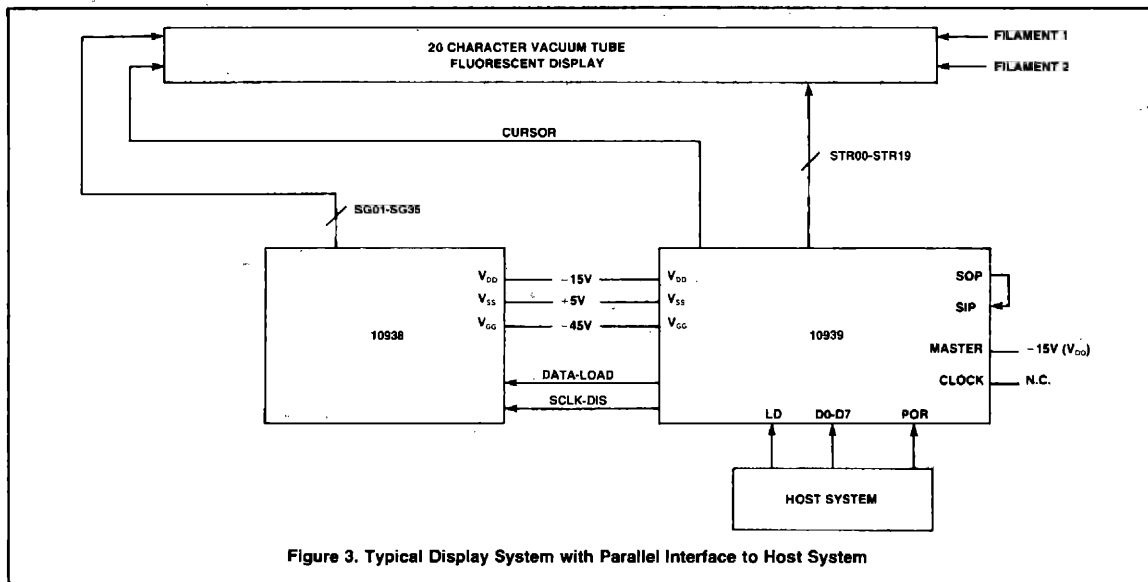
Figure 1. Dot Matrix Patterns

R \ C	1	2	3	4	5
1	SG01	SG02	SG03	SG04	SG05
2	SG06	SG07	SG08	SG09	SG10
3	SG11	SG12	SG13	SG14	SG15
4	SG16	SG17	SG18	SG19	SG20
5	SG21	SG22	SG23	SG24	SG25
6	SG26	SG27	SG28	SG29	SG30
7	SG31	SG32	SG33	SG34	SG35

Figure 2. 5 x 7 Dot Matrix Assignments

TYPICAL SYSTEM HOOKUPS

Figure 3 shows a 10938 and a 10939 in a parallel interface with the host system driving a 20 character display. Figure 4 shows a 10938 and a 10939 in a serial interface with the host system driving a 20 character display. Figure 5 shows a 10938 and two 10939's interfaced parallel with the host system driving a 40 character display.



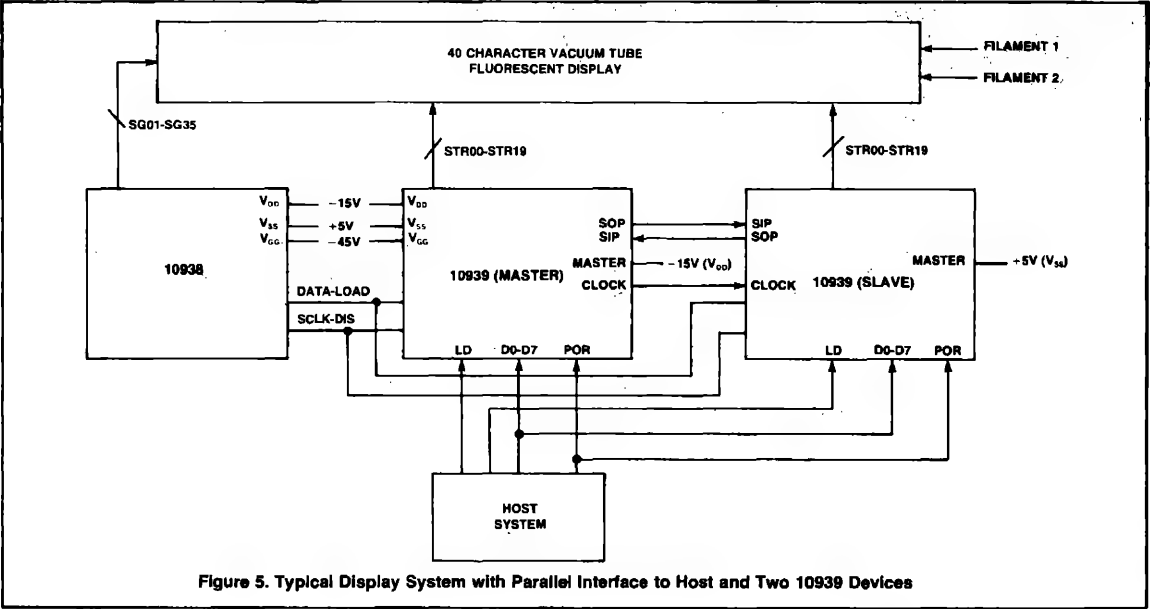


Figure 5. Typical Display System with Parallel Interface to Host and Two 10939 Devices



10939, 10942, & 10943 DOT MATRIX DISPLAY CONTROLLER

DESCRIPTION

The Rockwell 10939, 10942, and 10943 Dot Matrix Display Controller is a three-chip MOS/LSI general purpose display controller system designed to interface to dot matrix displays (gas discharge, vacuum-fluorescent or LED).

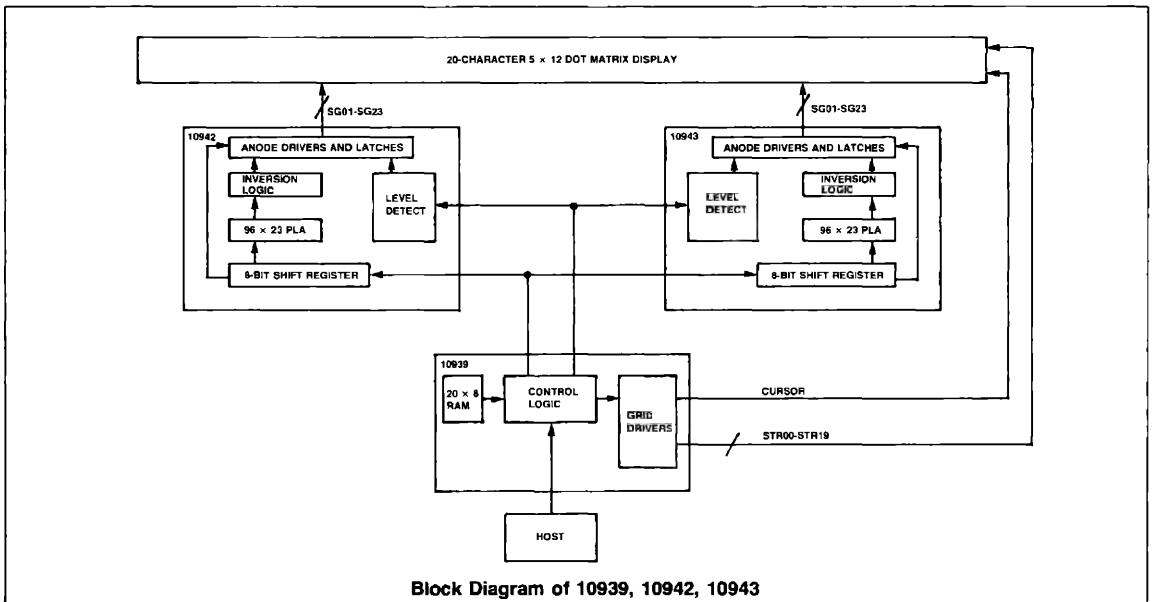
The three-chip set will drive displays with up to 46 anodes (dots) and up to 20 grids (characters) plus a cursor. The chips can be cascaded to drive larger displays of up to 80 characters with any number of segments. An internal PLA-type segment decoder provides character decoding and dot pattern generation for the full 96-character ASCII set.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
10939P	Plastic	0°C to +70°C
10939PE	Plastic	-40°C to +85°C
10942P	Plastic	0°C to +70°C
10942PE	Plastic	-40°C to +85°C
10943P	Plastic	0°C to +70°C
10943PE	Plastic	-40°C to +85°C

FEATURES

- 20-character display driver cascadable to 80 characters
- Standard 5 × 12 character font. Custom fonts available by special order
- Separate cursor driver output
- Direct drive capability for vacuum-fluorescent displays
- Two 96 × 23 PLA's provide segment decoding for full 96-character ASCII set
- Serial or parallel data input for 8-bit display and control characters
- Brightness, refresh rate, and display mode controls
- 10939 provided in 40-pin DIP
- 10942 and 10943 provided in 28-pin DIP



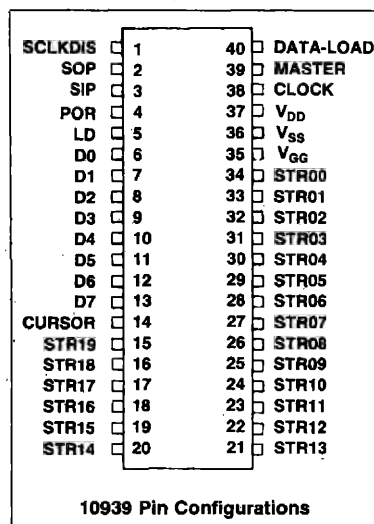
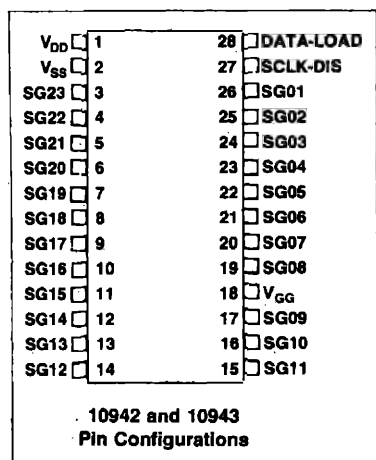
INTERFACE DESCRIPTION

10942 and 10943 Pin Functions

Signal Name	Pin No.	Function
V _{DD}	1	DC Power
V _{SS}	2	Power and signal ground
SG01-SG23	3-17 19-26	Segment (Anode) driver outputs
V _{GG}	18	Pull down driver voltage
SCLK-DIS	27	Serial data shift
DATA-LOAD	28	Serial data output/latch control

10939 Pin Functions

Signal Name	Pin No.	Function
V _{SS}	36	Power and signal ground
V _{DD}	37	DC Power
CLOCK	38	Synchronization Clock
CURSOR	14	Cursor drive output
MASTER	39	Master/Slave Mode control
SIP	3	Sync Input
SOP	2	Sync Output
D0-D7	6-13	Serial or parallel data input
LD	5	Input data strobe
POR	4	Power-on reset
SCLK-DIS	1	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
STR00-STR19	15-34	Anode Drive Outputs
V _{GG}	35	Pull down driver voltage



SPECIFICATIONS

Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Operating Temperature	T _A				
Commercial		0		+70	°C
Industrial		-40		+85	°C
Storage Temperature	T _S	-55		+125	°C
Operating Voltage	V _{DD}	-22	-20	-18	Volts
Operating Display Voltage	V _{GG}	-50		-30	Volts

D.C. Characteristics ($V_{DD} = -18$ to -22 Vdc, $V_{SS} = 0$ Vdc, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Units
10942 & 10943					
Output Segments					
Logic "1" ($I_{LOAD} = 2$ mA)	V_{OH}	-1.5			V
Logic "0" ($I_{LOAD} = 0$ mA)	V_{OL}	V_{GG}		$0.95V_{GG}$	V
10939					
Input D0-D7, LD, SIP					
Logic "1"	V_{IH}	-1.2		+0.3	V
Logic "0"	V_{IL}	V_{DD}		-4.2	V
Input POR					
Logic "1"	V_{IHPO}	-3.0		+0.3	V
Logic "0"	V_{ILPO}	V_{DD}		-10.0	V
Output SOP					
Logic "1"	V_{OHSY}	-1.2		+0.3	V
Logic "0"	V_{OLSY}	V_{DD}		-4.2	V
Output Digits, Cursor					
Logic "1" ($I_{load} = 10$ mA)	V_{OH}	-1.5			V
Logic "0" ($I_{load} = 0$ mA)	V_{OL}	V_{GG}		$0.96V_{GG}$	V

Note: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ (commercial) or -40°C to $+85^\circ\text{C}$ (industrial), unless otherwise noted.

Operating Currents

Parameters	Maximum		Typical	Units
	Industrial $T_A = -40^\circ\text{C}$ $V_{DD} = -22\text{Vdc}$	Commercial $T_A = 0^\circ\text{C}$ $V_{DD} = -22\text{Vdc}$	$T_A = 25^\circ\text{C}$ $V_{DD} = -20\text{Vdc}$	
10942 & 10943				
$I_{DD}^{(1)}$	4.5	3.6	2.2	mA
$I_{GG}^{(1)}$	11.2	9.0	5.6	mA
$I_{SS}^{(3)}$	85.7	82.6	77.8	mA
10939 (master)				
$I_{DD}^{(2)}$	13.6	10.9	6.0	mA
$I_{GG}^{(2)}$	1.0	0.8	0.5	mA
$I_{SS}^{(3)}$	84.6	71.7	76.5	mA
10939 (slave)				
$I_{DD}^{(2)}$	9.1	7.3	4.0	mA
$I_{GG}^{(2)}$	1.0	0.8	0.5	mA
$I_{SS}^{(3)}$	80.1	78.1	74.5	mA

Notes:

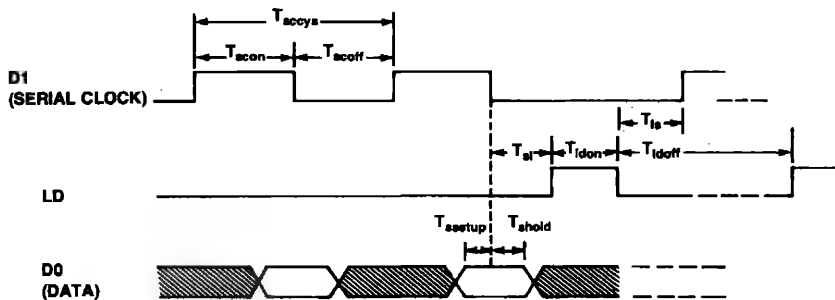
- The 10942 and 10943 each have 35 internal driver outputs, 23 of which are brought out. I_{GG} is proportional to the number of drivers on. The values given are for all 35 drivers on. Divide I_{GG} shown by 35 to determine I_{GG} for one driver.
- The 10939 will never have more than two drivers on at any one time; one grid driver and the cursor. The values shown are for two drivers on with 100% duty cycle.
- $I_{SS} = I_{DD} + I_{GG} + I_{DVR}$ ($I_{DVR} = 35 \times I_{LOAD}$)
Example: For 10939 and 10943 ($T_A = -40^\circ\text{C}$ and $V_{DD} = -22\text{V}$):
 $I_{SS} = 4.5 + 11.2 + (35 \times 2.0) = 85.7\text{mA}$.

A.C. Characteristics

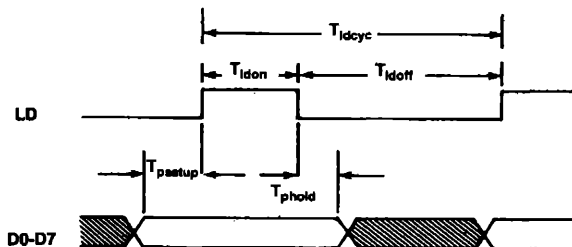
Parameter	Symbol	Min	Typ	Max	Unit
CLOCK Cycle Time	T_{cyc}	6.66		20.0	μs
Commercial		5.88		22.2	μs
Industrial					
Display Outputs (STR00-STR19 and CURSOR)	T_{stoft}			7.5*	μs
	T_{ston}			1.54*	μs
Data Load (LD)					
On Time	T_{ldon}	1.0			μs
Off Time	T_{ldoff}				μs
Commercial		40.0			μs
Industrial		44.5			μs
Cycle Time	T_{ldcyc}				μs
Commercial		60.0			μs
Industrial		66.7			μs
SERIAL INTERFACE TIMING					
Serial Clock (D1)				20.0	μs
On Time	T_{scon}	1.0			μs
Off Time	T_{scoff}	1.0			μs
Cycle Time	T_{scyc}	2.0			μs
Serial Data (D0)					
Set-up Time	T_{ssetup}	400			ns
Hold Time	T_{shold}	400			ns
Serial Clock to LD Time	T_{sl}	1.0			μs
LD to Serial Clock	T_{ls}	1.0			μs
PARALLEL INTERFACE TIMING					
Parallel Data (D0-D7)					
Set-up Time	T_{psetup}	0			ns
Hold Time	T_{phold}	200			ns

*40 pf. maximum load capacitance.

SERIAL INTERFACE TIMING WAVEFORMS



PARALLEL INTERFACE TIMING WAVEFORMS



FUNCTIONAL DESCRIPTION

Once the display buffer has been loaded from the host processor, the 10939, 10942, and 10943 system generates all timing signals required to control the display.

Input data is loaded into the Display Data Buffer via the Serial or Parallel Data Input channel on the 10939. Internal timing and control logic synchronize the digit output signals with the Serial Data and Load signals to the 10942/10943 to provide the proper timing for the multiplexing operation. Two 92×23 bit PLA's, one in the 10942 and the other in the 10943, decode the full 96-character ASCII set.

Input data is loaded into the 10939 as a series of 8-bit words. If the Serial Mode is selected, Input Data lines D2-D7 should be tied down to V_{DD} externally. Raising any one of these lines to the V_{SS} level automatically shifts the 10939 into the Parallel Mode. Input data may be Control or Display data. The following paragraphs describe the format and functions of these control and display data words.

CONTROL DATA WORDS

Control data words are distinguished from Display Data words by the fact that they must be preceded by a Control Prefix word (0000 0001 or 01₁₆). Control words and their functions are defined in Table 1.

Table 1. Control Word Assignments

Hex Value	Function
00	Not used
01	Load 01 into Data Buffer
02	Not used
03	Not used
04	Not used
05	Load Digit Time to 16 cycles per grid
06	Load Digit Time to 32 cycles per grid
07	Load Digit Time to 64 cycles per grid
08	Enable Normal Display Mode (MSB in data words is ignored)
09	Enable Blank Mode (data words with MSB = 1 will be blanked)
0A	Enable Inverse Mode (data words with MSB = 1 will be "inversed")
0B	Not used
0C	Not used
0D	Not used
0E	Start Display Refresh Cycle (use only once after reset)
0F	Not used
10-3F	Not used
40-7F	Load Duty Cycle Register
80-9F	Load Digit Counter (80=32, 81=1, 82=2, etc.)
A0-BF	Not used
C0-DF	Load Buffer Pointer Register with lower 5 bits
E0-FF	Not used

Load Buffer Pointer

The Load Buffer Pointer code sets the Display Data Buffer pointer. The lower 5 bits of the code are loaded into the buffer pointer (see Table 2).

Table 2. Load Buffer Pointer Codes

Code Value	Pointer Value	Character Position
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15
D0	10	16
D1	11	17
D2	12	18
D3	13	19
D4	14	20
D5	15	21
D6	16	22
D7	17	23
D8	18	24
D9	19	25
DA	1A	26
DB	1B	27
DC	1C	28
DD	1D	29
DE	1E	30
DF	1F	31

Note: Do not use character positions 20-31.

Load Digit Counter

The Load Digit Counter defines the number of character positions (grids) to be controlled. This code is normally used only during initialization routines, but it may also be used in conjunction with the Load Duty Cycle control code to extend the range of brightness control (see Table 3).

Load Duty Cycle

The Load Duty Cycle code is used to turn the display on and off, to adjust display brightness, or to modify display timing. The time slot for each character is 16, 32, or 64 cycles as selected by the Load Digit Time codes (see Table 1). The segment and digit drivers for each character are on for a maximum of 13, 29, or 61 cycles with a 3.0 cycle inter-digit off-time. The lower 6 bits of the Load Duty Cycle code are loaded into the Duty Cycle Register. Resultant duty cycles are shown in Table 4.

Table 3. Load Digit Counter Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Table 4. Duty Cycle Control Codes

Code	Digit Time=16		Digit Time=32		Digit Time=64	
	On	Off	On	Off	On	Off
40	—	16	—	32	—	64
41	—	16	—	32	—	64
42	—	16	—	32	—	64
43	1	15	1	31	1	63
44	2	14	2	30	2	62
45	3	13	3	29	3	61
46	4	12	4	28	4	60
47	5	11	5	27	5	59
48	6	10	6	26	6	58
49	7	9	7	25	7	57
4A	8	8	8	24	8	56
4B	9	7	9	23	9	55
4C	10	6	10	22	10	54
4D	11	5	11	21	11	53
4E	12	4	12	20	12	52
4F	13	3	13	19	13	51
50	13	3	14	18	14	50
51	13	3	15	17	15	49
52	13	3	16	16	16	48
.	"	"	17	15	17	47
.	"	"
.	"	"
.	"	"
5B	"	"	25	7	25	39
5C	"	"	26	6	26	38
5D	"	"	27	5	27	37
5E	"	"	28	4	28	36
5F	"	"	29	3	29	35
60	"	"	29	3	30	34
.	"	"	29	3	31	33
.	"	"	"	"	32	32
.	"	"
.	"	"
.	"	"
7C	"	"	"	"	58	6
7D	"	"	"	"	59	5
7E	"	"	"	"	60	4
7F	"	"	"	"	61	3

Load Digit Time

The Load Digit Time codes set the total time for each character during the refresh cycle. Three values can be set using the three codes shown in Table 1. The default value set at power-on is 64 cycles per grid. For displays with 40 or more characters, or under conditions where the display can be subjected to quick movements during viewing (e.g. portable or vehicle-mounted applications), it may be necessary to increase the refresh rate by selecting 16 or 32 cycles per grid with the appropriate control code.

Enable Display Mode

Each ASCII character is represented by the lower seven bits of the 8-bit value loaded into the 10939. The eighth (most significant) bit is used to turn the cursor on in Normal display mode. If either Blank or Inverse mode is selected, however, a "0" in this bit selects Normal display mode, while a "1" selects either Blank or Inverse mode, depending on which mode is enabled. Three control codes are provided (see Table 1) to enable blank mode, enable inverse mode, or enable normal mode.

In the Blank mode, any character with the MSB="1" will be blanked. In the Inverse mode, it will be displayed with all segment driver outputs inverted. On video displays, this is referred to as "Inverse Video" format. These controls allow individual characters or groups of characters to be blinked or blanked by simply changing the mode without changing the data in the Display Buffer.

Start Refresh

At power on, the 10939 is held in an internal Halt mode. The normal display refresh sequence starts upon receipt of a Start Refresh control code. This is particularly useful for synchronizing systems using more than one 10939. Only the Master 10939 is a multi-chip system will recognize the Start Refresh code. The Master starts the Slave(s) at the appropriate time, using the SYNCO signal.

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit codes. The eighth (most significant) bit (bit 7) is a dual purpose bit. This bit specifies normal (0) or blank/inverse (1) display mode, depending on the blank/inverse mode selection (see control data words 09 and 0A in Table 1). Bit 7 also controls the cursor output from the 10939; on (1) or off (0). Note, however, that this bit always controls the cursor no matter what display mode is selected.

Twenty display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer automatically increments after each data word is stored in the buffer. To select the next character position to be loaded out of sequence, use the Load Buffer Pointer command. The Buffer Pointer will automatically reset to character position 0 when its value is equal to the Digit Counter programmed value.

DIGIT DRIVERS (STR00-STR19) PLUS CURSOR

The 20 Digit Drivers select each of the display character positions sequentially during a refresh scan. Display segments will be illuminated when both the Digit Drivers and Segment Drivers for a particular character are energized simultaneously. The Cursor segment is generated by the 10939, but its timing characteristics are identical to the 46 segment outputs generated by the 10942 and the 10943.

SEGMENT DRIVERS (SG01-SG23)

46 Segment Drivers are provided by the 10942 and the 10943. The output states for each ASCII character pattern are internally decoded from the 8-bit characters received from the 10939 by means of two 96×23 -bit PLA's, one in the 10942 and the other in the 10943. Data codes and the corresponding ASCII patterns are shown in Figure 1.

POWER-ON RESET

The Power-On Reset (POR) initializes the internal circuits of the 10939. This is normally accomplished when power (V_{DD}) is applied. The following conditions are established by application of POR:

- The Grid Drivers (STR00-STR19) on the 10939 are in the off state.
- The Anode Drivers, SG01-SG23 on the 10942 and SG01-SG23 on the 10943, are in the off state.
- The Duty Cycle is set to 0.
- The Digit Counter is set to 32.
- The Buffer Pointer is set to 0.
- The Digit time is set to 64.
- The Normal display mode is set.
- DATA-LOAD is set to high impedance state.
- SCLK-DIS is set to V_{OL} to disable the segment drivers in the 10942 and 10943.
- SOP is set to V_{OL} to disable the sync pulse.

NOTES:

- When the POR signal is removed, SCLK-DIS is set to the high impedance state.
- During the initial rise time of V_{DD} at power turn-on, the magnitude of V_{GG} should not exceed the magnitude of V_{DD} .

SEGMENTS DRIVEN BY 10942	ROW	COL				
		1	2	3	4	5
	1	SG01	SG02	SG03	SG04	SG05
	2	SG06	SG07	SG08	SG09	SG10
	3	SG11	SG12	SG13	SG14	SG15
	4	SG16	SG17	SG18	SG19	SG20
	5	SG21	SG22	SG23	SG01	SG02
SEGMENTS DRIVEN BY 10943	6	SG03	SG04	SG05	SG06	SG07
	7	SG08	SG09	SG10	SG11	SG12
	8	SG13	X	X	SG14	SG15
	9	SG16	X	X	SG17	SG18
	10	SG19	SG20	SG21	SG22	SG23
	11	X	X	X	X	X
12 TIE THESE FIVE TOGETHER ⁽¹⁾						
Note: 1. DRIVEN BY CURSOR LINE OF 10939.						

Figure 2. 5 × 12 Dot Matrix Assignments

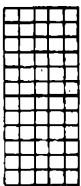
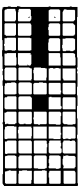
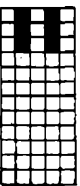
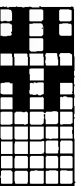
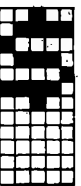
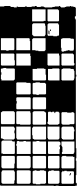
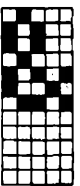
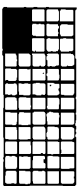
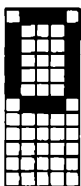
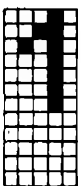
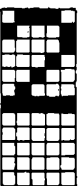
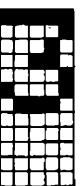

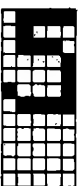
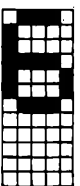
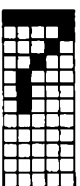
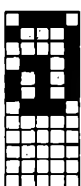
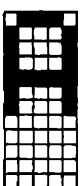
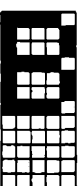
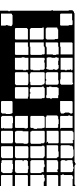
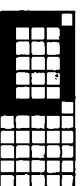
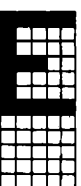
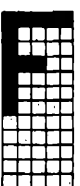
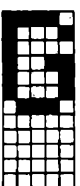
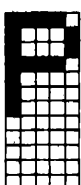
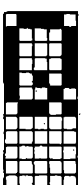
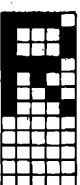
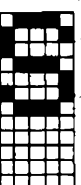
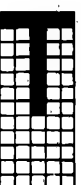
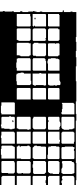
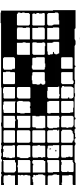
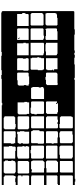
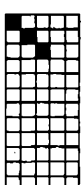
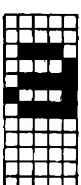
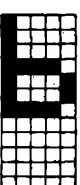

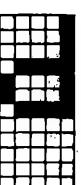
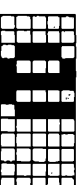
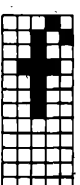
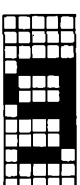
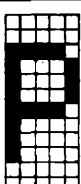
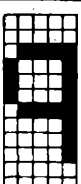
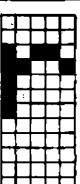
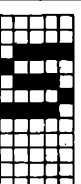
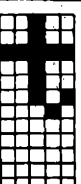
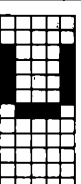
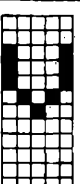
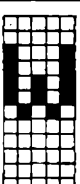
$\begin{matrix} L & S & B \\ M & S & B \end{matrix}$	0000	0001	0010	0011	0100	0101	0110	0111
X010								
X011								
X100								
X101								
X110								
X111								

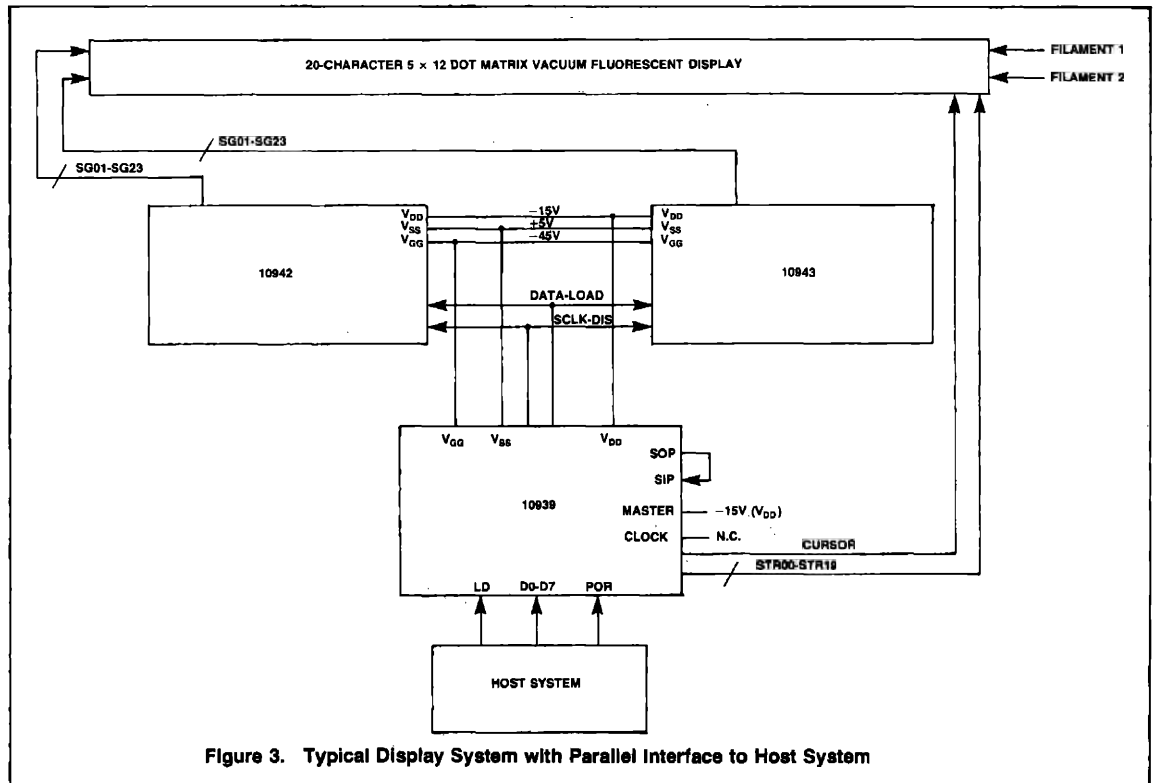
Figure 1. Dot Matrix Patterns

$\begin{matrix} L & S & B \\ M & S & B \end{matrix}$	1000	1001	1010	1011	1100	1101	1110	1111
X010								
X011								
X100								
X101								
X110								
X111								

Figure 1. Dot Matrix Patterns (Cont.)

TYPICAL SYSTEM HOOKUPS

Figure 3 shows a 10939, 10942, and a 10943 in a parallel interface with the host system driving a 20-character display. Figure 4 shows a 10939, 10942, and a 10943 in a serial interface with the host system driving a 20-character display. Figure 5 shows two 10939's, a 10942, and a 10943 interfaced parallel with the host system driving a 40-character display.



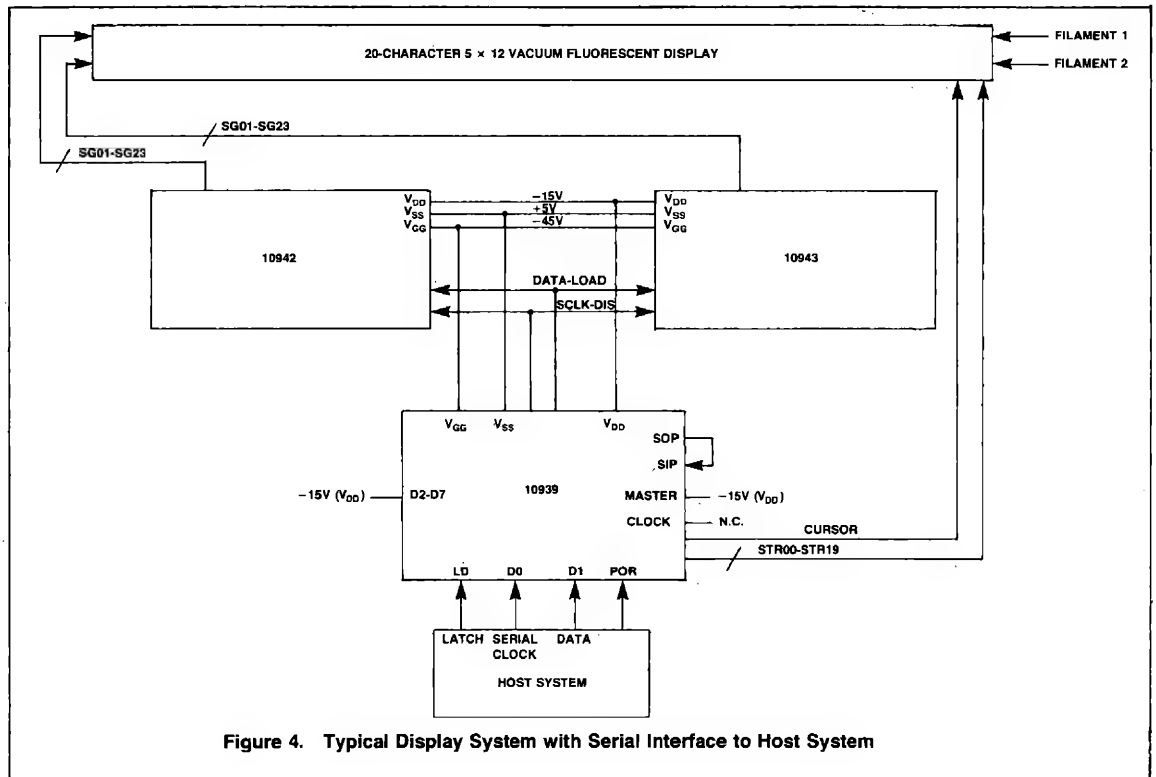


Figure 4. Typical Display System with Serial Interface to Host System

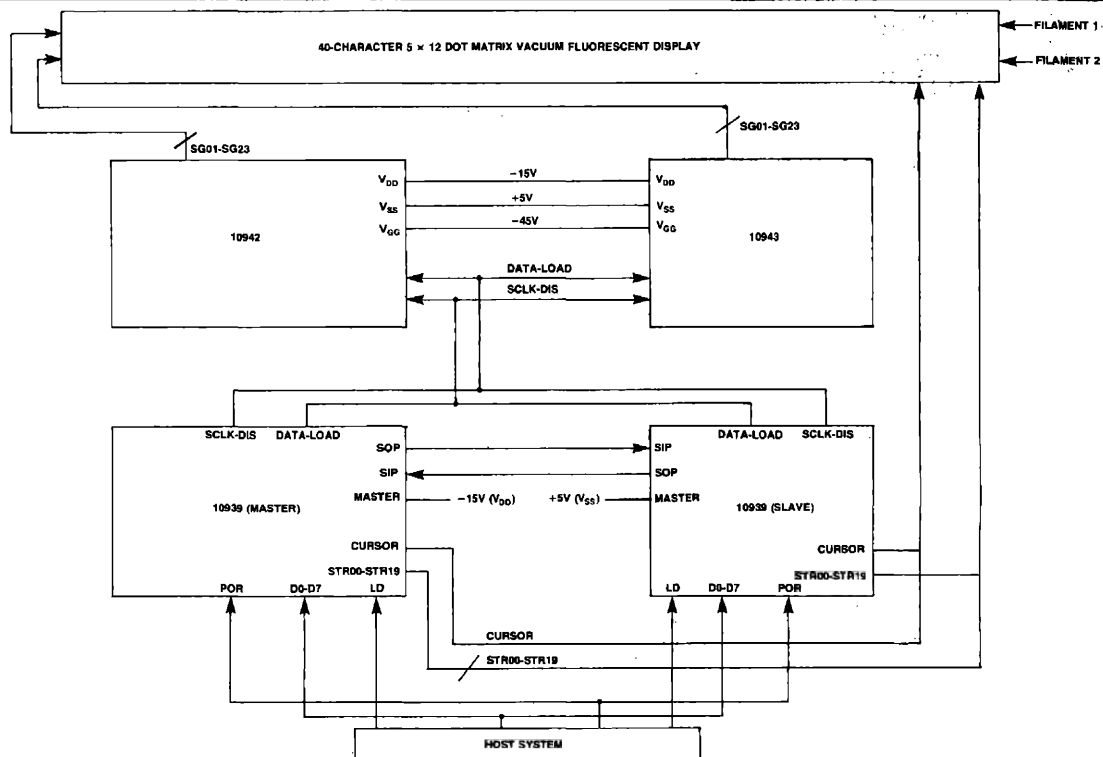


Figure 5. Typical Display System with Parallel Interface to Host and Two 10939 Devices



10941 AND 10939 ALPHANUMERIC AND BARGRAPH DISPLAY CONTROLLER

DESCRIPTION

The Rockwell 10939 and 10941 Alphanumeric and Bargraph Display Controller is a two-chip MOS/LSI general purpose display controller system designed to interface with bargraph and segmented displays (gas discharge, vacuum-fluorescent or LED).

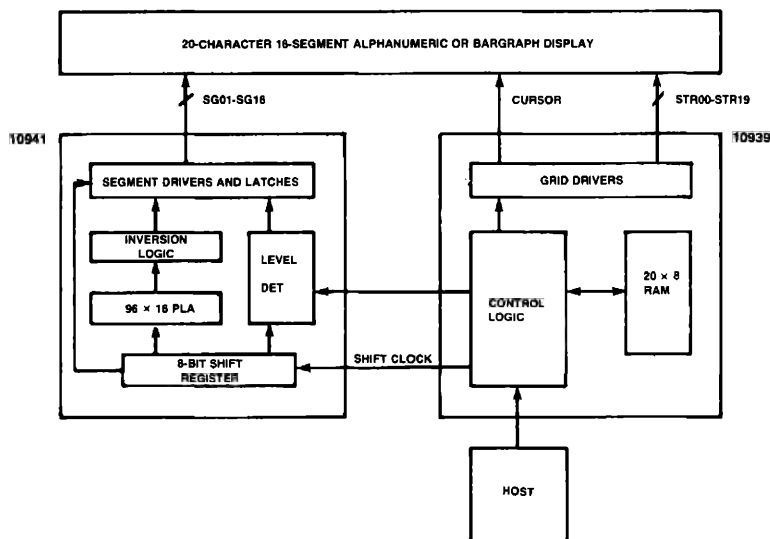
The two-chip set will drive up to 20 segments and up to 20 grids (characters) plus a cursor. The chips can be cascaded to drive larger displays of 80 characters or more. Segment decoding for ASCII characters or the bargraph patterns is accomplished through an internal PLA.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
10941P	Plastic	0°C to +70°C
10941PE	Plastic	-40°C to +85°C
10939P	Plastic	0°C to +70°C
10939PE	Plastic	-40°C to +85°C

FEATURES

- 20-character display driver cascadable to 80 or more characters
- Direct drive capability for vacuum-fluorescent displays
- 96×16 PLA provides segment decoding for ASCII characters (all caps only) and bargraph patterns
- Serial or parallel data input for 8-bit display and control characters
- Brightness, refresh rate, and display mode controls
- Separate cursor driver output
- 10939 comes in 40-pin DIP
- 10941 comes in 24-pin DIP



Block Diagram of 10941 and 10939

INTERFACE DESCRIPTION

10941 Pin Functions

Signal Name	Pin No.	Function
V _{SS}	2	Power and signal ground
SG01-SG16	6-15, 17-22	Segment driver outputs
SCLK-DIS	23	Serial data shift
DATA-LOAD	24	Serial data output/latch control
V _{DD}	1	DC Power
V _{GG}	16	Pull down driver voltage

V _{DD}	1	24	DATA-LOAD
V _{SS}	2	23	SCLK-DIS
NOT USED	3	22	SG01
NOT USED	4	21	SG02
NOT USED	5	20	SG03
SG16	6	19	SG04
SG15	7	18	SG05
SG14	8	17	SG06
SG13	9	16	V _{GG}
SG12	10	15	SG07
SG11	11	14	SG08
SG10	12	13	SG09

10941 Pin Configuration

10939 Pin Functions

Signal Name	Pin No.	Function
V _{SS}	36	Power and signal ground
V _{DD}	37	DC Power
CLOCK	38	Synchronization Clock
CURSOR	14	Cursor drive output
MASTER	39	Master/Slave Mode control
SIP	3	Sync Input
SOP	2	Sync Output
D0-D7	6-13	Serial or parallel data input
LD	5	Input data strobe
POR	4	Power-on reset
SCLK-DIS	1	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
STR00-STR19	15-34	Anode Drive Outputs
V _{GG}	35	Pull down driver voltage

SCLK-DIS	1	40	DATA-LOAD
SOP	2	39	MASTER
SIP	3	38	CLOCK
POR	4	37	V _{DD}
LD	5	36	V _{SS}
D0	6	35	V _{GG}
D1	7	34	STR00
D2	8	33	STR01
D3	9	32	STR02
D4	10	31	STR03
D5	11	30	STR04
D6	12	29	STR05
D7	13	28	STR06
CURSOR	14	27	STR07
STR19	15	26	STR08
STR18	16	25	STR09
STR17	17	24	STR10
STR16	18	23	STR11
STR15	19	22	STR12
STR14	20	21	STR13

10939 Pin Configuration

SPECIFICATIONS

Maximum Ratings

Parameters	Notes	Symbol	Min	Typ	Max	Unit
Operating Temperature	1		0		+70	°C
Commercial		T _c	-40		+85	°C
Industrial		T _i	-55		+125	°C
Storage Temperature						
Operating Voltage	1	V _{DD}	-22	-20	-18	Volts
Operating Display Voltage	1	V _{GG}	-50		-30	Volts
Power Dissipation (total)	2					
I _{load} = 0 mA per driver		PDO		40	100	mW
I _{load} = 2 mA per driver		PDL		200	750	mW
Power Dissipation	3	PD		200	400	mW

NOTES: 1. Designates characteristics for both 10941 and 10939.

2. Designates characteristics for 10941.

3. Designates characteristics for 10939.

D.C. Characteristics

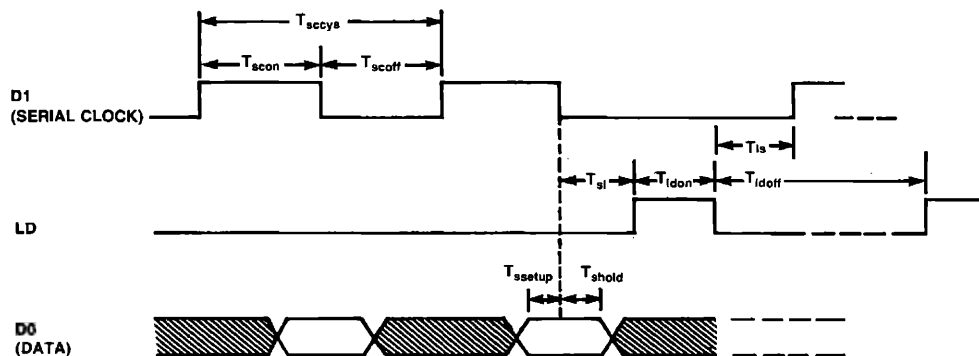
Parameter	Notes	Symbol	Min	Typ	Max	Unit
Input D0-D7, LD, SIP Logic "1" Logic "0"	3	V_{IH} V_{IL}	-1.2 V_{DD}		+0.3 -4.2	V V
Input POR Logic "1" Logic "0"	3	V_{IHPO} V_{ILPO}	-3.0 V_{DD}		+0.3 -10.0	V V
Output SOP Logic "1" Logic "0"	3	V_{OHsy} V_{OLsy}	-1.2 V_{DD}		+0.3 -4.2	V V
Output Digits, Cursor, and Segments Logic "1" ($I_{load} = 10\text{ mA}$) Logic "0" ($I_{load} = 0\text{ mA}$)	1	V_{OH} V_{OL}	-1.5 V_{GG}		.95 V_{GG}	V V
NOTES: 1. Designates characteristics for both 10941 and 10939. 2. Designates characteristics for 10941. 3. Designates characteristics for 10939.						

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
CLOCK Cycle Time Commercial Industrial	T_{cyc}	6.66 5.88		20.0 22.2	μs μs
Display Outputs (STR00-STR19 and CURSOR)	T_{stff} T_{sten}			7.5* 1.54*	μs μs
SERIAL INTERFACE TIMING					
Serial Clock (D1) On Time Off Time Cycle Time	T_{scon} T_{scoff} T_{scyc}	0.4 0.4 1.0		20.0	μs μs μs
Serial Data (D0) Set-up Time Hold Time	T_{ssetup} T_{shold}	400 400			ns ns
Serial Clock to LD Time	T_{sl}	600			ns
LD to Serial Clock	T_{ls}	400			ns
PARALLEL INTERFACE TIMING					
Parallel Data (D0-D7) Set-up Time Hold Time	T_{psetup} T_{phold}	0 200			ns ns
Data Load (LD) On Time Off Time	T_{ldon} T_{ldoff}	250			ns
Commercial Industrial Cycle Time	T_{ldcyc}	40.0 44.5			μs μs
Commercial Industrial		60.0 66.7			μs μs

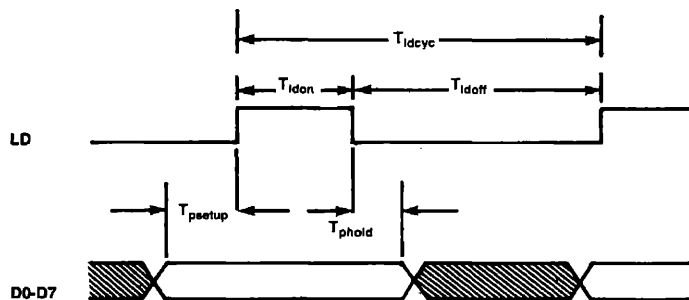
*40 pf. maximum load capacitance.

SERIAL INTERFACE TIMING WAVEFORMS



5

PARALLEL INTERFACE TIMING WAVEFORMS



FUNCTIONAL DESCRIPTION

Once the display buffer has been loaded from the host processor, the 10941/10939 system generates all timing signals required to control the display.

Input data is loaded into the Display Data Buffer via the Serial or Parallel Data Input channel on the 10939. Internal timing and control logic synchronize the digit output signals with the Serial Data and Load signals to the 10941 to provide the proper timing for the multiplexing operation. A 96×35 bit PLA is provided for decoding the full 96 character ASCII set.

Input data is loaded into the 10939 as a series of 8-bit words. If the Serial Mode is selected, Input Data lines D2-D7 should be tied down to V_{DD} externally. Raising any one of these lines to the V_{SS} level automatically shifts the 10939 into the Parallel Mode. Input data may be Control or Display data. The following paragraphs describe the format and functions of these control and display data words.

CONTROL DATA WORDS

Control data words are distinguished from Display Data words by the fact that they must be preceded by a Control Prefix word (0000 0001 or 01₁₆). Control words and their functions are defined in Table 1.

Table 1. Control Word Assignments

Hex Value	Function
00	Not used
01	Load 01 into Data Buffer
02	Not used
03	Not used
04	Not used
05	Set digit time to 16 cycles per grid
06	Set digit time to 32 cycles per grid
07	Set digit time to 64 cycles per grid
08	Enable Normal Display Mode (MSB in data words is ignored)
09	Enable Blank Mode (data words with MSB = 1 will be blanked)
0A	Enable Inverse Mode (data words with MSB = 1 will be "Inversed")
0B	Not used
0C	Not used
0D	Not used
0E	Start Display Refresh Cycle (use only once after reset)
0F	Not used
10-3F	Not used
40-7F	Load Duty Cycle Register with lower 6 bits (0-63)
80-9F	Load Digit Counter (80=32, 81=1, 82=2, etc.)
A0-BF	Not used
C0-DF	Load Buffer Pointer Register with lower 5 bits
E0-FF	Not used

Load Buffer Pointer

The Load Buffer Pointer code sets the Display Data Buffer pointer. The lower 5 bits of the code are loaded into the buffer pointer (see Table 2).

Table 2. Load Buffer Pointer Codes

Code Value	Pointer Value	Character Position
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15
D0	10	16
D1	11	17
D2	12	18
D3	13	19
D4	14	20
D5	15	21
D6	16	22
D7	17	23
D8	18	24
D9	19	25
DA	1A	26
DB	1B	27
DC	1C	28
DD	1D	29
DE	1E	30
DF	1F	31

NOTE: DO NOT USE CHARACTER POSITIONS 20-31.

Load Digit Counter

The Load Digit Counter defines the number of character positions (grids) to be controlled. This code is normally used only during initialization routines, but it may also be used in conjunction with the Load Duty Cycle control code to extend the range of brightness control (see Table 3).

Load Duty Cycle

The Load Duty Cycle code is used to turn the display on and off, to adjust display brightness, or to modify display timing. The time slot for each character is 16, 32, or 64 cycles as selected by the Load Digit Time codes (see Table 3). The segment and digit drivers for each character are on for a maximum of 13, 29, or 61 cycles with a 3.0 cycle inter-digit off-time. The lower 6 bits of the Load Duty Cycle code are loaded into the Duty Cycle Register. Resultant duty cycles are shown in Table 4.

Table 3. Load Digit Counter Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Load Digit Time

The Load Digit Time codes set the total time for each character during the refresh cycle. Three values can be set using the three codes shown in Table 1. The default value set at power-on is 64 cycles per grid. For displays with 40 or more characters, or under conditions where the display can be subjected to quick movements during viewing (e.g. portable or vehicle-mounted applications), it may be necessary to increase the refresh rate by selecting 16 or 32 cycles per grid with the appropriate control code.

Enable Display Mode

Each ASCII character is represented by the lower seven bits of the 8-bit value loaded into the 10939. The eighth (most significant) bit is ignored in Normal display mode. If either Blank or Inverse mode is selected, however, a "0" in this bit selects Normal display mode, while a "1" selects either Blank or Inverse mode, depending on which mode is enabled. Three control codes are provided (see Table 1) to enable blank mode, enable inverse mode, or enable normal mode.

Table 4. Duty Cycle Control Codes

Code	Digit Time=16		Digit Time=32		Digit Time=64	
	On	Off	On	Off	On	Off
40	—	16	—	32	—	64
41	—	16	—	32	—	64
42	—	16	—	32	—	64
43	1	15	1	31	1	63
44	2	14	2	30	2	62
45	3	13	3	29	3	61
46	4	12	4	28	4	60
47	5	11	5	27	5	59
48	6	10	6	26	6	58
49	7	9	7	25	7	57
4A	8	8	8	24	8	56
4B	9	7	9	23	9	55
4C	10	6	10	22	10	54
4D	11	5	11	21	11	53
4E	12	4	12	20	12	52
4F	13	3	13	19	13	51
50	13	3	14	18	14	50
51	13	3	15	17	15	49
52	13	3	16	16	16	48
.	"	"	17	15	17	47
.
.
.
5B	"	"	25	7	25	39
5C	"	"	26	6	26	38
5D	"	"	27	5	27	37
5E	"	"	28	4	28	36
5F	"	"	29	3	29	35
60	"	"	29	3	30	34
.	"	"	29	3	31	33
.	"	"	"	"	32	32
.
.
.
7C	"	"	"	"	58	6
7D	"	"	"	"	59	5
7E	"	"	"	"	60	4
7F	"	"	"	"	61	3

In the Blank mode, any character with the MSB="1" will be blanked. In the Inverse mode, it will be displayed with all segment driver outputs inverted. On video displays, this is referred to as "Inverse Video" format. These controls allow individual characters or groups of characters to be blinked or blanked by simply changing the mode without changing the data in the Display Buffer.

Start Refresh

At power on, the 10939 is held in an internal Halt mode. The normal display refresh sequence starts upon receipt of a Start Refresh control code. This is particularly useful for synchronizing systems using more than one 10939. Only the Master 10939 in a multi-chip system will recognize the Start Refresh code. The Master starts the Slave(s) at the appropriate time, using the SYNCO signal.

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit codes. The eighth (most significant) bit specifies normal (0) or blank/inverse (1) display mode, depending on the blank/inverse mode selection (see Control data words 09 and 0A in Table 1). Figure 1 shows the ASCII codes for the segment patterns for a bargraph display.

Twenty display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer automatically increments after each data word is stored in the buffer. To select the next character position to be loaded out of sequence, use the Load Buffer Pointer command. The Buffer Pointer will automatically reset to character position 0 when its value is equal to the Digit Counter programmed value.

POWER-ON RESET

The Power-On Reset (POR) initializes the internal circuits of the 10939. This is normally accomplished when power (V_{DD}) is applied. The following conditions are established by application of POR:

- The Grid Drivers (STR00-STR19) on the 10939 are in the off state.
- The Segment Drivers (SG01-SG16) on the 10941 are in the off state.
- The Duty Cycle is set to 0.
- The Digit Counter is set to 32.
- The Buffer Pointer is set to 0.
- The Digit time is set to 64.
- The Normal display mode is set.
- DATA-LOAD is set to high impedance state.
- SCLK-DIS is set to V_{OL} to disable the segment drivers in the 10941.
- SOP is set to V_{OL} to disable the sync pulse.

NOTES:

- When the POR signal is removed, SCLK-DIS is set to the high impedance state.
- During the initial rise time of V_{DD} at power turn-on, the magnitude of V_{GS} should not exceed the magnitude of V_{DD} .

DIGIT DRIVERS (STR00-STR19) PLUS CURSOR

The 20 Digit Drivers select each of the display character positions sequentially during a refresh scan. Display segments will be illuminated when both the Digit Drivers and Segment Drivers for a particular character are energized simultaneously. The Cursor segment is generated by the 10939, but its timing characteristics are identical to the 16 segments generated by the 10941.

SEGMENT DRIVERS (SG01-SG16)

Sixteen Segment Drivers are provided in the 10941. The output states for each ASCII character pattern and each bargraph pattern are internally decoded from the 8-bit characters received from the 10939 by means of a 96×16 -bit PLA. Data codes and the corresponding of the ASCII patterns are shown in Figure 1. Data codes and the corresponding bargraph patterns are shown in Figure 2.

MSD	100	101	110	111	000	001	010	011
LSB	100	101	110	111	000	001	010	011
000	SPACE	/	0	1	2	3	4	5
001	6	7	8	9	A	B	C	D
010	E	F	G	H	I	J	K	L
011	M	N	O	P	Q	R	S	T
100	U	V	W	X	Y	Z	DECIMAL POINT	TAIL
101	Blank	Blank	Blank	Blank	Blank	Blank	Blank	Blank
110	Blank	Blank	Blank	Blank	Blank	Blank	Blank	Blank
111	Blank	Blank	Blank	Blank	Blank	Blank	Blank	Blank

Figure 1. 10941 14-Segment Display Patterns

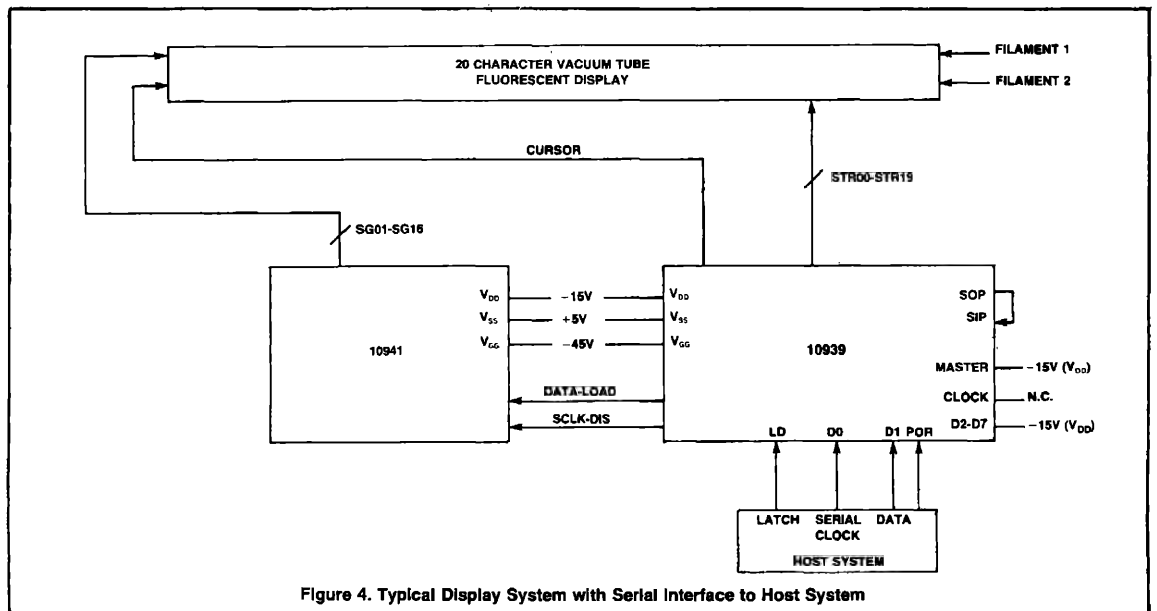
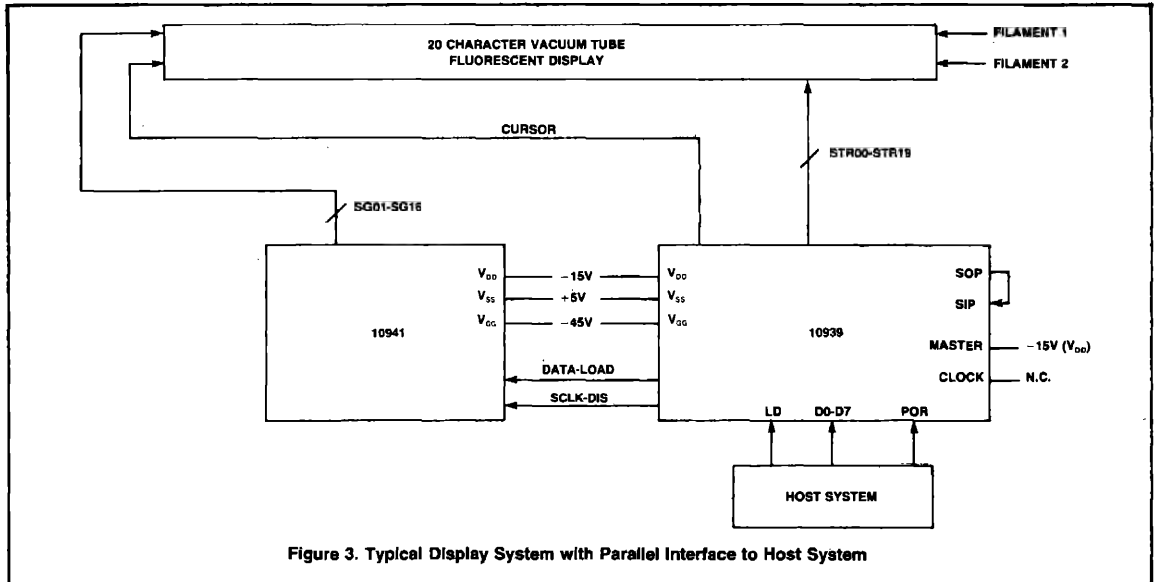
Input Code	Segment Patterns (1=On)
7 6 5 4 3 2 1 0	A B C D E F G H I J K L M N O P
0 1 1 0 0 0 0 0	1
0 1 1 0 0 0 0 1	1
0 1 1 0 0 0 1 0	1
0 1 1 0 0 0 1 1	1
0 1 1 0 0 1 0 0	1
0 1 1 0 0 1 0 1	1
0 1 1 0 0 1 1 0	1
0 1 1 0 0 1 1 1	1
0 1 1 0 1 0 0 0	1
0 1 1 0 1 0 0 1	1
0 1 1 0 1 0 1 0	1
0 1 1 0 1 0 1 1	1
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0 1 1 1 0 0 0 0	1
0 1 1 1 0 0 0 1	1
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0 1 1 1 0 1 1 1	1
0 1 1 1 1 0 0 0	1
0 1 1 1 1 0 0 1	1
0 1 1 1 1 0 1 0	1
0 1 1 1 1 0 1 1	1
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0 1 1 1 1 1 0 1	1
0 1 1 1 1 1 1 0	1
0 1 1 1 1 1 1 1	1

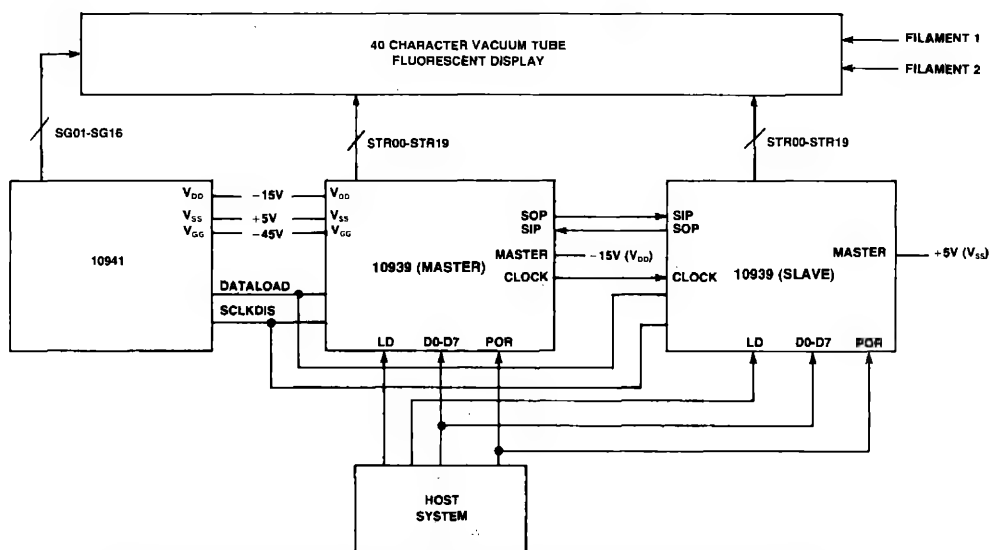
Figure 2. 10941 Bargraph PLA Codes

TYPICAL SYSTEM HOOKUPS

Figure 3 shows a 10941 and a 10939 in a parallel interface with the host system driving a 20 character display. Figure 4 shows a 10941 and a 10939 in a serial interface with the

host system driving a 20 character display. Figure 5 shows a 10941 and two 10939's interfaced parallel with the host system driving a 40 character display.







10951 BARGRAPH & NUMERIC DISPLAY CONTROLLER

Preliminary

DESCRIPTION

The Rockwell 10951 Bargraph & Numeric Display Controller (referred to as the 10951) is a LSI general purpose display controller designed to interface to segmented displays (gas discharge, vacuum fluorescent, or LED).

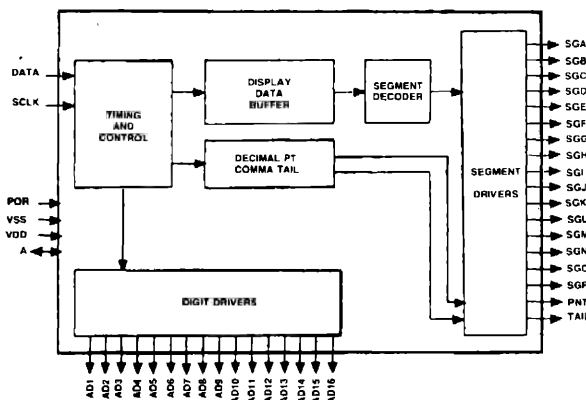
The 10951 will drive 16-segment bargraph or seven-segment plus comma and decimal numeric displays with up to 16 display positions. The controller accepts command and data input words on a clocked serial input line. Commands control the on/off duty cycle, starting character position and number of characters to display. Encoded data words display bargraph position (single segment or increasing bar length), numbers, comma, decimal and selected upper and lower case letters. No external drive circuitry is required for displays that operate on 10 ma of drive current up to 40 volts. A 64 × 16-bit segment decoder provides internal ASCII character set decoding for the display.

ORDERING INFORMATION

Part Number	Package Type	Drive Voltage	Temperature Range
10951P-50	Plastic	50V	0°C to +70°C
10951PE-50	Plastic	50V	-40°C to +85°C

FEATURES

- 16 segment drivers plus decimal point and comma tail drivers
- 16 digit drivers
- Average data rate: 66 kHz
- Single character burst rate: 500 kHz
- TTL compatible
- Direct digit drive of 10 ma for 30, 35, and 40 volt displays
- Supports gas-discharge, vacuum fluorescent, or LED displays
- Serial data input for 8-bit display and control data words
- 64 × 16-bit PLA provides data decoding driving
 - Any 1 of 16 bargraph segments
 - 1 to 16 bargraph segments
 - Ten seven-segment numeric characters (0-9)
 - Comma and decimal
 - Eight upper and lower case seven-segment characters
- Command functions
 - On/off duty cycle
 - Character position
 - Number of characters
- 40-Pin DIP



10951 Block Diagram

INTERFACE DESCRIPTION

10951 Pin Functions

Signal Name	Pin No.	Function
VSS	1	Power and signal ground
AD16-AD1	2-17	Digits 16 through 1 driver outputs
VDD	18	DC power connection
A	19	A clock used only for device testing
POR	20	Power-on reset input
DATA	21	Serial data input
SCLK	22	Serial data clock input
SGA-SGP	23-38	Segments A through P driver outputs
TAIL	39	Comma tail driver output
PNT	40	Decimal point driver output

SPECIFICATIONS

Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	+0.3		-20	V
Power Dissipation	P_D		40	100	mW
Input Voltage	V_{IN}	+0.3		-20	V
Output Voltage	V_{OUT}	+0.3		-40	V
Operating Temperature					
Commercial	T_C	0		+70	°C
Industrial	T_I	-40		+85	°C
Storage Temperature	T_{STG}	-55		+125	°C
Input Capacitance	C_{IN}			5	pf
Output Capacitance	C_{OUT}			10	pf

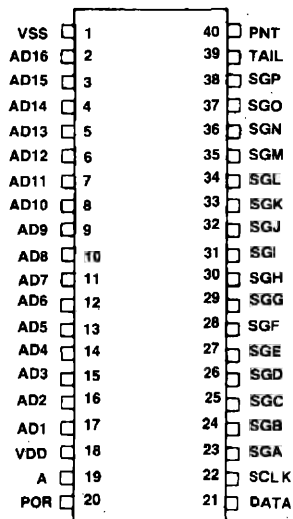
DC Characteristics

Parameter	Limits ($V_{SS} = 0$)			Limits ($V_{SS} = +5V$)			Conditions	Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.		
Supply Voltage (V_{DD})	-16.5	-15.0	-13.5	-11.5	-10.0	-8.5		V
Input DATA, SCLK, Logic "1"	-1.0		+0.3	+4.0		+5.3		V
Logic "0"	V_{DD}		-4.2	V_{DD}		+0.8		V
Input POR Logic "1"	-3.0		+0.3	+2.0		+5.3		
Logic "0"	V_{DD}		-10.0	V_{DD}		-5.0		
Output Digit and Segment Strobes Driver On								
Commercial			-1.5			+3.5	At 10mA Actual value determined by external circuit	V
Industrial			-1.7			+3.3		V
Driver Off 10951-50			-50			-45		V
Output Leakage			10			10	Per driver at driver off	μA
Input Leakage			10			10		μA

NOTES: All outputs require Pulldown Resistors.

AC Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Clock (1 Bit Time)	T_{cyc}				
Commercial		6.67	10.0	20.0	μs
Industrial		5.88	10.0	22.2	μs
Segment or Digit Strobe Output	T_{out}	200			ns
SCLK Clock					
On Time	T_{on}	1.0		20.0	μs
Off Time	T_{off}	1.0			μs
Data Input Sample Time					
Before SCLK Clock Off	T_{boff}	200			ns
After SCLK Clock Off	T_{aoff}	100			ns

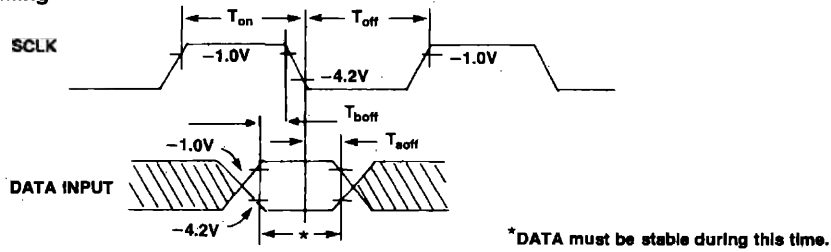


10951 Pin Configuration

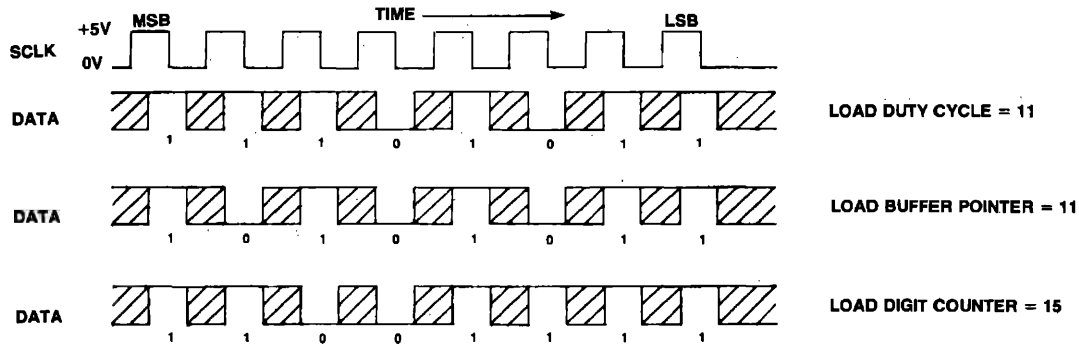
This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated to this circuit.

All voltages are specified relative to V_{SS} .

SCLK and Serial Data Timing

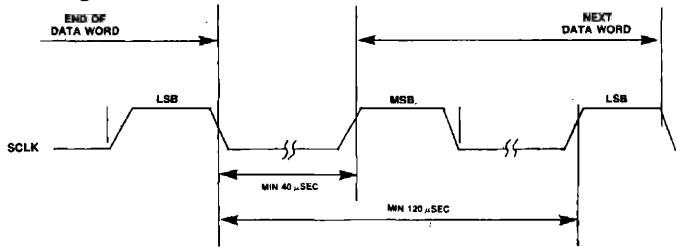


SCLK and Serial Data (Control Word) Examples

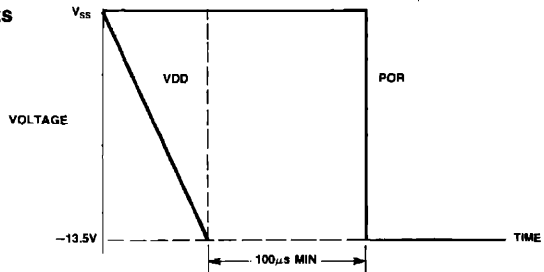


NOTE: Crosshatch = don't care

Data Word LSB/MSB Timing



Power-On Reset Voltage Limits



NOTE: V_{SS} referenced to 0V

FUNCTIONAL DESCRIPTION

The 10951 receives commands and data on a serial input line clocked externally by a separate clock input line. The controller decodes the commands from control data words, decodes the data words in accordance with an internal 64×16-bit programmable logic array (PLA) and turns on and off segment and digit output drivers. The segment output patterns are controlled by the decoded data words while the digit output and segment output timing are controlled by the decoded control words. All timing signals required to control the display are generated in the 10951 device without any refresh input from the host processor.

Input data is loaded into the Display Data Buffer via the Serial Data Input (Data) channel. Internal timing and control blocks synchronize the segment and digit output signals to provide the proper timing for the multiplexing operation. The 16×64 PLA decodes 8-bit data words to drive the 16 segment, comma and decimal point drivers. The decoded data words will drive 16 segments to display bargraph patterns (single segment and multiple segment for increasing length displays) or seven-segment patterns to display numbers, selected upper and lower case letters, comma and decimal point.

Input data is loaded into the 10951 as a series of 8-bit words with the most significant bit (MSB), bit 7. If bit 7 of any word loaded is a logical 1 (this bit is referred to as the control bit C), the loaded word is a control data word. If the C bit of any word is a logical 0, the loaded word is a display data word. The following paragraphs describe the format and functions of these control and display data words.

INPUT CONTROL DATA WORDS

When the C-Bit (bit 7) of the 8-bit input word is a logical 1, bits 5 and 6 are decoded into one of four control commands while data associated with the command are extracted from bits 0-4. There are three control codes which perform the following display functions:

- Load the Display Data Buffer pointer,
- Load the Digit Counter,
- Load the Duty Cycle register.

A fourth control code is defined but is not intended as a user function (see note associated with Table 1). Table 1 lists the control codes and their functions.

Load Buffer Pointer

The LOAD BUFFER POINTER code allows the Display Data Buffer pointer to be set to any digit position so that individual characters may be modified. The LOAD BUFFER PTR is loaded with a decimal equivalent value 2 less than the desired value (i.e., to point to character 6 of the display, a value of 4 is entered).

Load Digit Counter

The LOAD DIGIT COUNTER code is normally used only during initialization routines to define the number of character positions to be controlled. This code maximizes the duty cycle for any display. If 16 characters are to be controlled, enter a value of 0 (zero). Otherwise, enter the value desired.

Load Duty Cycle

The LOAD DUTY CYCLE code is used to turn the display on and off, to adjust display brightness, or to modify display timing for gas discharge displays. As shown in the block diagram, the time slot for each character is 32 clock cycles. The Segment and Digit Drivers for each character are on for a maximum of 31 cycles with a 1 cycle inter-digit off-time. The LOAD DUTY CYCLE code contains a 5-bit numeric field which modifies the on-time for segment Driver Outputs from 0 to 31 cycles. A duty cycle of 0 puts both the segment and digit drivers into the off state. Figure 1 shows the timing characteristics for the segment outputs.

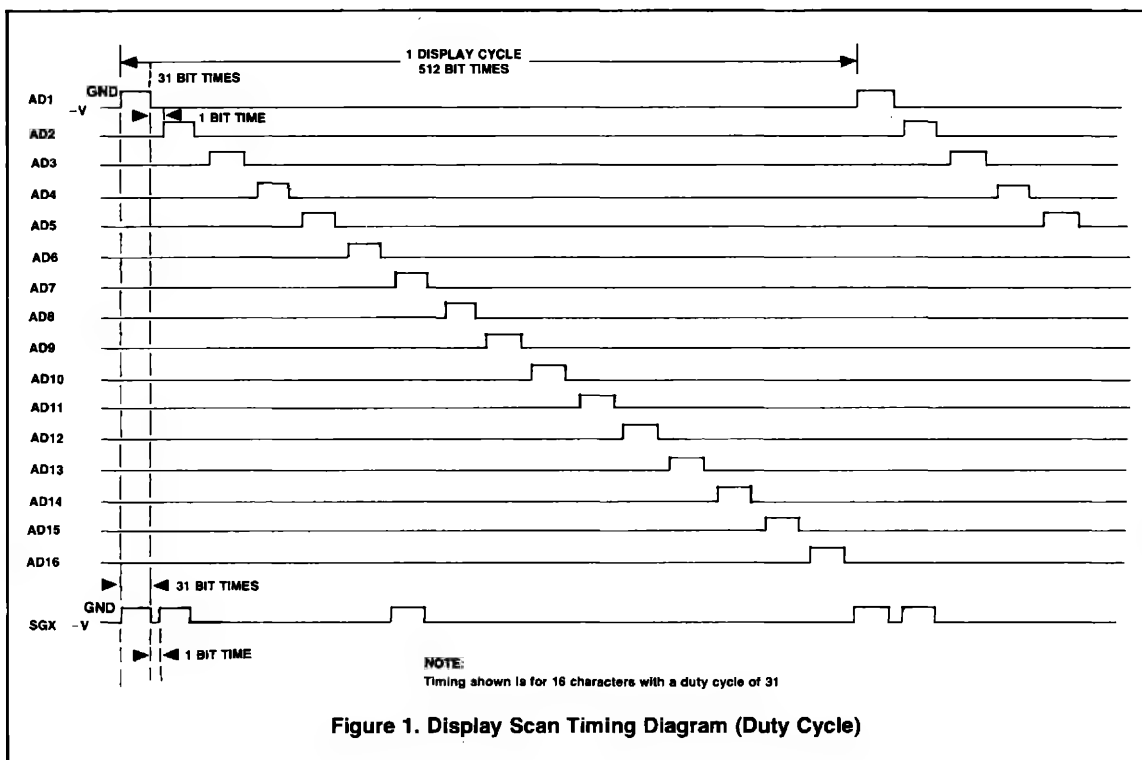
POWER-ON RESET (POR)

The Power-On Reset (POR) initializes the internal circuits of the 10951 when power (V_{DD}) is applied. The following conditions are established after a Power-On Reset:

- a. The Digit Drivers (AD1-AD16) are in the off state (floating).
- b. The Segment Drivers (SGA-SGP) are in the off state (floating). This includes PNT and TAIL.
- c. The cycle on-time for the LOAD DUTY CYCLE is set to 0 cycles.
- d. The LOAD DIGIT COUNTER is set to 16 (a bit code value of 0).
- e. The LOAD BUFFER POINTER is set to 15 to allow the first character to be entered into position 1.

Table 1. Control Data Words

8-Bit Control Word		Function
C-Bit	7-Bit Code	
1	010NNNN ⁽¹⁾	LOAD BUFFER POINTER (Position of character to be changed)
1	100NNNN ⁽¹⁾	LOAD DIGIT COUNTER (Number of characters to be output)
1	11NNNNN ⁽²⁾	LOAD DUTY CYCLE (On/off and brightness control)
1	00NNNNN ⁽³⁾	TEST MODE ONLY (Not a user function)
NOTE: 1. NNNN is a 4-bit binary value representing the digit number to be loaded. 2. NNNNN is a 5-bit binary value representing the number of clock cycles each digit is on.		3. This code is a device test function only. If executed it will lock the device in the test mode which can be removed only by performing a power-on reset.



INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit format codes. There are 64 codes available (with the C-bit set to 0 to indicate a display data word).

Sixteen display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer is automatically incremented before each data word is stored in the Display Buffer except for decimal point and comma words. The decimal point and comma words do not cause the Buffer Pointer to increment and thus are always associated with the previous character entered. To select the next character position to be loaded out of the normal sequence, use the LOAD BUFFER POINTER command before entering the display data word. It is not necessary to use the LOAD BUFFER POINTER command to cycle back to position 1 when less than 16 character positions are being used (DIGIT COUNTER \neq 0).

DIGIT DRIVERS (AD1-AD16)

The sixteen Digit Drivers (AD1-AD16) are used to select each of the display digits sequentially during a refresh scan. Display segments will be illuminated when both the Digit

Drivers and Segment Drivers for a particular character are energized simultaneously. The timing characteristics of both the digits and segments are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

SEGMENT DRIVERS (SGA-SGP)

Sixteen (16) Segment Drivers are provided (SGA-SGP), plus the decimal point (PNT) and comma tail (TAIL). The segment, PNT and TAIL outputs are internally decoded from the 8-bit characters in the Display Data Buffer by means of a 64×16 -bit PLA. The allocations for the 16-segment bargraph display and the seven-segment alphanumeric character plus comma and decimal point are shown in Figure 2. The input codes associated with seven-segment alphanumeric, comma and decimal point display are shown in Figure 3. The complete set of 8-bit codes for the bargraph and alphanumeric display is shown in Table 2. Note that only segment drivers SGA-SGG are used to drive the seven-segment characters. Segment drivers SGH-SGP may be used for other purposes as decoded in accordance with Table 2. Timing characteristics for the segment outputs are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

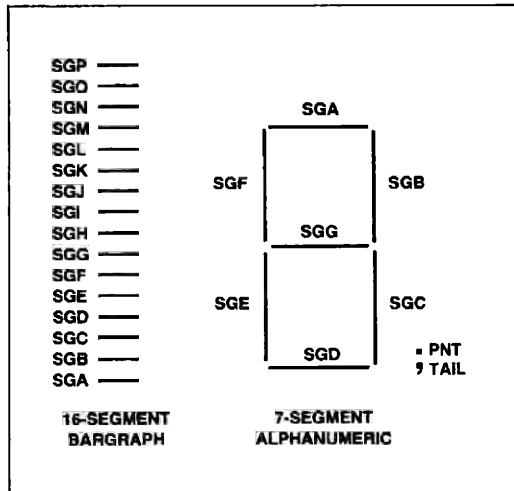


Figure 2. Segment Allocation

INPUT CODE (BITS 2-0)	INPUT CODE (BITS 7-3)			
	0X100	0X101	0X110	0X111
000	0	8	0	8
001	1	9	1	9
010	2	P	2	P
011	3	L	3	6
100	4	,	4	C
101	5		5	d
110	6	.	6	E
111	7		7	F

Figure 3. 7-Segment Patterns

Table 2. 10951 Data Codes

Input Code								Function	Segment Driver Output Patterns (1 = On)																		
7	6	5	4	3	2	1	0		SGA	SGB	SGC	SGD	SGE	SGF	SGG	SGH	SGI	SGJ	SGK	SQL	SGM	SGN	SGO	SGP	PNT	TAIL	
0	X	0	0	0	0	0	0	Segment A On	1																		
0	X	0	0	0	0	0	1	Segment B On		1																	
0	X	0	0	0	0	1	0	Segment C On			1																
0	X	0	0	0	0	1	1	Segment D On				1															
0	X	0	0	0	1	0	0	Segment E On					1														
0	X	0	0	0	1	0	1	Segment F On						1													
0	X	0	0	0	1	1	0	Segment G On							1												
0	X	0	0	0	1	1	1	Segment H On								1											
0	X	0	0	1	0	0	0	Segment I On									1										
0	X	0	0	1	0	0	1	Segment J On										1									
0	X	0	0	1	0	1	0	Segment K On											1								
0	X	0	0	1	0	1	1	Segment L On												1							
0	X	0	0	1	1	0	0	Segment M On													1						
0	X	0	0	1	1	0	1	Segment N On														1					
0	X	0	0	1	1	1	0	Segment O On															1				
0	X	0	0	1	1	1	1	Segment P On																1			
0	X	0	1	0	0	0	0	Segment A On	1																		
0	X	0	1	0	0	0	1	Segments A&B On	1	1																	
0	X	0	1	0	0	1	0	Segment A-C On	1	1	1																
0	X	0	1	0	0	1	1	Segment A-D On	1	1	1	1															
0	X	0	1	0	1	0	0	Segment A-E On	1	1	1	1	1														
0	X	0	1	0	1	0	1	Segment A-F On	1	1	1	1	1	1													
0	X	0	1	0	1	1	0	Segment A-G On	1	1	1	1	1	1	1												
0	X	0	1	0	1	1	1	Segment A-H On	1	1	1	1	1	1	1	1											
0	X	0	1	1	0	0	0	Segment A-I On	1	1	1	1	1	1	1	1	1										
0	X	0	1	1	0	0	1	Segment A-J On	1	1	1	1	1	1	1	1	1	1									
0	X	0	1	1	0	1	0	Segment A-K On	1	1	1	1	1	1	1	1	1	1	1								
0	X	0	1	1	0	1	1	Segment A-L On	1	1	1	1	1	1	1	1	1	1	1	1							
0	X	0	1	1	1	0	0	Segment A-M On	1	1	1	1	1	1	1	1	1	1	1	1	1						
0	X	0	1	1	1	0	1	Segment A-N On	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
0	X	0	1	1	1	1	0	Segment A-O On	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
0	X	1	1	1	1	1	1	Segment A-P On	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
0	X	1	0	0	0	0	0	Number 0	1	1	1	1	1	1			1	1	1	1	1						
0	X	1	0	0	0	0	1	Number 1		1	1					1	1	1	1	1	1						
0	X	1	0	0	0	1	0	Number 2	1	1		1	1		1		1	1	1	1	1	1					
0	X	1	0	0	0	1	1	Number 3	1	1	1	1			1		1	1	1	1	1	1	1				
0	X	1	0	0	1	0	0	Number 4		1	1			1	1		1	1	1	1	1	1	1				
0	X	1	0	0	1	0	1	Number 5	1		1	1		1	1		1	1	1	1	1	1	1				
0	X	1	0	0	1	1	0	Number 6	1		1	1	1	1	1		1	1	1	1	1	1	1				
0	X	1	0	0	1	1	1	Number 7	1	1	1					1	1	1	1	1	1	1	1				
0	X	1	0	1	0	0	0	Number 8	1	1	1	1	1	1	1	1				1	1	1	1				
0	X	1	0	1	0	0	1	Number 9	1	1	1	1	1	1	1	1				1	1	1	1				
0	X	1	0	1	0	1	0	Letter A	1	1			1	1	1					1	1	1	1				
0	X	1	0	1	0	1	1	Letter b			1	1	1	1	1					1	1	1	1				
0	X	1	0	1	1	0	0	Letter C	1				1	1	1					1	1	1	1				
0	X	1	0	1	1	0	1	Letter d		1		1	1		1					1	1	1	1				
0	X	1	0	1	1	1	0	Letter E	1			1		1	1					1	1	1	1				
0	X	1	0	1	1	1	1	Letter F	1				1	1	1					1	1	1	1				

<

Bargraph
Codes

5

Alphanumeric
and
Special
Codes

NOTES:

* Sets comma and decimal outputs for last character entered.

** Sets decimal output for last character entered.

TYPICAL SYSTEM HOOK-UP

Figure 4 shows the 10951 driven by a Host System as it would be connected to a V-F display. E_K is determined by the V-F display specifications and R_C is selected to provide proper biasing

current for zeners. Pull down resistors R_A and R_G are determined by the interconnection capacitance between the 10951 and the display.

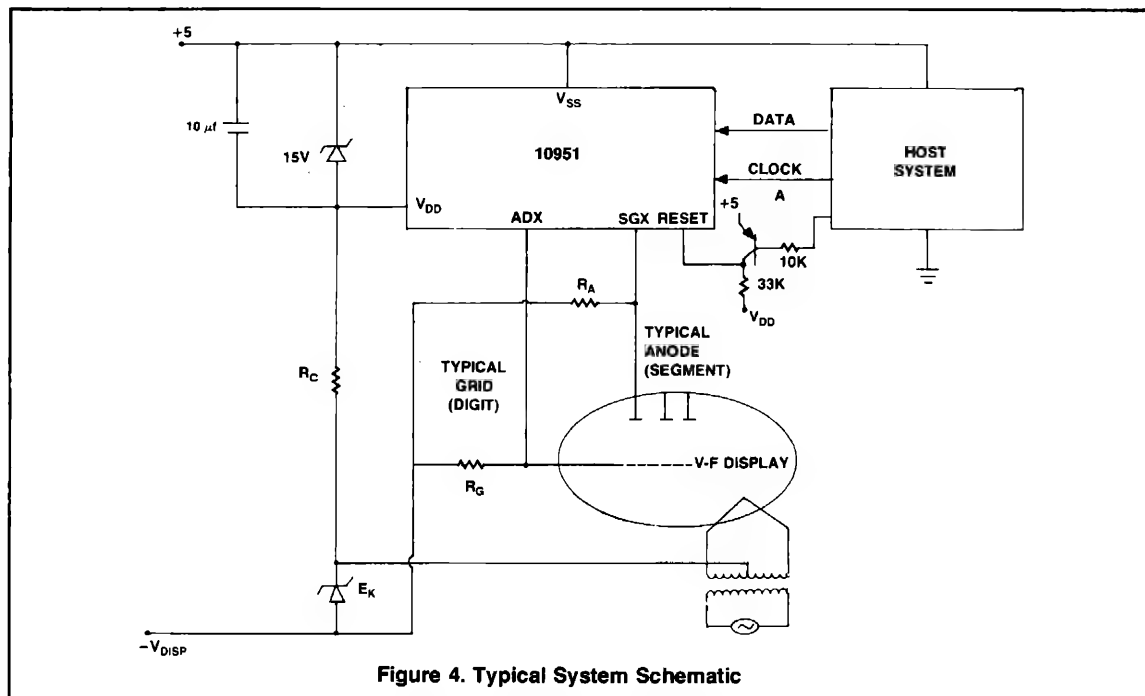


Figure 4. Typical System Schematic

SECTION 6

MICROCOMPUTER DEVELOPMENT SYSTEMS

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Product Family Overview	6-2
 Rockwell Design Center (RDC)	
RDC-1001 and RDC-1002 RDC System	6-3
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MICROCOMPUTER DEVELOPMENT SYSTEMS

Low Cost, Flexible Systems Work With Multiple μ Cs

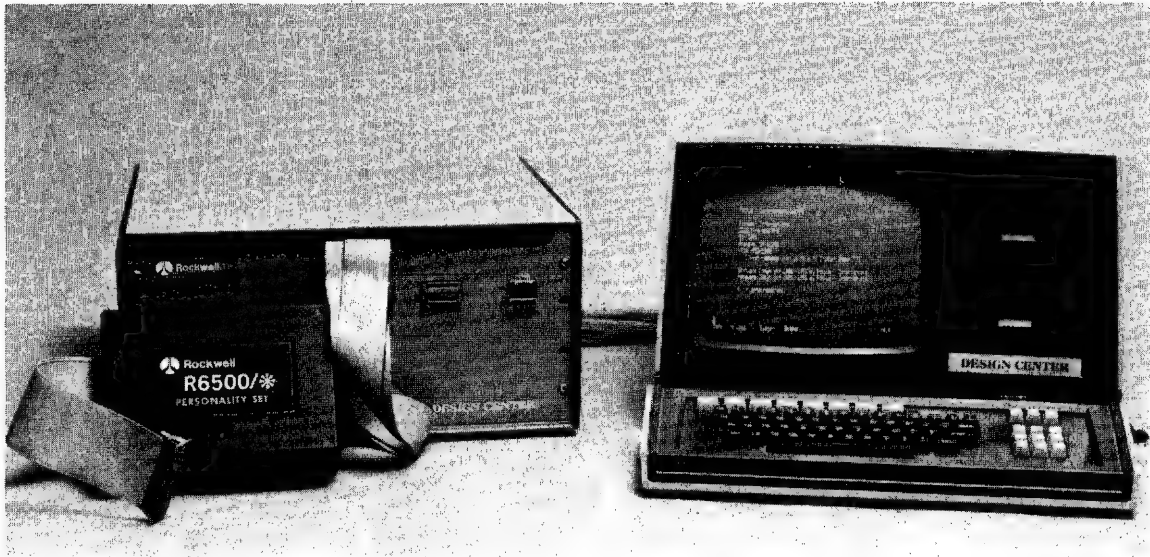
To support product development, Rockwell offers a range of microcomputer development systems, each extremely economical when compared on a cost/performance basis with competitive development systems.

The Rockwell AIM 65 microcomputer described in Section 7 functions as an extremely low cost, expandable, development system when used with the Rockwell Software Preparation System kit. The Rockwell Design Center (RDC) is an excellent, low cost, disk based development system, allowing concurrent development of up to four target R6500 and R6500/* systems.

The RDC is an easy to use, powerful development system for multi-chip and one-chip R6500 systems. A full line of support modules, macro assembler, link editor and high level PL/65 language are also available. R6500/* personality modules, additional RAM and a PROM programmer help add versatility.

The RDC supports the growing trend to using single-chip microcomputers as slaves with multi- or single-chip microprocessor systems. The advantages of slaves include both cost and technical savings, such as eliminating some complex timing relationships. With the RDC, up to four different microprocessor personality modules can be performing in-circuit-emulation under control of the system. The RDC mainframe is constructed modularly, using the proven RM Eurocard design, so it can be expanded readily, as needed. The terminal unit includes CRT, disk drives, and keyboard. Up to 1.28 Mbytes can be addressed on the two 96 TPI, double sided, double density, 5 1/4-inch disk drives.

The RDC allows designers to economically and efficiently develop multiple microcomputer systems, regardless of the microcomputer device involved. Personality sets and target RAM modules are available for all R6500 and R6500/* configurations.



Rockwell Design Center Development System



RDC-1001/2 ROCKWELL DESIGN CENTER (RDC)

INTRODUCTION

The Rockwell Design Center (RDC) is a development system vertically integrated to support the entire R6500 family of microprocessors and microcomputers. The RDC allows emulation, development, and software debugging of up to four separate microprocessors and microcomputers concurrently, even if the four devices are different members of the R6500 family. The RDC is a disk-based system with two 96 TPI, double-sided, double-density 5¼-inch floppy disk drives that provide a storage capacity of up to 1.3M bytes of data (formatted).

A unique bus structure provides a separate system bus and four target busses which can operate at different speeds (up to 4 MHz). Construction of the RDC is modular based on the proven RM 65 design using both single- and double-sized Eurocards and highly reliable DIN 41612 pin and socket connectors. The double Eurocards allow use of both the system bus and a target bus which can operate at different speeds.

Featuring Softkey function keys, the RDC eliminates the need for an operator to learn extra key strokes and command structures. A command line of operating modes is displayed across the bottom of the CRT screen so that the user need only push the corresponding function key to command the RDC to enter the mode of operation desired.

FEATURES

Hardware

- Modular construction based on proven RM 65 architecture
- Highly reliable, standard DIN 41612 pin and socket connectors
- Non-glare 12-inch CRT, green phosphor
- Detachable full ASCII intelligent keyboard
- Dual 96 TPI, double-sided, double-density 5¼-inch floppy disk drives
- Separate system bus and four independent target busses
- Two serial ports—one for RDC terminal interface—one for host system download
- Two parallel ports—one for RDC terminal interface—one for external printer
- 64K byte RAM system memory
- Internal self-test panel for system troubleshooting
- Three separate CPUs for keyboard, CRT, and system control
- Designed for built-in PROM programmer option

For users who already have an Intel ISIS II with mass storage program management, an R6500 cross-assembler is available. This allows the RDC to function as a satellite, providing a powerful debug system. The RDC is also capable of receiving files from the Rockwell SYSTEM 65 Microcomputer.

When used with the R6500/* Microcomputer or R6502-R65C02 Microprocessor Personality Sets, the RDC is a powerful emulation system for the complete family of Rockwell R6500/* one-chip microcomputers or NMOS R6502 and CMOS R65C02 families of microprocessors. The multiple target bus structure of the RDC allows the user to emulate four devices concurrently, and at different speeds.



Rockwell Design Center System

Functional

- Self-contained, disk-based operating system
- Softkey function access to menu-driven operational modes
- Text Editor
- R6500 Macro Assembler/Linking Leader
- SYSGEN configurable to user environment
- Automatic power-up initialization of system and configurations
- Separate system and target memory map
- 4 target simultaneous emulation
- Real-time in-circuit emulation, up to 4 MHz
- Five hardware breakpoints per target, 32-bits wide with "don't care" bits
- Inside or outside window breakpoint with 1 byte resolution
- Configurable as a satellite for an Intel ISIS II host system or Rockwell SYSTEM 65
- Self-test software

PRODUCT OVERVIEW

The RDC consists of three assemblies; the mainframe, a CRT terminal with floppy disk drives and a full ASCII keyboard. The mainframe contains the following components:

- The system bus and target/user busses
- Power supply and system cooling fans
- Two 32K Dynamic RAM modules for system memory
- Single Board Computer (SBC) module
- Floppy Disk Controller (FDC) module
- Asynchronous Communications Interface Adapter (ACIA) module with 2 channels for keyboard interface and user RS-232C
- Multi-function Peripheral Interface (MPI) module with two ports for interface to the CRT terminal and to a printer
- 24-pin and 28-pin PROM sockets for optional PROM Programmer module

The terminal assembly consists of a non-glare 12-inch, green phosphor CRT, a video display controller module, and two 5¼-inch floppy disk drives. The keyboard is intelligent for full ASCII operation.

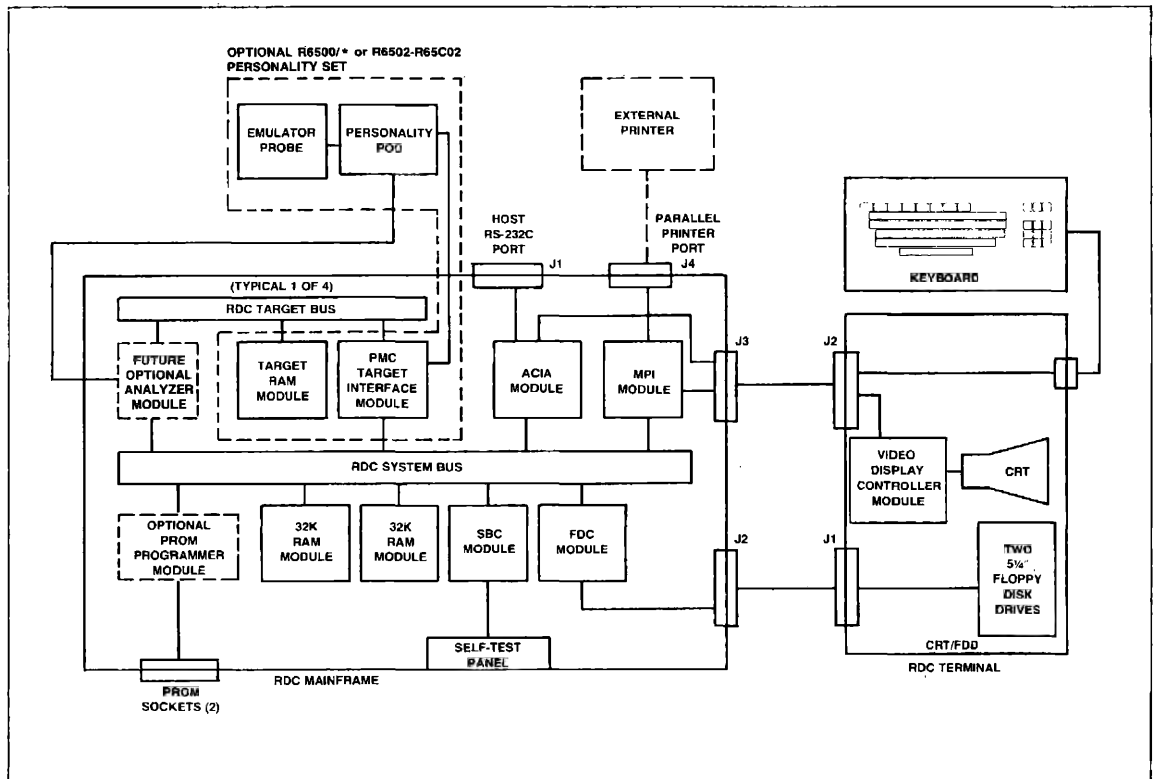
FUNCTIONAL DESCRIPTION

Major Components and Interfaces

The block diagram shows the architecture of the RDC system and identifies the relationship between the system bus and the target busses. Although the block diagram shows only one Target Interface, it represents the architecture of each of the four target busses. The terminal keyboard interfaces with the RDC system through one of the RS-232C ports (J3 connected to the ACIA module). The CRT interfaces with the RDC system through a parallel port (J3 connected to the MPI module). The disk drives interface to the RDC system through a separate port (J2 connected to the FDC module). All other control functions of the RDC system interface directly through the RDC system bus. Note that the Personality Set PMC module interfaces the RDC system bus to the target bus.

Bus Structure

The RDC system operates through a multiple bus structure—a system bus and four target busses. The system bus contains 21 card slots to accommodate single Eurocard modules or



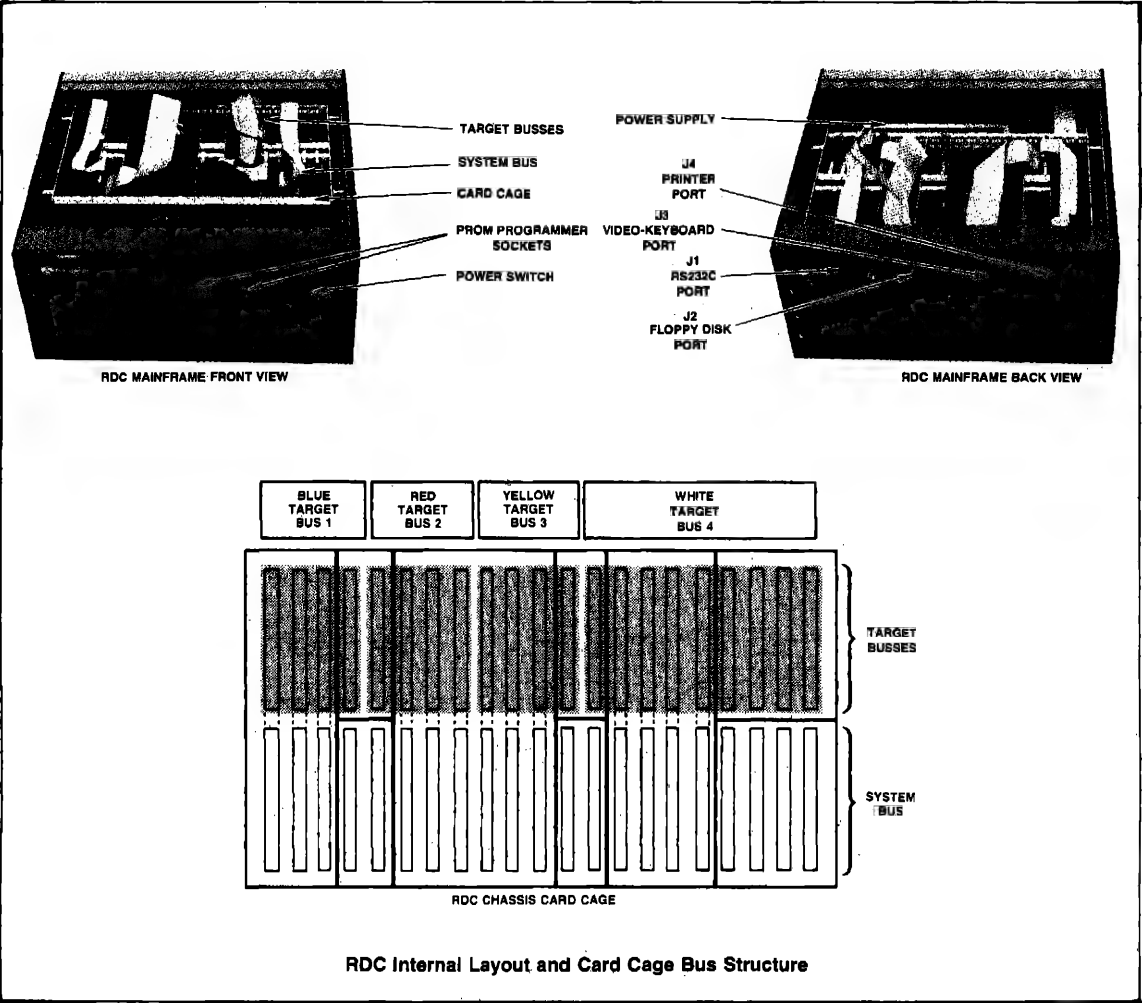
RDC System Block Diagram

double Eurocard modules. Double Eurocard modules plugged into the system bus are common to the system bus and the target bus. Double Eurocard modules (such as the R6500/* Personality Set PMC module) are used for microcomputer emulation support. Single Eurocard module connectors on the system bus are used to interface with RDC microcomputer system modules such as the 32K RAM(2), SBC, FDC, ACIA, and MPI.

The four target busses are segmented so that four separate emulations can be controlled by the system concurrently. Three of the target busses have four card slots each. Three of these slots will accept double Eurocard modules, and the fourth will accept a single Eurocard module. The double card slots are intended for a Personality Module Controller (PMC) module and future growth up to two Analyzer modules. The single card slot is

intended for plugging in a target (emulation) RAM module (8K × 8 or 64K × 8 depending upon the microcomputer to be emulated). These three target busses are color coded (blue, red, and yellow) on the RDC card cage for easy identification of the division of the target bus segments. The fourth target bus consists of nine Euroconnectors, four of which will accept double Eurocard modules and five of which will accept single Eurocard modules.

A typical single target emulation configuration will consist of an R6500/* or R6502-R65C02 Personality Set (comprising a PMC module, Personality Pod, and Emulator Interface) and a target RAM module, as a minimum. Since up to four fully configured emulation systems can be supported concurrently, the RDC could be configured with any combination of four R6500/* or R6502-R65C02 Personality Sets, and four target RAM modules in addition to the RDC system control modules.



Operating Modes

The RDC bootstrap ROM is initiated whenever the system is powered-up. The bootstrap program then loads the SYSGEN data and system program from the system disk drive. When the bootstrap is completed the CRT displays a Softkey menu for the function keys on the keyboard. It is this menu that prompts the user to select the mode of operation required. The Softkey prompts displayed at this time are:

SATELLITE LOCAL SYSGEN HELP

These Softkey prompts represent the primary modes of operation for the RDC system. When the function key corresponding to the CRT prompt location is pressed, one of the following modes is selected:

SATELLITE—This mode provides the menus available for interfacing the RDC as a satellite to the host system (Intel ISIS II)

LOCAL —This mode provides the menus available to the user from within the RDC without requiring host resources.

SYSGEN —This mode allows the user to modify the diskette-stored system parameters on either a permanent (until another power-up condition) or a temporary basis.

HELP —This mode displays information which briefly describes the operational mode options available in SATELLITE, LOCAL and SYSGEN modes. All Softkey menus include a HELP which is always located on the CRT screen directly over the far right hand function key on the keyboard.

Each Softkey prompt, when selected by the function key, invokes a new set of Softkey prompts which further define the tasks to be performed by the mode. As an example, if the LOCAL prompt is selected, a new Softkey prompt menu displays:

UTILITY, DEBUG HELP

If UTILITY is selected from this prompt, a new menu displays:

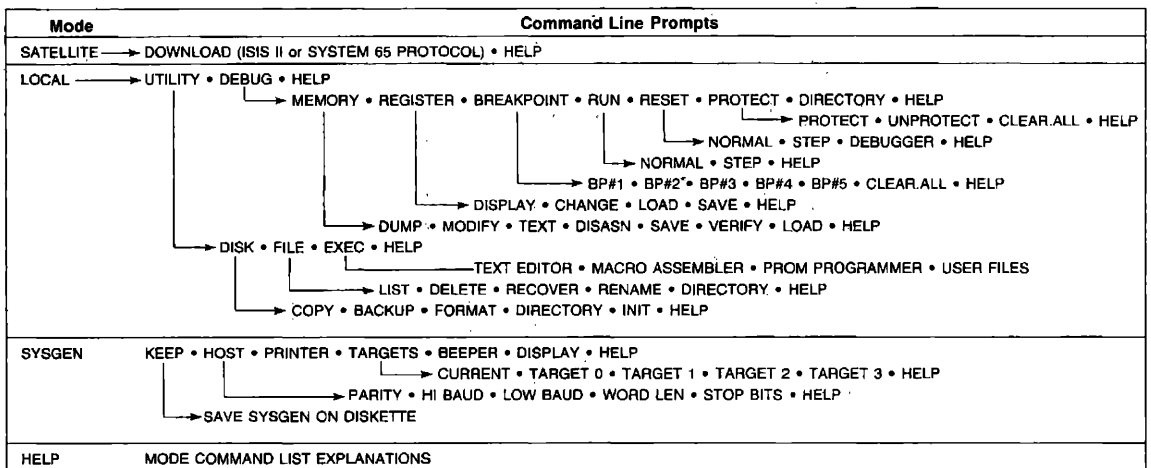
DISK FILE EXEC HELP

Selecting DISK invokes a new menu which asks:

COPY BACKUP FORMAT DIR INIT HELP

This hierarchy continues until all parameters of the tasks of the mode selected have been established. At any time during the mode selection process the user has the option of calling back the previous set of Softkey menu prompts by simply pushing the – (minus) key.

The illustration shows the depth to which the command line prompts guide the user through selecting the desired mode of operation.

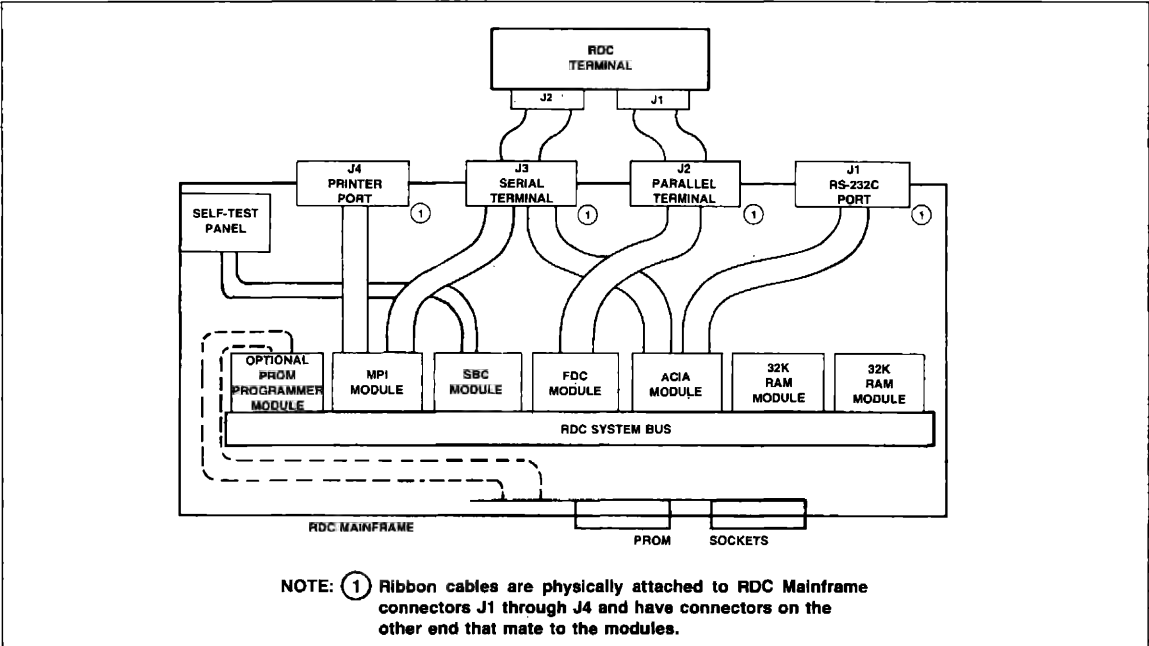


Command Line Hierarchy (Typical)

INTERFACE

Interface between the RDC system control modules and the port connectors on the back panel are made through ribbon cables. The ribbon cables are permanently attached to the port connectors. The terminal interfaces to the RDC system through two cables with mating connectors on each end that are keyed for proper installation. The RDC Cable Interface figure shows how

these cables are routed in the system. The Self-Test Panel interface ribbon cable is attached to the test panel and has a connector on the other end that mates to the SBC module I/O connector. The optional PROM programmer module connects to the two PROM sockets through a single ribbon cable.



RDC Mainframe Internal/External Ribbon Cable Connections

SPECIFICATIONS

Parameter	RDC Mainframe	RDC Terminal	
		CRT/FDD	Keyboard
Dimensions			
Height	11 in. (27.94 cm)	14 in. (35.56 cm)	3 in. (7.62 cm)
Width	20 in. (50.80 cm)	20 in. (50.80 cm)	20 in. (50.80 cm)
Depth	18 in. (45.72 cm)	16 in. (40.64 cm)	8 in. (20.32 cm)
Weight	40 lbs. (18 Kg)	42 lbs. (19 Kg)	6 lbs. (2.7 Kg)
Electrical			
AC Input Voltage	105 to 125 (RDC-1001) 210 to 250 (RDC-1002)	105 to 125 (RDC-1001) 210 to 250 (RDC-1002)	
AC Frequency	47 to 63 Hz	47 to 63 Hz	
Fuse Requirement	3 A slo-blo (RDC-1001) 1.5 A slo-blo (RDC-1002)	3 A slo-blo (RDC-1001) 1.5 A slo-blo (RDC-1002)	
Environmental			
Temperature	59°F to 104°F (15°C to 40°C) operating		
With/Disk Media	- 4°F to 140°F (- 20°C to 60°C) shipping		
	- 4°F to 122°F (- 20°C to 50°C) storage		
Humidity	20% to 80% non-condensing operating*		
	1% to 95% non-condensing shipping		
	1% to 95% non-condensing storage		
NOTE: *Disk media maximum wet bulb temperature 84.9°F (29.4°C)			

NOTE: *Disk media maximum wet bulb temperature 84.9°F (29.4°C)

ORDERING INFORMATION

Part Number	Description
RDC-1001	RDC System (100 Vac) ⁽¹⁾
RDC-1002	RDC System (220 Vac) ⁽¹⁾
RDC-1010	32K System RAM Module
RDC-1011	8K Target RAM Module
RDC-1012	64K Target RAM Module
RDC-1030	PROM Programmer Module
RDC-2000	R6500 Cross Assembler for Intel i8080 II
Order Number ⁽²⁾	Document Title
RDC06	RDC R6500/* Personality Set Data Sheet
RDC11	RDC R6502-R65C02 Personality Set Data Sheet
RDC12	RDC PROM Programmer Data Sheet
RM08	ACIA Module Data Sheet
RM10	SBC Module Data Sheet
RM15	FDC Module Data Sheet
RM24	MPI Module Data Sheet
RM11	32K Dynamic RAM Module Data Sheet
Notes:	
(1) Both system configurations are shipped with the following components:	
<ul style="list-style-type: none"> • RDC Mainframe • RDC Terminal with 12" CRT and Dual 5¼" Floppy Disk Drives and detached Keyboard • Six System Control modules—ACIA, FDC, SBC, MPI, and two 32K DRAM • All Required Interface Cables • Software Package (Utilities, Text Editor, Macro Assembler) • Documentation Package 	
(2) Documents provide further information about the RDC system.	

PERSONALITY SETS

Personality Sets are available for the RDC that allow emulation, development, and software debugging of the complete family of R6500/* Microcomputers and R6502-R65C02 Microprocessors. The microcomputers and microprocessors supported by these Personality Sets are:

- | | | | |
|-------------|-------------|-------------|----------|
| • R6500/11P | • R6500/13P | • R6500/42P | • R6511Q |
| • R6500/12P | • R6500/41P | • R6500/43P | • R65C02 |
| • R6541Q | • R6501Q | • R6502 | • R6503 |
| • R65C102 | • R65C112 | • R6506 | • R6507 |
| • R6504 | • R6505 | • R6514 | • R6515 |
| • R6512 | • R6513 | • R6500/1P | |

For complete information on ordering any particular Personality Set or groups of Personality Sets, refer to the RDC R6500/* Personality Set Data Sheet, Order Number RDC06, or RDC R6502-R65C02 Personality Set Data Sheet, Order Number RDC11.



RDC-1XX AND RDC-3XX ROCKWELL DESIGN CENTER R6500/* PERSONALITY SET

INTRODUCTION

The RDC R6500/* Personality Set is a Rockwell Design Center (RDC) option that allows the RDC user to develop, debug and verify programs intended for use by any R6500 one-chip microcomputer system. The R6500/* offers the user a high performance development system specifically designed for emulation of a microcomputer system. This RDC option supports in-circuit emulation for the entire R6500 family of one-chip microcomputers.

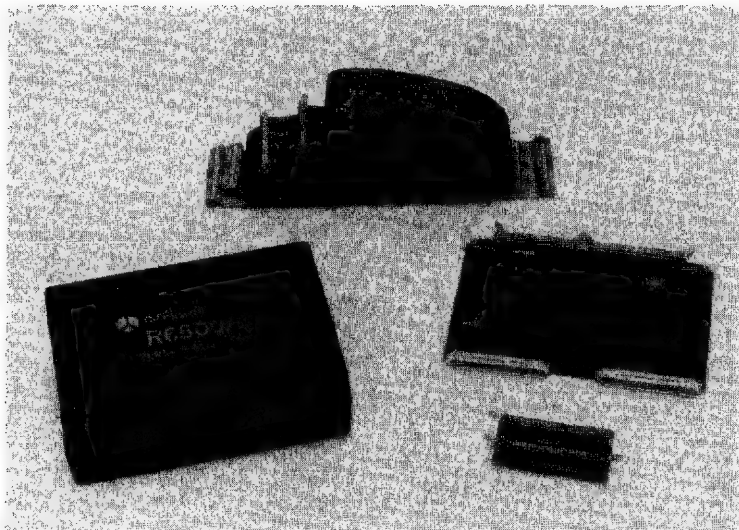
The basic R6500/* Personality Set includes a Personality Module Controller (PMC), two Personality Emulator Pod Modules, a Device Adapter, an In-Circuit Emulation Probe assembly, an interconnect cable set, and the required software and support documentation.

The R6500/* Personality Set provides the RDC with a dual CPU capability. This added feature permits the RDC CPU to maintain control, even while the R6500/* is executing a program, thus providing the user with complete control over the development process.

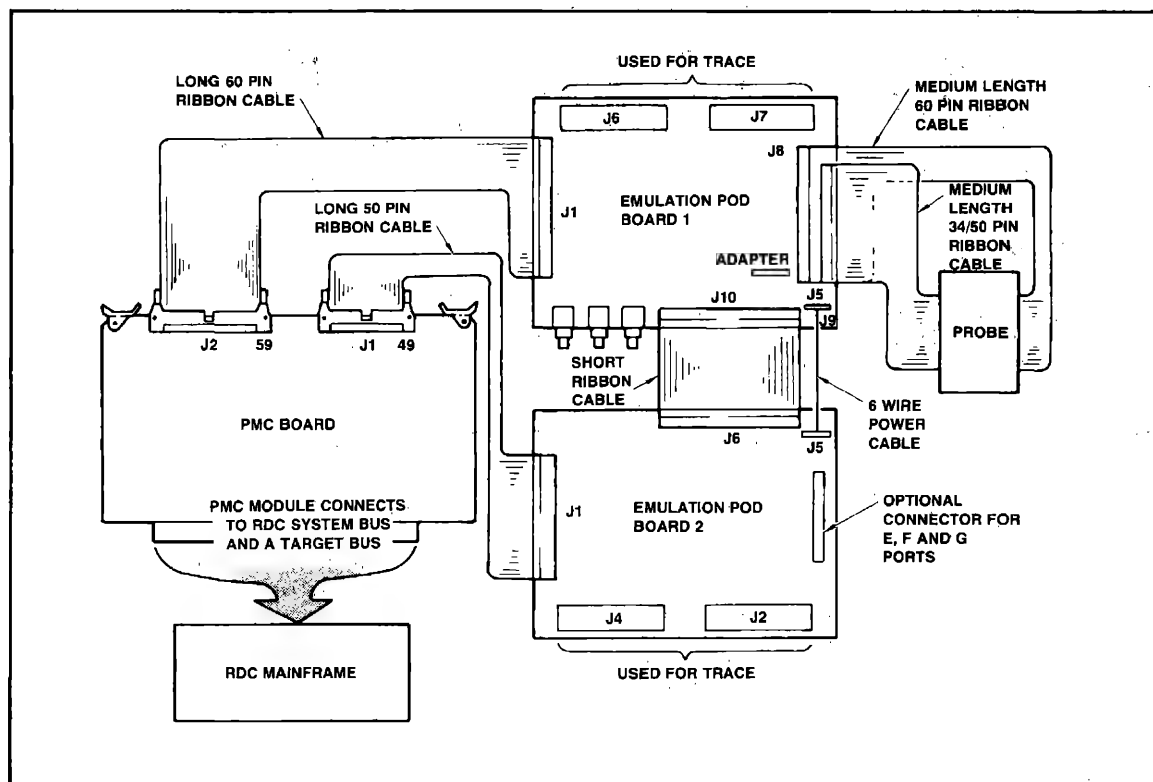
The R6500/* Personality Set can be expanded to include four separate emulation systems which can be run concurrently on the RDC.

FEATURES

- Disk based macro assembler and debug monitor
- Provides 8K RAM in system (optional)
- Supports 65K address range in target environment
- Five hardware breakpoints with SYNC outputs
- User defined external break signal
- Single step through interrupts
- Supports four simultaneous target developments
- No zero page address conflicts
- Power down capability
- RAM write protection
- User or system supplied power and clock
- Real-time in-circuit emulation
- Menu-driven Softkey command selection



RDC R6500/* Personality Set



System Interconnection

RUN MODE/CONTROLLED EXECUTION COMMAND SUMMARY

The R6500/* Personality Set is designed to allow the R6500/* to execute independent of the RDC. Thus, while the R6500/* is executing code, the RDC CPU is still in operation. This allows certain functions to be performed by the RDC CPU without disturbing the execution of the R6500/*.

RUN MODE COMMANDS

The R6500/* debug monitor allows certain commands to be performed while the R6500/* is in the Run mode. The Run Mode commands are highlighted as follows:

Description
RUN MODE COMMANDS
Issue Reset
Examine or Modify Hardware Breakpoint
Exit Run Mode
Return to RDC Operating System
Select a New PMC Module
Enable/Disable the System Pointer
Halt/Resume Run

CONTROLLED EXECUTION MODE COMMANDS

The Controlled Execution Mode commands are divided into five groups, as follows:

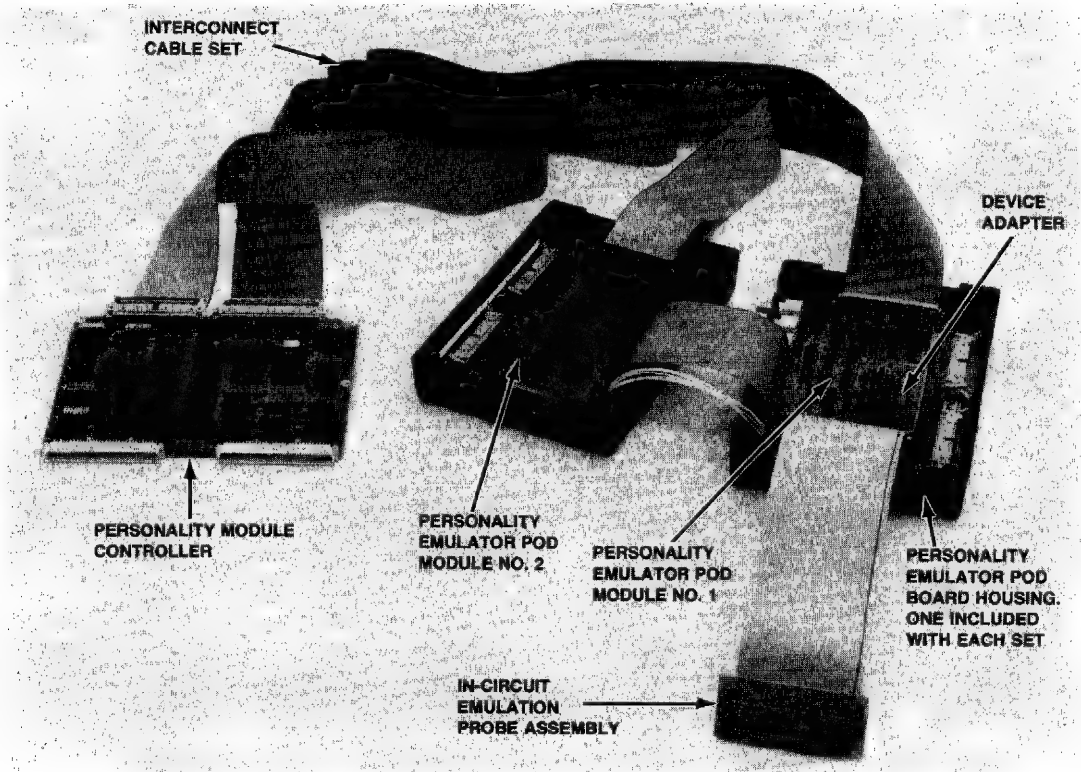
Description
COMMANDS TO DISPLAY MEMORY OR REGISTERS
Display or alter sixteen selected memory locations
Display or alter next sixteen memory locations
Display or alter previous sixteen memory locations
Examine/modify RAM and I/O one byte at a time
Dump memory in Hex and ASCII format
Invoke disassembler
Display or alter register contents
COMMANDS TO SET PROGRAM BREAKPOINTS
Set or reset software breakpoint addresses
Enable or disable single step mode
Set or modify hardware breakpoint

Description
COMMANDS TO TRACE PROGRAM FLOW
Toggle instruction trace on or off
Toggle register printout on or off
Show register form for printout
Show last nine instruction addresses
DISK FUNCTIONS
Special disk functions
Display disk directory
Delete file
MISCELLANEOUS COMMANDS
Write protect memory blocks
Load object code
Start execution of user's program
Dump memory
Issue RESET
Verify object code against memory
Return control to RDC Operating System
Initialize the current board
Enable/disable printer
Allow single step through interrupts

CONFIGURATIONS

The RDC Personality Sets for the R6500/* Microcomputers, shown in the chart below, include one Personality Module Controller (PMC), two Personality Emulator Pod Modules, a Device Adapter, an In-Circuit Emulation Probe assembly, an interconnect cable set, and the required software and support documentation. The RDC Personality Sets are available either bundled with an 8K Target RAM (the 100 series part numbers in the table below) or unbundled without the 8K Target RAM (the 300 series part numbers below)...

R6500/* Personality Sets	
Part Number	Description
RDC-101 or -301	R6500/11P Personality Set, 1 MHz
RDC-102 or -302	R6500/11AP Personality Set, 2 MHz
RDC-111 or -311	R6500/12Q Personality Set, 1 MHz
RDC-112 or -312	R6500/12AQ Personality Set, 2 MHz
RDC-121 or -321	R6500/13Q Personality Set, 1 MHz
RDC-122 or -322	R6500/13AQ Personality Set, 2 MHz
RDC-131 or -331	R6500/41P Personality Set, 1 MHz
RDC-132 or -332	R6500/41AP Personality Set, 2 MHz
RDC-141 or -341	R6500/42Q Personality Set, 1 MHz
RDC-142 or -342	R6500/42AQ Personality Set, 2 MHz
RDC-151 or -351	R6500/43Q Personality Set, 1 MHz
RDC-152 or -352	R6500/43AQ Personality Set, 2 MHz
RDC-161 or -361	R6500/1P Personality Set, 1 MHz
RDC-162 or -362	R6500/1AP Personality Set, 2 MHz



DEVICE ADAPTERS

The Adapter/Emulator Devices are used to reconfigure RDC-1XX Personality Sets for use with other R6500/* Microcomputers. They replace the Adapter/Emulator Devices in the Personality Emulator Pod Module and contain the desired emulator device.

Part Number	Description
RDC-211	Adapter/Emulator Device (R6511Q) for R6500/11/12/13, 1 MHz
RDC-212	Adapter/Emulator Device (R6511AQ) for R6500/11/12/13, 2 MHz
RDC-221	Adapter/Emulator Device (R6541AQ) for R6500/41/42/43, 1 MHz
RDC-222	Adapter/Emulator Device (R6541AQ) for R6500/41/42/43, 2 MHz
RDC-231	Adapter/Emulator Device (R6500/1EC) for R6500/1, 1 MHz
RDC-232	Adapter/Emulator Device (R6500/1EAC) for R6500/1, 2 MHz

IN-CIRCUIT EMULATION PROBES

The In-Circuit Emulation Probe assemblies used to reconfigure the RDC-1XX Personality Sets for use with other R6500/* Microcomputers are shown in the chart below.

Part Number	Description
RDC-200	40-Pin Probe and cable for R6500/11P. Prerequisite, RDC-211 or -212
RDC-201	64-Pin Probe and cables for R6500/12Q. Prerequisite, RDC-211 or -212
RDC-202	64-Pin Probe and cables for R6500/13Q. Prerequisite, RDC-211 or -212
RDC-203	40-Pin Probe and cable for R6500/41P. Prerequisite, RDC-221 or -222
RDC-204	64-Pin Probe and cables for R6500/42Q. Prerequisite, RDC-221 or -222
RDC-205	64-Pin Probe and cables for R6500/43Q. Prerequisite, RDC-221 or -222
RDC-206	40-Pin Probe and cable for R6500/1P. Prerequisite, RDC-231 or -232



RDC-502 AND RDC-504 ROCKWELL DESIGN CENTER R6502-R65C02 PERSONALITY SET

INTRODUCTION

The RDC R6502-R65C02 Personality Set is a Rockwell Design Center (RDC) option that allows the RDC user to develop, debug and verify programs intended for use by any R6500 one-chip microprocessor system. The R6502-R65C02 offers the user a high performance development system specifically designed for emulation of a microprocessor system. This RDC option supports in-circuit emulation for the entire R6500 and R65C00 family of one-chip microprocessors.

The basic R6502-R65C02 Personality Set includes a Personality Module Controller (PMC), two Personality Emulator Pod Modules, five emulator devices (R6502, R6512, R65C02, R65C102, and R65C112), two prototype-to-pod interface cables, an RDC interconnect cable set, and the required software and support documentation.

The R6502-R65C02 Personality Set provides the RDC with a dual CPU capability. This added feature permits the RDC CPU to maintain control, even while the microprocessor is executing a program, thus providing the user with complete control over the development process.

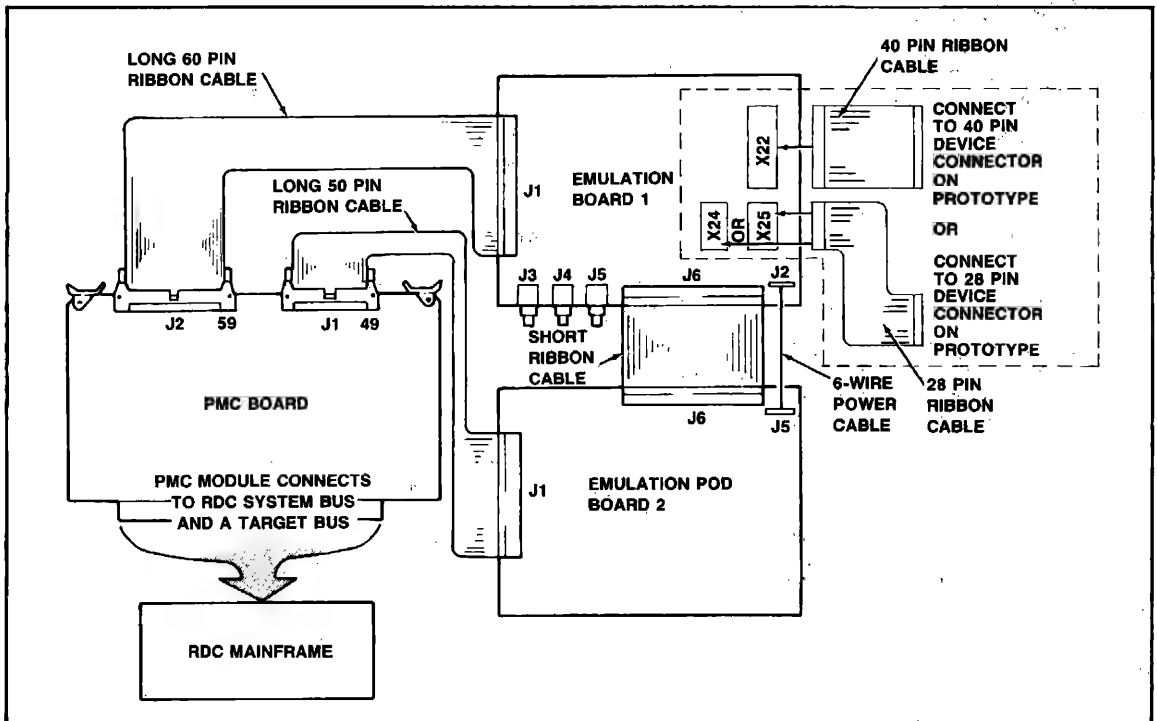
The R6502-R65C02 Personality Set can be expanded to include four separate emulation systems which can be run concurrently on the RDC.

FEATURES

- Disk based macro assembler and debug monitor
- Provides 8K or 64K RAM in system (optional)
- Supports 65K address range in target environment
- Five hardware breakpoints with SYNC outputs
- User defined external break signal
- Single step through interrupts
- Supports four simultaneous target developments
- No zero page address conflicts
- Power down capability
- RAM write protection
- User or system supplied power and clock
- Real-time in-circuit emulation
- Menu-driven Softkey command selection



RDC R6502-R65C02 Personality Set



System Interconnection

RUN MODE/CONTROLLED EXECUTION COMMAND SUMMARY

The R6502-R65C02 Personality Set is designed to allow R650X, R651X or R65XXX devices to execute independent of the RDC. Thus, while the emulator is executing code, the RDC CPU is still in operation. This allows certain functions to be performed by the RDC CPU without disturbing the execution of the emulator device.

RUN MODE COMMANDS

The R6502-R65C02 debug monitor allows certain commands to be performed while the emulator is in the Run mode. The Run Mode commands are highlighted as follows:

Description
RUN MODE COMMANDS
Issue Reset
Examine or Modify Hardware Breakpoint
Exit Run Mode
Return to RDC Operating System
Select a New PMC Module
Enable/Disable the System Pointer
Halt/Resume Run

CONTROLLED EXECUTION MODE COMMANDS

The Controlled Execution Mode commands are divided into five groups, as follows:

Description
COMMANDS TO DISPLAY MEMORY OR REGISTERS
Display or alter sixteen selected memory locations
Display or alter next sixteen memory locations
Display or alter previous sixteen memory locations
Examine/modify RAM and I/O one byte at a time
Dump memory in Hex and ASCII format
Invoke disassembler
Display or alter register contents
COMMANDS TO SET PROGRAM BREAKPOINTS
Set or reset software breakpoint addresses
Enable or disable single step mode
Set or modify hardware breakpoint

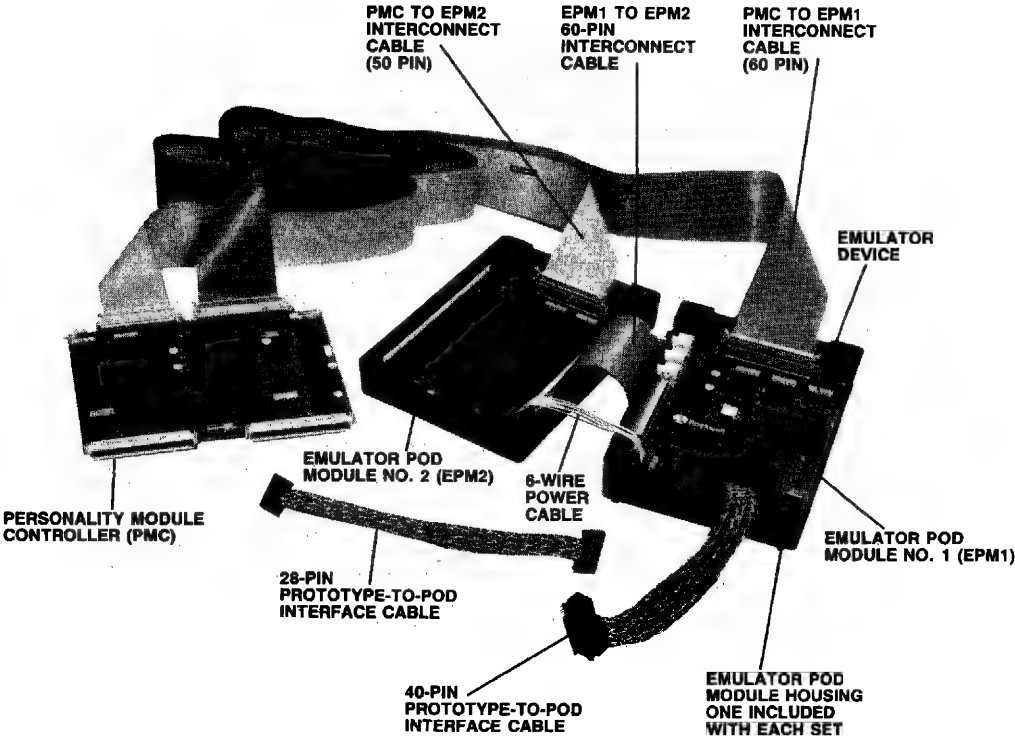
Description
<p>COMMANDS TO TRACE PROGRAM FLOW</p> <p>Toggle instruction trace on or off</p> <p>Toggle register printout on or off</p> <p>Show register form for printout</p> <p>Show last nine instruction addresses</p>
<p>DISK FUNCTIONS</p> <p>Special disk functions</p> <p>Display disk directory</p> <p>Delete file</p>
<p>MISCELLANEOUS COMMANDS</p> <p>Write protect memory blocks</p> <p>Load object code</p> <p>Start execution of user's program</p> <p>Issue RESET</p> <p>Verify object code against memory</p> <p>Return control to RDC Operating System</p> <p>Initialize the current board</p> <p>Enable/disable printer</p> <p>Allow single step through interrupts</p>

CONFIGURATIONS

The RDC Personality Sets for the R6502-R65C02 Micro-processors, shown in the chart below, includes one Personality Module Controller (PMC), two Personality Emulator Pod Modules, one Emulator Device set, an interconnect cable set, and the required software and support documentation.

R6502-R65C02 Personality Sets and Memory

Part Number	Description
RDC-502	R6502-R65C02 Personality Set, 1-2 MHz
RDC-504	R6502-R65C02 Personality Set, 4 MHz
RDC-1011	8K RAM Target Memory, 1-2 MHz only
RDC-1012	64K RAM Target Memory, 1-4 MHz



Typical R6502-R65C02 Personality Set Hardware Components

R6502-R65C02 Personality Set Component List

QUANTITY	ITEM	DESCRIPTION
1	PMC Module	Controller module that plugs into the RDC Mainframe.
1	Emulator Pod Module Assembly	Pod that contains EPM-1 and EPM-2, a short ribbon cable, a six-wire power cable, and the R6502 Emulator Device.
1	Emulator Package	Package contains the R6512, R65C02, R65C102 and R65C112 Emulator devices and 5 jumper headers for the 28-pin processors.
2	PMC to Pod Interface Ribbon Cables (Long Length)	One cable with 60-pin connector on each end with one cable with a 50-pin connector on each end.
2	Prototype-to-Pod Interface Cables (Medium Length)	One of two possible configurations: a. One ribbon cable with 40-pin connectors on each end. Used for emulating the R6502, R6512, R65C02, R65C102 or R65C112. b. One cable with a 28-pin connector on each end. Used for emulating the R6503, R6504, R6505, R6506, R6507, R6513, R6514 or R6515.



RDC-2000 R6500 CROSS ASSEMBLER FOR INTEL DEVELOPMENT SYSTEM

CROSS ASSEMBLY

The R6500 Cross Assembler provides the user with the capability of developing assembly language programs on the Intel Development System and downloading these programs to the Rockwell Design Center (RDC) for debugging and in-circuit operation.

The process of translating microprocessor instructions for a computer program written in symbolic form to executable machine instructions is called an assembly, and the computer program that performs this translation is called an assembler. Assemblers that run on a host computer different from the target computer that the generated machine code is to operate in are called cross assemblers. One assembly language statement usually translates into a single processor instruction. Each statement consists of a label (if required), a mnemonic operation code, an operand (if required), an arithmetic operator (if required) and an optional comment. Constants comprising one or more bytes of memory are generated from data statements while one or more bytes of memory are assigned to variables. This cross assembler is a symbolic assembler that allows the programmer to represent memory locations and numeric values with names or symbols.

PRODUCT OVERVIEW

The R6500 Cross Assembler for the Intel Development System allows users who have access to such a system and are accustomed to its text editor (ISIS CREDIT) to enter and edit source code, assemble the program and save both the source and object code on floppy disk. The object code can then be loaded into a Rockwell Design Center (RDC) for program debugging and in-circuit validation using an R6500, R6500/* or R65C00 Personality Set. Up to four personality sets can be installed in one RDC Main Frame to maximize the utility of one Intel Development System and RDC. The object code can also be programmed into PROM/ROM for execution by an R6500 NMOS or R65C00 CMOS microprocessor or masked in R6500/* NMOS one-chip microcomputer ROM for execution.

The disk-based R6500 cross assembler is a two-pass symbolic assembler which produces absolute 6500 object code. It performs symbol (1-6 characters) definition, syntax checking, assembly/symbol table listings and cross reference generation for effective program development. Assembler operation is automatic once started.

The assembler outputs to the console the pass it is currently performing and a dot for every 16 lines of source code assembled. This enables viewing of the assembly process and observation of detected errors. List (.LST), object (.OBJ), and symbol (.SYM) files are automatically generated with the source name assigned as the header and the particular extension added.

FEATURES

- Intel Development System Host
- Supports Rockwell's 8-bit CPU devices:
 - R6500 NMOS microprocessor family
 - R6500/* NMOS microcomputer family
 - R65C00 CMOS microprocessor family
- Symbolic notation—operands and labels
- Interactive assembler operation
- Operator selected object code output devices
 - Display/printer
 - Printer
 - Floppy Disk
 - Download to RDC
- Operator selected assembly/error listing output
 - Display/Printer
 - Printer
 - Floppy Disk
- Assembler directives
- Symbolic cross-reference
- Communications support—downloading of object code

ORDERING INFORMATION

Part No.	Description
RDC-2000	R6500 Cross Assembler for Intel Development System Disk (8" ISIS II compatible disk)
Order No.	Description
RDC02	R6500 Cross Assembler for Intel Development System User's Manual (included with RDC-2000)

SYSTEM REQUIREMENTS

The Intel Development System must provide 64K bytes of memory and the Dual-Density Drive option to support the R6500 Cross Assembler. 32K bytes are then available for application source code. The other 32K bytes contain the ISIS system (14K) and the cross assembler (18K).

Assembler Directives**Assembly Listing Control**

.TTL	Title	.WIDTH	Line Length
.PAGE	Page	.SKIP	Skip
.LINE	Page Length		

Source File Control

.END	End of Assembly
.MOD	Assembly Type

Data Storage

.BYTE	Initialize byte memory location
.WORD	Generate 16-bit address
.DBYTE	Generate 16-bit data word
.SBYTE	Initialize ASCII string

Equate

=	Assign value to symbol
---	------------------------

Error Codes**Pass 1**

- 1 OPERAND VALUE IS INVALID OR GT HEX FFFF
- 2 OPERAND VALUE IS GREATER THAN HEX FFFF
- 3 INCORRECT ADDRESSING MODE
- 4 SYMBOL NOT PREVIOUSLY DEFINED
- 5 NO OPERAND
- 6 ASCII STRING NOT PROPERLY ENCLOSED
- 7 MISSING .END STATEMENT
- 8 UNDEFINED ASSEMBLER DIRECTIVE
- 9 IMPROPER EQUATE FORMAT
- 10 UNRECOGNIZABLE ASTERISK DEFINITION
- 11 INDIRECT ADDRESSING OFF OF ZERO PAGE
- 12 INCORRECT FORM OF INDIRECT ADDRESSING, MISSING Y
- 13 INCORRECT FORM OF INDEX ADDRESSING, MISSING X
- 14 OPERAND MUST BE ON ZERO PAGE (00-\$FF)
- 15 ILLEGAL INSTRUCTION FOR THIS ASSEMBLER

Pass 2

- 1 .MOD DIRECTIVE MUST BE FIRST LINE ON LISTING
- 2 INCORRECT FORMAT OF INDEX ADDRESSING, MISSING X OR Y
- 3 MISSING RIGHT PARENTHESIS
- 4 LABEL LONGER THAN 6 CHARACTERS
- 5 LABEL IS DEFINED MORE THAN ONCE
- 6 RELATIVE BRANCH IS OUT OF RANGE
- 7 ILLEGAL OR MISSING OPCODE
- 8 OPERAND LABEL IS DEFINED MORE THAN ONCE
- 9 SYMBOL TABLE FULL
- 10 MISSING LABEL FOR EQUATE
- 11 OPERAND LABEL GREATER THAN 6 CHARACTERS LONG
- 12 .MOD VALUE IS INCORRECT FOR THIS ASSEMBLER
- 13 OPERAND NOT BETWEEN 0-7
- 14 SYMBOL HAS ILLEGAL CHARACTER OR IS GREATER THAN ZIFFFF

Operators

Prefix Character	Base
(none)	10 (Decimal)
\$	16 (Hexadecimal)
@	8 (Octal)
%	2 (Binary)

Constants (Prefix)

Operator	Operation
+	Addition
-	Subtraction
>	High-Byte Selection
<	Low-Byte Selection



M65-1XX AND M65-2XX SYSTEM 65 R6500/* PERSONALITY SET

INTRODUCTION

The Rockwell R6500/* Personality Set is a System 65 Development System option that allows the System 65 user to develop, debug and verify special programs intended for use by any R6500 one-chip microcomputer system. The R6500/* offers the user a high performance development system specifically designed for emulation of a microcomputer system. This System 65 option supports in-circuit emulation for the entire R6500 family of one-chip microcomputers.

The basic R6500/* Personality Set includes a Personality Module Controller (PMC), two Personality Emulator Pod Modules, a Device Adapter, an In-Circuit Emulation Probe assembly, an interconnect cable set, and the required software and support documentation.

The R6500/* Personality Set provides the System 65 with a dual CPU capability. This added feature permits the System 65 CPU to maintain control, even while the R6500/* is executing a program, thus providing the user with complete control over the development process.

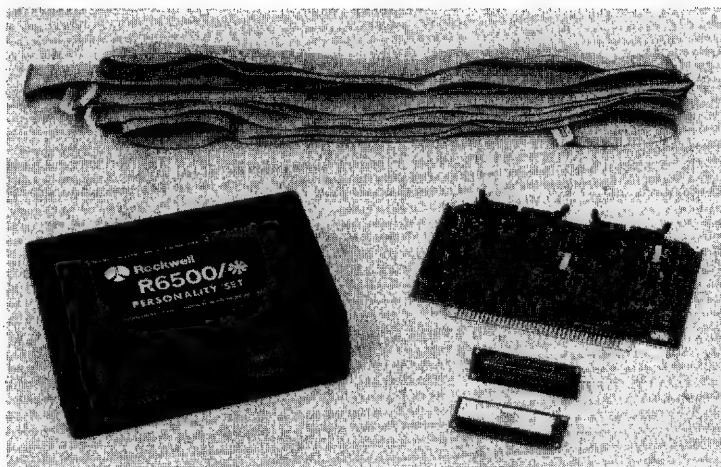
The R6500/* Personality Set can be expanded to include four separate emulation systems which can be run concurrently on the System 65 Development System.

FEATURES

- Disk based macro assembler and debug monitor
- Provides 8K RAM in system
- Supports 65K address range in target environment
- Two hardware breakpoints with SYNC outputs
- User defined external break signal
- Single step through interrupts
- Supports four simultaneous target developments
- No zero page address conflicts
- Power down capability
- RAM write protection
- User or system supplied power and clock
- Real-time in-circuit emulation

RUN MODE/CONTROLLED EXECUTION MODE COMMANDS

The R6500/* Personality Set is designed to allow the R6500/* to execute independent of the System 65. Thus, while the R6500/* is executing code, the System 65 CPU is still in operation. This allows certain functions to be performed by the System 65 CPU without disturbing the execution of the R6500/*. Tables 1 and 2 list the commands for the Run Mode and Controlled Execution Mode respectively. The R6500/* debug monitor allows certain commands to be performed while the R6500/* is in the Run mode.



System 65 R6500/* Personality Set

Table 1. Run Mode Commands

Command	Description
I	Issue reset
C	Examine or modify hardware breakpoint
Q	Exit run mode
ESC	Return to System 65 monitor
F	Select a new PMC board
•	Give board number/emulator model
\$	Enable/disable the system pointer
<SPACE>	Halt/resume run

Table 2. Controlled Execution Mode Commands

Command	Description
Commands to Display Memory or Registers	
M	Display sixteen selected memory locations
<SPACE>	Display next sixteen memory locations
-	Display previous sixteen memory locations
:	Examine/modify RAM and I/O one byte at a time
U	Dump memory in Hex and ASCII format
.	Invoke disassembler
R	Display register contents
Commands to Alter Memory or Registers	
/	Alter memory location
*	Alter program counter
A	Alter accumulator
X	Alter X register
Y	Alter Y register
P	Alter processor status
S	Alter stack pointer
Commands to Set Program Breakpoints	
B	Set or reset software breakpoint addresses
4	Enable or disable single step mode
?	Show all software breakpoint addresses
#	Clear all software breakpoints
C	Set or modify hardware breakpoint
Commands to Trace Program Flow	
Z	Toggle instruction trace on or off
V	Toggle register printout on or off
J	Show register form for printout
H	Show last nine instruction addresses
Disk Functions	
1	Special disk functions
2	Display disk directory
3	Delete file
Miscellaneous Commands	
W	Write project memory blocks
L	Load object code
G	Start execution of user's program
D	Dump memory
I	Issue RESET
K	Verify object code against memory
Q	Return control to System 65
7	Reinitialize R6500/1 Monitor either from System 65 or R6500/1 Monitor
8	Reenter R6500/1 Monitor from System 65
E	Enter the Text Editor
T	Reenter the Text Editor
N	Invoke the Assembler
F	Select a new PMC board
O	Initialize the current board
S	Enable/disable printer
	Give board number/emulator model
ESC	Stop on-going process
+	Allow single step through interrupts

ORDERING INFORMATION

R6500/* Personality Module Sets

Part Number	Description
M65-101	R6500/11P Personality Set, 1 MHz
M65-102	R6500/11AP Personality Set, 2 MHz
M65-111	R6500/12Q Personality Set, 1 MHz
M65-112	R6500/12AQ Personality Set, 2 MHz
M65-121	R6500/13Q Personality Set, 1 MHz
M65-122	R6500/13AQ Personality Set, 2 MHz
M65-131	R6500/41P Personality Set, 1 MHz
M65-132	R6500/41AP Personality Set, 2 MHz
M65-141	R6500/42Q Personality Set, 1 MHz
M65-142	R6500/42AQ Personality Set, 2 MHz
M65-151	R6500/43Q Personality Set, 1 MHz
M65-152	R6500/43AQ Personality Set, 2 MHz
M65-161	R6500/1P Personality Set, 1 MHz
M65-162	R6500/1AP Personality Set, 2 MHz

Adapter/Emulator Devices ⁽¹⁾

Part Number	Description
M65-211	Adapter/Emulator Device (R6511Q) for R6500/11/12/13, 1 MHz
M65-212	Adapter/Emulator Device (R6511AQ) for R6500/11/12/13, 2 MHz
M65-221	Adapter/Emulator Device (R6541Q) for R6500/41/42/43, 1 MHz
M65-222	Adapter/Emulator Device (R6541AQ) for R6500/41/42/43, 2 MHz
M65-231	Adapter/Emulator Device (R6500/1EC) for R6500/1, 1 MHz
M65-232	Adapter/Emulator Device (R6500/1EAC) for R6500/1, 2 MHz

Note:

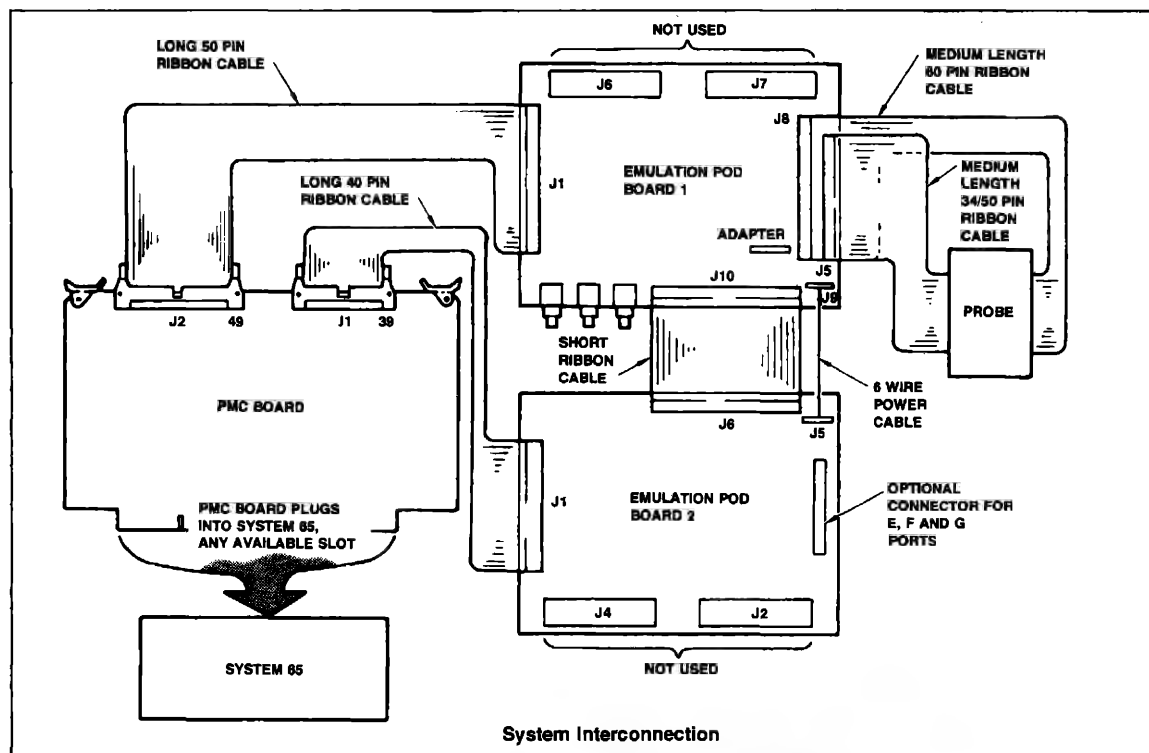
1. Used to reconfigure M65-1XX Personality Sets for use with other R6500/* Microcomputers. Replaces Adapter/Emulator Device in Personality Emulator Pod Module.

In-Circuit Emulation Probes ⁽¹⁾

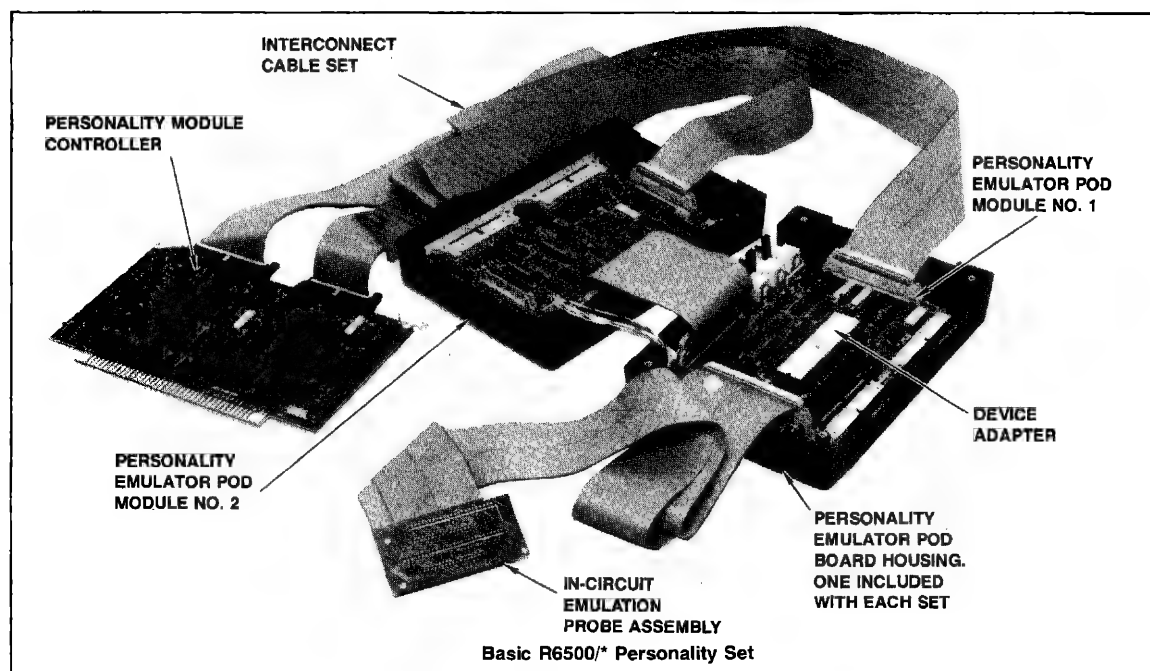
Part Number	Description
M65-200	40 Pin Probe and cable for R6500/11P. Prerequisite, M65-211 or 212
M65-201	64 Pin Probe and cables for R6500/12Q. Prerequisite, M65-211 or 212
M65-202	64 Pin Probe and cables for R6500/13Q. Prerequisite, M65-211 or 212
M65-203	40 Pin Probe and cable for R6500/41P. Prerequisite, M65-221 or 222
M65-204	64 Pin Probe and cables for R6500/42Q. Prerequisite, M65-221 or 222
M65-205	64 Pin Probe and cables for R6500/43Q. Prerequisite, M65-221 or 222
M65-206	40 Pin Probe and cable for R6500/1P. Prerequisite, M65-231 or 232

Note:

1. Used to reconfigure M65-1XX Personality Sets for use with other R6500/* Microcomputers.



6



ADDITIONAL PROBES AND ADAPTERS SELECTION GUIDE

If you already have a System 65 Personality Set for a member of the R6500/* family you need not purchase a complete new set to support another member of the family. The following matrix shows the minimum probes and adapters that need to

be purchased to reconfigure your set for another R6500/* device. Select the device now being supported in the FROM row, find the device you wish to support in the TO column. The P/N's in the intersection will reconfigure your Personality Set.

TO	FROM						
	R6500/11P	R6500/12Q	R6500/13Q	R6500/41P	R6500/42Q	R6500/43Q	R6500/1P
R6500/11P		M65-200	M65-200	M65-211 or 212 M65-200	M65-211 or 212 M65-200	M65-211 or 212 M65-200	M65-211 or 212 M65-200
R6500/12Q	M65-201		M65-201	M65-211 or 212 M65-201	M65-211 or 212 M65-201	M65-211 or 222 M65-201	M65-211 or 212 M65-201
R6500/13Q	M65-202	M65-202		M65-211 or 212 M65-202	M65-211 or 212 M65-202	M65-211 or 212 M65-202	M65-211 or 212 M65-202
R6500/41P	M65-221 or 222 M65-203	M65-221 or 222 M65-203	M65-221 or 222 M65-203		M65-203	M65-203	M65-221 or 222 M65-203
R6500/42Q	M65-221 or 222 M65-204	M65-221 or 222 M65-204	M65-221 or 222 M65-204	M65-204		M65-204	M65-221 or 222 M65-204
R6500/43Q	M65-221 or 222 M65-205	M65-221 or 222 M65-205	M65-221 or 222 M65-205	M65-205	M65-205		M65-221 or 222 M65-205
R6500/1P	M65-231 or 232 M65-206	M65-231 or 232 M65-206	M65-231 or 232 M65-206	M65-231 or 232 M65-206	M65-231 or 232 M65-206	M65-231 or 232 M64-206	



M65-001, -002, -003 USER 65 MODULES

OVERVIEW

The USER 65 Module permits users developing R6500-based products to extend the full power of System 65 Development System into their equipment for in-circuit emulation. Available in both 1- and 2-MHz versions (M65-001 and 002), USER 65 supports all ten R6500 CPU's. M65-003 configuration is without the controller.

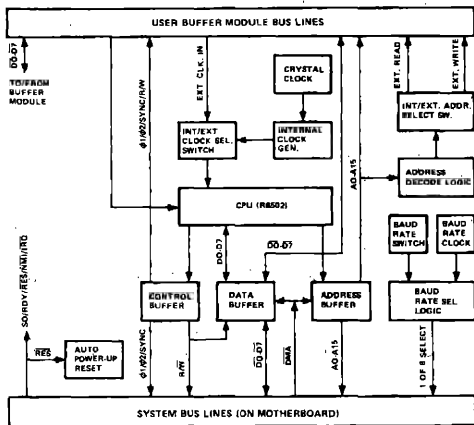
USER 65 consists of two modules—a Host Module and a Buffer Module—and two interconnect cables. The USER 65 Host Module replaces the CPU Module in the System 65 chassis; it performs all CPU Module functions, plus several external functions. The USER 65 Buffer Module extends the System 65 bus lines (address, data, and control) to the user equipment.

FUNCTIONAL DESCRIPTION

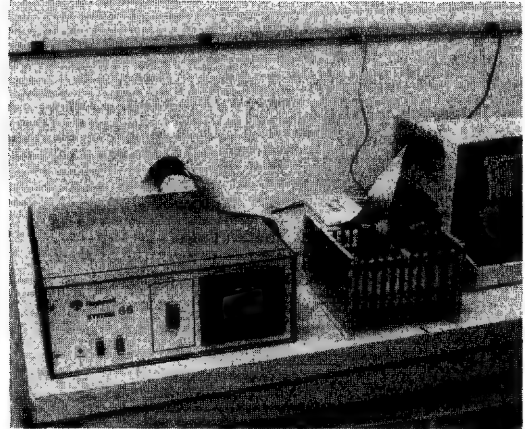
USER 65 HOST MODULE

The USER 65 Host Module shown in block diagram replaces the CPU Module in the System 65 chassis. It is capable of performing all functions of the CPU Module, plus external address selection, automatic power up, and external clock selection. The Host Module interface signals are listed in Table 1.

The heart of the Host Module is the R6502 (Z11) microprocessor. It controls all functions of the System 65 and the user's external equipment. Crystal Y1 (1 or 2 MHz) generates the internal clock for the R6502 CPU. Switch S3 is used to select either the internal generated clock or an externally provided clock input.



USER 65 Host Module Functional Block Diagram



M65-001 USER 65 Module

The Host Module has automatic power-up circuit consisting of an NE555 timer (Z3) and associated discrete capacitors and resistors. This circuit will generate a 100 msec reset pulse following power-up.

The Host Module also contains the RS-232C and TTY baud rate generator circuitry. Crystal Y2 (1.8432 MHz) and baud rate generator MC14411 (Z13) generate a baud rate clock. The Clock rate is multiplied by 16 ($\times 16$) to provide a selectable output baud rate from 110 to 9600. Switch S4 and the SN74152 (Z12) select the baud rate. This output is then provided to the System 65 bus to be used by the Monitor Module.

The internal/external address selection is based on a decode of A15-A12, using an SN74159N (Z1) decoder. This device has sixteen active low outputs. Each output represents a 4K address space and is selected by Switches S1 and S2. The outputs are ORed together and inverted by SN7406 (Z2). This enable signal is then gated with R/W signal to form a READ signal and a WRITE signal, which are used in the USER 65 Buffer Module.

The address lines and control lines \overline{RDY} , \overline{RES} , \overline{DMA} , and \overline{SYNC} are buffered with I.C.'s 8T97 (Z8-Z10, Z5). The data lines are inverted and buffered with I.C.'s 8T26 (Z6, Z7). All of these lines are brought to the System 65 bus and are also taken out to the USER 65 Buffer Module through series terminators (A1-A4).

The Control lines $\overline{S.O.}$, \overline{RDY} , \overline{RES} , \overline{NMI} , \overline{IRQ} are brought to the System 65 bus and are also brought from the USER 65 Host Module, then buffered with open collector buffers SN7407 (Z15). These inputs come only from the user's equipment; the RESET switch on the front panel will not reset the external equipment.

6

System 65 bus line \overline{DMA} is used to control the address and data bus lines. This line is pulled up internally with a 3K resistor. By pulling \overline{DMA} low, the address, data and R/W lines are set to the float state, allowing an external board to control them for DMA operations. The \overline{DMA} line does not stop the CPU—this must be done by controlling the RDY line as outlined in the R6500 Microprocessor Data Sheet Order No. D39.

USER 65 BUFFER MODULE

The USER 65 Buffer Module receives the address, data and control lines from the USER 65 Host Module, buffers these signals and interfaces them to the user's equipment.

The address lines, SYNC and R/W lines are buffered with I.C.'s 8T97 (Z1-Z3). The control lines RDY, \overline{RES} , NMI, \overline{IRQ} , and S.O. are buffered with open collector I.C.'s SN7407 (Z4). The data lines are inverted and buffered with I.C.'s 8T26A (Z7 and Z8). They have series terminators of 150 ohms (Z9).

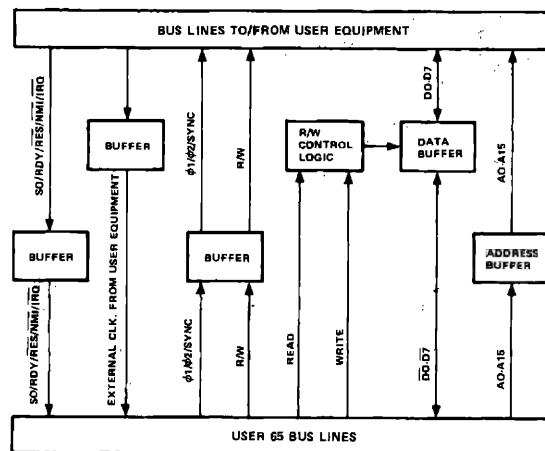
The $\phi 1$ and $\phi 2$ clocks are buffered by 8T97 (Z5). To use an external clock, jumper N must be installed. To use $\phi 1$, jumper M must be installed. The DBE signal is provided for use during emulation of the R6512 CPU. This line has an internal pullup resistor of 3K. When brought low it will disable the data bus drivers.

Two other signals, READ and WRITE, are buffered by Z5. The READ signal is generated by the Host Module and is high when the R/W line is high and an external address is active. The WRITE signal, also generated by the Host Module, is high when R/W line is low and an external address is active. These two lines control the data bus buffers Z7 and Z8.

Table 1. USER 65 Host Board to Buffer Board Interface Signals

CONNECTOR J1		CONNECTOR J2	
PIN	SIGNAL	PIN	SIGNAL
1	A0	1	EXT. CLOCK
3	A1	3	$\phi 2$
5	A2	5	$\phi 1$
7	A3	7	GATED READ
9	A4	9	GATED WRITE
11	A5	11	$\overline{D7}$
13	A6	13	$\overline{D6}$
15	A7	15	$\overline{D5}$
17	A8	17	$\overline{D4}$
19	A9	19	$\overline{D3}$
21	A10	21	$\overline{D2}$
23	A11	23	$\overline{D1}$
25	A12	25	$\overline{D0}$
27	A13	27	+5V
29	A14	29	+5V
31	A15	31	+5V
33	SYNC	33	+5V
35	R/W	35	+5V
37	RDY	37	+5V
39	\overline{RESET}	39	+5V
41	NMI		
43	\overline{IRQ}		
45	S0		

Note: Even-numbered pins are connected to Ground.



USER 65 Buffer Module Functional Block Diagram

USER 65 CABLES

The cable assembly supplied with the USER 65 option provides the signal paths between the USER 65 Host and Buffer Modules, and between the Buffer Module and the user's equipment. Since the USER 65 option is designed to emulate all versions of the R6500 Family of CPU's, both a 40-pin cable and two 28-pin types of cables are provided.

INSTALLATION

USER 65 HOST MODULE

Install the USER 65 Host Module in the System 65 as follows:

1. Turn System 65 power off.

CAUTION

Never install or remove modules with System 65 power on—it may cause damage to the module and/or to the system.

2. Remove the top cover of the System 65.
3. Remove the CPU Module.
4. Set switches S1, S2, S3 and S4 on the USER 65 Host Module per Table 2. The switch positions are shown in Figure 1.
5. Plug the USER 65 Host Module into any convenient slot in the System 65 chassis.
6. Route the cables from the Buffer Module through the back panel of System 65, through the slot provided.
7. Connect the 40- and 50-pin cables from the Buffer Module to the top of the Host Module (the connectors are keyed with arrows).

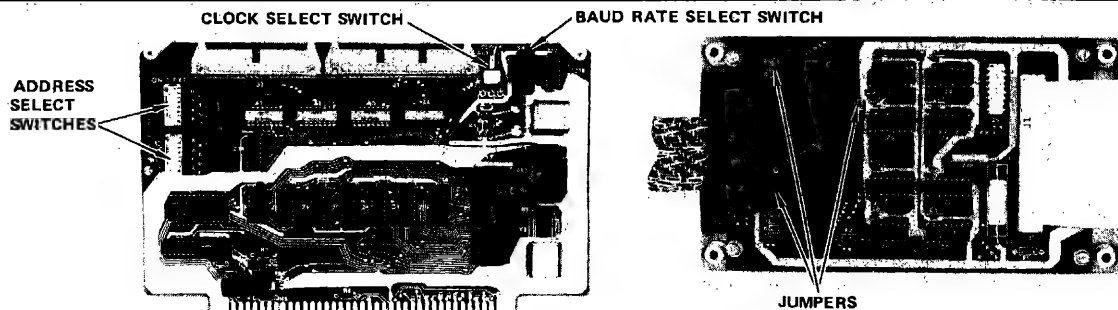


Figure 1. USER 65 Host and Buffer Modules

Table 2. USER 65 Host Module Switches

SWITCH	FUNCTION
S1/S2	ADDRESS SELECT
	These switches determine whether address selection is internal or external for each 4K byte portion of memory space. External memory is selected when the switch is ON, internal memory is selected when the switch is OFF.
	S1 Switch
	Address Range
	1 \$0000 - \$0FFF
	2 \$1000 - \$1FFF
	3 \$2000 - \$2FFF
	4 \$3000 - \$3FFF
	5 \$4000 - \$4FFF
	6 \$5000 - \$5FFF
	7 \$6000 - \$6FFF
	8 \$7000 - \$7FFF
	S2 Switch
	Address Range
	1 \$8000 - \$8FFF
	2 \$9000 - \$9FFF
	3 \$A000 - \$AFFF
	4 \$B000 - \$BFFF
	5 \$C000 - \$CFFF
	6 \$D000 - \$DFFF
	7 \$E000 - \$EFFF
	8 \$F000 - \$FFFF
S3	CLOCK SELECT
	Switch S3 selects either the SYSTEM 65 clock (INT) or an external, user-supplied clock (EXT). If an external supplied clock is used, the frequency must be 1 or 2 MHz \pm 1% if operation of the SYSTEM 65 mini-floppy disks is required. It must always be a TTL level, square wave, clock input.
S4	BAUD RATE SELECT
	This switch determines the baud rate for either the RS-232C or TTY ports. Switch settings are:
	(S4) POSITION
	BAUD RATE
	0 110
	1 150
	2 300
	3 600
	4 1200
	5 2400
	6 4800
	7 9600

8. Set switches S1 and S2 on the RAM Module per Tables 3 and 4 to enable/disable and to select the address range of the internal System 65 RAM.

NOTE

If external RAM addresses are selected on the USER 65 and the same addresses are selected and enabled on the System 65 internal RAM board(s), the internal RAM will override and prevent proper operation of the external RAM.

9. Install the top cover.

Table 3. RAM Module Enable/Disable Switch Definition

Switch S1/S2-4 Position	RAM Enable/Disable State
Up	RAM Disabled (Deselected)
Down	RAM Enabled (Selected)

Table 4. RAM Address Range Select Switch Settings

Switch S1/S2 Position			8K Address Range Selected
-1	-2	-3	
Up	Up	Up	\$0000 - \$1FFF
Down	Up	Up	\$2000 - \$3FFF
Up	Down	Up	\$4000 - \$5FFF
Down	Down	Up	\$6000 - \$7FFF
Up	Up	Down	\$8000 - \$9FFF
Down	Up	Down	\$A000 - \$BFFF
Up	Down	Down	\$C000 - \$DFFF
Down	Down	Down	\$E000 - \$FFFF

Note: "Up" is toward the top edge of the module

USER 65 BUFFER MODULE

Since the Buffer Module is designed to support all CPU's in the R6500 family, specific jumpers or straps must be inserted to support the exact CPU being emulated. Table 5 gives the strapping requirements. Jumper locations are shown in Figure 1.

The Buffer Module has two modes for the R/W line. For 40-pin CPU emulation (R6502 and R6512), the R/W line is connected to the user's equipment as is. Since the 28-pin CPU's do not provide all the address lines to the user's equipment, address conflicts can occur during System 65 Monitor execution. A gated R/W line is provided to prevent these conflicts; this line is normally high, and goes low only when an external address is present and R/W is low.

The Buffer Module also has straps for clock selection. One strap allows the $\phi 1$ (OUT) signal to go to the user's equipment. The other strap is used to allow an external clock ($\phi 0$ (IN) or $\phi 2$ (IN)) to be used. Switch S3 on the Host Module must be set to EXT when the external clock is used.

The Buffer Module is provided with three sockets and three cables. The 40-pin socket (J3) should be used for either of the 40-pin CPU's, R6502 or R6512. The cable labeled PS00-D603-001 should be used to connect from J3 to the user's equipment. The other two sockets (J4 and J5) are for use with the 28-pin CPU's. Table 5 correlates the socket and 28-pin cable to be used for each of the 28-pin CPU versions.

The DBE (Data Bus Enable) line for the R6512 is available to the user's equipment. There is an internal 3K pullup resistor in the Buffer Module, so it can be left open if desired. To disable the data output drivers, pull the DBE line low.

The installation procedure is:

1. Remove the top of the USER 65 Buffer Module assembly.
2. Insert the desired jumpers, per Table 5.
3. Connect either the 40-pin cable to plug J3 or the 28-pin cable to plug J4 or J5, as appropriate.
4. Reinstall the top of the Buffer Module assembly.
5. Plug the free connector of the cable into the user's equipment.

NOTE

Any conductive foam must be removed from the CPU plug pins to allow proper System 65 operation even when the CPU plug is not connected to user equipment.

6. Turn System 65 and user's equipment power on.

Table 5. USER 65 Buffer Module
Connection Requirements

User Equipment CPU	Buffer Module Socket	Cable To User Equipment	Jumper	Signal	User's CPU Pin
R6502	J3	PS00-D603-001	R M N*	R/W $\phi 1$ (OUT) $\phi 0$ (IN)	34 3 37
R6503	J4	PS00-D605-001	P B D E F A N*	R/W RES VSS IRQ NMI $\phi 2$ (OUT) $\phi 0$ (IN)	26 1 2 3 4 28 27
R6504	J5	PS00-D605-001	P B D E A N*	R/W RES VSS IRQ $\phi 2$ (OUT) $\phi 0$ (IN)	26 1 2 3 28 27
R6506	J4	PS00-D605-001	P B D K S A N*	R/W RES VSS RDY IRQ $\phi 2$ (OUT) $\phi 0$ (IN)	26 1 2 3 4 28 27
R6506	J4	PS00-D605-001	P B D L S A M N*	R/W RES VSS $\phi 1$ (OUT) IRQ $\phi 2$ (OUT) $\phi 1$ (OUT) $\phi 0$ (IN)	26 1 2 3 4 28 3 27
R6507	J5	PS00-D605-001	P B D K A N*	R/W RES VSS RDY $\phi 2$ (OUT) $\phi 0$ (IN)	26 1 2 3 28 27
R6512	J3	PS00-D603-001	R N*	R/W $\phi 2$ (IN)	34 37
R6513	J4	PS00-D604-001	P C E F T N*	R/W VSS IRQ NMI RES $\phi 2$ (IN)	26 1 3 4 28 27
R6514	J5	PS00-D604-001	P C E T N*	R/W VSS IRQ RES $\phi 2$ (IN)	26 1 3 28 27
R6515	J4	PS00-D604-001	P C J L S T N*	R/W VSS RDY IRQ RES $\phi 2$ (IN)	26 1 2 4 28 27

*Jumper N is required with an external clock. Switch S3 on the USER 65 Host Module must be positioned to the EXT position when the extended clock or frequency reference is used.

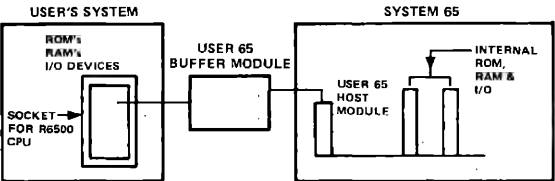
TYPICAL APPLICATION

A typical application for the USER 65 module is illustrated. The user's system may include any combination of ROM's, PROM's, RAM's, I/O devices, and a 40- or 28-pin CPU socket. For emulation purposes, the USER 65 module is installed in the CPU socket instead of a CPU. The user must provide page 0(\$0000-\$00FF) and page 1(\$0100-\$01FF) either internally or externally for use by the System 65 Monitor. For system development purposes, the user's ROM may be emulated with one or more RAM modules provided in the System 65 chassis. This permits easy manipulation, debugging, and reassembly of the user's program during the development phase. For editing and assembling of the source program, the user may use the System 65 RAM or may provide his own RAM modules externally.

The USER 65 module may be used with the System 65 Monitor enabled or disabled. With System 65 Monitor enabled, the full resources of the System 65 Monitor are available for program checkout and debugging. In this mode the System 65 uses addresses \$C000-\$FFFF; these addresses cannot be used by the programmer.

SPECIFICATIONS

Parameter	Value
Common Specifications	
Operating Frequency:	1 MHz or 2 MHz
Operating Temperature:	0° to 70°C
Power Requirements	+5 Vdc ± 5% @ 1.5A
Host Module Specifications	
Module Dimensions:	9.75 in. wide × 7.50 in. high
Edge Contacts:	86 pins on 0.156 in. centers
Edge Contact Signals:	System 65 compatible
Buffer Module Specifications	
Module Dimensions:	4.125 in. wide × 7.375 in. high
Cable Lengths:	
To System 65	60 in.
To User Equipment	12 in.



USER 65 Module Hook-up



M65-031 AND M65-032 16K STATIC RAM MODULES

OVERVIEW

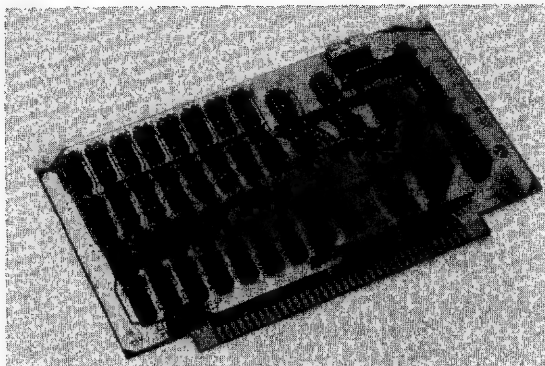
The 16K Static RAM Module contains 16K (16,384) bytes of Random Access Memory (RAM), implemented with 32 R2114 1024 × 4 Static RAM devices and is available in either 1 MHz (M65-031) or 2 MHz (M65-032) version. Also included are address decoding and selection, write protection and data buffering circuitry.

The module's 16K bytes of RAM memory are segmented into two independent 8K-byte sections. Each 8K section is controlled by an enable/disable switch and three address range select switches, located at the top of the Module. Each 8K section can be independently write-protected via special lines.

The Static RAM Module is directly compatible with the Rockwell System 65 Microcomputer Development System, and can be used to increase the system's read/write memory capacity from 16K bytes to 48K bytes, without hardware modification. The module may also be installed in user-designed equipment, via the Auxiliary Card Cage.

FEATURES

- System 65 compatible
- Available in 1 MHz (450 ns access) and 2 MHz (250 ns access) versions
- 16K bytes of Random Access Memory, with two independent 8K sections
- Separate write protect capability for each 8K section
- Static—no clocks or strobes required
- 9.75 in × 6.00 in. module
- Single +5V supply



M65-031 16K Static RAM Module

FUNCTIONAL DESCRIPTION

The edge connector pin assignments for the RAM Module are compatible with the Motherboard pin assignments given in Section 4 of the System 65 User's Manual (Document No. 29650 N35; Order No. 206).

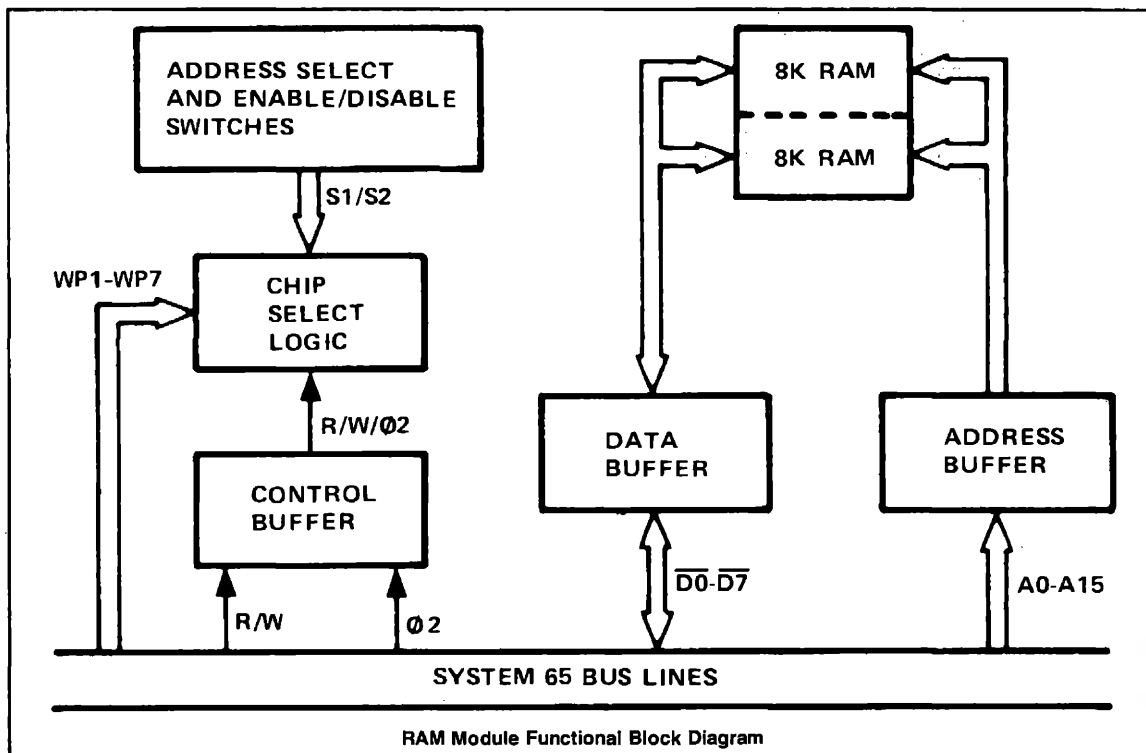
The RAM Module's 16K bytes of read/write memory are provided by 32 R2114 1024 × 4-bit Static RAM devices.

Address Buffers Z47, Z46 and Z33 and Data Buffers Z32 and Z45 present a single TTL load to the Motherboard edge connector. The data signals are inverted to make them compatible with the system 65 Data Bus ($\overline{D0-D7}$).

Module Switches S1 and S2 provide independent 8K RAM section enable/disable and address selection. S1-4 and S2-4 permit each 8K section of RAM to be enabled or disabled. S1-1, -2 and -3 and S2-1, -2, and -3 select the base address to which the respective 8K sections will respond. These switch settings are compared to upper address bits A13, A14 and A15 in Address Comparator devices Z10 and Z21. The Comparator outputs enable or disable 1-of-8 Decoder devices Z9 and Z20 to provide the input chip select signals to the two 8K RAM sections.

Write protection is controlled by seven Write Protect lines, WP1-WP7, one line for each 8K section of memory (the lowest section, addresses \$0000-\$1FFF, may not be write protected; note that Z48-2 is tied to ground to permanently enable writing to this section). A low voltage on WP1-WP7 enables writing into the associated 8K section.

When the Address Comparator enables the RAM Device Select Decoders, Address Select switches S1-1 through S1-3 and S2-1 through S2-3 are used by Z35 and Z36 to select one of the seven Write Protect lines. The selected line controls the RAM Write Control signals, Z34-6 and Z34-8.



INSTALLATION

Use the following procedure to install 16K Static RAM Modules in the System 65 or, with appropriate changes, in an Auxiliary Card Cage.

1. Turn System 65 power off.

CAUTION

Never install or remove modules with System 65 power on—it may cause damage to the module and/or to the System.

2. Remove the top cover of the System 65.
3. The RAM Module has two banks of switches—S1 and S2—one bank for each 8K section of RAM. Using Tables 1 and 2, select the enable/disable and address range characteristics for each 8K section.

NOTES

For proper System 65 operation . . .

- a. Page 0 (address range \$0000-\$00FF) and Page 1 (\$0100-\$01FF) must be provided in RAM—either internal RAM or external RAM as interfaced by USER 65 or its equivalent.
- b. RAM addresses in the range \$C000-\$FFFF are used by

the System 65 Monitor Board, and must not be enabled in RAM Modules.

4. Insert the RAM Module(s) into any vacant slot(s) in the System 65 chassis.
5. Install System 65 top cover.
6. Turn system 65 power on.

Table 1. RAM Enable/Disable Switch Settings

Switch S1/S2-4 Position	RAM Enable/Disable State
Up (Off)	RAM Disabled (Deselected)
Down (On)	RAM Enabled (Selected)

Table 2. RAM Address Range Select Switch Settings

Switch S1/S2 Position			8K Address Range Selected
-1	-2	-3	
Up	Up	Up	\$0000-\$1FFF
Down	Up	Up	\$2000-\$3FFF
Up	Down	Up	\$4000-\$5FFF
Down	Down	Up	\$6000-\$7FFF
Up	Up	Down	\$8000-\$9FFF
Down	Up	Down	\$A000-\$BFFF
Up	Down	Down	\$C000-\$DFFF
Down	Down	Down	\$E000-\$FFFF

Note: "Up" is toward the top edge of the Module.

SPECIFICATIONS

Memory Size:	16K bytes
Word Length:	8 bits
Interface:	System 65 compatible
Max. Access Time:	450 ns (P/N M65-031) 250 ns (P/N M65-032)
Module Components:	32 R2114 Static 1024 × 4-bit RAM devices
Module Dimensions:	9.75 in. wide × 6.00 in. high
Edge Connector:	86 pins on 0.156-in. centers
Operating Temperature:	0°C to +70°C
Power Requirements:	+5 Vdc ±5% @ 3.0 amps (typical)

LOGIC LEVELS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$

Characteristic	Symbol	Min	Max	Unit	Condition
Inputs ($\overline{D0-D7}$, A0-A15, WP1-WP7, $\overline{\phi 2}$, $\overline{R/\overline{W}}$)					
Input Low Voltage	V_{IL}		0.8	V	$I_{IL} = 400 \mu\text{a}$
Input High Voltage	V_{IH}	2.0	V_{CC}	V	$I_{IH} = 40 \mu\text{a}$
Outputs ($\overline{D0-D7}$)					
Output Low Voltage	V_{OL}		0.5	V	$I_{OL} = 48 \text{ ma}$
Output High Voltage	V_{OH}	2.4	V_{CC}	V	$I_{OH} = 10 \text{ ma}$



M65-040 PROM PROGRAMMER MODULE

OVERVIEW

The M65-040 PROM Programmer Module provides System 65 users with a means to program, verify, read and check Programmable Read Only Memory (PROM) devices, and supports 2704, 2708, 2716, 2516, 2532, and 2758 devices. The PROM Programmer Module connects directly to the PROM Socket on the front panel of the System 65 chassis, via supplied cable.

The Module is supplied with a mini-floppy diskette which holds a set of software routines that allow the user to check a PROM for proper initialization, program the PROM from System 65 memory, verify the PROM with System 65 memory, and read the contents of the PROM into memory. Utility functions to load, verify and dump memory are also supplied.

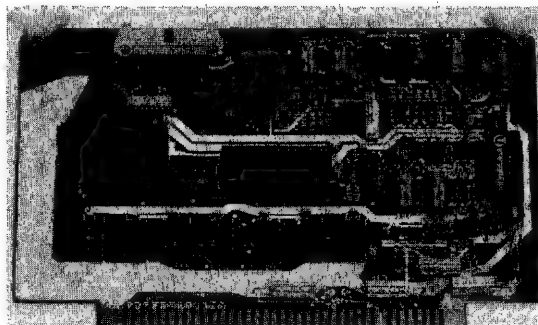
FEATURES

- System 65 development system compatible
- Supports programming of 2704, 2708, 2516, 2532, 2716 (Intel and Texas Instruments) and 2758 PROM devices.
- Comes with software on mini-floppy diskette

FUNCTIONAL DESCRIPTION

The edge connector pin assignments for the PROM Programmer Module are identical to the Motherboard pin assignments given in Section 4 of the System 65 User's Manual (Document No. 29650N35).

Table 1 summarizes the PROM Socket interface, and applies to both the PROM socket located on the PROM Programmer Module and the PROM socket located on the System 65 front panel.



M65-040 PROM Programming Module

The PROM Programmer Module consists of two R6520 Peripheral Interface Adapters (PIAs), data buffers, address decoders, 26V power supply, level shifters and power-up circuitry.

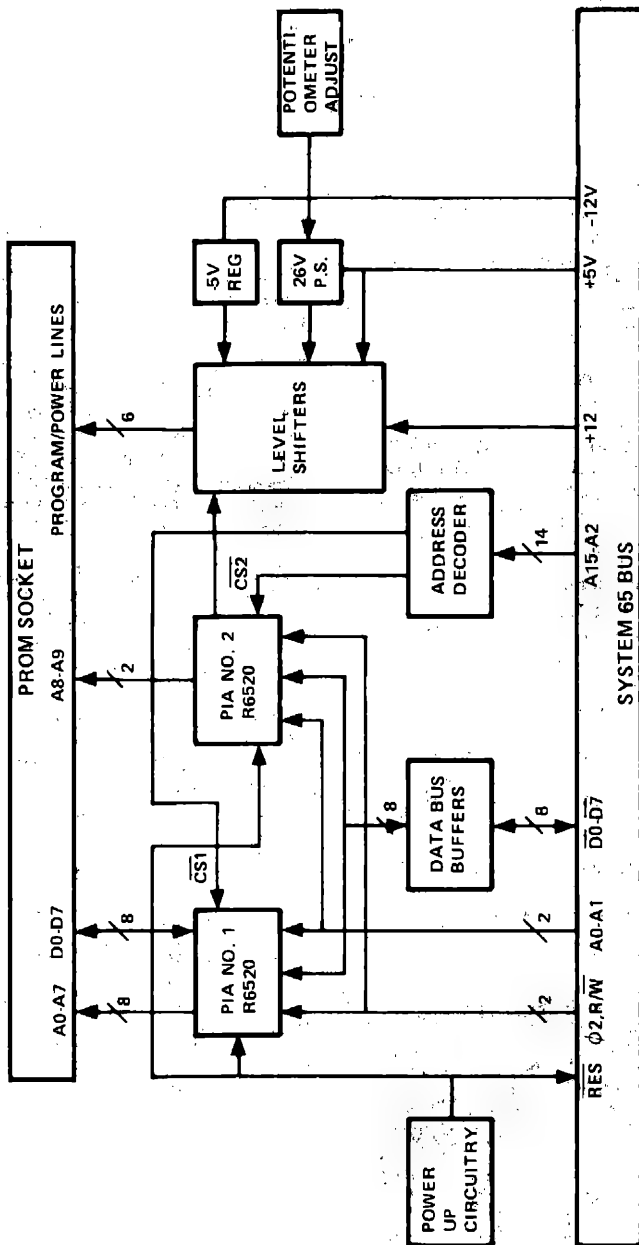
The power-up circuitry (Z9) generates an automatic reset during power-up. A reset signal may also come from the Reset line of the System 65 Bus.

The PROM Programmer Module contains data bus buffers, Z12 and Z13, to provide a logical inversion and a single TTL load to the System 65 bus signals. The two R6520 PIAs, Z5 and Z8, are used to store the address, data and control information for the PROM device. The address, Read/Write (R/W), and Ø2 signals are buffered and decoded by Z10, Z11, Z14, Z15 and Z16. PIA No. 1 is addressed at locations \$C018-\$C01B. PIA No. 2 is addressed at locations \$C01C-\$C01F.

The PROM device receives address lines A0-A9 and data lines D0-D7 directly from the PIA devices. The program lines (see Table 1, PROM socket pin nos. 18, 19 and 20) are level-shifted to provide either 0V, +5V, +12V, +25V or +26V to the PROM device, depending on the device type. The 26-volt power is generated from the +5-volt power through a DC-DC converter, Z6, and an adjustable voltage regulator, Z1. Relays XR1 through XR4 are used to switch the power lines (see Table 1, PROM socket pin nos. 21 and 23) to +5V, +12V and -5V to the PROM device, depending on the device type. The -5V power is generated from the -12V power line through a voltage regulator, Q9.

Table 1. System 65 PROM Socket Interface Summary

PROM Socket Pin Number	PROM Device Type							Connector J1 Pin Number
	2704	Intel 2708	Intel 2758	Intel 2716	T.I. 2716	T.I. 2516	T.I. 2532	
1	A7	A7	A7	A7	A7	A7	A7	21
2	A6	A6	A6	A6	A6	A6	A6	19
3	A5	A5	A5	A5	A5	A5	A5	17
4	A4	A4	A4	A4	A4	A4	A4	15
5	A3	A3	A3	A3	A3	A3	A3	23
6	A2	A2	A2	A2	A2	A2	A2	25
7	A1	A1	A1	A1	A1	A1	A1	26
8	A0	A0	A0	A0	A0	A0	A0	24
9	D0	D0	D0	D0	Q1	Q1	Q1	22
10	D1	D1	D1	D1	Q2	Q2	Q2	20
11	D2	D2	D2	D2	Q3	Q3	Q3	18
12	GND	GND	GND	GND	VSS	VSS	VSS	16
13	D3	D3	D3	D3	Q4	Q4	Q4	10
14	D4	D4	D4	D4	Q5	Q5	Q5	8
15	D5	D5	D5	D5	Q6	Q6	Q6	6
16	D6	D6	D6	D6	Q7	Q7	Q7	2
17	D7	D7	D7	D7	Q8	Q8	Q8	4
18	PGM	PGM	CE/PGM	CE/PGM	CS/PGM	PD/PGM	PD/PGM	A11
19	VDD	VDD	GND	A10	VDD	A10	A10	11
20	CS/WE	CS/WE	OE	OE	A10	C5	PD/PGM	9
21	VBB	VBB	VPP	VPP	VBB	VPP	VPP	7
22	GND	A9	A9	A9	A9	A9	A9	5
23	A8	A8	A8	A8	A8	A8	A8	3
24	VCC	VCC	VCC	VCC	VCC(PE)	VCC	VCC	1



Note: All examples were prepared
using SYSTEM 65 Operating
System Version 3

MODULE INSTALLATION

Install the PROM Programmer Module as follows:

1. Turn System 65 off.

CAUTION

Never install or remove modules with System 65 power on—it may cause damage to the module and/or to the System.

2. Remove the top cover of the System 65.
3. Insert the PROM Programmer Module into any vacant slot in the System 65 chassis.
4. Connect one end of the supplied cable to the connector on top of the PROM Programmer Module and the other end to the connector mounted on the inside front panel of System 65. Observe the correct polarity of the plugs and sockets; i.e., align the arrows marked on the plugs and sockets.
5. Install the top cover of the System 65.
6. Set the System 65 RUN/STEP Switch to RUN.

NOTE

The PROM programmer will not operate properly if the RUN/STEP Switch is in the STEP position.

7. Turn System 65 power on.
8. The PROM Programmer Module has an automatic reset feature. The standard power-up message should appear on the system terminal device at power-on. A manually-initiated reset may, however, be performed whenever required.

PROM DEVICE INSERTION/REMOVAL

CAUTION

The Prom device is fragile, and dropping, twisting or uneven pressure may break it. Never press down on the window area of the chip.

The PROM device may be inserted into System 65 front panel socket or into the socket located on the PROM Programmer Module.

CAUTION

Only one PROM device should be installed at a time—in either the System 65 socket or the PROM Programmer Module socket. Programming with PROM devices installed in both locations may cause erroneous results and/or damage to the PROM.

PROM INSERTION/REMOVAL ON THE SYSTEM 65 FRONT PANEL

To insert the PROM device:

1. Push the PROM socket lever out from the System 65 front panel, to release pin pressure.
2. Position the PROM device in front of the socket, being careful to observe the Pin 1 location.

CAUTION

Incorrect PROM installation may cause PROM damage and/or may blow Fuses F1 and F2 on the PROM Programmer Module.

3. Insert the PROM into the socket, then push up and in on the socket lever to apply pressure to the pins.

To remove the PROM device, grasp the PROM device at each end, then push the socket lever away from the System 65 front panel to release pin pressure.

PROM INSERTION/REMOVAL ON PROM PROGRAMMER MODULE

To insert the PROM device, position the PROM device in front of the socket, being careful to observe the Pin 1 location.

CAUTION

Incorrect PROM installation may cause PROM damage and/or may blow Fuses F1 and F2 on the PROM Programmer Module.

With the PROM properly oriented, gently start all pins evenly into the socket pin guides. Then press firmly and evenly on the device (avoiding contact with the light window) until the device is securely seated.

To remove the PROM device, exert an even, upward force on both sides of the device while counteracting with a lesser, evenly applied downward force. This will prevent the PROM device from popping out one side and bending or breaking pins still engaged at the other end of the socket.

6

OPERATION

The PROM Programmer software allows checking, reading, verifying and programming 2704, 2708, 2758, 2516, 2532 or 2716 type devices. The data/instructions are copied to/from the System 65 RAM memory in the address range specified by the user. The user can then transfer this information to/from the diskette (or other I/O device) using System 65 software routines.

LOADING THE PROM PROGRAMMER ROUTINES

There is one PROM programmer object file supplied on the PROM Programmer diskette, PROM*n, where "n" is the program release revision letter. File PROM*n occupies from \$0200 to \$0FFF. User programs can be loaded starting at \$1000. To load the PROM*n program, use the System 65 Load Command L. Then enter the file name (PROM*n) and disk drive number desired. Since the PROM*n program may occupy the same memory area in which user's data may reside, an offset may be applied to the user's data to locate it to \$1000 or above (see Load, Verify and Dump functions with offset). PROM*n uses page 0 (\$0080-\$009A) and page 1 (\$0100-\$01FF).

NOTE

The System 65 RUN/STEP switch must be in the RUN position for PROM programming.

After the program is loaded, use the five (5) key to start the PROM Programmer routines for a 1 MHz system or the six (6) key for a 2 MHz system. The 5 (or 6) key may also be used for reentry into the PROM Programmer routines. Once the routines are entered, the only way to exit back to the System 65 monitor is to press the ESC key, if the program is waiting for input, or the Reset switch.

The PROM Programmer PROGRAM PROM(P) and VERIFY PROM (V) functions require that the data to be programmed and/or verified be in RAM memory prior to execution. If the program data resides on diskette (or other media), use the System 65 Monitor L command to load the object code into memory before entering the PROM programmer functions with key 5 (or 6). Alternatively, use the PROM Programmer L command to load the program data with optional offset after the PROM Programmer functions have been entered.

PROM PROGRAMMER OPERATION

Before entering any of the PROM Programmer functions to follow, ensure that the required PROM device is installed in the desired PROM socket—the System 65 front panel socket or the PROM Programmer Module's PROM socket—per the PROM Device Insertion/Removal instructions. The PROM Programmer functions may be entered in the absence of an installed PROM device, but this may cause verify errors.

CAUTIONS

1. Insert a PROM device only when System 65 power is on and either the Monitor prompt (<) or the PROM Programmer prompt (=) is the last character displayed on the system terminal. Failure to do so may cause damage to the PROM device.
2. DC power to the PROM device installed in the PROM socket is set to zero upon System 65 power-up or depression of the Reset switch. During a PROM Programmer function, DC power is supplied to the PROM socket after entry of the last address, then the commanded PROM programming function is performed. The DC power is removed upon completion of the programming function, before the next PROM Programmer prompt character (=) is displayed.

Once started, the routines will ask the user for certain information. This information should be entered on the system terminal. For numbers or addresses, type in the number followed by a space or carriage return to terminate the number. Leading zeros are not necessary. Only the last four digits of the number are used. If a mistake is made before pressing the space bar or carriage return, reenter the correct number (all four digits). If a mistake is made after entering a number, exit the PROM Programmer routines using the ESC key or Reset switch on the front panel and restart with key 5 (or 6). If an invalid command or number is entered the routines will print WHAT? and ask you to reenter.

Following illustration is an example of a PROM Programmer load and initialization along with the user's response.

Next, the data to be copied to the PROM device can be loaded using the L command. In this example, the file USERIN was loaded. Type 5 (or 6) to start the routines. Next, enter the device type. If a 2716 was entered, the message TMS 2716 (Texas Instruments) PROM? will be printed. Enter Y for yes or N for no. The routines will reprint the device type for verification each time a new function is requested. A single character should now be entered to indicate the function requested as outlined in the subsequent text.

```

<L>OFFSET=0000 IN=F FILE=PROM=F DISK=1
DONE
<5>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)
ENTER 2704, 2708, 2758, 2716, 2516, 2532
=2716
TMS 2716 PROM?
N
*****
DEVICE TYPE=
2716
*****
ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)

```

Power-Up and Loading Responses

PROM PROGRAMMER RE-ENTRY

After initialization by the (5) or (6) entry and selection of a PROM type, the PROM Programmer function may be re-entered from the System 65 Monitor by typing 7. This allows the Monitor to be entered from the PROM Programmer to perform utility functions then the PROM Programmer quickly re-entered to continue PROM operations. Initial entry using key 5 or 6 must be used, however, to change PROM type selection. The message WHAT? will be displayed if Key 7 is typed prior to initialization of the PROM Programmer function.

ADDRESS SELECTION

The addresses entered are the hexadecimal locations of the RAM memory used for checking, programming, reading, or verifying. The upper address bits are then stripped off to form the address for the PROM devices. In general, the addresses must comply with the following restrictions:

1. Cannot be Page 0 (\$0000-\$00FF) or Page 1 (\$0100-\$01FF).
2. Cannot overlap the PROM Programmer routine for file name PROM*n (\$0200-\$0FFF).
3. The last address must be greater than or equal to the first address entered.
4. The address range from first to last must not exceed the size of the PROM being programmed.

In addition, there are further restrictions on certain PROM devices, imposed by the PROM manufacturer. The 2704, 2708, and TI TMS2716 must be programmed using their total address space during one programming. This means that the 2704, 2708, and TI TMS2716 must start on a 1/2K, 1K or 2K address boundary, respectively. They also have to extend 1/2K, 1K or 2K bytes in length, respectively. The 2516, 2532, 2758 and Intel 2716 do not have this requirement. Therefore, single byte or multi-bytes may be programmed within the address range of the device. The routines are designed to check for any invalid address entered and will print WHAT? and ask for the address again.

NOTES

1. A verification error showing a series of 1's in a specific PROM bit position after programming may indicate a poor connector contact caused by improper PROM installation in the PROM socket. See the PROM Device Insertion/Removal instructions.
2. If fuse F1 or F2 on the PROM Programmer Module is blown, the PROM may not verify correctly. Verify that both are good if a verify error occurs.

VERIFY FUNCTION (THE V COMMAND)

The routines will request where any errors detected should be printed. This is indicated by the message ERROR LIST OUT=. Enter any of the standard I/O device characters defined in the System 65 User's Manual (space for CRT, P for Printer, etc.). Next, type in the first and last addresses. As soon as the last address is entered, power will be applied to the PROM device and the contents of the PROM compared to the respective content of the RAM. If no errors are found, the message DONE will be printed, and the next operation requested. If errors are detected, the address, contents of PROM, and contents of RAM in disagreement will be displayed/printed on the selected I/O device.

```

(35)
FROM PROGRAM FOR 1 MHZ SYSTEM (VER E3)

ENTER 2784, 2788, 2758, 2716, 2516, 2532
=2716
1MS 2716 FROM?
=N

*****
DEVICE TYPE=
2716
*****

ENTER FROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)
=V
VERIFY
ERROR LIST
OUT=L
ENTER FIRST ADDRESS
=1000
ENTER LAST ADDRESS
=17FF
ERROR
ADDR FROM RAM
1000 C8 20
1400 C8 4C
17FF C8 15

DONE

*****
DEVICE TYPE=
2716
*****

ENTER FROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)

```

READ FUNCTION (THE R COMMAND)

After the first and last addresses are entered, power will be applied to the PROM and the contents copied into the specified RAM locations. When completed, the message DONE will be printed and the next operation requested.

6-35

The PROM Programmer READ function reads program data into System 65 RAM memory from PROM. After reading is complete, save the PROM data on diskette (or other media) using the System 65 Monitor D Command after exiting the PROM Programmer functions. Alternatively, use the PROM Programmer D command to dump the data with optional offset before the PROM Programmer functions are exited. The amount to be stored or loaded at one time is limited only by the RAM locations available.

```

<S>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)
ENTER 2704, 2708, 2758, 2716, 2516, 2532
=2716
TMS 2716 PROM?
=N

*****
DEVICE TYPE=
2716
*****
ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)
=R
READ
ENTER FIRST ADDRESS
=1000
ENTER LAST ADDRESS
=17FF
DONE
*****
DEVICE TYPE=
2716
*****
ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)

```

Read Function Example

CHECK FUNCTION (THE C COMMAND)

The Check Function (C) is used to check that the PROM is initialized. It is entered by pressing the C key in response to the ENTER command message.

After the first and last addresses are entered, power is applied to the device and all specified locations are checked for \$FF. The message PROM NOT INITIALIZED will be printed if all locations do not contain \$FF. The message DONE will be printed when the Check Function is complete.

```

<S>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)
ENTER 2704, 2708, 2758, 2716, 2516, 2532
=2716
TMS 2716 PROM?
=N

*****
DEVICE TYPE=
2716
*****
ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)
=C
CHECK
ENTER FIRST ADDRESS
=1000
ENTER LAST ADDRESS
=17FF
PROM NOT INITIALIZED
DONE
*****
DEVICE TYPE=
2716
*****
ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)

```

Check Function Example

LOAD MEMORY WITH OFFSET FUNCTION (THE L COMMAND)

The Load Memory with Offset Function (L) copies data from an input object code file into memory addresses offset by an entered amount from the addresses on the input file. The entered offset value is additive with carry from bit 15 ignored, e.g.:

Input File Address	Offset Value	Address in Memory
\$1000	0	\$1000
\$1000	\$2000	\$3000
\$7000	\$A000	\$1000
\$E000	\$2000	\$1000

```

<S>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)
ENTER 2704, 2708, 2758, 2716, 2516, 2532
=2716
TMS 2716 PROM?
=N

*****
DEVICE TYPE=
2716
*****
ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)
=L
LOAD
OFFSET=0800 IN=F FILE=AIMBAS DISK=2
*****
DEVICE TYPE=
2716
*****
ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)

```

Load Memory with Offset Function Example

VERIFY MEMORY WITH OFFSET FUNCTION (THE F COMMAND)

The Verify Memory with Offset Function (F) compares the contents of an object code file with the contents of memory at addresses in memory offset by an entered amount from the addresses on the reference object code file. The entered offset is additive in the same manner as the Load with Offset function. The contents of both memory (MEM) and reference file (FILE) are displayed/printed along with the address (ADDR) if any differences in value are detected.

```

<S>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)
ENTER 2704, 2708, 2758, 2716, 2516, 2532
=2716
TMS 2716 PROM?
=N

*****
DEVICE TYPE=
2716
*****
ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)
=F
VERIFY
OFFSET=0800 IN=F FILE=AIMBAS DISK=2
ERROR LIST
OUT=L ADDR/MEM/FILE
2800 E8 50 2200 4C 52
*****
DEVICE TYPE=
2716
*****
ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)

```

Verify Memory with Offset Function Example with Errors

DUMP MEMORY WITH OFFSET FUNCTION (THE D COMMAND)

The Dump Memory with Offset Function (D) copies data from memory to an output object code file with addresses in the output file offset an entered amount from the addresses in memory. The entered offset value is additive from the output file to memory with carry from bit 15 ignored; e.g.:

Output File Address (FROM=)	Offset Value	Address in Memory
\$1000	0	\$1000
\$4000	\$D000	\$1000
\$1000	\$8000	\$9000
\$A000	\$1000	\$B000

```
<S>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)

ENTER 2704, 2708, 2758, 2716, 2516, 2532
=2716
TMS 2716 PROM?
=N

*****
DEVICE TYPE=
2716
*****

ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)
=D
DUMP
OFFSET=D000 OUT=F FILE=PRMOUT DISK=2
FROM=4000 TO=47FF

MORE?N

*****
DEVICE TYPE=
2716
*****

ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)
```

Dump Memory with Offset Function Example

MEMORY FILL FUNCTION (THE M COMMAND)

The Memory Fill Function (M) allows a user selected range of RAM to be initialized to an entered bit pattern. The desired PROM object code can then be loaded. All unloaded memory in the PROM address range will remain initialized with the previously filled bit pattern. This allows PROM codes over a total PROM address range to be easily verified without invalid data errors being indicated due to random bit patterns in unused addresses.

Enter the bit pattern to be loaded in hexadecimal in response to the MEM FILL= prompt. The last two digits entered will be accepted. Terminate the entry with a carriage return. Then enter the starting and ending addresses in hexadecimal of the RAM to be filled. Terminate entries with a carriage return. The last four digits entered will be accepted.

```
<S>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)

ENTER 2704, 2708, 2758, 2716, 2516, 2532
=2716
TMS 2716 PROM?
=N

*****
DEVICE TYPE=
2716
*****

ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)
=M
MEM FILL=00
FROM=1000 TO=13FF

*****
DEVICE TYPE=
2716
*****

ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)
```

Memory Fill Function Example

INVERT MEMORY (THE I COMMAND)

The Invert Memory Function (I) allows selected bits to be inverted within a selected address range. This function allows the contents of RAM to be easily one's complemented if the PROM code is to be inverted from the ROM code.

Enter the bit pattern to be exclusively or'ed with memory. A "1" in a bit position will invert the bit value while a "0" will leave the bit value unchanged. Enter "FF" to invert all bit values and "00" to invert none of the bit values. Terminate the entry with a carriage return. The last two digits entered will be accepted. Enter the starting and ending addresses as described for the MEM FILL function.

```
<S>
PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER E)

ENTER 2704, 2708, 2758, 2716, 2516, 2532
=2716
TMS 2716 PROM?
=N

*****
DEVICE TYPE=
2716
*****

ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)
=I
INVERT BITS=FF
FROM=1000 TO=13FF

*****
DEVICE TYPE=
2716
*****

ENTER PROM COMMAND: VERIFY(V), PROGRAM(P), READ(R), OR CHECK(C)
OR MEMORY COMMAND: VERIFY(F), LOAD(L), DUMP(D), MEM FILL(M), INVERT(I)
```

Invert Bits Function Example

SPECIFICATIONS

Parameter	Value
PROM Devices Supported	2704, 2708, 2758, Intel 2716 and Texas Instruments 2716
Programming Time (approximately)	2704—100 sec. 2708—200 sec. 2758— 60 sec. Intel 2716—120 sec. T.I. 2716—400 sec. 2516—120 sec. 2532—240 sec.
Interface	System 65 compatible
Module Dimensions	9.75 in. wide × 6.00 in. high
Edge Connector	86 pins on 0.156 in. centers
Operating Temperature	0° to + 70°C
Power Requirements	+5 Vdc ± 5% @ 750 ma (fused at 2 amps) +12 Vdc ± 5% @ 50 ma (fused at ½ amp) -12 Vdc ± 5% @ 50 ma.
Fuse Description	F1—AGC ½A—250V (Bussman) F2—AGC 2A—250V (Bussman)

M65-045 PROM/ROM MODULE



OVERVIEW

The M65-045 PROM/ROM Module permits system read only memory to be increased by up to 16K bytes. The module provides 16 24-pin DIP sockets for accepting industry-standard 2708, 2716, or 2758 PROM devices, or 2316 or 2332 ROM devices. PROMs and ROMs cannot be mixed on the module.

The PROM/ROM Module's 16K-byte address space is segmented into four independent 4K-byte sections. Each 4K-byte section is provided with a switch for selecting its base address. Further, each socket has an individual enable/disable switch, providing resolution down to 1K bytes.

FEATURES

- System 65 compatible
- 16K-byte read only memory capacity
- Accepts 2708, 2716 or 2758 PROM devices
- Accepts 2316 or 2332 ROM devices
- Sockets can be individually enabled/disabled
- Base address is switch-selectable for each 4K-byte address space
- Single +5V supply

FUNCTIONAL DESCRIPTION

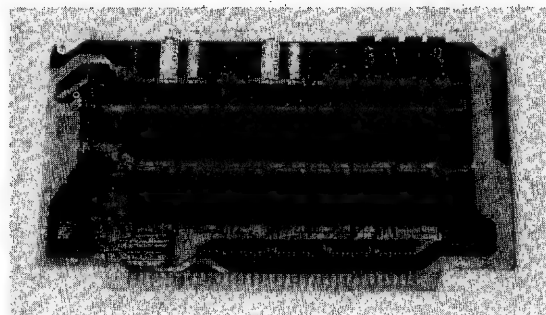
The edge connector pin assignments for the PROM/ROM Module are identical to the motherboard pin assignments given in Section 4 of the System 65 User's Manual (Document No. 29650N35, Order No. 206).

The PROM/ROM Module comes with 16 sockets for accepting the following types of memory devices:

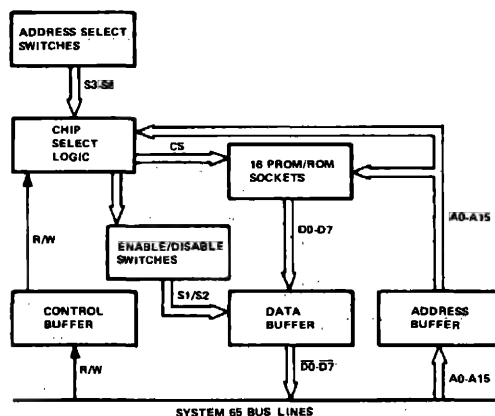
- Up to four 2332 ROMs, or
- Up to eight 2316 ROMs, or
- Up to eight 2716 PROMs, or
- Up to 16 2708 or 2758 PROMs

The address switches on the module are set in accordance with the type and number of PROM or ROM devices installed. Each socket may also be selected by a switch. Further, each 4K address space also has a separate switch for selection of its base address. The Chip Select Logic specifies the PROM/ROM to be accessed and the address lines from the System bus select the memory location. The selected PROM/ROM device responds by placing 8 bits of data on the data lines ($\overline{D0}$ through $\overline{D7}$) for transfer to the CPU.

6



M65-045 PROM/ROM Module



PROM/ROM Module Functional Block Diagram

SWITCHES AND JUMPERS

The PROM/ROM Module can accommodate a variety of standard PROM and ROM devices. The user must configure the Module for his specific application, and does so with various switches and jumpers on the Module itself.

The PROM/ROM Module has a total address space of 16K bytes, divided into four 4K-byte sections. Each 4K section has a separate base address select switch, S3 through S6, which must be set to the desired hexadecimal value (0 - F). For example, if Switch S3 is set to C, the base address for Sockets Z4, Z5, Z6 and Z7 is \$C000 (where \$ indicates hexadecimal). Further, each individual socket can be enabled or disabled from driving the Data Bus by setting/resetting Switches S1 and S2.

There is a further restriction for ROMs: Since ROMs have chip selects, they will only work in the proper sockets with proper base address switch settings. For example, a 2316 ROM with CS3=1, CS2=0 and CS1=1 will work only in Socket Z22 (see Table 4) and with a selected base address value of 2, 6, A or E.

The PROM/ROM Module must also be jumper-configured for the device being used. Jumper information is given with switch select tables. The function of each jumper is summarized in Table 1.

Table 1. PROM/ROM Board Jumper Functions

Jumper No.	Jumper Function
1	Connects A12 to Pin 18 of all sockets
2	Enables 1K address selection
3	Connects +12VDC to Pin 19 of all sockets
4	Enables 2K address selection
5	Connects A13 to Pin 21 of all sockets
6	Connects A10 to Pin 19 of all sockets
7	Connects A11 to Pin 21 of all sockets
8	Connects +5VDC to Pin 21 of all sockets
9	Connects A11 to Pin 18 of all sockets
10	Connects -5VDC to Pin 21 of all sockets
11	Connects GND to Pin 18 of all sockets
12	Enables active low chip selects on Sockets Z7, Z14, Z22 and Z29

Table 2. Switch Settings for 2716 PROM Operation

Base Address (A15, A14, A13, A12)	Address A11	Socket	Enable/Disable Switch
S3 (0-F)	0	Z5	S1-2
	1	Z7	S1-4
S4 (0-F)	0	Z11	S1-6
	1	Z14	S1-8
S5 (0-F)	0	Z18	S2-2
	1	Z22	S2-4
S6 (0-F)	0	Z24	S2-6
	1	Z29	S2-8

Note: For 2716 PROMs, add Jumpers 4, 6, 8, 11 and 12.

Table 3. Switch Settings for 2708 or 2758 PROM Operations

Base Address (A15, A14, A13, A12)	Address A11 A10	Socket	Enable/Disable Switch
S3 (0-F)	0 0	Z4	S1-1
	0 1	Z5	S1-2
	1 0	Z6	S1-3
	1 1	Z7	S1-4
S4 (0-F)	0 0	Z10	S1-5
	0 1	Z11	S1-6
	1 0	Z13	S1-7
	1 1	Z14	S1-8
S5 (0-F)	0 0	Z17	S2-1
	0 1	Z18	S2-2
	1 0	Z21	S2-3
	1 1	Z22	S2-4
S6 (0-F)	0 0	Z23	S2-5
	0 1	Z24	S2-6
	1 0	Z28	S2-7
	1 1	Z29	S2-8

Note: For 2708 PROMs, add Jumpers 2, 3, 4, 11 and 12 and add Capacitors C6-C9, C14-C17, C21-C24, C29-C32, C37-C40, C45-C48, C52-C55 and C59-C62. All capacitors are 0.1 μ f.
For 2758 PROMs, add Jumpers 2, 8, 11 and 12 and jumper left post of Jumper 3 to right post of Jumper 4.

Table 4. Switch Settings for 2316 ROM Operation

Base Address (A15, A14, A13, A12)	ROM Chip Selects*			Socket	Enable/Disable Switch
	A13 CS3	A12 CS2	A11 CS1		
S3 (0, 4, 8, C)	0	0	0	Z5	S1-2
	0	0	1	Z7	S1-4
S4 (1, 5, 9, D)	0	1	0	Z11	S1-6
	0	1	1	Z14	S1-8
S5 (2, 6, A, E)	1	0	0	Z18	S2-2
	1	0	1	Z22	S2-4
S6 (3, 7, B, F)	1	1	0	Z24	S2-6
	1	1	1	Z29	S2-8

Note: *Assumes CS1=A11, CS2=A12 and CS3=A13. For 2316 ROMs, add Jumpers 1, 4, 5 and 6.

Table 5. Switch Settings for 2332 ROM Operation

Base Address (A15, A14, A13, A12)	ROM Chip Selects*		Socket	Enable/Disable Switch
	A13 S2	A12 S1		
S3 (0, 4, 8, C)	0	0	Z7	S1-4
S4 (1, 5, 9, D)	0	1	Z14	S1-8
S5 (2, 6, A, E)	1	0	Z22	S2-4
S6 (3, 7, B, F)	1	1	Z29	S2-8

Note: *Assumes S1=A12 and S2=A13. For 2332 ROMs, add Jumpers 2, 5, 6 and 9.

INSTALLATION

Install PROM/ROM Modules in the System 65 chassis or, with appropriate changes, in an Auxiliary Card Cage as follows:

1. Turn System 65 power off.

CAUTION

Never install or remove modules with System 65 power on—it may cause damage to the module and/or to the System.

2. Remove the top cover of the System 65.
3. Set the switches on the PROM/ROM Module per Tables 2 through 5. The base memory address are assigned by four hexadecimal switches, S3 through S6. Individual sockets are enabled/disabled by Switches S1 and S2.
4. Install the required jumpers per directions given with the switch table.
5. Install the required PROM or ROM devices in their appropriate sockets.

6. Insert the PROM/ROM Module(s) into any vacant slot(s) in the System 65 chassis.
7. Install the top cover of the System 65.
8. Turn System 65 power on.

SPECIFICATIONS

Parameter	Value
Memory Capacity	16K bytes
Word Length	8 bits
Interface	System 65 compatible
Module Components	16 24-pin DIP sockets
Module Dimensions	9.75 in. wide × 6.00 in. high
Edge Connector	86 pins on 0.156-in. centers
Operating Temperature	0°C to +70°C
Power Requirements	+5 Vdc + 5% @ 500 ma. with no devices installed

LOGIC LEVELS $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$

Characteristic	Symbol	Min	Max	Unit	Condition
Inputs ($\overline{D0-D7}$, A0-A15, $\phi2$, $\overline{R/W}$)					
Input Low Voltage	V_{IL}		0.8	V	$I_{IL} = 400 \mu\text{a}$
Input High Voltage	V_{IH}	2.0	V_{CC}	V	$I_{IH} = 40 \mu\text{a}$
Outputs ($\overline{D0-D7}$)					
Output Low Voltage	V_{OL}		0.5	V	$I_{OL} = 48 \text{ ma}$
Output High Voltage	V_{OH}	2.4	V_{CC}	V	$I_{OH} = 10 \text{ ma}$



M65-060 EXTENDER CARD

OVERVIEW

The M65-060 Extender Card provides easy access to a printed circuit module installed in its system enclosure, for signal tracing or troubleshooting. In that context, the Extender Card consists of a series of bus lines connecting the Card's standard contact edge, on one end, and a connector used for accepting the standard contact edge of an 86-pin system module.

This contact edge and the edge connector pins are connected pin-for-pin via the bus lines on the Card. Each of the bus lines is provided with a clip-on terminal to allow test equipment to be readily connected. With the module under test connected to the Extender Card and this assembly installed in the system's Auxiliary Card Cage or System 65 chassis, the user is given free access to both sides of the module being tested.

The edge connector pin assignments for the System 65 Motherboard are given in Section 4 of the System 65 User's Manual (Document No. 29650N35).

SPECIFICATIONS

Parameter	Value
Edge Contacts	86 pins on 0.156-in. centers
Edge Connector	86 pins on 0.156-in. centers
Extender Card Dimensions	9.75 in. wide × 9.00 in. high × 0.062 in. thick

INSTALLATION

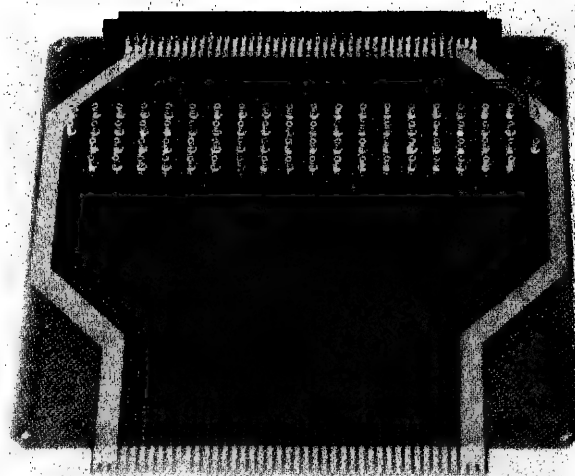
The procedure below should be used to install an Extender Card in the System 65 chassis or, with appropriate changes, in an Auxiliary Card Cage.

1. Turn System 65 power off.

CAUTION

Never install or remove modules with System 65 power on—it may cause damage to the module and/or to the System.

2. Remove the top cover of the System 65.
3. Remove the desired circuit module from System 65, if installed.
4. Insert the Extender Card into any vacant slot in the System 65 chassis.
5. Insert the desired circuit module into the plug on top of the Extender Card.
6. Turn System 65 power on.



M65-060 Extender Card



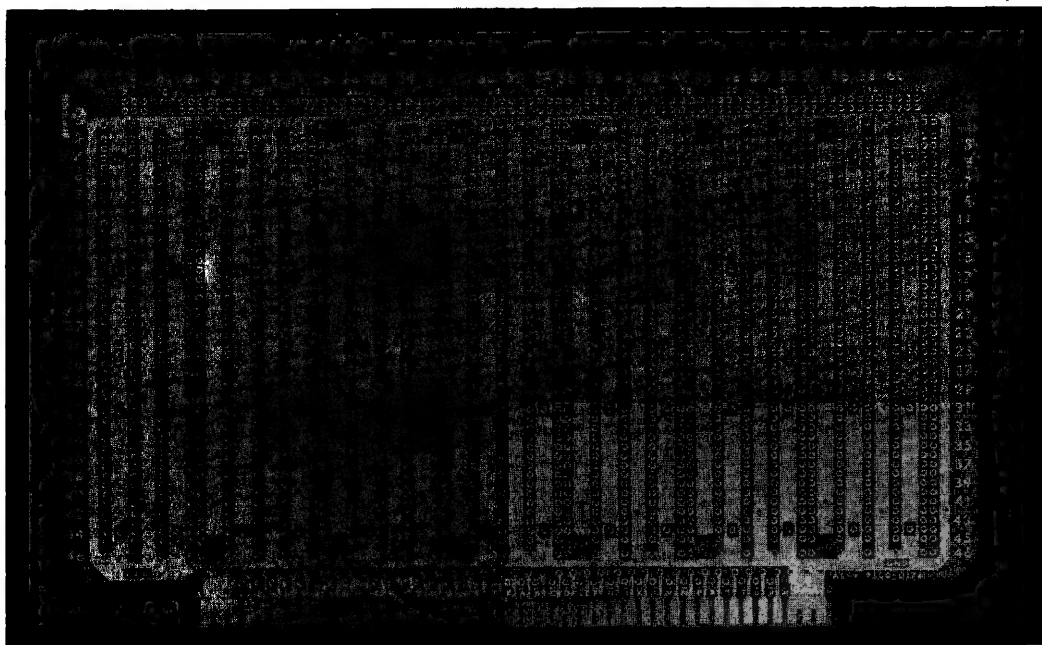
M65-071 DESIGN PROTOTYPING MODULE

OVERVIEW

The M65-071 Design Prototyping Module allows development of custom circuits for installation in either Rockwell's System 65 Microcomputer Development System or in user-designed equipment, via the Auxiliary Card Cage.

This Module is a System 65-compatible printed circuit module with no mounted components, but with prerouted power bus and power return lines. Spaced beside the power lines are plated-through holes that permit wire-wrap sockets to be installed. Additional holes, at the top edge of the module, permit a variety of wire-wrap flat ribbon cable connectors to be installed.

The pin assignments for the Design Prototyping Module's 86-pin edge connector are identical to the Motherboard pin assignments given in Section 4 of the System 65 User's Manual (Document No. 29650N35; Order No. 206).



M65-071 Design Prototyping Module

INSTALLATION

Install a Design Prototyping Module in the System 65 or, with appropriate changes, in an Auxiliary Card Cage as follows:

1. Turn System 65 power off.

CAUTION

Never install or remove modules with System 65 power on—it may cause damage to the module and/or to the System.

2. Remove the top cover of the System 65.
3. Insert the Design Prototyping Module into any vacant slot in the System 65 chassis.

CAUTION

Installation of improperly-operating circuits may cause malfunction and/or damage to the System 65.

4. Install the top cover of the System 65.
5. Turn System 65 power on.

SPECIFICATIONS

Parameter	Value
Component Mounting Area	
Number of Component Rows	14
Number of Hole Rows	35
Vertical Hole Spacing	46 holes on 0.1-in. centers
Horizontal Hole Spacing	35 holes on either 0.3-in. or 0.1-in. centers
Flat Ribbon Connector Mounting Area	
Number of Pins Per Connector	170
Module Dimensions	7.50 in. high × 9.75 in. wide × 0.062 in. thick
Edge Connector	86 pins on 0.156-in. centers



M65-660 SYSTEM 65 MACRO ASSEMBLER & LINKING LOADER

DESCRIPTION

The System 65 Macro Assembler and Linking loader is a disk-based computer program that generates computer program absolute machine code or relocatable object code and links relocatable object code into absolute machine code. The assembler/loader operates on the System 65 Development System and generates code for execution by any central processing unit (CPU) in the Rockwell R6500 NMOS microprocessor, R6500/* NMOS one-chip microcomputer and R65C00 CMOS microprocessor device families.

MACRO ASSEMBLER

The macro assembler translates CPU instructions and data statements written in symbolic form (the source program), into absolute or relocatable code. Instructions, consisting of a label (if included), a mnemonic operation code, an operand (if required) and an arithmetic operator (if included), are assembled one-at-a-time into one- to three-byte machine instructions (with absolute or relocatable address information). Constants comprising one or more bytes of memory are generated from data statements while one or more bytes of memory are assigned to variables. The macro capability allows sequences of instructions to be pre-defined for in-line code inclusion by specifying only the macro name. Conditional assembly allows portions of instruction sequences or macros to be included in (or excluded from) in-line code. The combination of the macro and conditional assembly capability speeds program development by eliminating duplicate coding efforts for similar processing tasks and increases program flexibility and reliability by allowing one source program to generate different computer programs based on specified control parameters.

LINKING LOADER

The linking loader combines independently assembled modules of absolute and/or relocatable object code into a single executable object file. This allows a large program to be developed in manageable size modules by separate software designers and integrated by the linking process. This also allows program changes to be made to one module without affecting any of the other modules—a key requirement in many program validation and certification procedures.

Small programs can still be assembled into absolute executable code without using the linking loader, however, to simplify development.

The assembler/loader operates in conjunction with the ROM-resident System 65 Debug Monitor/Text Editor (OS 3.1).

MACRO ASSEMBLER FEATURES

- Supports three CPU families
 - R6500 NMOS microprocessor
 - R6500/* NMOS microcomputer
 - R65C00 CMOS microprocessor
- Flexible object code generation
 - Absolute code (executable)
 - Relocatable code (linkable)
- Macro definition includes
 - Multiple parameters
 - Other macros
 - CPU instructions
 - Assembler directives
- Macro call includes
 - Macro name
 - Argument list
- Condition assembly
 - IF condition
 - ELSE complementary condition
 - 12 conditional operators
- Symbol cross reference table
 - Lists defined and used symbols
 - Listed in alphanumeric order

LINKING LOADER FEATURES

- Resolves inter-module symbol linkage
- Assigns absolute addresses
- Generates absolute executable code
- Produces reports
 - Load map of module locations
 - Symbolic debug table
 - Symbol table
- Interactive or command file setup

ORDERING INFORMATION

Part No.	Description
M65-660-3	Macro Assembler and Linking Loader ⁽¹⁾
Order No.	Description
249	Macro Assembler and Linking Loader User's Manual ⁽²⁾
Notes:	
1. Requires System 65 OS 3.1 ROMs	
2. Included with M65-660-3.	

Assembler Directives**Assembly Listing Control**

.TTL	Title
.SBTTL	Subtitle
.PAG	Page
.SKI	Skip
.ERR	Error

Source File Control

.END	End of Assembly
.FILE	Next File
.INCL	Include

Data Storage

.BYTE	Initialize byte memory location
.WORD	Generate 16-bit address
.DBYTE	Generate 16-bit data word
.SBYTE	Initialize ASCII string

Equate

=	Assign value to symbol
---	------------------------

Conditional

.IF	Condition
.ELSE	Complementary condition
.EIF	End of conditional

Macro

.MACRO	Define Macro
.ENDM	End of macro definition
.MEXIT	End of macro expansion
.NARG	Number of passed arguments

Option Control

.OPT	Option	
	LIST/NOLIST	Assembly listing
	GEN/NOGEN	Object code listing
	ERR/NOERR	Error generation
	SYM/NOSYM	Symbol generation
	CREF/NOCREF	Cross reference generation
	ABS	Absolute object code
	REL	Relocatable object code
	MEM	Absolute object code to memory
	TOC/NOTOC	Table of contents
	OBJ/NOOBJ	Object code generation
	MD/NOMD	Macro definition
	ME/NOME	Macro expansion
	CC/NOCC	Conditional list
	PLEN	Page length
	LLEN	Line length
	FF/NOFF	Form feed
	CLS	Clear definitions
.RAD		Radix 2, 8, 10, or 16

Relocation/Linking

.DEF	Internal definition
.REF	External reference
.ZREF	Zero page reference
.PSECT	Program section
.IDENT	Module identification

Linking Loader Directives

ERR	Errors destination
OBJ	Object code generation
MAP	Load map generation
CALS	Symbol table location
SYM	Global symbol table
DEBUG	Debug symbol table

ORG	Origin
ORDER	Section order
DEF	Symbol definition
LOAD	Load code specification
END	Command file end



SPS-200
SOFTWARE PREPARATION SYSTEM (SPS)
PERIPHERAL CONNECTOR MODULE

The optional SPS Peripheral Connector Module (PCM) (Part No. SPS-200), which connects directly to the AIM 65 Microcomputer Master Module connector, provides the Software Preparation System (SPS) with a complete set of external I/O interfaces. These I/O interfaces support external printers, serial devices, audio cassette 20 mA current loop and parallel I/O devices such as the RM 65 board family.

The external printer interface routes and buffers (TTL levels) the printer signals to a Centronics compatible 34-pin connector for printer support.

The RS-232 interface operates at the $\pm 5V$ level. No handshaking signals are provided, but selectable handshake signals have been wired for static levels. Feed throughs are provided to cut and jumper these signals. Data Set/Data Terminal operation is selected using a jumper pair.

The 20mA current loop interface routes four 20mA current loop signals from the AIM 65 Master Module connector (J1) to a dedicated Molex connector to provide current loop I/O support.

The audio cassette recorder interface signals are routed to two mini-phone (3.5 mm) jacks for audio cassette support. The remote control lines are controlled by reed relays and routed to two sub-mini-phone (2.5 mm) jacks.

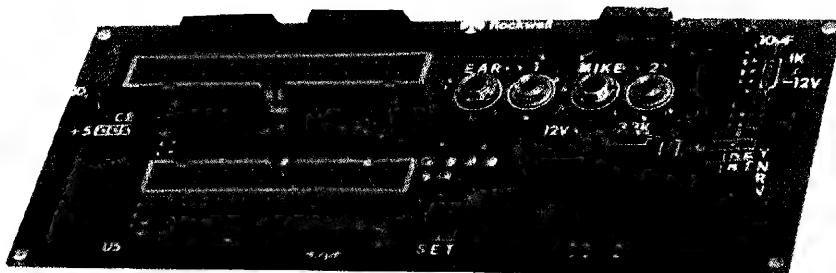
The parallel I/O connector interface supports the 40-pin signals routed to the interface by the AIM 65 Master Module User

VIA (Z22). The parallel interface connector is compatible with many of the RM 65 modules, e.g., single Board Computer (SBC) and Multi-function Peripheral Interface (MPI), and with the AIM 65/40 Microcomputer connector, e.g., User Parallel I/O, Display Interface and Printer Interface.

- 34-pin connector for Centronics compatible printer support
- RS-232 connector for serial interface support
- Molex connector for 20 mA current loop support
- 3.5 mm mini-phone jack connectors for audio cassette support
- 2.5 mm sub-mini-phone jack connectors for remote tape control
- 40-pin parallel I/O connector, compatible with the RM 65 module family

The following documents contain information regarding set-up and operation of SPS-200.

Order No.	Title
2167	R6500 Software Preparation System (SPS) User's Manual
209	AIM 65 Microcomputer User's Guide

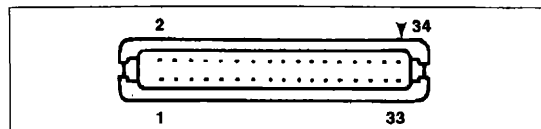


SPS-200 Peripheral Connector Module

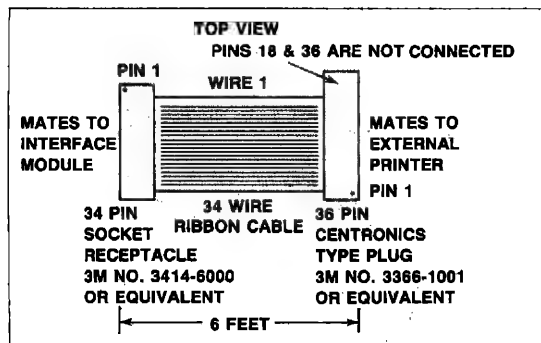
EXTERNAL PRINTER INTERFACE

SPS Module Printer Connector

Pin	Signal	Pin	Signal
1	STROBE	13	Data 6
2	Ground	14	Ground
3	Data 1	15	Data 7
4	Ground	16	Ground
5	Data 2	17	Data 8
6	Ground	18	Ground
7	Data 3	19	ACK
8	Ground	20	Ground
9	Data 4	21	Not Used
10	Ground	22	Ground
11	Data 5	23 to 34	Not Used
12	Ground		



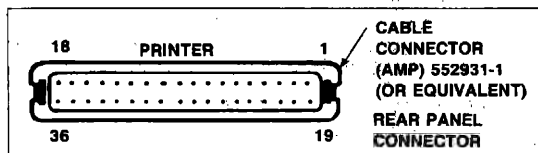
Interface Module Connector



Printer Interface Cable (User Supplied)

Centronics Type Connector Pin Assignment

Pin	Signal	Pin	Signal
J-1	STROBE	J-8	Data 7
J-2	Data 1	J-9	Data 8
J-3	Data 2	J-10	ACK
J-4	Data 3	J-11 to -17	Not Used
J-5	Data 4	J-19 to -29	Ground
J-6	Data 5	J-30 to -35	Not Used
J-7	Data 6	J-18 and J-36	Not Connected

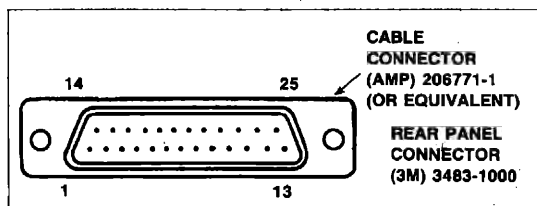


External Printer Connector

RS-232 INTERFACE

RS-232 Connector Pin Assignments

Pin	Signal Mnemonic	Signal Name	Input/Output	
			Data Set	Data Term
1	GND	Chassis Ground		
2	TD	Transmit Data	I	O
3	RD	Receive Data	O	I
5	CTS	Clear to Send ¹	+5V Always	+5V Always
6	DSR	Data Set Ready ¹	+5V Always	+5V Always
7	GND	Signal Ground		
8	DCD	Data Carrier Detected ¹	+5V Always	+5V Always
9-25		Not Used		

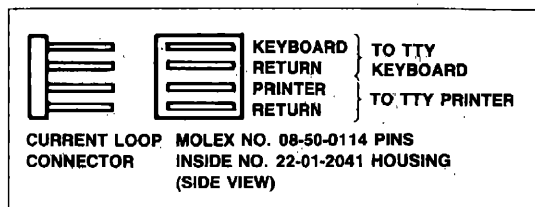
¹This can be cut for a No Connect option

RS-232 Connector Pin Locations

20 mA CURRENT LOOP INTERFACE

20 mA Current Loop Connector Pin Assignments

Pin	Signal Mnemonic	Signal Name
1	TTY KYBD	TTY Keyboard
2	TTY KYBD RETURN (+)	TTY Keyboard Return (+)
3	TTY PTR	TTY Printer
4	TTY PTR RETURN (+)	TTY Printer Return (+)



20 ma Current Loop Connector Pin Locations

PARALLEL I/O CONNECTOR INTERFACE

Parallel I/O Connector Pin Assignments

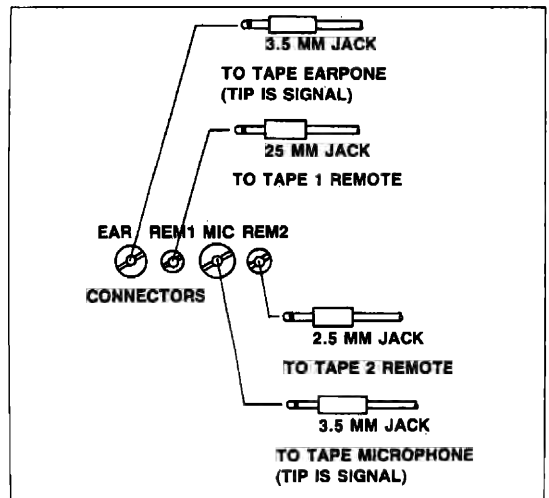
Pin	Mnemonic	Signal Name	Input/Output
1*	CB2	Port B, Control No. 2 ¹	I/O
2		No Connect	
3*	CB1	Port B, Control No. 1	I/O
5*	PB7	Port B, Bit 7	I/O
7*	PB6	Port B, Bit 6	I/O
9*	PB5	Port B, Bit 5	I/O
11*	PB4	Port B, Bit 4	I/O
13*	PB3	Port B, Bit 3	I/O
15*	PB2	Port B, Bit 2	I/O
17*	PB1	Port B, Bit 1	I/O
19*	PB0	Port B, Bit 0	I/O
21	PA7	Port A, Bit 7	I/O
23	PA6	Port A, Bit 6	I/O
25	PA5	Port A, Bit 5	I/O
27	PA4	Port A, Bit 4	I/O
29	PA3	Port A, Bit 3	I/O
31	PA2	Port A, Bit 2	I/O
33	PA1	Port A, Bit 1	I/O
35	PA0	Port A, Bit 0	I/O
37	CA2	Port A, Control No. 2	I/O
39	CA1	Port A, Control No. 1	I/O
40		No Connect	

Note: Even Numbered pins connected to GND.

*These signals are used by the Printer Interface.

¹ This can be cut/jumpered to +5V.

AUDIO CASSETTE RECORDER INTERFACE



Audio Cassette Recorder Interface

WARNING

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

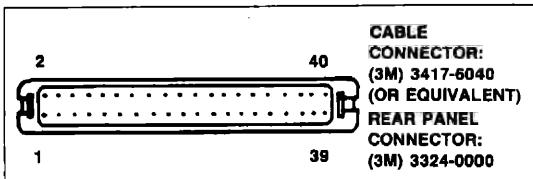
INFORMATION TO USER: If this equipment does cause interference to radio or television reception which can be determined by turning the equipment on and off, the user is encouraged to try to correct the interference by one or more of the following measures:

- reorient the receiving antenna
- relocate the computer with respect to the receiver
- move the computer with respect to the receiver
- plug the computer into a different outlet so that the computer and receiver are on different circuits

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

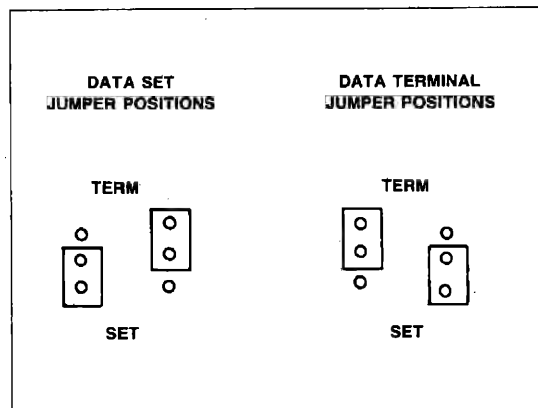
"How to Identify and Resolve Radio and TV Interference Problems:

This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock Number 004-000-0345-4.



Parallel I/O Connector Pin Locations

DATA SET/DATA TERMINAL SETUP



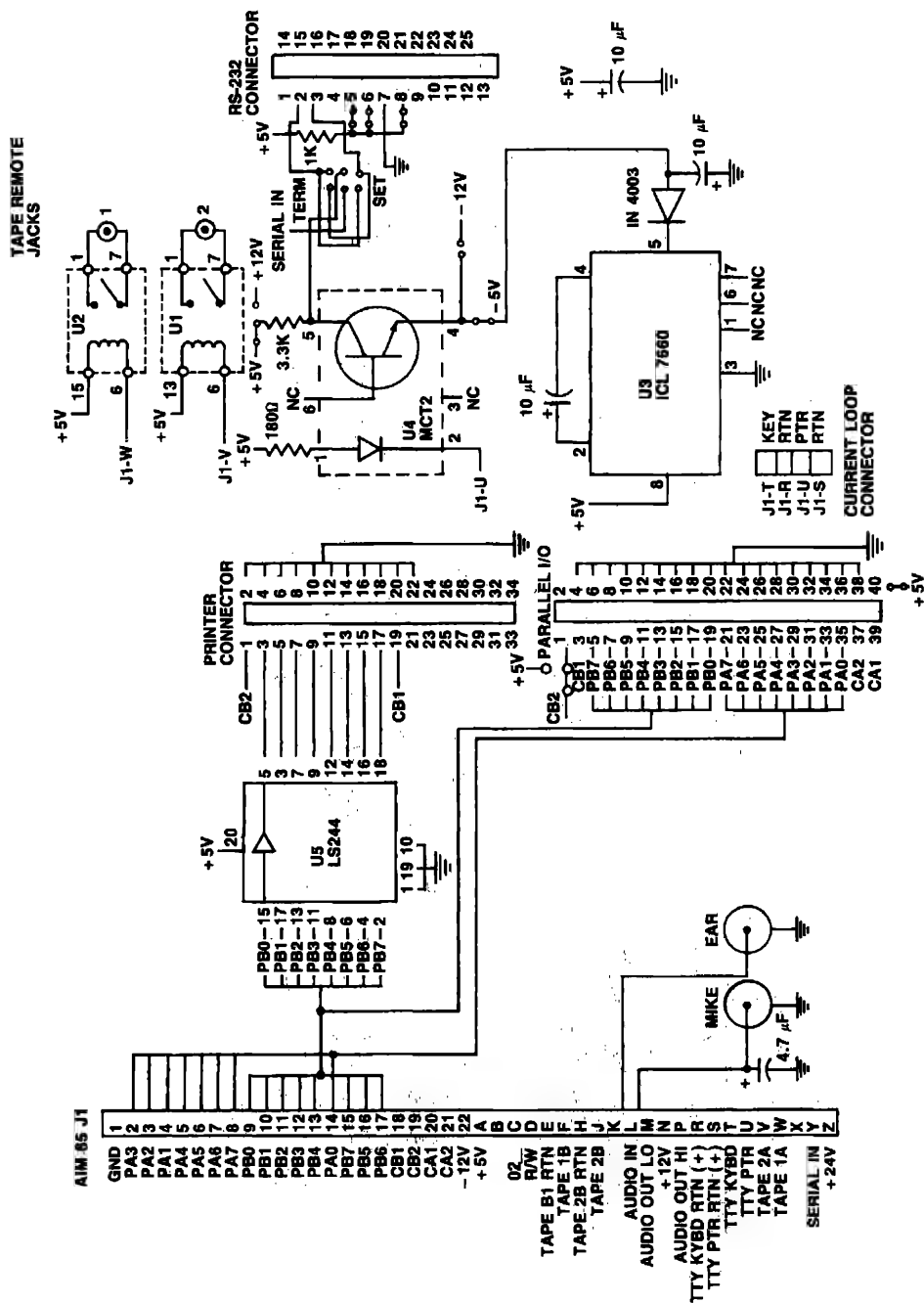


Figure 1. Peripheral Connector Module Schematic

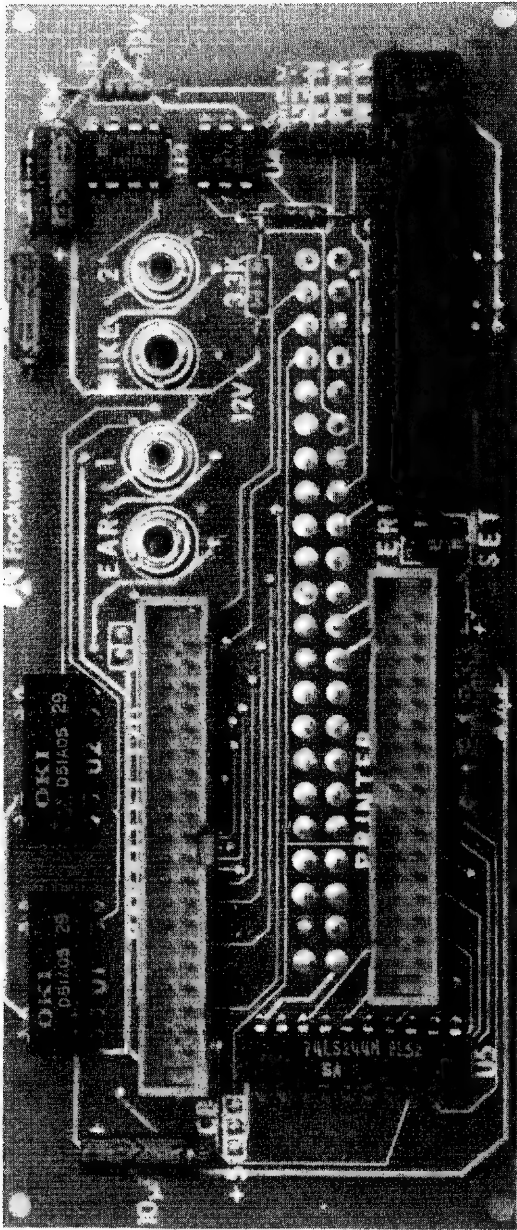


Figure 2. SPS-200 Peripheral Connector Module

SECTION 7

AIM 65 MICROCOMPUTER FAMILY

	Page
Product Family Overview	7-2
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AIM 65 MICROCOMPUTER FAMILY

Professional, Hard Working, Low Cost, Blue Collar Microcomputer

For low cost prototypes or low to medium volume production, Rockwell offers an extended family of board level "blue collar" products, easy to design-in and implement. All are built around the R6502 CPU and R6500 peripherals so that applications using the modules can be readily redesigned into devices as volume warrants. And, all of the board products are available with a wide range of languages—Microsoft BASIC, FORTH, PL/65, assembly, instant Pascal—for optimum system solutions.

The AIM 65 (R6500 based Advanced Interactive Microcomputer) is an under \$500 microcomputer, complete with keyboard, display and hard copy printer. It has extensive options, many interfaces and expansion capabilities. If you're planning on computerizing a product, AIM 65 is designed to do the job. If you're interested in designing a system around the R6500 family of devices,

AIM 65 is also a mini-development system at the price of most evaluation boards. And, AIM 65 comes with complete documentation, making it simple to use. Since it is a "best seller" widely used in universities and industry, a large library of commercially available texts and manuals has developed, making it even easier to use.

In addition to bare board blue-collar versions, the AIM 65 is available in an enclosure, complete with power supply, for use as a desk top computer. Additional memory cartridges are available to plug onto the desk top AIM 65 providing additional languages or memory. These can let AIM 65 function as a test instrument, analyzer or controller.

Whatever your application, for a learning tool, evaluation system or industrial controller, a blue collar AIM 65 Microcomputer is an economical solution.

*AIM 65 Microcomputer is a trademark of the Rockwell International Corp.





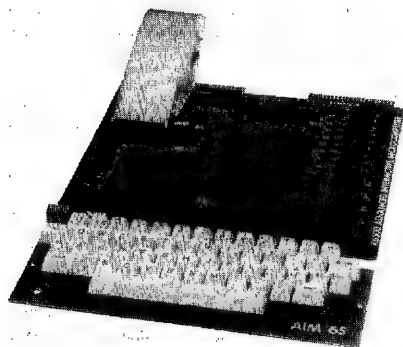
A65-100 AND A65-400 AIM 65 MICROCOMPUTER

PRODUCT OVERVIEW

The AIM 65 microcomputer is a complete, assembled microcomputer system featuring a 20-column thermal printer, a 20-character alphanumeric display, and a full-size terminal style keyboard. On-board memory sockets accept up to 20K bytes of PROM/ROM and 4K bytes of static RAM. A user R6522 Versatile Interface Adapter (VIA) dedicates 16 parallel I/O data lines and four handshaking control lines to application usage. The address, data, and control lines are also accessible for off-board memory, peripheral and I/O expansion. An 8K-byte ROM-resident debug monitor and text editor provides immediate interactive operation upon power turn-on.

With its self-contained printer and display, the AIM 65 microcomputer is ideal for educational and industrial desk-top applications. The on-board printer, unique to single-board microcomputers in its class, make the AIM 65 microcomputer a natural for any control and monitor application requiring hard copy output—such as equipment performance monitoring, data logging, test and evaluation, specialized data acquisition and reduction, laboratory measurements and analysis, and untold others.

The interactive monitor simplifies computer program checkout with single step functions which trace instruction execution and register contents as well as stop execution at specified breakpoint addresses. Memory and registers can be examined and altered to set up controlled execution conditions and to allow detailed analysis of program performance. The text editor allows computer program assembly and high level language instructions and data to be easily entered and edited at the source code level.



A65-400 AIM 65 Microcomputer

FEATURES

- Single Board Computer with on-board RAM, ROM, and I/O
 - Powerful and Popular 6502 CPU
 - Up to 4K bytes of 2114 Static RAM
 - Up to 20K bytes of 2532 PROM or R2332 ROM
 - User-Dedicated Application Parallel I/O Interface
 - Low-Cost Audio Cassette Recorder Interface with 2 Recorder Remote Control Lines
 - 20 mA Current Loop Serial Interface
 - Expansion Bus Interface
- 20-Column Thermal Printer
 - 64 Character ASCII Format
 - 120 Lines per Minute
 - 5 × 7 Dot Matrix Character Font
- 20-Character Display
 - 64-Character ASCII Format
 - 16-Segment Font
 - High Contrast Monolithic Characters
- Full-Size 54-key Terminal Style Keyboard
 - 26 Alphabetic, 10 Numeric, and 22 Special Characters
 - 9 Control Functions and 3 User-Defined Functions
- ROM-Resident Interactive Debug Monitor
 - Monitor-Generated Prompts and Single Keystroke Commands
 - Single-Step Execution with Tracing and Breakpoints
 - Memory and Register Examine and Alter
 - Mnemonic Instruction Entry and Disassembly
- Text Editor
 - Line Oriented Commands (Read, Insert, Delete, List)
 - Character String Find and Change
- Parallel Application Interface
 - R6522 Versatile Interface Adapter (VIA)
 - Two 8-bit Parallel Bidirectional Data Ports
 - Two 2-bit Handshake Control Ports
 - Two Programmable 16-bit Counter/Timers
 - 8-bit Serial Interface
- Optional ROM-Based Languages
 - 4K Symbolic Assembler
 - 8K BASIC Interpreter
 - 8K PL/65 Compiler
 - 8K FORTH Compiler/Interpreter
 - 20K Pascal Compiler/Interpreter (16K Bytes Off-Board)

ORDERING INFORMATION

Part No.	Description
A65-100	AIM 65 with 1K RAM
A65-400	AIM 65 with 4K RAM
A65-415	AIM 65 with 4K RAM & BASIC Interpreter ROMs
A65-420	AIM 65 with 4K RAM, BASIC Interpreter ROMs & Assembler ROM
A65-450	AIM 65 with 4K RAM & FORTH ROMs
Order No.	Description
209	AIM 65 Microcomputer User's Guide ⁽¹⁾
209L	AIM 65 Monitor Listing ⁽¹⁾
217	AIM 65 Reference Card ⁽¹⁾
219	AIM 65 Schematic (Wall Chart) ⁽¹⁾
201	R6500 Hardware Manual ⁽¹⁾
202	R6500 Programming Manual ⁽¹⁾
200	R6500 Programming Reference Card ⁽¹⁾
221	AIM 65 BASIC Language Reference Manual ⁽²⁾
233	AIM 65 BASIC Reference Card ⁽²⁾
265	AIM 65 FORTH User's Manual ⁽²⁾
283	AIM 65 FORTH Reference Card ⁽³⁾
Notes:	
1. Included with all models.	
2. Included with A65-0415 and A65-0420.	
3. Included with A65-0450.	

FUNCTIONAL DESCRIPTION

The AIM 65 microcomputer consists of a Master Module (which includes the central processing and control circuitry, decoders, memory, I/O and printer control circuitry), an attached Display Module and a separate Keyboard Module. A thermal printer is mounted directly on the Master Module while the Display Module is mounted on angle brackets which are fastened to the Master Module.

Central Processing and Control

The R6502 8-bit microprocessor, the central processing unit (CPU) of the AIM 65 microcomputer, provides the overall control and monitoring of all AIM 65 operations. The R6502 communicates with other AIM 65 elements on three separate buses. A 16-bit address bus allows the CPU to directly address 65,536 memory locations. An 8-bit bidirectional data bus carries data from the CPU to/from memory and interface devices. The control bus carries various timing and control signals between the CPU and interfacing peripherals, devices, and off-board elements.

The CPU operates at 1 MHz, which is derived from a 4 MHz crystal-controlled oscillator. The $\phi 2$ system clock and read/write control signals are generated by the CPU, and are buffered and routed to other devices on-board and to the expansion connector.

A decoder circuit provides chip select signals to the on-board PROM/ROM and RAM sockets and to the I/O devices. 4K-byte chip selects are sent to the PROM/ROM sockets (\$BXXX-\$FXXX) while 1K-byte select signals are routed to the RAM sockets (\$00XX-\$XCXX). On-board I/O is also decoded to 1K-byte selects (\$A0XX-\$ACXX).

A pushbutton switch initiates RESET to the on-board devices and to interfacing equipment through the expansion connector. Installed terminal posts allow connection to a remote RESET switch. The STEP/RUN switch selects program execution in either the single-step mode or the run mode. In single-step mode, execution of all instructions in the address range 0-\$9FFF can be traced or can be stopped at any of four specified breakpoints. The KB/TTY switch selects operation using the AIM 65 keyboard and display or using a teletypewriter attached to the 20 mA current loop interface.

Memory

Two 1024 \times 4 2114 static RAM devices are required for each 1K-byte of installed RAM. Both 1K and 4K versions are available. The 1K version may be expanded on-board in 1K increments up to 4K using the spare RAM sockets.

Five PROM/ROM sockets accept installation of the 4K-byte R2332 ROM, 2532 PROM, or smaller devices with compatible pinouts, e.g., 2K-byte 2516 PROM. The AIM 65 microcomputer comes with two R2332 ROMs containing the Debug Monitor/Text Editor installed at addresses \$E000-\$FFFF.

I/O

The 16 bidirectional data lines and 4 handshake control lines of the user-dedicated R6522 VIA are routed directly to the application connector. The high current capacity of the VIA's eight "B" port lines can directly drive many industry-standard devices, such as solid state relays. One of the lines can be used as either a serial input or output line.

The audio recorder interface connects to one or two low-cost audio cassette recorders. Two remote control lines can control two separate recorders independently during read and write operations using the AIM 65 blocked audio recording format.

Peripherals

The printer prints on heat-sensitive roll paper by means of ten thermal elements, mounted on a movable head, each of which can print two 5 \times 7 matrix dot characters. The printed characters are formed by dot patterns stored in the AIM 65 Monitor/Editor ROMs. A motor-driven platen advances the paper after each row of horizontal dots is printed. The motor and thermal element driver voltages are derived from an external +24V power supply. The printing is controlled by subroutines resident in the Monitor/Editor ROMs.

The AIM 65 display consists of five four-digit 16-segment alphanumeric displays and an R6520 Peripheral Interface Adapter (PIA) mounted on the Display Module which connects to the Master Module through two short solid-conductor ribbon cables. Each display quad contains internal memory, decoder, and driver circuitry. The display quads interface with the Master Module through the PIA. Data may be sent to the display using Monitor ROM subroutines.

The Keyboard Module connects to the Master Module by a removable 16-conductor flat ribbon cable. The interface is through an R6532 RAM, I/O, and Timer (RIOT) device which supports the Monitor with the RAM and timer. The key matrix is strobed by eight lines output through the RIOT with the matrix returns routed back through eight R6532 input lines.

OPTIONS

Optional hardware and accessory items are available which expand the functionality of the AIM 65 Microcomputer. The microcomputer can be easily installed in an attractive, professional, injection molded plastic enclosure for desk-top applications. Plug-in memory cartridges (A65-905 series) connect to the AIM 65 enclosure to expand memory in configurations of RAM and/or PROM/ROM. System expansion via RM 65 modules adds memory, input/output and peripheral (e.g., floppy disk and CRT display interface) functions to the on-board AIM 65 resources. Three different adapters/buffer modules connect the AIM 65 Expansion Connector to either one RM 65 module or to one of the multi-slot RM 65 motherboards. PROM programming can be performed using either the AIM 65 PROM Programmer or the RM 65 PROM Programmer Module (RM65-2901). The latter module has the advantage of being able to be used with other RM 65 modules connected to the system, e.g., RM 65 FDC module with AIM 65 DOS 1.0 (A65-090) firmware, to simplify source and object code handling.

Optional ROM-based languages support computer program development in both R6500 assembly language and high level languages. BASIC (by Microsoft) is the most popular microcomputer language used for computation and low speed control applications. FORTH is a highly efficient language in terms of memory utilization and execution speed—and also greatly shortens program development time. PL/65 provides structured control statements and compiles to 6500 assembly language to serve as an efficient system implementation language. The AIM 65 Pascal is a unique implementation of a substantial subset of standard Pascal which features interactive statement entry and execution with debug features at the source statement level.

OPTION ORDERING INFORMATION

Part No.	Description
Accessories and Hardware	
A65-002	AIM 65 Enclosure
A65-003	AIM 65 Service Test Board
A65-004	AIM 65 Power Supply & Cable
A65-006	AIM 65 Enclosure and Power Supply
A65-901	AIM 65 PROM Programmer
A65-905	AIM 65 Memory Cartridge
RM65-7101E	RM 65 Single Card Adapter for AIM 65
RM65-7104E	RM 65 Adapter/Buffer Module for AIM 65
RM65-7116E	RM 65 Cable Driver & Buffer Module for AIM 65
Firmware	
A65-010	AIM 65 Assembler ROM
A65-020	AIM 65 BASIC Interpreter ROMs
A65-030	AIM 65 PL/65 Compiler ROMs
A65-040	AIM 65 Math Package ROM
A65-050	AIM 65 FORTH Interpreter System ROMs
A65-060	AIM 65 Instant Pascal ROMs
A65-090	AIM Disk Operating System Version 1.0 (DOS 1.0) ROM ⁽¹⁾
Software	
A65-024	AIM 65 BASIC Compiler ^(1, 2, 3)
A65-052	AIM 65 FORTH Compiler ^(1, 2, 3, 4)

Notes:

1. Requires RM 65 Floppy Disk Controller (FDC) module. (RM65-5101NE).
2. Requires AIM 65 DOS 1.0 ROM (A65-090).
3. Provided on 5¼" double-density disk.
4. Requires AIM 65 FORTH Interpreter ROMs (A65-050).

Expansion Connector Pin Assignments

Top (Component Side)				Bottom (Solder Side)			
Signal Mnemonic	Signal Name	Input/Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/Output
SYNC	SYNC	O	1	A	A0	Address Bit 0	O
RDY	Ready	I	2	B	A1	Address Bit 1	O
Ø1	Phase 1 Clock	O	3	C	A2	Address Bit 2	O
IRQ	Interrupt Request	I	4	D	A3	Address Bit 3	O
S.O.	Set Overflow	I	5	E	A4	Address Bit 4	O
NMI	Non-Maskable Interrupt	I	6	F	A5	Address Bit 5	O
RES	Reset	I	7	H	A6	Address Bit 6	O
D7	Data Bit 7	I/O	8	J	A7	Address Bit 7	O
D6	Data Bit 6	I/O	9	K	A8	Address Bit 8	O
D5	Data Bit 5	I/O	10	L	A9	Address Bit 9	O
D4	Data Bit 4	I/O	11	M	A10	Address Bit 10	O
D3	Data Bit 3	I/O	12	N	A11	Address Bit 11	O
D2	Data Bit 2	I/O	13	P	A12	Address Bit 12	O
D1	Data Bit 1	I/O	14	R	A13	Address Bit 13	O
D0	Data Bit 0	I/O	15	S	A14	Address Bit 14	O
-12V	*-12 Vdc	O	16	T	A15	Address Bit 15	O
+12V	*+12 Vdc	O	17	U	SYS Ø2	System Phase 2 Clock	O
CS8	Chip Select 8	O	18	V	SYS R/W	System Read/Write	O
CS9	Chip Select 9	O	19	W	R/W	Read/Write "Not"	O
CSA	Chip Select A	O	20	X	TEST	Test	O
+5V	+5 Vdc	O	21	Y	Ø2	Phase 2 Clock "Not"	O
GND	Ground		22	Z	RAM R/W	RAM Read/Write	O

Note: *Not used on AIM 65.

Application Connector Pin Assignments

Top (Component Side)					Bottom (Solder Side)				
Signal Mnemonic	Signal Name	Type	I/O	Pin	Pin	Signal Mnemonic	Signal Name	Type	I/O
GND	Ground			1	A	+5V	+5V	Power	O
PA3	Port A Data Bit 3	NMOS	I/O	2	B		NC		
PA2	Port A Data Bit 2	NMOS	I/O	3	C	Ø2	CPU Phase 2 Clock	NMOS	O
PA1	Port A Data Bit 1	NMOS	I/O	4	D	R/W	CPU Read/Write	NMOS	
PA4	Port A Data Bit 4	NMOS	I/O	5	E	TAPE 1B RTN	Tape 1B Remote Control Return		I/O
PA5	Port A Data Bit 5	NMOS	I/O	6	F	TAPE 1B	Tape 1B Remote Control		I/O
PA6	Port A Data Bit 6	NMOS	I/O	7	H	TAPE 2B RTN	Tape 2B Remote Control Return		I/O
PA7	Port A Data Bit 7	NMOS	I/O	8	J	TAPE 2B	Tape 2B Remote Control		I/O
PB0	Port B Data Bit 0	NMOS	I/O	9	K		NC		
PB1	Port B Data Bit 1	NMOS	I/O	10	L	AUDIO IN	Audio Input Low		I
PB2	Port B Data Bit 2	NMOS	I/O	11	M	AUDIO OUT LO	Audio Output Low Level		O
PB3	Port B Data Bit 3	NMOS	I/O	12	N	+12V	+12 Vdc	Power	O
PB4	Port B Data Bit 4	NMOS	I/O	13	P	AUDIO OUT HIGH	Audio Output High Level		O
PA0	Port A Data Bit 0	NMOS	I/O	14	R	TTY KYBD RTN (+)	TTY Keyboard Return	20 mA (+)	
PB7	Port B Data Bit 7	NMOS	I/O	15	S	TTY PWR RTN (+)	TTY Power Return	20 mA (+)	
PB5	Port B Data Bit 5	NMOS	I/O	16	T	TTY KYBD	TTY Keyboard (Data In)	20 mA (-)	I
PB6	Port B Data Bit 6	NMOS	I/O	17	U	TTY PWR	TTY Power (Data Out)	20 mA (-)	O
CB1	Port B Control Bit 1	NMOS	I/O	18	V	TAPE 2A	Tape 2A Remote Control		I/O
CB2	Port B Control Bit 2	NMOS	I/O	19	W	TAPE 1A	Tape 1A Remote Control		I/O
CA1	Port A Control Bit 1	NMOS	I	20	X		NC		
CA2	Port A Control Bit 2	NMOS	I/O	21	Y	SERIAL IN	Serial Input		I
-12V	-12 Vdc**	Power	O	22	Z	+24V	+24 Vdc**	Power	O

Notes: *Pin 22 jumpered to -12V through jumper.

**Pin Z jumpered to +24V through jumper.

SPECIFICATIONS

Parameter	Value
Outside Dimensions*	
Master Module	
Width	11.5 in. (292 mm)
Depth	10.5 in. (267 mm)
Height**	2.35 in. (60 mm)
Weight	1 lb. 11 oz. (630 g)
Keyboard Module	
Width	11.5 in. (292 mm)
Depth	4.0 in. (102 mm)
Height	1.2 in. (30 mm)
Weight	1 lb. 3 oz. (443 g)
Environment	
Operating Temperature	0° to 50°C
Storage Temperature	0° to 70°C
Relative Humidity	0% to 85% (without condensation)
Power Connector	6-Post Terminal Block
Interface Connector	
J1 (Application) and J3 (Expansion)	44-pin edge connector (0.156 in. centers). Mates with Viking 2VH22/1AND5 or equivalent.
J2 (Printer)	17-pin flexible cable strip connector
J4 (Keyboard)	16-pin DIP connector
J5 (Display)	32-pin strip connector
Shipping Specifications	
Size (in box)	13 in. (330 mm) x 14 in. (355 mm) x 7.5 in. (190 mm)
Weight (in box)	8 lb. (3 kg)

Notes: *Reference PA00-D010.

**To top of the display.

ELECTRICAL CHARACTERISTICS

Power Requirements

Voltage	Typ	Max	Peak	Units
+5V $\pm 5\%$ Regulated				
1K RAM + 2 ROMs*	1.1	1.8	1.8	A
4K RAM + 5 ROMs	1.8	2.8	2.8	A
+24V $\pm 15\%$ Unregulated	0.5	1.5	2.5**	A

Notes:

*For additional RAM and ROM, allow

	Typ	Max	Units
1K 2114 RAM (2 devices)	0.160	0.200	A
4K 2332 ROM (1 device)	0.080	0.120	A

**+24V peak current specified as worst case with printer duty cycle of 75%. For most cases, a +24V 2A power supply is sufficient.

NMOS Interface (Input Voltage = +5.0V, $T_A = 25^\circ\text{C}$)

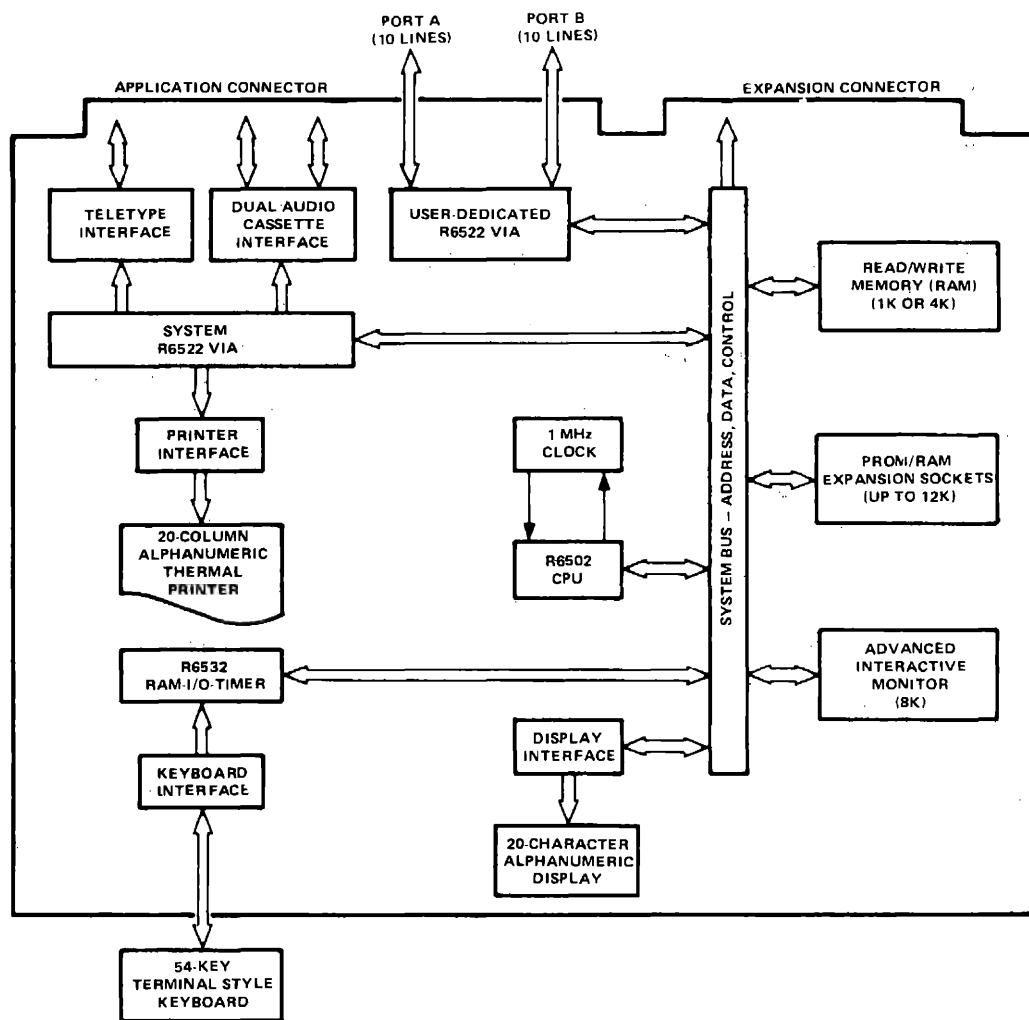
Symbol	Parameter	Min	Max	Unit
V_{IH}	Input High Voltage	2.4	5.0	V
V_{IL}	Input Low Voltage	-0.3	+0.4	V
I_{IH}	Input High Current ($V_{IH} = 2.4\text{V}$)	-100	-300	μA
I_{IL}	Input Low Current ($V_{IL} = 0.4\text{V}$)	-1.0	-1.6	mA
V_{OH}	Output High Voltage ($I_{LOAD} < -100\text{A}$)	2.4	5.0	V
V_{OL}	Output Low Voltage ($I_{LOAD} < -3\text{mA}$)	—	0.4	V
I_{OH}	Output High Current (Sourcing) ($V_{OH} \geq 2.4\text{V}$)	-100	—	μA
	($V_{OH} \geq 1.5\text{V}$, VIA PB0-PB7 only)	-1.0	—	mA
I_{OL}	Output Low Current (Sinking) ($V_{OL} \leq 0.4\text{V}$)	1.6	—	mA

TTL —Industry standard LS TTL.

OC TTL —Industry standard Open Collector LS TTL.

3S TTL —Industry standard Tri-State LS TTL.

TP TTL —Industry standard Totem Pole LS TTL.



AIM 65 Microcomputer Block Diagram

MONITOR COMMANDS

Major Function Entry

(RESET Button)—Enter and Initialize Monitor
 ESC — Reenter Monitor
 E — Enter and Initialize Text Editor
 T — Reenter Text Editor
 N — Jump to D000
 5 — Jump to B000
 6 — Jump to B003

Instruction Entry and Disassembly

I — Enter mnemonic instruction entry mode
 K — Disassemble memory

Display/Alter Registers and Memory

* — Alter Program Counter to (address)
 A — Alter Accumulator to (byte)
 X — Alter X Register to (byte)
 Y — Alter Y Register to (byte)
 P — Alter Processor Status to (byte)
 S — Alter Stack Pointer to (byte)
 R — Display all registers
 M — Display four memory locations, starting at (address)
 (SPACE) — Display next four memory locations
 / — Alter current memory location

Manipulate Breakpoints

— Clear all breakpoints
 4 — Toggle breakpoint enable on/off
 B — Set one to four breakpoint addresses
 ? — Display breakpoint addresses

Control Instruction/Trace

G — Execute user's program
 Z — Toggle instruction trace mode on/off
 V — Toggle register trace mode on/off
 H — Trace Program Counter history

Control Peripheral Devices

L — Load object code into memory from peripheral I/O device
 D — Dump object code to peripheral I/O device
 1 — Toggle Tape 1 control on/off
 2 — Toggle Tape 2 control on/off
 3 — Verify tape checksum
 CTRL PRINT — Toggle Printer on/off
 LF — Line Feed
 PRINT — Print Display contents

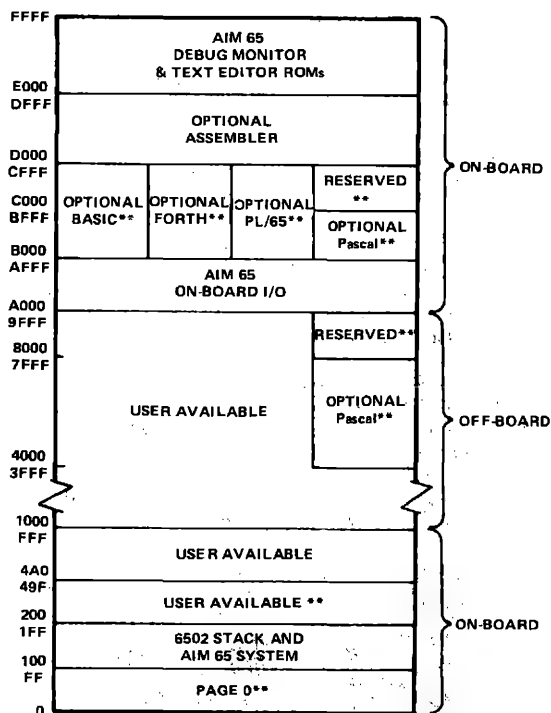
Call User-Defined Functions

F1 — Call User Function 1
 F2 — Call User Function 2
 F3 — Call User Function 3

TEXT EDITOR COMMANDS

R — Read lines into text buffer
 I — Insert line into text buffer
 K — Delete current line of text
 (SPACE) — Display current line of text
 L — List lines of text to peripheral I/O device
 U — Move up one line
 D — Move down one line
 T — Go to top line of text
 B — Go to bottom line of text
 F — Find character string
 C — Change character string
 Q — Quit Text Editor, return to Monitor

AIM 65 Memory Map



NOTES: *USER AVAILABLE IF MONITOR/EDITOR IS NOT USED.
 **USER AVAILABLE IF OPTIONAL LANGUAGE IS NOT USED:

LANGUAGE	PAGE 0	PAGE 2-4
Assembler	0-DE-	NOT USED
BASIC	0-D6	200 - 211
FORTH	0-A4	200 - 30A
PL/65	0-04	200 - 49F
Pascal	06-B4, FC-FF	200 - 2FF
Monitor/Editor	DF-FF	NOT USED

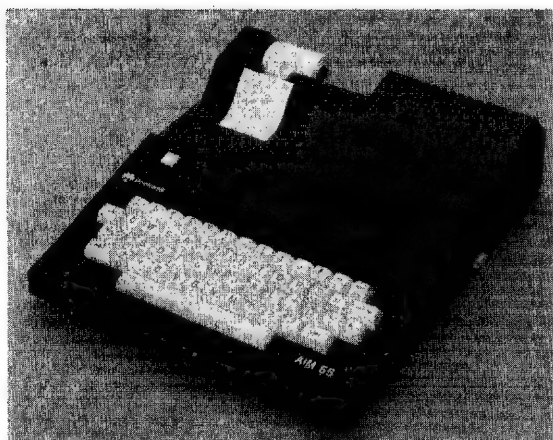


A65-0500 AIM 65 MICROCOMPUTER SYSTEM

DESCRIPTION

The AIM 65 "500" Series Microcomputer System offers the popular AIM 65 Microcomputer, power supply, interconnect wiring, switches, and attractive injection molded enclosure—all fully connected, assembled, and ready for operation. Four models, pre-configured with varying combinations of ROM-based languages, support many different educational, scientific, or industrial applications. The stylistic, low profile, compact enclosure with fine textured, nonreflective brown finish complements classroom, industrial, office or laboratory environments.

All models include a full-size terminal-style keyboard and 20-character alphanumeric display for interactive operator communications and a 20-column printer for hard copy records of computed results of programs and/or data. Serial interface and control lines are provided for audio cassette storage of programs and data files. The microcomputer memory features 4K bytes of RAM and 8K bytes of ROM-resident interactive debug monitor and text editor in addition to the available languages. Most important may be the flexibility afforded by the user-dedicated I/O port that interfaces to application sensors, actuators or peripherals. Built-in I/O features include two 8-bit parallel handshake and one serial bidirectional data ports. Two 16-bit timer/controllers are available for time measurement or event counting. Finally, the microcomputer bus is accessible at a connector for external expansion with the AIM 65 memory cartridge system (A65-905-XX), AIM 65 PROM programmer (A65-901) or a selection of RM 65 modules such as floppy disk or CRT controllers.



AIM 65 Microcomputer System

FEATURES

- R6502 CPU-based single board computer
- 20-character 16-segment display
- 20-column thermal printer
- Full-size 54-key terminal-style keyboard
- ROM-resident Debug Monitor/Text Editor
- Parallel application connection
- Expansion bus connection
- Includes power supply, switches and wiring
- Sturdy aluminum base
- Low-profile injection molded ABS top cover
- Enclosed, plug-in memory cartridge option for desk-top expansion
- RM 65 peripheral, input/output and memory module expansion interface
- Fully assembled, tested and warranted.

ORDERING INFORMATION

Part No.	Description
A65-0500	AIM 65 Microcomputer System with 4K RAM and 12K PROM/ROM capacity
A65-0515	AIM 65 Microcomputer System with 4K RAM, 8K BASIC Interpreter ROMs and 4K PROM/ROM capacity
A65-0520	AIM 65 Microcomputer System with 4K RAM, 8K BASIC Interpreter ROMs and 4K Assembler ROM
A65-0550	AIM 65 Microcomputer System with 4K RAM, 8K FORTH ROMs and 4K PROM/ROM capacity
Order No.	Description
209	AIM 65 Microcomputer User's Guide ⁽¹⁾
209L	AIM 65 Monitor Listing ⁽¹⁾
217	AIM 65 Reference Card ⁽¹⁾
200	R6500 Programming Reference Card ⁽¹⁾
201	R6500 Hardware Manual ⁽¹⁾
202	R6500 Programming Manual ⁽¹⁾
221	AIM 65 BASIC Language Reference Manual ⁽²⁾
233	AIM 65 BASIC Reference Card ⁽²⁾
265	AIM 65 FORTH User's Manual ⁽³⁾
283	AIM 65 FORTH Reference Card ⁽³⁾
Notes:	
1. Included with all models.	
2. Included with A65-0515 and A65-0520.	
3. Included with A65-0550.	

SPECIFICATIONS

Characteristics	Values
Dimensions	
Width	13.0 in. (330 mm)
Depth	15.5 in. (395 mm)
Height	3.9 in. (100 mm)
Weight	11 lb. (5 kg)
Environment	
Operating Temperature	0° to 50°C
Storage Temperature	0° to 70°C
Relative Humidity	0% to 85% (without condensation)
Power	
Input voltage	115 Vac \pm 10%, 47-63 Hz ⁽¹⁾
Fuse	115 Vac, 1A
Power cord	6 ft., 3-conductor cord (125 VAC, 13A rating) with molded vinyl grounding plug (NEMA 5-15P) Class B
Power supply output	5 VDC (3.0A max.) 24 VDC (0.5 ave., 2.5A peak)
Interface Connector ⁽²⁾	
J1 (Application) and J3 (Expansion)	44-pin edge connector (0.156 in. centers) Mates with Viking 2VH22/1AND5 or equivalent
Notes: 1. Power supply transformer input connections can be changed for 230 Vac \pm 10% input voltage. 2. Refer to Data Sheet Order No. D79 for A65-100, -400 for additional specifications.	



A65-002, A65-006

AIM 65 MICROCOMPUTER ENCLOSURE

PRODUCT OVERVIEW

The AIM 65 Microcomputer Enclosure is an attractive, professional housing for the Rockwell AIM 65 Microcomputer. Featuring low-profile stylistic design, fine-textured, non-reflective finish and handsome brown color, the enclosure makes the AIM 65 Microcomputer a pleasing addition to the office, laboratory, classroom and light industrial environment. The 13 × 15.5 × 3.9 inches enclosure occupies minimal desk-top space.

The enclosure consists of a sturdy aluminum base and a durable injection-molded top cover. The base includes mounting provisions for the power supply, line cord, power switch and circuit breaker. The cover is UL approved flame-retardant ABS material with metal threaded inserts for firm attachment to the base.

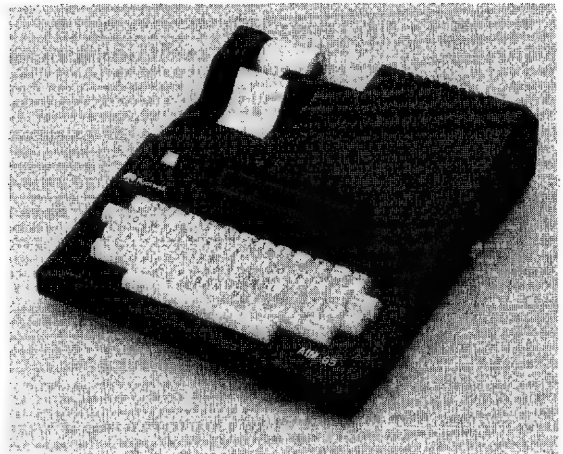
Offered with or without an internal power supply, the enclosure comes with a rocker-type power on/off switch, a pushbutton reset switch, a 6-foot, 115 Vac line cord with 3-prong plug, a fuse holder and fuse, and internal wiring for easy assembly to the AIM 65 Microcomputer.

The filtered power supply provides +5V (regulated) at 3A and +24V (regulated) at .5A (average)/2.5A (peak). Prewired DC power lines terminated with lugs connect directly to the AIM 65 Microcomputer power terminal strip. The AIM 65 Microcomputer system passes the FCC Class B radio frequency interference requirements for personal computers when used with the A65-006 Enclosure and power supply.

An external paper holder and paper feed guide allows easy printer paper replacement without top cover removal. A clear plastic tear bar with a straight knife edge is permanently attached to the top cover for convenient paper tear-off. Rear openings permit access to the application and expansion connectors. A remote Reset switch installed on the top cover is pre-wired to slip-on terminals to mate with external Reset switch posts on the AIM 65 Master Module. Removeable plugs allow access to the RUN/STEP and TTY/KB switches on the AIM 65 Master Module.

FEATURES

- Attractive, low-profile styling
- Compact and Portable
- Sturdy aluminum base with integral accessory mounting brackets
- Durable injection-molded ABS top cover
 - Access holes to Application and Expansion connectors
 - External RESET push-button switch
 - Pluggable access holes to STEP/RUN and TTY/KB switches
 - Clear plastic printer paper tear bar
- All necessary accessories
 - Rocker-style power on/off switch
 - Fuse holder
 - Line Cord
 - All assembly hardware included
- Optional +5V +24V internal power supply operates from 115/230Vac @ 50/60 Hz



ORDERING INFORMATION

Part No.	Description
A65-002	AIM 65 Enclosure (without Power Supply)
A65-006	AIM 65 Enclosure and Power Supply

SPECIFICATIONS

Characteristic	Value	Characteristic	Value
Dimensions		Accessories (cont.)	
Depth	12.9 in (328 mm)	Power Cord	
Width	15.5 in (394 mm)	Type	3-wire/18-gauge
Height	3/4.9 in (99 mm)	Plug	US 3-prong (NEMA 5-15P)
Weight		Length	6 feet
without Power Supply	5 lb. 0 oz. (2.24 kg)	Rating	125V/13A
with Power Supply	9 lb. 6 oz. (4.20 kg)	Power Supply	
Shipping Weight		AC Input	115/230 Vac \pm 10%, 47-63 Hz (Derate output current 10% for 50 Hz operation)
without Power Supply	6 lb. 8 oz. (2.9 kg)	DC Output 1	
with Power Supply	10 lb. 14 oz. (4.87 kg)	Voltage	Adjustable +5Vdc \pm 5% (regulated)
Construction		Current	3.0A
Base Material	Sheet Aluminum with Chem-film finish	Overvoltage Protection	6.2 \pm 0.4Vdc
Mounting Brackets	Integral	DC Output 2	
Cover		Voltage	Adjustable +24Vdc (regulated)
Material	Flame-retardant ABS plastic	Current	0.54 (average)/2.5A (peak)
Forming	Injection Molded	Short Circuit Protection	Automatic current limit/foldback
Color	Dark Brown	Temperature Rating	0° to 50°C full rated output (Derated linearly) to 40% @ 70°C
Finish	Non-Reflective, fine textured	UL Recognized	
Accessories			
Fuse	115 Vac @ 1A/ 230 Vac @ 0.5A		
Power On/Off Switch	Rocker-style		
Reset Switch	Square Push-button		



A65-003 AIM 65 SERVICE TEST BOARD

DESCRIPTION

The AIM 65 Service Test Board, in conjunction with the AIM 65 Microcomputer and AIM 65 Debug Monitor ROMs, performs a complete functional test of the microcomputer. This test board provides a convenient way to test the AIM 65 microcomputer either after repair or during periodic inspection and preventative maintenance. The module connects directly to the AIM 65 Microcomputer Application and Expansion connectors. Power is supplied from the AIM 65 Microcomputer eliminating additional power connection requirements.

The ROM-based test program can be initiated immediately after microcomputer power turn-on. Menu type command prompts simplify test selection. Five separate commands allow test level selection appropriate to the test objective. ALL TESTS selection performs nine separate tests consecutively to check all microcomputer circuits as well as the application and expansion interfaces. Once initiated, operation is automatic with operator response required only to type keys to test the keyboard and to advance testing after printer adjustment. SINGLE TEST mode allows a specific test to be performed—this is especially useful when testing a particular device or circuit. CONTINUOUS TEST performs a repetitive test of the microcomputer without operator intervention—thus supporting burn-in operation and test after component replacement. R6532 and 2114 RAM can be selectively checked with the R6532 RAM and 2114 RAM tests, respectively.

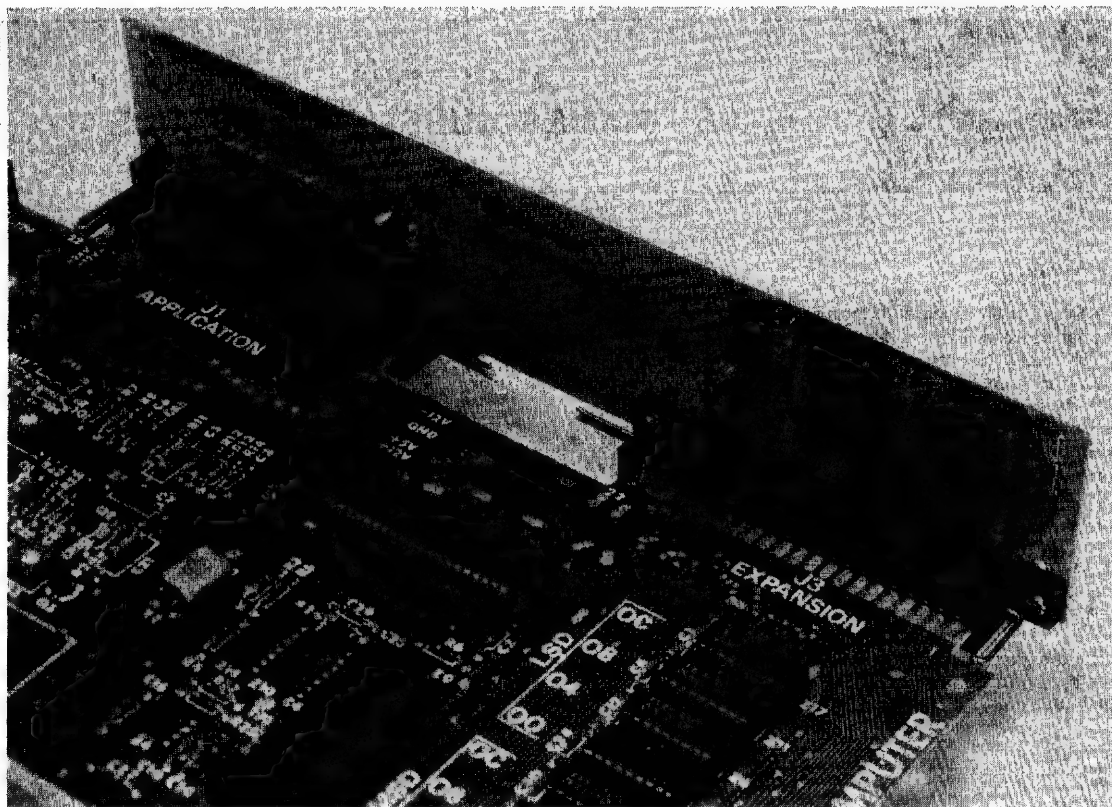
Test commands and results are displayed and printed. The printout provides hardcopy test results for easy inclusion in equipment maintenance records. Adjustment of potentiometers controlling printer speed, printer dot intensity and audio tape circuit gain enables proper and consistent settings. An LED provides visual indication of proper audio circuit gain adjustment. Mechanical adjustment of printer gear alignment is also supported.

FEATURES

- Performs complete functional test
- No external equipment required
- Provides hardcopy test results
- ROM-based 4K-byte test program for immediate operation
- Performs five tests upon command
 - ALL TESTS
 - SINGLE TEST
 - CONTINUOUS TEST
 - R6532 RAM TEST
 - 2114 RAM TEST
- Tests nine separate functions in ALL TEST mode or upon SINGLE TEST command
 - Chip select logic
 - ROM checksum
 - R6532 and 2114 RAM
 - User R6522 VIA
 - System R6522 VIA
 - Display
 - Printer
 - Switch
 - Keyboard
- Isolates most failures to component level
- Supports calibration of variable adjustments
 - Audio tape circuit gain
 - Printer speed
 - Print intensity
 - Printer dot alignment
- Audio tape circuit gain adjustment LED indicator
- Easy installation—connects directly to AIM 65 Application and Expansion connectors
- No external power required

ORDERING INFORMATION

Part No.	Description
A65-003	AIM 65 Service Test Board
Order No.	Description
2117	AIM 65 Self-Test Module User's Manual (Included with A65-003)



A65-003 AIM 65 Service Test Module



A65-004-03 AIM 65 POWER SUPPLY AND CABLE

DESCRIPTION

The AIM 65 Power Supply and Cable is a compact open frame DC power supply with output cable for connection to an AIM 65 Microcomputer. The power supply fits compactly inside the AIM 65 Enclosure (A65-002) to provide a complete table top microcomputer system. The +5V/3A output provides plenty of power for full on-board PROM/ROM and RAM expansion. The +24V/1.5A output supplies power for the AIM 65 microcomputer printer.

Slip-on terminals on the AC input terminal strip simplify connection to a wide range of input power: 110/115/215/230 Vac at 47-63 Hz. The 3-wire DC output cable, factory connected to the power supply output terminals, can be readily connected to the AIM 65 input power terminals.

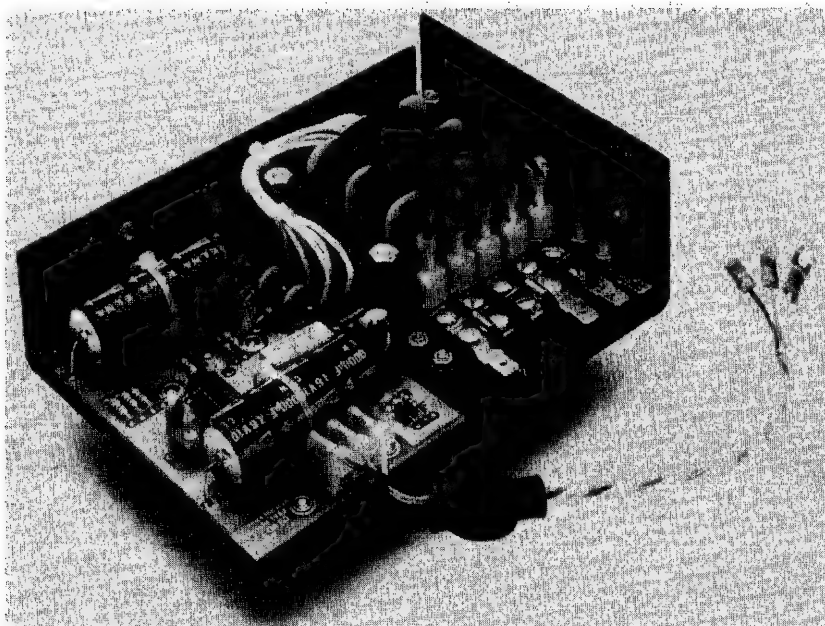
Both outputs are current limited to prevent damage to the power supply if the outputs are overloaded or accidentally shorted together. Full power is provided from 0° to 50°C.

FEATURES

- Dual AC input voltage
 - 110 or 115 Vac @ 47-63 Hz or
 - 215 or 230 Vac @ 47-63 Hz
- Two DC output voltages
 - +5V for AIM 65 Microcomputer logic
 - +24V for AIM 65 Microcomputer printer
- Slip-on input connection
- Compact size—fits in AIM 65 Enclosure
- Meets FCC Class B RFI requirements for personal computers when connected to the AIM 65 Microcomputer
- DC output cable included

ORDERING INFORMATION

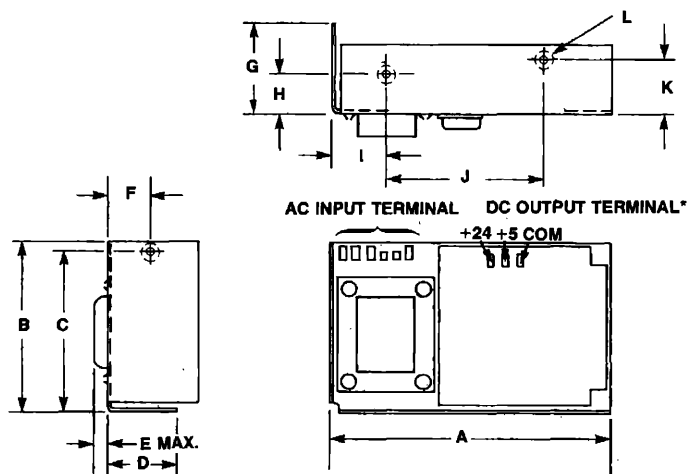
Part No.	Description
A65-004-03	Power Supply and Cable



A65-004-03 Power Supply

SPECIFICATIONS

Parameter	Value	Parameter	Value
AC Input	115/230 Vac \pm 10%, 47-63 Hz (Derate output current 10% for 50 Hz operation)	Dimensions	
DC Output 1		A	6.31 in. (160.3 mm)
Voltage	Adjustable +5 Vdc \pm 5% (regulated)	B	4.50 in. (114.3 mm)
Current	3.0A	C	3.78 in. (96.0 mm)
Overvoltage Protection	6.2 \pm 0.4 Vdc	D	1.62 in. (41.3 mm)
DC Output 2		E	0.45 in. (11.4 mm)
Voltage	Adjustable +24 Vdc (regulated)	F	1.10 in. (27.9 mm)
Current	0.5A (average)/2.5A (peak)	G	2.12 in. (53.8 mm)
Short Circuit Protection	Automatic current limit/foldback	H	0.95 in. (24.1 mm)
Temperature Rating	0°C to 50°C full rated output (Derated linearly to 40% @ 70°C)	I	1.24 in. (31.5 mm)
		J	3.62 in. (91.9 mm)
		K	1.20 in. (30.5 mm)
		L	8-32 THD (3)
		Output Cable	
		Length	10 in. (254.0 mm)
		Type	3-wire jacketed with internal balun
		Load Termination	Spade lugs
		Routed Outputs	+5V, +24V and COM



*SHOWN WITHOUT DC OUTPUT CABLE ATTACHED



A65-010 AIM 65 ASSEMBLER ROM

ASSEMBLY LANGUAGE

An assembler translates microprocessor instructions and data statements written in symbolic form (the source program) into machine executable code (the object program). The AIM 65 Assembler translates one instruction, consisting of a label (if required), a mnemonic operation code, an operand (if required) and arithmetic operator (if required) into a machine instruction consisting of from one to three bytes of memory. Constants comprising one or more bytes of memory are generated from data statements while one or more bytes of memory are assigned to variables. The assembler operates in two passes. Pass 1 checks for syntax errors and assigns values to symbols in a symbol table. Pass 2 generates the actual machine code and outputs the assembly listing which lists the source code and the corresponding machine code.

The source code is usually entered using the AIM 65 Text Editor then assembled to generate the machine code for program execution and debugging. Program changes to the source program can easily be edited then the program reassembled to generate the new machine code thus eliminating the need for the programmer to code and recode the program in machine code—a time consuming and laborious process.

PRODUCT OVERVIEW

The AIM 65 Assembler is a 4K-byte ROM-resident, two-pass symbolic assembler that plugs into socket Z24 on the AIM 65 Microcomputer Master Module and operates in conjunction with the AIM 65 Debug Monitor/Text Editor ROMs. The assembler translates computer program instructions written in standard assembly language for the 6502 microprocessor into machine code that will operate in any 6502 or 65XX CPU. Operating options are selected interactively by the operator upon assembly command. These options specify source code device, object code device, symbol table location, full assembly or errors only output listing and output listing device. Memory to memory assembly is supported for rapid program generation. Compatibility with the RM 65 Floppy Disc Controller (FDC) module (RM65-5101NE) and AIM 65 DOS 1.0 ROM (A65-090) allows source code to be input from one or more files on floppy disk and object code to be output to a floppy disk file to assemble very large programs and to permanently save source and object code.

FEATURES

- AIM 65 Microcomputer host
- 6502 machine code generation
- ROM-resident for immediate operation
- Symbolic linkage—operands and labels
- Interactive assembler operation setup
- Operator selected input device
 - Memory (text buffer)
 - Audio tape
 - TTY
 - User defined
- Operator selected object code output device
 - Memory (RAM)
 - Audio tape
 - TTY
 - Display/printer
 - Printer
 - User-defined
- Operator selected assembly/error listing output device
 - Display/printer
 - Printer
 - User-defined
- Assembler directives
- AIM 65 DOS 1.0 compatible

MEMORY MAP

Address (Hex)	Contents
\$D000-\$DFFF	Assembler Program
\$0-\$AC	Assembler Variables

ORDERING INFORMATION

Part No.	Description
A65-010	AIM 65 Assembler ROM
Order No.	Description
209	AIM 65 User's Guide (includes AIM 65 Assembler User's Instructions)

R6502 CPU INSTRUCTIONS

Mnemonic	Instruction	Mnemonic	Instruction
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	AND Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
BCC	Branch on Carry Clear	LSR	Shift Right One Bit (Memory or Accumulator)
BCS	Branch on Carry Set	NOP	No Operation
BEQ	Branch on Result Zero	ORA	OR Memory with Accumulator
BIT	Test Bits in Memory with Accumulator	PHA	Push Accumulator on Stack
BMI	Branch on Result Minus	PHP	Push Processor Status on Stack
BNE	Branch on Result Not Zero	PLA	Pull Accumulator from Stack
BPL	Branch on Result Plus	PLP	Pull Processor Status from Stack
BRK	Force Break	ROL	Rotate One Bit Left (Memory or Accumulator)
BVC	Branch on Overflow Clear	ROR	Rotate One Bit Right (Memory or Accumulator)
BVS	Branch on Overflow Set	RTI	Return from Interrupt
CLC	Clear Carry Flag	RTS	Return from Subroutine
CLD	Clear Decimal Mode	SBC	Subtract Memory from Accumulator with Borrow
CLI	Clear Interrupt Disable Bit	SEC	Set Carry Flag
CLV	Clear Overflow Flag	SED	Set Decimal Mode
CMP	Compare Memory and Accumulator	SEI	Set Interrupt Disable Status
CPX	Compare Memory and Index X	STA	Store Accumulator in Memory
CPY	Compare Memory and Index Y	STX	Store Index X in Memory
DEC	Decrement Memory by One	STY	Store Index Y in Memory
DEX	Decrement Index X by One	TAX	Transfer Accumulator to Index X
DEY	Decrement Index Y by One	TAY	Transfer Accumulator to Index Y
EOR	Exclusive-OR Memory with Accumulator	TSX	Transfer Stack Pointer to Index X
INC	Increment Memory by One	TXA	Transfer Index X to Accumulator
INX	Increment Index X by One	TXS	Transfer Index X to Stack Pointer
INY	Increment Index Y by One	TYA	Transfer Index Y to Accumulator
JMP	Jump to New Location		
JSR	Jump to New Location Saving Return Address		

AIM 65 ASSEMBLER DIRECTIVES

Command	Function	Command	Function
=	Equate	.OPT	Listing control option
.BYTE	Byte constant	LIS/NOL	Assembly listing generation
.WORD	Word constant	GEN/NOG	Object code question
.DBYTE	Double-byte constant	ERR/NOE	Error listing generation
.PAG	Page heading	.FILE	Source code file linkage
.SKIP	Skip line	.END	Last statement/first source code file linkage



A65-020

AIM 65 BASIC INTERPRETER ROMS

BASIC LANGUAGE

BASIC is a simple but powerful computer program language. Originally developed at Dartmouth University, BASIC has gained universal acceptance and is commonly used world-wide in schools, industry, and science.

The heart of BASIC is a set of easily learned English words which are used as commands. Complex and powerful statements can be constructed by adding operands and operators to the commands. Equations involving complex formulas and multiple variables can easily be solved. Internal floating point arithmetic handles a wide range of numeric values (2.93873588E-39 to 1.70141183E+38) and provides nine-digit accuracy to most calculations. In addition to addition, subtraction, multiplication and division, a full set of transcendental functions support trigonometric, exponential, square, square root, polynomial and logarithmic operations.

PRODUCT OVERVIEW

The AIM 65 BASIC Interpreter, consisting of input formatter, lister, floating point functions, interpreter and input/output functions, is contained in two 4K-byte ROMs that plug into sockets Z25 and Z26 on the AIM 65 Microcomputer Master Module. AIM 65 BASIC operates in one of two modes, development and run-time. In the development mode, BASIC statements are entered and executed as either direct or indirect commands. Direct commands are executed upon entry to provide immediate results, however, the statements are not stored for subsequent execution. Indirect commands are entered along with an associated line number and are executed upon RUN command entry. The AIM 65 microcomputer peripherals, i.e., the keyboard, 20-character single line display and 20 column printer, are used in the development mode to enter statements, to list entered indirect statements and to display/print execution results. The AIM 65 Debug Monitor/Text Editor ROMs must be resident in both the run-time and the development mode.

In the run-time mode, BASIC begins execution of the application program (i.e., previously entered indirect statements) without entering the BASIC command level. A short user-provided driver program initializes BASIC upon entry from the AIM 65 Monitor command level via key depression or execution command (or upon power turn-on or RESET if the RESET vector points to the application program).

The AIM 65 BASIC Interpreter ROMs, when installed in the AIM 65 Microcomputer, support development and checkout of an application program written in BASIC that is to be installed in an RM 65 Single Board Computer (SBC) module for run-time operation. The developed program, located in PROM or loaded from mass storage, will run with RM 65 Run-Time BASIC ROM

installed in the RM 65 SBC module. In this configuration, all RM 65 input/output operations must be user-provided and can be tested using the AIM 65 Microcomputer prior to being installed in the RM 65 environment.

LANGUAGE FEATURES

- BASIC is easy to learn
- Microsoft BASIC is universally accepted
- BASIC is widely used
- Supports simple and complex statements
- Floating point arithmetic functions
 - Add, subtract, multiply, divide
 - Trigonometric (sine, cosine, tangent, arctangent)
 - Exponential, square, square root
 - Natural logarithm
- String variables and arrays
- Integer variables
- Subroutine calls
- Conditional expressions
- User function

INTERPRETER FEATURES

- AIM 65 Microcomputer host
- ROM resident for immediate operation
- Operates in development and run-time modes
- Fast execution (reference Microsoft 6502 BASIC interpretation)
- Develops programs for execution in AIM 65 Microcomputer with AIM 65 BASIC installed or in RM 65 Single Board Computer (SBC) module based system with RM 65 Run-Time BASIC installed
- Executes application program from RAM or PROM

ORDERING INFORMATION

Part No.	Description
A65-020	AIM 65 BASIC ROMs
RM65-0122	RM 65 Run-Time BASIC ROM
Order No.	Description
221	AIM 65 BASIC Language Reference Manual ⁽¹⁾
233	AIM 65 BASIC Reference Card ⁽¹⁾
810	RM 65 Run-Time BASIC User's Manual ⁽²⁾
Notes:	
1. Included with A65-020.	
2. Included with RM65-0122.	

MEMORY MAP

Address (Hex)	Contents
\$B000-\$CFFF	AIM 65 BASIC Program
\$200-\$20F	AIM 65 BASIC Variables
\$0-\$D6	AIM 65 BASIC Variables

PROM PROGRAMMING

The application program is easily programmed into a PROM for operation in an OEM or end-user environment using the AIM 65 Microcomputer connected to either an RM 66 PROM Programmer module (RM65-2901E) or an AIM 65 PROM Programmer and CO-ED Module (A65-901).

BASIC STATEMENTS

Program Statements	Commands	String Functions
DEF FN	CLEAR	ASC
DIM	CONT	CHR\$
END	FRE	LEFT\$
FOR	LIST	LEN
GOSUB	LOAD	MID\$
GOTO	NEW	RIGHT\$
IF ... GOTO	PEEK	STR\$
IF ... THEN	POKE	VAL
LET	RUN	
NEXT	SAVE	
ON ... GOSUB		Arithmetic Functions
ON ... GOTO	Input/Output	ABS
REM	DATA	ATN*
RESTORE	GET	COS
RETURN	INPUT	EXP
STOP	READ	INT
USR	PRINT	LOG
WAIT	SPC	RND
	TAB	SIN
	POS	SGN
		SQR
		TAN

*Links to user-provided function.



A65-024 AIM 65 BASIC COMPILER

BASIC LANGUAGE

BASIC is a simple but powerful computer program language. Originally developed at Dartmouth University, BASIC has gained universal acceptance and is commonly used world-wide in schools, industry, and science.

The heart of BASIC is a set of easily learned English words which are used as commands. Complex and powerful statements can be constructed by adding operands and operators to the commands. Equations involving complex formulas and multiple variables can easily be solved. Internal floating point arithmetic handles a wide range of numeric values (2.93873588E-39 to 1.70141183E+38) and provides nine-digit accuracy to most calculations. In addition to addition, subtraction, multiplication and division, a full set of transcendental functions support trigonometric, exponential, square, square root, polynomial and logarithmic operations.

PRODUCT OVERVIEW

The AIM 65 BASIC Compiler, consisting of the BASIC compiler and BASIC run-time library, is contained on an AIM 65 diskette. The BASIC Compiler, in conjunction with the BASIC run-time library, compiles a program written in the BASIC language into a 6500 assembly language source file and an optimized run-time library file. The BASIC source code file is made up of indirect BASIC commands and statements. The two output files, assembly source file and optimized run-time file, are then assembled using the AIM 65 Assembler to create a BASIC object code file for execution.

The AIM 65 Text Editor can be used to create and edit the application program source code. The AIM 65 peripherals, i.e., keyboard, 20-character single-line display and 20-column printer, are used to enter and list BASIC statements and to display/print execution results.

The disk-based compiler operates on the AIM 65 Microcomputer in conjunction with the RM65 Floppy Disk Controller (FDC) module and the AIM 65 DOS 1.0. The AIM 65 Assembler (Part No. A65-010) is required to support the BASIC Compiler on the AIM 65 Microcomputer.

LANGUAGE FEATURES

- BASIC is easy to learn
- Microsoft BASIC is universally accepted
- BASIC is widely used
- Supports simple and complex statements
- Floating point arithmetic functions
 - Add, subtract, multiply, divide
 - Trigonometric (sine, cosine, tangent, arctangent)
 - Exponential, square, square root
 - Natural logarithm
- String variables and arrays
- Integer variables
- Subroutine calls
- Conditional expressions
- User function

COMPILER FEATURES

- Aim 65 Microcomputer host
- Generates standalone object code
- Compiles to 6500 assembly language easing optimization
- Fast execution
- Develops programs for execution in AIM 65 Microcomputer without AIM 65 BASIC installed or in RM 65 Single Board Computer (SBC) module based system without RM 65 Run-Time BASIC installed
- Executes application program from RAM or PROM

ORDERING INFORMATION

Part No.	Description
A65-024	AIM 65 BASIC Compiler
Order No.	Description
2159	AIM 65 BASIC Compiler User's Manual ⁽¹⁾
233	AIM 65 BASIC Reference Card ⁽¹⁾
Note:	
1. Included with A65-024.	

MEMORY MAP

Address (Hex)	Contents
\$1000-\$3C00	AIM 65 BASIC Compiler
\$0-\$FF	AIM 65 BASIC Variables

PROM PROGRAMMING

The application program is easily programmed into a PROM for operation in an OEM or end-user environment using the AIM 65 Microcomputer connected to either an RM 65 PROM Programmer module (RM65-2901E) or an AIM 65 PROM Programmer and CO-ED Module (A65-901).

BASIC STATEMENTS

Program Statements	Commands	String Functions
DEF FN	PEEK	ASC
DIM	POKE	CHR\$
END		LEFT\$
FOR	Input/Output	LEN
GOSUB	DATA	MID\$
GOTO	GET	RIGHT\$
IF... GOTO	INPUT	STR\$
IF... THEN	READ	VAL
LET	PRINT	
NEXT	SPC	Arithmetic Functions
ON... GOSUB	TAB	ABS
ON... GOTO	POS	ATN*
REM		COS
RESTORE		EXP
RETURN		INT
STOP		LOG
USR		RND
WAIT		SIN
		SGN
		SQR
		TAN

*Links to user-provided function.



A65-030 AIM 65 PL/65 COMPILER ROMS

PL/65 LANGUAGE

PL/65 is a high level language developed for the R6500 family of microprocessors. Resembling PL/I and Algol in general form, PL/65 combines high level language attributes with the power and flexibility of assembly language for efficient generation of time-critical and system implementation software. High level constructs speed program development and eliminate machine coding errors by the use of compiler generated algorithms. All language features are aimed at improving the productivity of the systems programmer by simplifying the writing of computer programs normally written in assembly language.

PRODUCT OVERVIEW

The AIM 65 PL/65 Compiler is contained in two 4K-byte ROMs that plug into sockets Z25 and Z26 on the AIM 65 Microcomputer Master Module. The compiler operates in conjunction with the AIM 65 Debug Monitor/Text Editor ROMs. Source code written in PL/65 is compiled into assembly language instructions rather than 6502 CPU machine code to allow program enhancement at the assembly level, if needed, and to avoid symbol manipulation in the compiler. Drop down capability allows assembly language to be incorporated in-line in the source code, however. The generated assembly language may then be assembled on the AIM 65 Microcomputer using the AIM 65 Assembler ROM.

Compatibility with the RM 65 Floppy Disk Controller (FDC) module and AIM 65 DOS 1.0 firmware allows efficient mass storage and file handling of source code written in PL/65, the PL/65 compiler generated assembly language and the assembled machine code—especially for large programs. The compiler inputs source code from the AIM 65 Text Editor, audio tape, TTY or user-defined devices and outputs assembly code to display/printer, memory, audio tape, TTY or user defined devices. The floppy disk interface is implemented through the user-defined functions via DOS 1.0 firmware.

PL/65 compilers have also been implemented on the AIM 65/40 Microcomputer and the System 65 Development system to allow programs written in PL/65 to be transported between these systems. AIM 65 and AIM 65/40 PL/65 is a subset of the System 65 PL/65.

FEATURES

- AIM 65 Microcomputer host and target
- ROM resident for immediate operation
- Resembles PL/I and Algol
- Increases program productivity and efficiency
- Improves program reliability
- Reduces programming errors
- Drops down to assembly language by block or single instruction for optimal code efficiency
- Includes control structures for conditional branching and iterative looping
- Supports structured programming and self-documentation
- Encourages modular program design
- Compatible with RM 65 FDC module and AIM 65 DOS 1.0.

MEMORY MAP

Address (Hex)	Contents
\$B000-\$CFFF	PL/65 Compiler Program
\$0200-\$049F	PL/65 Compiler Variables (Compilation Only)
\$0-\$4	PL/65 Compiler Variables (Compilation and Runtime)

ORDERING INFORMATION

Part No.	Description
A65-030	AIM 65 PL/65 Compiler ROMs
A65-010	AIM 65 Assembler ROM ⁽²⁾
Order No.	Description
257	AIM 65 PL/65 Compiler User's Manual ⁽¹⁾

NOTES:

1. Included with A65-030.
2. User's instructions included in AIM 65 User's Guide (Order No. 209).

PL/65 LANGUAGE STATEMENTS

Specification	Block	Imperative
ENTRY	BEGIN	SHIFT
EXIT	DO	ROTATE
TFILE	END	ASSEMBLY CODE
DFILE		INC
	Declaration	INCW
Conditional Execution	DECLARE	DEC
IF-THEN-ELSE	DEFINE	DECW
	DATA	STACK
Branching		UNSTACK
GOTO	Assignment	
CALL	Direct Single Byte Move	Looping
RETURN	Indirect Single Byte Move	FOR-TO-BY
RTI	Direct Multiple Byte Move	WHILE
BREAK		
HALT		Miscellaneous
		Comment
		Tab



A65-040 AIM 65 MATH PACKAGE ROM

FLOATING POINT ARITHMETIC

Floating point arithmetic is often desired to perform mathematical operations in calculation intensive applications such as scientific computation, industrial data acquisition and reduction, process control, and laboratory measurements. In the AIM 65 Math Package, a number is represented in floating point form as an unsigned exponent, a normalized mantissa and an arithmetic sign. The magnitude of the number is equal to two raised to the exponent power times the fractional mantissa, where the exponent may range from -127 to $+127$. The mantissa is a 32-bit number normalized such that the most significant bit (MSB) is always equal to "1". Operating on floating point numbers alleviates programming difficulty and additional development time usually associated with fixed point scaling and minimizes uncertainties when performing calculations involving both very large and very small numbers. Numbers in magnitude from $2.93873588\text{E}-39$ to $1.70141183\text{E}+38$ can be handled in the AIM 65 Math Package. In addition, nine digit accuracy is provided in most calculations.

PRODUCT OVERVIEW

The AIM 65 Math Package contains a full complement of floating point arithmetic, conversion, trigonometric, utility and other transcendental functions as user callable subroutines in a 4K-byte ROM. Programmed in 6502 machine language for fast execution, these functions support calculation intensive applications. These functions are host computer independent and may be installed in any 6502 CPU based microcomputer supporting the memory map requirements. The math package is located at $\$D000-\$DFFF$ to allow direct installation in an AIM 65 Microcomputer, an RM 65 Single Board Computer (SBC) module or in an RM 65 PROM/ROM module.

In addition to the machine language interface, direct linkage to AIM 65 FORTH and RM 65 Run-Time FORTH provides floating point processing in the FORTH language. When installed in an AIM 65 Microcomputer with AIM 65 FORTH also installed, the floating point words can be automatically linked to the FORTH vocabulary during FORTH initialization. Application programs written in FORTH can thus be both developed and executed on the AIM 65 Microcomputer. For OEM or end user installation in an RM 65 system with user-provided input/output functions, such programs can be developed on an AIM 65 Microcomputer then transferred to an RM 65 SBC based system with RM 65 Run-Time FORTH installed for execution in the RM 65 environment.

FEATURES

- Floating point arithmetic
 - Addition and subtraction
 - Multiplication and division
- Integer arithmetic
 - Multiplication
 - Division
- Comparison ($<$, $=$, $>$)
- Trigonometric
 - Sine and cosine
 - Tangent and arctangent
- Conversion
 - Degrees to radians
 - Radians to degrees
- Polynomials
 - Consecutive power
 - Odd power
- Logarithmic
 - Natural log
 - Common log
- Square root, power, exponential
- Absolute value, integer and floating point sign, greatest integer
- 6502 CPU machine instruction linkage
- Host computer independent
- AIM 65 FORTH and RM 65 Run-time FORTH compatible
- 4K-byte ROM based
- Nine digit accuracy
- Wide range ($2.93873588\text{E}-39$ to $1.70141183\text{E}+38$)

ORDERING INFORMATION

Part No.	Description
A65-040	AIM 65 Math Package ROM
A65-050	AIM 65 FORTH ROMs
RM65-0152	RM 65 Run-Time FORTH ROMs
Order No.	Description
2118	AIM 65 Math Package User's Manual ⁽¹⁾
265	AIM 65 FORTH User's Manual ⁽²⁾
812	RM 65 Run-Time FORTH User's Manual ⁽³⁾
Notes:	
1. Included with A65-040.	
2. Included with A65-050.	
3. Included with RM65-0152.	

MEMORY MAP

Address (Hex)	Contents
\$D000-\$DFFF	AIM 65 Math Package Program
\$AB-\$C4	AIM 65 Math Package Variables
\$25C-\$27E	AIM 65 Math Package Variables

MATH PACKAGE FUNCTIONS

Assembly Language Label	FORTH Word	Function	Assembly Language Label	FORTH Word	Function
INIT		Initialize Math Package	SIN	SIN	Sine
FADDT	F+	Floating Point Add	COS	COS	Cosine
FADD		Floating Point Add (Memory)	TAN	TAN	Tangent
FSUBT	F-	Floating Point Subtract	ARCTAN	ARCTAN	Arc Tangent
FSUB		Floating Point Subtract (Memory)	DEGRE	DEGREES	Convert Radians to Degrees
FMULTT	F*	Floating Point Multiply	RADS	RADIANS	Convert Degrees to Radians
FMULT		Floating Point Multiply (Memory)	POLYX	POLYODD	Odd Exponent Polynomial
FDIVT	F/	Floating Point Divide	POLY	POLY	Consecutive Exponent Polynomial
FDIV		Floating Point Divide (Memory)	MOVFM	M>F	Move Number from Memory to FAC
IMULT		Integer Multiply	MOVMF	F>M	Move Number from FAC to Memory
IDIVID		Integer Divide	MOVFA		Move Number from ARG to FAC
FTOD		Convert Floating Point to Integer	MOVAF		Move Number from FAC to ARG
DTOD		Convert Integer to Floating Point	CONUPK	M>A	Move Number from Memory to ARG
NEGFAC		Negate Floating Point Number		S>A	Move Number from Stack to ARG
ABS	FABS	Absolute Value of Floating Point Number		S>F	Move Number from Stack to FAC
INT	INT	Truncate Floating Point Number		F>S	Move Number from FAC to Stack
SGN	SGN	Sign of FAC to FAC	FIN	FIN	Convert ASCII to Floating Point
SIGN	FSIGN	Sign of FAC to ARG	FOUT	FOUT	Convert Floating Point to ASCII
FCOMP	FCOMP	Compare Floating Point Number	MINLN	MIN-WIDTH	FOUT Minimum Field Width Variable
SQR	SQR	Square Root	DECLN	DEC-LENGTH	FOUT No. of Places to the Right of the Decimal Point Variable
FPWRT	↑	Raise to a Power			
EXP	EXP	Exponential			
LOG10	LOG	Common Log			
LOG	LN	Natural Log			



A65-050 AIM 65 FORTH ROMS

FORTH LANGUAGE

FORTH is a unique programming language well suited to a variety of applications. Because it was originally developed for real-time control applications, FORTH is ideal for machine and process control, energy managements, data acquisition, automatic testing, robotics and other applications where assembly language was previously the only possible language choice.

FORTH actually provides the best of two worlds. It has the looping and branching constructs of high-level languages (DO ... LOOP, BEGIN ... END, IF ... THEN and IF ... ELSE ... THEN) and the code efficiency of machine and assembly languages. And programmers will be pleased to know that FORTH allows you to specify addresses, operands and data in hexadecimal, octal, binary or any other number base from two to 40—a distinct advantage over languages like BASIC, where all information must be in decimal.

In most time-critical applications, at least part of the program must be written in assembly language. FORTH has a built in 6502 macro assembler, and lets you drop into assembly language at almost any point in your program, without perarate assembly and load steps or awkward machine level linkage. FORTH programs typically run up to ten times faster than other interpretive languages, and can even approach the speed of machine language programs for some applications.

FEATURES

- AIM 65 Microcomputer host and target
- ROM resident for immediate operation
- Application oriented
- Extensible language
- Over 200 pre-defined functions
- Interactive compilation
- Reverse polish notation
- Compact memory usage
- Fast execution
- Easy debugging
- Stack implementation
- 16-bit words
- Built-in structured macro assembler
- Shortens software development time

PRODUCT OVERVIEW

AIM 65 FORTH, consisting of primitives, interpreter, macro assembler and input/output functions, is contained in two 4K-byte ROMs that plug into the AIM 65 Microcomputer Master Module sockets Z25 and Z26. FORTH functions are linked to AIM 65 Debug Monitor and Text Editor ROMs providing access to the AIM 65 peripherals (keyboard, single-line display and 20 column printer) as well as user-defined input/output functions. Both interactive and batch modes of operation are supported. Interactive operation interprets FORTH words upon entry for immediate execution and debugging or for compilation. In the batch mode, FORTH words can be entered into the Text Buffer then input to FORTH for interpretation. The batch mode allows an application program to be easily edited using Text Editor commands. Application programs written in FORTH can thus be developed, as well as executed for checkout or production operation, on the AIM 65 Microcomputer.

AIM 65 FORTH ROMs, when installed in an AIM 65 Microcomputer, can also be used to develop and checkout an application program written in FORTH that is to be installed in an RM 65 Single Board Computer (SBC) module for runtime operation. The developed program will run with RM 65 Run-Time FORTH ROMs installed in the RM 65 SBC module. In this configuration, all RM 65 input/output operations must be user-provided and can be tested using the AIM 65 Microcomputer as the host computer prior to being installed in the RM 65 environment.

ORDERING INFORMATION

Part No.	Description
A65-050	AIM 65 FORTH ROMs
A65-040	AIM 65 Math Package ROM
RM65-0152	RM 65 Run-Time FORTH ROM
Order No.	Description
265	AIM 65 FORTH User's Manual ⁽¹⁾
283	AIM 65 FORTH Reference Card ^(1, 2)
2118	AIM 65 Math Package User's Manual ⁽²⁾
812	RM 65 Run-Time FORTH User's Manual ⁽³⁾
NOTES: 1. Included with A65-050. 2. Included with A65-040. 3. Included with RM65-0152.	

DEVELOPING FORTH PROGRAMS

FORTH is built on subroutine-like functions, called "words." These words are linked together to form a "dictionary," which is the central core of the language. Writing a program in FORTH consists of using several predefined words to define each new word. Once the new word has been added to the system dictionary, it becomes as much a part of the language as any other word that has been previously defined. In this way new features and extensions can be added by simply defining one or more new words. Adding new features to conventional languages like BASIC or Pascal requires the language system to be completely reassembled or recompiled.

FORTH is a stack-oriented language, and is programmed in Reverse Polish Notation (RPN), the notation that is used in Hewlett-Packard scientific calculators. Using a data stack is an extremely efficient way of passing variables back and forth between operations. A data stack eliminates the need to tie up memory locations with variable tables, and allows you to use only as much memory as you need.

FORTH programs are developed using "top-down/bottom-up" techniques. That is, the programmer begins by defining the program in very general terms, then systematically breaks these definitions down into more and more detailed sub-modules. When the lowest levels of sub-modules have been defined, he starts coding, in FORTH, at those levels, working back up toward the top of the program, in pyramid fashion. Each sub-module is a stand-alone component of the program, and can be completely debugged without having the complete program in the system. This type of software development is difficult, if not impossible, to do with most other high-level languages.

FLOATING POINT FUNCTIONS

AIM 65 FORTH contains both a single- (16-bit) and double- (32-bit) precision integer arithmetic capability. In AIM 65 applications where floating point arithmetic is desired, the AIM 65 Math Package may be used in conjunction with the FORTH ROMs. These floating point functions may be called using FORTH words included in the math package ROM. When this ROM is installed in socket Z24 on the AIM 65 Microcomputer, the floating point math words can be automatically linked to the FORTH dictionary during FORTH initialization. The AIM 65 Math Package ROM can also be installed in either an RM 65 SBC or PROM/ROM module.

MEMORY MAP

Address (Hex)	Contents
\$D000-\$DFFF	Math Package Program
\$B000-\$CFFF	FORTH Program
\$280-\$2FF	Terminal Input Buffer
\$25C-\$27F	Math Package Variables
\$200-\$257	FORTH User Variables
\$AB-\$C4	Math Package Variables
\$10-\$AA	FORTH Variables

FORTH WORDS

STACK MANIPULATION

DUP	Duplicate top of stack.
2DUP	Duplicate top two stack items.
DROP	Delete top of stack.
2DROP	Delete top two stack items.
SWAP	Exchange top two stack items.
OVER	Copy second item to top.
ROT	Rotate third item on top.
- DUP	Duplicate only if non-zero
>R	Move top item to return stack.
R>	Retrieve item from return stack.
R	Copy top of return stack onto stack.
PICK	Copy the nth item to top.
SP@	Return address of stack position
RP@	Return address of return stack pointer.
BOUNDS	Convert "address count" to "end-address start-address."
.S	Print contents of stack.

DEFINING WORDS

:<name>	Begin colon definition of <name>.
:	End colon definition.
VARIABLE <name>	Create a variable <name> with initial value n; returns address when executed.
CONSTANT <name>	Create a constant <name> with value n; returns value when executed.
CODE <name>	Begin definition of assembly-language primitive operation <name>.
:CODE	Used to create a new defining word, with execution-time "code routine" for this data type in assembly.
<BUILDS ... DOES>	Used to create a new defining word, with execution-time routine for this data type in higher-level FORTH.
USER	Create a user variable.

MEMORY

@	Fetch value addressed by top of stack.
!	Store n1 at address n2.
C@	Fetch one byte only.
C!	Store one byte only.
?	Print contents of address.
+!	Add second number on stack to contents of address on top.
CMOVE	Move n3 bytes starting at address n1 to area starting at address n2.
FILL	Put byte n3 into n2 bytes starting at address n1.
ERASE	Fill n2 bytes in memory with zeroes, beginning at address n1.
BLANKS	Fill n2 bytes in memory with blanks, beginning at address n1.
TOGGLE	Mask memory with bit pattern.

NUMERIC REPRESENTATION

DECIMAL	Set decimal base.
HEX	Set hexadecimal base.
BASE	Set number base.
DIGIT	Convert ASCII to binary.
0	The number zero.
1	The number one.
2	The number two.
3	The number three.

FORTH WORDS (CONT'D)

ARITHMETIC AND LOGICAL

+	Add.
D+	Add double-precision numbers.
-	Subtract (n1 - n2).
*	Multiply.
/	Divide (n1/n2).
MOD	Modulo (i.e., remainder from division).
/MOD	Divide, giving remainder and quotient.
*/MOD	Multiply, then divide (n1-n2/n3), with double intermediate.
./	Like /MOD, but give quotient only.
U.	Unsigned multiply leaving double product.
U/	Unsigned divide.
M*	Signed multiplication leaving double product.
M/	Signed remainder and quotient from double dividend.
M/MOD	Unsigned divide leaving double quotient and remainder from double dividend and single divisor.
MAX	Maximum.
MIN	Minimum.
+ -	Set sign.
D+ -	Set sign of double-precision number.
ABS	Absolute value.
DABS	Absolute value of double-precision number.
NEGATE	Change sign.
DNEGATE	Change sign of double-precision number.
S- >D	Sign extend to double-precision number.
1 +	Increment value on top of stack by 1.
2 +	Increment value on top of stack by 2.
1 -	Decrement value on top of stack by 1.
2 -	Decrement value on top of stack by 2.
AND	Logical AND (bitwise).
OR	Logical OR (bitwise).
XOR	Logical exclusive OR (bitwise).

COMPARISON OPERATORS

<	True if n1 less than n2.
>	True if n1 greater than n2.
=	True if top two numbers are equal.
0<	True if top number negative.
0=	True if top number zero.
U<	True if u1 less than u2.
NOT	Same as 0=.

MISCELLANEOUS AND SYSTEM

(<comment>)	Begin comment (terminate by right parentheses on same line).
CFA	Alter PFA to CFA.
NFA	Alter PFA to NFA.
PFA	Alter NFA to PFA.
LFA	Alter PFA to LFA.
LIMIT	Top of memory.
QUIT	Clear return stack and return to terminal.

CONTROL STRUCTURES

DO ... LOOP	Set up loop, given index range.
DO ... +LOOP	Like DO ... LOOP, but adds stack value to index.
I	Place current index value on stack.
LEAVE	Terminate loop at next LOOP or +LOOP.
BEGIN ... UNTIL	Loop back to BEGIN until true at UNTIL.
BEGIN ... WHILE	Loop while true at WHILE; REPEAT loops unconditionally to BEGIN.
... REPEAT	
BEGIN ... AGAIN	Unconditional loop.
IF ... THEN	If top of stack true, execute following clause THEN continue; otherwise continue at THEN.
IF ... ELSE ... THEN	If top of stack true, execute ELSE clause THEN continue; otherwise execute following clause, THEN continue.
END	Alias for UNTIL.
ENDIF	Alias for THEN.

COMPILER-TEXT INTERPRETER

[COMPILE]	Force compilation of IMMEDIATE word.
COMPILE	Compile following <name> into dictionary.
LITERAL	Compile a number into a literal.
DLITERAL	Compile a double-precision number into a literal.
EXECUTE	Execute the definition on top of stack.
[Suspend compilation, enter execution.
]	Resume compilation.

DICTIONARY CONTROL

CREATE	Create a dictionary header.
FORGET	FORGET all definitions from <name> on.
HERE	Returns address of next unused byte in the dictionary.
ALLOT	Leave a gap of n bytes in the dictionary.
TASK	A dictionary marker.
	Find the address of <name> in the dictionary.
- FIND	Search dictionary for <name>.
DP	User variable containing the dictionary pointer.
C.	Store byte into dictionary.
.	Compile a number into the dictionary.
PAD	Pointer to temporary buffer.
IMMEDIATE	Force execution when compiling.
INTERPRET	The Text Interpreter executes or compiles.
LATEST	Leave name field address (NFA) of top word in CURRENT.
LIT	Place 16-bit literal on the stack.
CLIT	Place byte literal on the stack.
LITERAL	Compile a 16-bit literal.
SMUDGE	Toggle name SMUDGE bit.
STATE	User variable containing compilation state.

FORTH WORDS (CONT'D)

USER VARIABLES

UABORT	User variable for ABORT.
UB/BUF	User variable for B/BUF.
UB/SCR	User variable for B/SCR.
UC/L	User variable for C/L.
UEMIT	User variable for EMIT.
UFIRST	User variable for FIRST.
UKEY	User variable for KEY.
ULIMIT	User variable for LIMIT.

MONITOR & CASSETTE I/O

COLD	AIM 65 FORTH cold start.
MON	Exit to AIM 65 Monitor.
?TTY	Switch; true = TTY; false = KB
CHAIN	Chain tape file.
CLOSE	Close tape file.
?IN	Set to active input device (AID).
?OUT	Set to active output device (AOD).
GET	Input a character from the AID.
PUT	Output a character to the AOD.
READ	Input n2 characters from AID to address n1.
WRITE	Output n2 characters to AOD at address n1.
SOURCE	Compile from the AID.
FINIS	Terminate compile from SOURCE.

INPUT-OUTPUT

- CR	Output CR to printer only.
CR	Carriage return.
SPACE	Type one space.
SPACES	Type n spaces.
CLRLINE	Output a CTRL B.
"	Print text string (terminated by ").
DUMP	Dump n2 words starting at address.
TYPE	Type string of n1 characters starting at address n2.
?TERMINAL	True if terminal break request present.
KEY	Read key, put ASCII value on stack.
EMIT	Output ASCII value from stack.
EXPECT	Read n1 characters from input to address n2.
WORD	Read one word from input stream, until delimiter.
IN	User variable contained within TIB.
BAUD	Set BAUD rate.
BL	Output a SPACE character.
C/L	Number of characters/line.
TIB	Pointer to terminal input buffer start address.
QUERY	Input text from terminal.
ID.	Print <name> from name # field address (nfa).
HANG	Wait for keystroke.

OUTPUT FORMATTING

NUMBER	Convert string at address to double-precision number.
<#	Start output string.

OUTPUT FORMATTING (CONT'D)

#	Convert next digit of double-precision number and add character to output string.
#S	Convert all significant digits of double-precision number to output string.
SIGN	Insert sign of n into output string.
#>	Terminate output string (ready for TYPE).
HOLD	Insert ASCII character into output string.
HDL	Hold pointer, user variable.
- TRAILING	Suppress trailing blanks.
.LINE	Display line of text from mass storage.
COUNT	Change length of byte string to type form.
	Print number on top of stack.
.R	Print number n1 right justified n2 places.
D.	Print double-precision number n2 n2.
D.R	Print double-precision number n2 n1 right justified n3 places.
DPL	Number of digits to the right of decimal point.

VOCABULARIES

CONTEXT	Returns address of pointer to CONTEXT vocabulary.
CURRENT	Returns address of pointer to CURRENT vocabulary.
FORTH	Main FORTH vocabulary.
ASSEMBLER	Assembler vocabulary.
DEFINITIONS	Set CURRENT vocabulary to CONTEXT.
VOCABULARY <name>	Create new vocabulary.
VLIST	Print names of all words in CONTEXT vocabulary.
VOC-LINK	Most recently defined vocabulary.

VIRTUAL STORAGE

LOAD	Load mass storage screen (compile or execute).
BLOCK	Read mass storage block to memory address.
B/BUF	System constant giving mass storage block size in bytes.
B/SCR	Number of blocks/editing screen.
BLK	System variable containing current block number.
SCR	System variable containing current screen number.
UPDATE	Mark last buffer accessed as updated.
FLUSH	Write all updated buffers to mass storage.
EMPTY-BUFFERS	Erase all buffers.
+BUF	Increment buffer address.
BUFFER	Fetch next memory buffer.
RW	User read write linkage.
USE	Variable containing address of next buffer.
PREV	Variable containing address of latest buffer.
FIRST	Leaves address of first block buffer.
OFFSET	User variable block offset to mass storage.
- ->	Interpret next screen.
:S	Stop interpretation.

FORTH WORDS (CONT'D)

PRIMITIVES

OBRANCH	Run-time conditional branch.
BRANCH	Run-time unconditional branch.
ENCLOSE	Text scanning primitive used by WORD.
R0	Location of Return Stack.
S0	Location of Parameter Stack.
RP!	Initialize Return Stack.
SP!	Initialize Parameter Stack.
NEXT	The FORTH virtual machine.

SECURITY

!CSP	Store stack position in check stack pointer.
?COMP	Error if not compiling.
?CSP	Check stack position.
?ERROR	Output error message.
?EXEC	Not executing error.
?PAIRS	Conditional not paired error.
?STACK	Stack out of bounds error.
ABORT	Error; operation terminates.
ERROR	Execute error notification and restart system.
MESSAGE	Displays message.
WARNING	Pointer to message routine.
FENCE	Prevents forgetting below this point.
WIDTH	Controls significant characters of <name>.

MATH PACKAGE FORTH WORDS (A65-040)*

FLOATING POINT ARITHMETIC

F+	Adds two floating point numbers.
F-	Subtracts one floating point number from another floating point number.
F*	Multiplies two floating point numbers.
F/	Divides one floating point number by another floating point number.

UTILITY, SIGN AND COMPARISONS

FABS	Takes the absolute value of a floating point number.
INT	Truncates a floating point number to an integer.
SGN	Converts the sign of a floating point number to a floating point number.
FSIGN	Gets a value corresponding to the sign of a floating point number.
FCOMP	Compares the value of a compacted number in memory to a floating point number.

POLYNOMIAL

POLY	Evaluates a polynomial with consecutive exponents.
POLYODD	Evaluates a polynomial with odd exponents.

EXPONENTIAL AND LOGARITHMIC

SQR	Takes the square root of a floating point number.
>	Raises one floating point number to the power of another floating point number.
EXP	Raises the transcendental number e to the power of a floating point number.
LOG	Computes the logarithm to the base 10 (i.e., common log) of a floating point number.
LN	Computes the logarithm to the base e (i.e., natural log) of a floating point number.

USER VARIABLE

MIN-WIDTH	Specifies the minimum field width to be output.
DEC-LENGTH	Specifies the number of places to the right of the decimal point to be output.

ASCII/FLOATING POINT CONVERSIONS

FIN	Converts a number in memory from ASCII to floating point format.
FOUT	Converts a number from floating point to ASCII.

FORMAT CONVERSION AND DATA MOVING

M>F	Unpacks the compacted number in memory to floating point.
F>M	Packs the floating point number to compacted format and stores the result in memory.
M>A	Unpacks the floating point number in memory.
S>A	Converts an integer to floating point format.
S>F	Converts an integer to floating point format.
F>S	Converts a number from floating point to an integer.

TRIGONOMETRIC AND UNITS CONVERSION

SIN	Calculates the sine of a floating point number (in radians).
COS	Calculates the cosine of a floating point number (in radians).
TAN	Calculates the tangent of a floating point number (in radians).
ARCTAN	Calculates the arc tangent of a floating point number.
DEGREES	Converts a floating point number from radians to degrees.
RADIANS	Converts a floating point number from degrees to radians.

*Requires AIM 65 FORTH or RM 65 FORTH be resident.



A65-052

AIM 65 FORTH TARGET COMPILER

FORTH LANGUAGE

FORTH is a unique programming language well suited to a variety of applications. Originally developed for real-time control applications, FORTH has features that make it ideal for machine and process control, energy management, data acquisition, automatic testing, robotics and other input/output intensive applications where assembly language was previously considered to be the only possible language choice.

FORTH actually provides the best of two worlds. It has the looping and branching constructs of high-level languages (DO ... LOOP, BEGIN ... END, IF ... THEN and IF ... ELSE ... THEN) and the code efficiency of machine and assembly languages. FORTH allows programmers to specify addresses, operands and data in hexadecimal, octal, binary or any other number base from two to 40—a distinct advantage over languages like BASIC, where all information must be in decimal.

FORTH TARGET COMPILER

The FORTH Target Compiler generates object code from application programs written in FORTH. The object code is a compiled composite of the user's application vocabulary and those portions of the Target Compiler nucleus necessary to support the application vocabulary. The disk-based FORTH Target Compiler operates on the AIM 65 Microcomputer in conjunction with the AIM 65 FORTH Interpreter ROMs, the RM 65 Floppy Disk Controller (FDC) module and the AIM 65 DOS 1.0 firmware.

The compiled object code, located at a user-specified origin with optional auto-start vectors, will execute in any 6502 CPU-based microcomputer system supporting the runtime nucleus memory map requirements. Application programs can also be developed to run on AIM 65 or RM 65 SBC module-based systems with supporting RM 65 memory and input/output modules, e.g., Analog Input/Output, IEEE-488 Interface, and Multi-function Peripheral Interface Linkage to RM 65 Floppy Disk Controller, CRT Controller, and IEEE-488 module as well as the AIM 65 Math Package, firmware can also be included for expanded application systems.

FEATURES

- Fully compatible with FORTH programs developed with AIM 65 or AIM 65/40 FORTH Interpreter ROMs
- Disk-based compiler operation with vocabulary overlays for
 - Text Editing
 - Disk Interfacing
 - Serial Input/Output
 - Compiling
 - Special Utilities
- Easy compiler operation
 - Load screen direction
 - Compile tracing (mapping)
 - Compiles to RAM and/or disk
- Includes 6502 Macro Assembler with
 - Forward references
 - Symbolic labels
 - Relative branches
- Efficient object code generation
 - ROMable object code
 - Standalone operation
 - Minimum runtime nucleus
 - Optimized FORTH compiled vocabulary
 - AIM 65 autostart capability
 - User-specified origin
- Flexible target computer installation
 - System independent (runs on any 6502 CPU-based system with minimal runtime memory map requirements)

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ORDERING INFORMATION

Part No.	Description
AIM 65-052	AIM 65 FORTH Target Compiler
AIM 65-050	AIM 65 FORTH Interpreter ROMs ⁽¹⁾
AIM 65-090	AIM 65 DOS 1.0 ROM ^(1,2)
AIM 65-040	AIM 65/40 Math Package ROM ⁽⁶⁾
Order No.	Description
2105	AIM 65 and AIM 65/40 FORTH Target Compiler User's Manual ⁽³⁾
265	AIM 65 FORTH User's Manual ⁽⁴⁾
2118	AIM 65 Math Package User's Manual ⁽⁵⁾
Notes:	
(1) Required for FORTH Target Compiler operation.	
(2) Requires RM65-5101NE FDC module.	
(3) Included with A65-052.	
(4) Included with A65-050.	
(5) Included with A65-040.	
(6) Optional.	

DEVELOPING FORTH PROGRAMS

FORTH is built on subroutine-like functions, called "words." These words are linked together to form a "dictionary," which is the central core of the language. Writing a program in FORTH consists of using the dictionary words to define each new word. Once the new word has been defined it is added to the system dictionary and it becomes as much a part of the language as any other word that has been previously defined. In this way new features and extensions can be added by simply defining one or more new words.

FORTH is a stack-oriented language, and is programmed in Reverse Polish Notation (RPN), the notation that is used in Hewlett-Packard scientific calculators. A data stack is an extremely efficient way of passing variables back and forth between operations and eliminates the need to tie up memory locations with variable tables.

FORTH programs are developed using "top-down/bottom-up" techniques. That is, the programmer begins by defining the program in very general terms, then systematically breaks these definitions down into more and more detailed submodules. When the lowest levels of sub-modules have been defined, FORTH coding begins at those levels, working back up toward the top of the program, in pyramid fashion. Each sub-module is a stand-alone component of the program, and can be debugged without having the complete program in the system. The interactive nature of FORTH supports this time efficient development technique.

In most time-critical applications, at least part of the program must be written in assembly languages. FORTH has a built-in 6502 macro assembler, and allows assembly language coding at almost any point in your program, without separate assembly and load steps or special machine level linkage. FORTH programs typically run up to ten times faster than other interpretive languages, and can even approach the speed of machine language programs for some applications.

The application program is developed, debugged and integrated with the user interface using the ROM-based FORTH Interpreter. After program validation, the application is compiled into stand-alone object code with only required portions of the Target Nucleus. The compiled byte count will generally be less than the separate application/interpreter byte count.

FORTH TARGET COMPILER OPERATION

The disk-based, two-pass, FORTH Target Compiler compiles object code in one of two modes: BIG.COMPILE or QUICK.COMPILE. The QUICK.COMPILE mode compiles the entire object code directly to RAM then saves the compiled code on disk. The BIG.COMPILE mode compiles to 1K-byte buffer areas in RAM. When the buffer is full, the buffer contents are transferred to disk then compilation continues. The BIG.COMPILE mode optimizes object code RAM requirements although it compiles slower than the QUICK.COMPILE mode.

Operation of the compiler is directed by one or more LOAD SCREENS. This technique provides the user with complete control of compiler variables, origin statements, cold start vectors and utility routines. The LOAD-SCREEN(s) then specify which user screens to compile and in what order.

FLOATING POINT OPERATION

The FORTH Target Compiler provides both single-precision (16-bit) and double-precision (32-bit) single integer arithmetic functions. If floating point arithmetic is desired, code words can easily be defined within the application program to link to external floating point subroutines. The AIM 65 Math Package ROM, located at address \$8000-\$BFFF, can be installed in the application system. Alternatively, user-defined floating point functions may be linked to or even provided within the code definitions.

SYSTEM REQUIREMENTS

The AIM 65 FORTH Target Compiler operates in an AIM 65 Microcomputer in conjunction with an RM 65 32K Dynamic RAM module and an RM 65 FDC module with an AIM 65 DOS 1.0 ROM installed on the FDC module. The following table lists two configurations of AIM 65/40 and RM 65 hardware and firmware which may be used. Other configurations can be easily composed depending on the user's development and application requirements.

Required Peripherals Firmware	Host Computer	
	A65-450 AIM 65 Microcomputer with 4K RAM and FORTH ROMs	A65-550 AIM 65 Microcomputer System with 4K RAM and FORTH ROMs
RM65-7104E RM 65 Adapter/Buffer for AIM 65, or RM65-7116E RM 65 Cable Adapter/Buffer for AIM 65 }	X	X
RM65-7004E RM 65 4-Slot Card Cage	X	X ⁽²⁾
RM65-3132E RM 65 32K Dynamic RAM Module	X	X
RM65-5101NE RM 65 Floppy Disk Controller (FDC) Module (without ROM)	X	X
A65-090 AIM 65 DOS 1.0 ROM	X	X
A65-050 AIM 65 FORTH ROMs	(1)	(1)
A65-040 AIM 65 Math Package ROM	Optional	Optional
Note: X = Required in addition to host computer. 1. Included in host computer. 2. Remote to AIM 65 enclosure.		

FORTH WORDS (Continued)

EDITOR VOCABULARY OVERLAY

BUFFERS

INSERT-BUF An 80-byte buffer beginning at PAD + 80.

FIND-BUF An 80-byte buffer beginning at PAD + 160.

LINE ORIENTED COMMANDS:

K Swaps the contents of the INSERT-BUF and FIND-BUF.

LINE On current screen, returns the RAM address of the beginning of the line#.

M Replaces INSERT-BUF and line# in block# with current referenced line.

NEW Beginning at line#, clears each line and allows a NEW line to be typed in. Input is terminated by a null line entry (CR CR). Clears remaining lines on the current screen.

P Copies text into the INSERT-BUF and the current line until the delimiter (CR) is encountered.

TILL Beginning at the current cursor address, deletes text UNTILL the end of the matching text string is encountered. The text is held in FIND-BUF.

T Moves cursor to beginning of line# in current screen. Shows the line.

U Copies text into the INSERT-BUF and the line on the current screen under the cursor.

X Copies the current line into INSERT-BUF. Then deletes the line and scrolls the screen up. The last line becomes a blank.

>LINE# Returns the current cursor line #.

(DELETE) Referring to the current cursor position, deletes n preceding characters and calls UPDATE.

(HOLD) Copies the referenced line number into INSERT-BUF and UPDATE.

(KILL) Blanks line# and UPDATE.

(PUT) Replaces the current line with contents of INSERT-BUF.

? Prints the current line with the cursor at current cursor position and the line number at the end of the line.

1LINE Searches the current line after cursor position for a match to contents of FIND-BUF. Repositions cursor to it if a match is found and sets f=1. If no match is found, sets f=0 and positions the cursor to the next line.

STRING ORIENTED COMMANDS

D Finds the text, deletes it and shows the line.

F Finds the text, positions the cursor at the end of the text string and shows the line.

I Inserts the contents of INSERT-BUF into line.

MATCH Searches the memory space beginning at ADDR2 for CNT2 for a match of the data beginning at ADDR1 for CNT1. If no match is found, sets f=1 and ADDR3=ADDR1 + CNT1. If a match is found, sets f=0 and ADDR3=address of the next byte after the matching string.

(F) Locates the text in the buffer.

#LAG Returns the address of the character following the cursor and then counts to the line end.

#LEAD Returns the address of the character preceding the cursor and the count to the beginning of the line.

SCREEN COMMANDS

B Moves to last block.

L Lists current screen.

N Moves to next block.

TOP Moves cursor to the top line of the text.

WIPE Clears the entire screen.

MISCELLANEOUS COMMANDS

BUF-MOVE Move non-null contents of PAD to ADDR.

E Erases the string in front of the cursor for a length equal to the string in FIND-BUFF.

R Replaces string identified by FIND-BUFF with TEXT.

S Beginning at current screen and continuing through screen #n, searches for a string match to TEXT and displays matches.

CURSOR COMMANDS

R# Returns the cursor position (n).

#LOCATE Returns byte position of cursor and line number.

>> Adds n to cursor position and displays line.

TEXT Takes text from input stream until DLIMiter character is encountered (65 characters maximum). Moves text to PAD and fills to 65 characters with blanks (\$20).

USE Displays CHAR as the cursor.

WHERE Displays where an error in LOADING occurred. Also shows context and current.

FORTH WORDS

GENERAL PURPOSE VOCABULARY

The following FORTH words are provided in addition to those provided in the A65-050 FORTH Interpreter ROMs (refer to Data Sheet Order No. D87).

ABORT	Prints TEXT if a run-time error occurs.	Y/N?	Asks the question YES? or NO?, depending on $f_1 = 1$ or 0. Returns f_2 as true or false depending on input match to f_1 .
ASCII	During compile time, places a CLIT and the literal value of CHAR in the dictionary. In immediate mode, returns the ASCII value on the stack.	2ROT	Rotates double-precision numbers d_1, d_2, d_3 .
COMBINE	Combines low byte of l and high byte of h to form n.	2*	Returns $d_3 = d_1 * d_2$.
COMPILING	Activates the Compiler Vocabulary Overlay.	2OVER	Double-precision OVER.
DISKING	Activates the Disk Vocabulary Overlay.	2SWAP	Double-precision SWAP.
EDITOR	Activates the Editor Overlay.	= =	Execution only. Creates a constant NAME with value n.
EXTERNAL	Execution only. NFA of next word to be defined.	-TEXT	Compares strings at ADDR1 and ADDR2 for n bytes. Returns $f=1$ if same.
FALSE	Returns a false flag.	?DEF	IF NAME is defined, returns $f=1$.
H.	Prints n as an unsigned hexadecimal value.	?RANGE	Returns $f=1$ if $u2 < n1 < n3$ for signed numbers.
HI	Returns the high byte of n.	?URANGE	Returns $f=1$ if $u2 < u1 < u3$ for unsigned numbers.
IFEND	Marks a place.		
IFTRUE	Compiles the following input if $f=1$, otherwise skips.		
INTERNAL	Returns the NFA of the latest word defined.		
LO	Returns the low byte of n.		
LOADER	Creates word NAME that loads screen no. n.		
MODULE	Execution only. Places NFA1 into LFA of NFA2.		
OFF	Stores a 0 in ADDR.		
ON	Stores a 1 in ADDR.		
ROLL	Rotates the nth number to the top of the stack.		
ROOM	$n = \text{RAM space left}$.		
SET	Places value n in variable or constant NAME.		
SPLIT	Returns low and high byte of n.		
THRU	Performs sequential LOAD's beginning at screen no. n and continuing through screen no. n.		
TRUE	Returns a true flag.		
U.	Outputs n as a double-precision number.		
UNRAVEL	Back traces the return stack.		

DISK VOCABULARY OVERLAY

BACKUP	Copies all of drive 0 to drive 1.
BLOCKS	Copies block b1 through b1+n to block b2 through b2+n.
COPY	Copies block b1 to block b2.
DOWN	Beginning at block b and continuing for n blocks, copies from drive 1 to drive 0.
MASSACRE	Clears n blocks beginning at block b, DR0.
SCREENS	Copies screens S1 through S1+n to screens S2 through S2+n.
SLATE	WRITES blanks (\$20) to block b relative to DRIVE 0.
SWEEP	READS blocks b through b+n searching for disk errors.
UP	Beginning at block b, copies n blocks from drive 0 to drive 1.
VERIFY	Compares blocks beginning at b1 to those beginning at b2 for n blocks and displays errors.
VOLUME	Returns the block number of the block 0 of drive 2 relative to drive 0.
?WRONG	If $b1 = b2$, then sets $f=1$, else sets $f=0$.

FORTH WORDS (Continued)

TARGET COMPILER VOCABULARY
OVERLAY

LISTS

SYMBOLS	Defines names in the object code.
LOCALS	Defines words at compile time only.
MAGICS	Immediate words.

SWITCHES & FLAG WORDS (directives active during compile)

ON	Changes switch state to ON.
OFF	Changes switch state to OFF.
MAPPING	Prints or displays the name and CFA of each WORD when created.
GAG	Suppresses most non-fatal error messages.
AUTO.FORWARD	Automatic forward reference for undefined words.
NUMERIC	Values must be preceded by a valid decimal character to be a valid number.
ROMABLE	Generates read-only code.

CONTROL WORDS

FORWARD	Forces forward reference of the name immediately following.
WIDE	Name field length (headerless code).
SET	Changes the value of FORTH user constants.
WINDOW.LO WINDOW.HI	Defines the Target address space boundaries.
DESTINATION	Defines the target buffer block number.
RAM.LO } RAM.HI }	Identifies nucleus RAM boundaries. Extends from RAM.LO for USER.SIZE bytes.
USER.SIZE	Number of bytes reserved beginning at RAM.LO. RAM between RAM.LO + USER.SIZE and RAM.HI is used for work buffers (PAD, etc.) when ROMABLE flag is set.
ORIGIN	Compiler's target dictionary.
FAST.COMPILE	Target space will be RAM only, based on WINDOW.LO and WINDOW.HI.
BIG.COMPILE	Target space maybe virtual data space on disk.
CLEAR.TARGET	Fills the target area with zeros.

READY	Initializes internal variables to their default value.
START	Begins the compilation. Everything following this command will be interpreted or compiled in the simulated target machine environment.

DEFINING WORDS

= =	Generates an equate type statement.
LABEL	For use in assembly language to provide flexibility and allow code sharing.
VARIABLE	If ROMABLE is true, VARIABLE becomes a USER variable, otherwise variable is identical to ROM-based FORTH.
BYTES	Sets aside bytes in RAM area (like ALLOT).
RAM	Equivalent to ROM command HERE. Returns current RAM address.
BCC, BCS, BNE, BEQ, BPL, BMI, BVC, BVS,	Relative branch opcodes for assembly operation.

MAGIC WORDS

DLITERAL	Compiles a double number in line.
ASCII	Compiles CLIT of following ASCII character.
DOES>	Immediate word to separate <BUILDS DOES> into TARGET NUCLEUS and Target Compiler.
:CODE	Identical to CODE but also sets a pointer for LOCATE.
LOCATE	Informs the compiler where the execution time CODE is located.
REVEAL	Similar to SMUDGE.
HIDE	Sets the SMUDGE bit on the last target word.



A65-060 AIM 65 INSTANT PASCAL ROMS

PASCAL LANGUAGE

Pascal is a powerful high-level computer programming language originally designed for educational purposes. Developed by Niklaus Wirth of the ETH Technical Institute of Zurich in 1971, Pascal has gained acceptance worldwide as the standard language to teach computer programming. The rich variety of Pascal language features allows a wide range of data structures to be specified and complex algorithms to be implemented. Programming in Pascal using structured programming techniques produces programs that are easy to write, understand and maintain. The widespread teaching of the language coupled with the increased productivity of the programmer and the improved reliability of compiler generated code is causing Pascal to be increasingly adopted in industrial and scientific applications as well as in the classroom.

PRODUCT OVERVIEW

AIM 65 Instant Pascal™ is a unique implementation of the Pascal language which combines the immediacy of ROM-based software, interactive source code entry and debug facilities, on-board AIM 65 printer and display peripherals and low-cost expansion memory, to provide a complete Pascal education, development and application system. The language is a major subset of Standard Pascal (defined by K. Jensen and N. Wirth in their book, "Pascal User Manual and Report") incorporating all of the simple and structured statements, and the most widely used simple and structured data types. Extensions to the language permit direct control in Pascal of the AIM 65 Microcomputer memory-mapped I/O and allow interfacing to machine-language programs developed with the AIM 65 Assembler.

Instant Pascal incorporates facilities to write and debug programs entirely at the source language level. These facilities include source-level editor, breakpoint, and trace—plus immediate source statement execution for examination and modification of data. Source statements are translated immediately upon entry into an intermediate language which is interpretively executed.

The 20K-byte AIM 65 Instant Pascal software comes in a five-ROM set. One ROM plugs into AIM 65 Master Module socket Z24 while the other four ROMs plug into an RM 65 16K-byte PROM/ROM (RM65-3216E) module.

™Instant Pascal is a trademark of Melvin E. Conway.

FEATURES

- AIM 65 Microcomputer host and target
- Substantial subset of Standard Pascal (Jensen and Wirth)
- ROM resident for immediate operation
- Direct control of memory mapped I/O
- Machine language interface linkage
- Source code editor
 - Position text pointer
 - Find character string
 - List, delete, insert statement
 - View statement
- Flexible program control
 - Check syntax for coding errors without executing program
 - Execute one statement to allow examination and modification of data
 - Execute entire program
- Source level debugging facilities
 - Breakpoint
 - Assignment trace lists values as they are changed
 - Statement trace lists statements as they are executed
- Device Source I/O
 - Input source code from specified device
 - Output source code to specified device

MEMORY MAP

Address (Hex)	Contents
\$B000-\$BFFF	Pascal Program
\$4000-\$7FFF	Pascal Program
\$FC3-\$FFF	Translator input area (default value)
\$ED2-\$FC2	Translator output area (default value)
\$300 up	Execution stack (default value)
\$FC-\$FF	Pascal Variables
\$06-\$B4	Pascal Variables

ORDERING INFORMATION

Part No.	Description
A65-060	AIM 65 Instant Pascal ROMs
Order No.	Description
279	AIM 65 Instant Pascal User's Manual*
Note: *Included with A65-060.	

INSTANT PASCAL EXTENSIONS TO STANDARD PASCAL

- Variables, both simple and structured, may be given absolute memory addresses. This permits Pascal programming of memory-mapped I/O and linkage to machine-language subroutines.
- The OTHERWISE: default clause is implemented in the CASE statement. Identifiers may have any length; the entire identifier is significant.
- Data of type STRING may have lengths which vary dynamically up to the declared maximum length. The type S:STRING[C] is implemented as S:ARRAY[0..C] OF CHAR, where S[0] is the value of the dynamic length. (C is a constant less than 256.)
- The predefined procedure BREAK causes interruption of program execution, if it is enabled.
- The predefined procedure SUBR(ENTRANCE) calls the machine-language subroutine whose entrance address is the declared address of the absolute variable ENTRANCE. The variant SUBR(ENTRANCE, DATA) places the address of the Pascal variable DATA in page 0 before giving control to the subroutine.
- The predefined functions FUNC(ENTRANCE) and FUNC(ENTRANCE, DATA) are the same as SUBR; in addition they return a CHAR-type value which the subroutine leaves in A.

STANDARD PASCAL FEATURES NOT IMPLEMENTED IN INSTANT PASCAL

- Files and their associated predefined procedures and variables (GET, PUT, RESET, REWRITE, EOLN, EOF) are not implemented. The predefined procedures READ, READLN, WRITE, WRITELN are implemented to interface with all character-serial devices available to the AIM 65 Monitor, including user-defined devices. The following types may be read and written: char, integer, real, Boolean (Y or N on input), variable-length string.
- Set expressions are not implemented. One-byte sets (with up to eight elements) and the relational operator IN are implemented; these permit Pascal-level testing of I/O device status.
- Records are implemented, but record variants are not.
- Dynamic storage allocation and the pointer type are not implemented.
- The directive FORWARD is not implemented.
- The constant definition identifier=identifier; is not implemented.
- Ambiguity between field and variable names at the same block level is not supported. Other Pascal visibility rules are fully supported.
- Packing of data is not done below the byte level. The word-symbol PACKED is accepted but ignored, and the predefined procedures PACK and UNPACK are not implemented.
- Procedural and functional parameters to procedures and functions are not implemented.
- GOTO may not jump outside its own block.
- The 60-character input line of the AIM 65 limits the length of certain constructs, in particular simple statements, procedure/function headings, and enumerated type lists, which may not be extended during input from one line to the next.

OPERATION OF INSTANT PASCAL

All operations in the Instant Pascal system are controlled by a set of single-letter commands. The system generally performs one of the following six major operations.

1. Source input from keyboard or input device.
2. Source output to printer or output device.
3. Program editing: positioning the text unit pointer or deleting text units.
4. Syntax checking a program. This operation is called automatically at the first call to execute a program after any change. It may also be called explicitly.
5. Executing a program.
6. Executing a single statement entered by the user.

All commands are preceded by the Instant Pascal prompt "+<." The numeric parameter n in some of the commands has either a decimal value or one of the following two default values: "."=forever; CR=1.

INSTANT PASCAL OPERATION COMMANDS

Text Unit Pointer Movement

+<T>	Position to top text unit.
+	Position to bottom text unit.
+<U>/n	Position up n text units.
+<D>/n	Position down n text units.
+<F>string	Find the line containing the argument string.

Source Text Editing

+<K>/n	Delete n text units.
+<I>	Insert one line of source.
+< >space	List current text unit.
+<V>	View a neighborhood of five text units centered at the current one.

Device Source I/O

+<R>IN=device	Read lines of source until empty line.
+<L>/nOUT=device	List n text units to the specified device.

Toggles

+<S>	Toggle statement trace.
+<A>	Toggle assignment trace.
+<E>	Toggle enabling of the BREAK procedure.

Program Control

+<C>	Check program syntax.
+<G>	Execute program. Starts at beginning of program unless a break is in progress. Break-in-progress status may be cancelled with the C command or by changing the program.
+<,>	Execute and trace until the start of the next statement and return with break-in-progress status set.
+<X>statement	Immediately execute the statement. Identifier visibility is defined by the position of the text unit pointer in the program.

Miscellaneous

+<W>	Redefine page width. The default value of 20 may be changed if a terminal is attached to the AIM 65.
+<N>	Initialize to empty program.
+<M>	Report number of free memory bytes.
+<Z>	Cold start.

MEMORY EXPANSION CONSIDERATIONS

About 1.5 bytes per character of source code is required to store an application program written in Pascal in memory due to the translation process. For minimum applications requiring less than 3.2K bytes of on-board user RAM, the PROM/ROM module can be connected to the AIM 65 Expansion Connector using an RM 65 Single Card Adapter. For larger applications, connection of an RM 65 multi-slot card cage through an RM 65 Adapter/Buffer module is recommended. One or more RM 65 RAM modules can then be added as required. Up to 15.2K bytes of contiguous RAM can be dedicated to the application program.



A65-090

AIM 65 DISK OPERATING SYSTEM

VERSION 1.0 (DOS 1.0) ROM

DISK OPERATING SYSTEM

A disk operating system (DOS) provides a standard interface between the user and one or more floppy disk drives, floppy disk control (FDC) hardware and executive-level software. The DOS, implemented in software, allows program and data files to be opened, closed, read and written under operator or program control. In an interactive environment, commands are usually initiated by the operator from the keyboard in response to user-friendly prompts displayed by the system.

PRODUCT OVERVIEW

The AIM 65 Disk Operating System Version 1.0 (DOS 1.0) provides disk and file management functions for the AIM 65 Microcomputer in conjunction with an RM 65 Floppy Disk Controller (FDC) module. With this configuration, mass storage files can be easily manipulated when connected to one to four 5¼" or 8" floppy disk drives. DOS 1.0 functions, contained on a 4K-byte ROM that plugs into the FDC module, are available immediately upon computer power turn-on without waiting for separate loading of a disk-based DOS into RAM.

DOS 1.0 functions are operator commandable through interactive AIM 65 Debug Monitor/Text Editor operation as well as language (assembler, compiler and/or interpreter) operation. Text and program source code may be written to, and read from, disk with the Editor List and Read commands, respectively. Binary data and program object code may be written to, and loaded from, disk using the Debug Monitor Dump and Load commands, respectively. Files containing source and object code for application programs written in AIM 65 Assembler, BASIC, FORTH, PL/65 and Instant Pascal languages are therefore supported. In addition, utility functions format a disk, list the contents of the disk directory, delete a file, recover a file and backup a disk upon command. The DOS functions may also be called under program control by the application program into order to read and write data files.

Disk read or write errors, both at the DOS and FDC hardware level, are reported upon detection. User-alterable variables allow changing of default values to application unique values.

Disks formatted by AIM 65 DOS 1.0 are compatible with AIM 65/40 DOS 1.0 and AIM 65/40 BDOS 1.0. Files written by any of these DOS programs may therefore be read by either microcomputer.

FEATURES

- AIM 65 Microcomputer compatible
- ROM resident for immediate operation
- Installs on-board RM 65 Floppy Disk Controller (FDC) module
- Provides mass storage of programs and data
- Compatible with AIM 65 high level language and Assembler ROMs
- Disk oriented commands (format, list, backup)
- File oriented commands (list, delete, recover)
- Input/Output commands
 - Read and write text and object code
 - Automatic file open and close
- User-alterable variables
 - Utility function and error handling vectors (before and after DOS functions)
 - Input/output vectors
 - I/O buffer vectors
- Extensive error detection and reporting

MEMORY MAP

Address (Hex)	Contents
\$8F00-\$8FFF	RM 65 FDC Module I/O
\$8000-\$8EFF	DOS 1.0 Program
\$600-\$7FF	DOS 1.0 I/O Buffer (default location)
\$500-\$563	DOS 1.0 Variables
\$4A0-\$4FA	DOS 1.0 Variables
\$D7-\$DE	DOS 1.0 Variables

ORDERING INFORMATION

Part No.	Description
A65-090	AIM 65 DOS 1.0 ROM
RM65-5101NE	RM 65 FDC Module (without ROM containing primitive subroutines ⁽²⁾)
Order No.	Description
802	RM 65 FDC Module User's Manual ⁽¹⁾

Notes:

1. Describes user's instructions for AIM 65 DOS 1.0. Included with A65-090 and RM65-5101NE.
2. The DOS 1.0 ROM includes primitive subroutines in addition to DOS functions.



A65-901 AIM 65 PROM PROGRAMMER AND CO-ED MODULE

PRODUCT OVERVIEW

The A65-901 PROM Programmer and CO-ED Module is one of the hardware options available for the AIM 65 Microcomputer family.

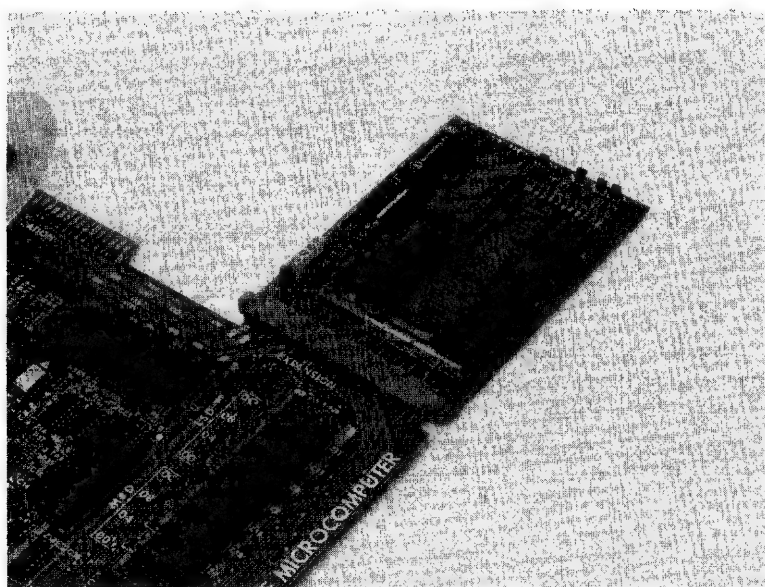
The A65-901 PROM Programmer and CO-ED Module programs 1K-, 2K-, and 4K-byte PROMs that can be installed in the AIM 65 microcomputer or in a RM 65 16K PROM/ROM Module. The PROM Programmer provides check, program, verify and read functions.

The utility of the Module is enhanced through the included Object Code Editor (CO-ED). CO-ED allows you to edit object code in much the same way as you can edit source code for the AIM 65 Assembler, using AIM 65's Text Editor. With CO-ED, patches can be made directly in your program without having to go through the time-consuming process of re-assembling.

The A65-901 PROM Programmer and CO-ED Module also supports data load, verify and dump with offset functions. And the Module plugs directly into the AIM 65 Expansion Connector.

FEATURES

- Plugs directly onto the AIM 65 Expansion Connector
- Programs the following 5 volt PROMs (or equivalents):
 - Intel 2758, 2716 and 2732
 - TI TMS 2508, 2516 and 2532
- Provides programming functions to check, program, verify and read PROM
- Includes utility functions to load, verify, dump, fill and invert memory
- Incorporates object code editor (CO-ED) functions to control program pointers; search for operands, jumps/branches and strings; and to modify instructions with automatic address adjustment
- 1K bytes of Static RAM are included to allow single-pass programming of a 4K-byte PROM when used with a 4K RAM version of AIM 65
- Zero insertion force (ZIF) socket for PROM being programmed
- On-board DC/DC Converter allows +5V-only operation
- Fully assembled, tested and warranted



A65-901 PROM Programmer and CO-ED Module

FUNCTIONAL DESCRIPTION

The R6520 Peripheral Interface Adapter (PIA) is the primary interface device between the AIM 65 Expansion Connector and the 24-pin Zero Insertion Force PROM socket and control circuits. During PROM programming, PROM address, PROM data and programming control signals are transmitted to the PIA on the AIM 65 Expansion Connector data lines. During PROM check, verify and read operations, only PROM address and control signals are issued to the PIA from the AIM 65.

Four PIA I/O Lines carry the most significant address signals to the PROM. Eight other PIA I/O lines multiplex the PROM data and least significant address signals. One output line controls the Tri-State Data Latch. Five other PIA I/O Lines control the Power Switches.

During PROM programming, PROM data is transferred to the tri-state Data Latch, which drives the latched data to the PROM. The PROM address is then sent to the PROM on the eight multiplexed data/address lines and the four dedicated address lines. The Power Switches are then turned on to apply the proper voltage levels for the required time duration to transfer the 8-bits of data into one PROM location. The process is repeated until the specified PROM address range is fully programmed. The tri-state Data Buffer is disabled during programming.

During PROM read operations, the PIA sets the address lines to the PROM. The tri-state Data Buffer drives the PROM data onto the AIM 65 Expansion Connector data lines. The Data Latch is disabled at this time.

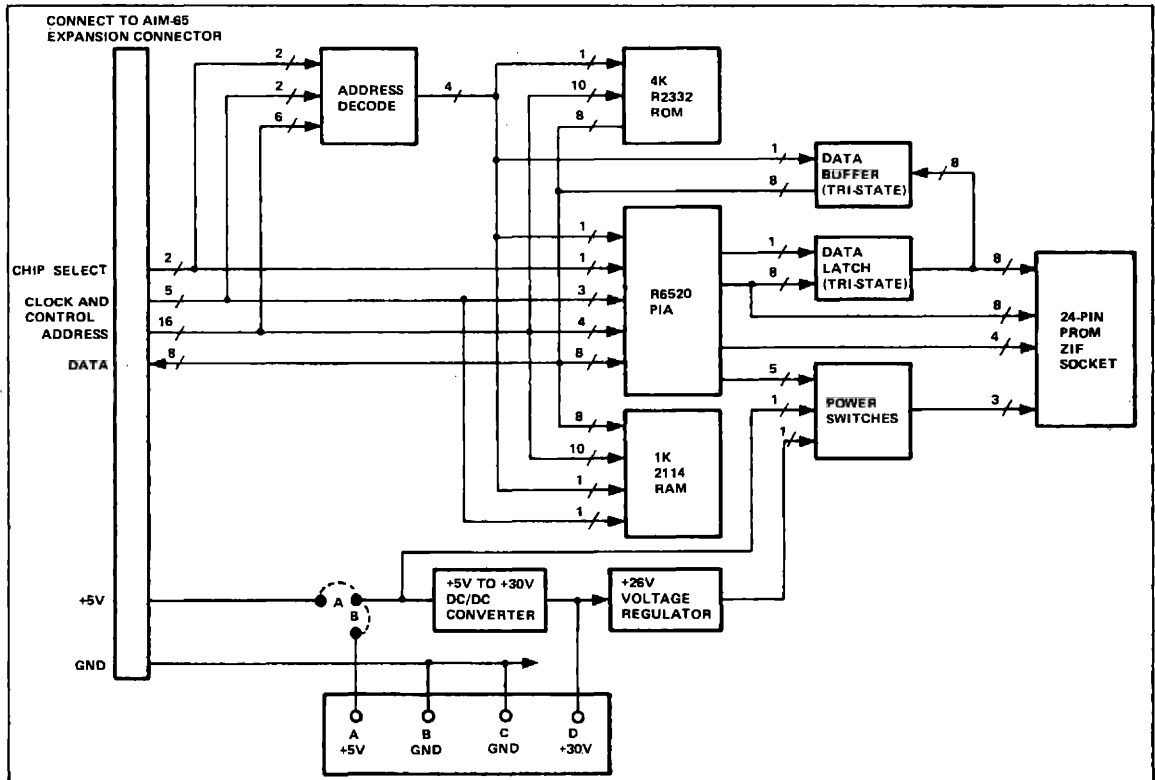
The Power Switches drive +5V or +26V onto three PROM socket programming lines depending on the PROM type selected.

The 4K R2332 ROM contains the PROM Programmer and CO-ED firmware.

1K bytes of on-board RAM are provided for use by the PROM Programmer and CO-ED software. The RAM is mapped from \$1000-\$13FF to provide contiguous addressing from the top of a 4K RAM AIM 65.

The Address Decode circuitry generates individual chip select signals to the RAM, ROM, PIA and the Data Buffer.

The PROM Programmer and CO-ED Module may be powered from the AIM 65 or from an external +5V power supply. A DC/DC Voltage Converter generates +30V from +5V. The +30V is regulated to +26V for on-board use. The +30V may be connected to an external power supply to minimize current drain on the +5V supply.



A65-901 PROM Programmer and CO-ED Module Block Diagram

AIM 65 Expansion Connector Pin Assignments

Top (Component Side)				Bottom (Solder Side)			
Signal Mnemonic	Signal Name	Input/Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/Output
SYNC	*Sync	O	1	A	A0	Address Bit 0	I
RDY	*Ready	I	2	B	A1	Address Bit 1	I
$\phi 1$	*Phase 1 Clock	O	3	C	A2	Address Bit 2	I
IRO	*Interrupt Request	I	4	D	A3	Address Bit 3	I
S.O.	*Set Overflow	I	5	E	A4	Address Bit 4	I
NMI	*Non-Maskable Interrupt	I	6	F	A5	Address Bit 5	I
RES	Reset	I	7	H	A6	Address Bit 6	I
D7	Data Bit 7	I/O	8	J	A7	Address Bit 7	I
D6	Data Bit 6	I/O	9	K	A8	Address Bit 8	I
D5	Data Bit 5	I/O	10	L	A9	Address Bit 9	I
D4	Data Bit 4	I/O	11	M	A10	Address Bit 10	I
D3	Data Bit 3	I/O	12	N	A11	Address Bit 11	I
D2	Data Bit 2	I/O	13	P	A12	Address Bit 12	I
D1	Data Bit 1	I/O	14	R	A13	Address Bit 13	I
D0	Data Bit 0	I/O	15	S	A14	Address Bit 14	I
-12V	*-12 Vdc		16	T	A15	Address Bit 15	I
+12V	*+12Vdc		17	U	SYS $\phi 2$	System Phase 2 Clock	O
CS8	Chip Select 8	O	18	V	SYS R/W	System Read/Write	O
CS9	Chip Select 9	O	19	W	R/W	Read/Write "Not"	O
CSA	*Chip Select A	O	20	X	TEST	Test	O
+5V	+5 Vdc		21	Y	$\phi 2$	Phase 2 Clock "Not"	O
GND	Ground		22	Z	RAM R/W	RAM Read/Write	O

NOTE:
" = Not used on this module.

PROM Programmer Commands

Category	Command	Function
ENTRY/EXIT	F1 F2 ESC	ENTER PROM PROGRAMMER RE-ENTER PROM PROGRAMMER ESCAPE TO MONITOR
BASE ADDRESS	B O	PROM BASE ADDRESS RAM BASE ADDRESS
PROM	C P V R	CHECK PROM PROGRAM PROM VERIFY PROM READ PROM
MEMORY	L T D M I	LOAD MEMORY VERIFY MEMORY DUMP MEMORY FILL MEMORY INVERT MEMORY
RECORDER CONTROL	1 2	TOGGLE RECORDER CONTROL LINE 1 ON/OFF TOGGLE RECORDER CONTROL LINE 2 ON/OFF

CO-ED Commands

Category	Command	Function
ENTRY/EXIT	F3 / ESC	ENTER CO-ED EXIT CO-ED ESCAPE TO MONITOR
POINTER CONTROL	W T B U D G X	LOCATE PROGRAM MOVE TO TOP OF PROGRAM MOVE TO BOTTOM OF PROGRAM MOVE UP ONE INSTRUCTION MOVE DOWN ONE INSTRUCTION GO TO ADDRESS EXCHANGE POINTERS
SEARCH	F J S	FIND AN OPERAND FIND JUMPS AND BRANCHES FIND A STRING
PROGRAM MODIFICATION	I \$ A C M R	INSERT AN INSTRUCTION STRIKEOUT AN INSTRUCTION ADJUST INSTRUCTION BLOCK CHANGE INSTRUCTION MOVE INSTRUCTION/DATA BLOCK RELOCATE
UTILITY	I K	FILL MEMORY DISASSEMBLE MEMORY

SPECIFICATIONS

Parameter	Value
Dimensions Width Length Height	4.4 in. (111 mm) 6.3 in. (160 mm) 0.75 in. (19 mm)
Weight	5.3 oz. (150 g)
Environment Operating Temperature Storage Temperature Relative Humidity	0°C to 70°C -40°C to 85°C 0% to 85% (without condensation)
Power Requirements With DC/DC Converter Without DC/DC Converter	+5V ± 5%, 1.1 A (5.5 W) — Maximum +5V ± 5%, 0.75 A (3.75 W) — Maximum +30V ± 5%, 0.04A (1.2 W) — Maximum
Memory Map User RAM I/O ROM	\$1000 — \$13FF \$8800 — \$8FFF \$9000 — \$9FFF



A65-905 AIM 65 MEMORY CARTRIDGE

PRODUCT OVERVIEW

The A65-905 Memory Cartridge is one of the hardware options available for the AIM 65 Microcomputer family.

Many applications of AIM 65 microcomputers, particularly in test equipment, instrumentation, monitors, analyzers or controllers, require that the resident application software or fixed parametric data be changed periodically. This may occur because the item under test or being controlled has been changed, or parameter values have been revised. For OEM installations, the change may be required to customize the system for different customers.

The AIM 65 Memory Cartridge system is an economical and convenient method for expanding the memory of an AIM 65 microcomputer. The cartridges are designed for use with the Rockwell packaged 500 Series of desktop microcomputers, but may also be used with any AIM 65 board-level microcomputer. A Buffer Module connects to the AIM 65 Master Module, buffers the expansion bus signals, and provides a covered host receptacle for a Memory Cartridge. In addition to expanded RAM and provisions for user application PROM firmware, a variety of pre-configured AIM 65 high level languages, assembler and math package routines are available in plug-in Memory Cartridge form. These language cartridges permit the user to program different applications in different languages. Unpopulated RAM and PROM/ROM cartridges are also available for complete user flexibility.

The Buffer Module fits under the AIM 65 Master Module and fastens securely to the Rockwell AIM 65 Enclosure. Rugged injection molded plastic covers for both the Buffer Module and the Memory Cartridge complement the AIM 65 Enclosure in color, texture and sturdiness. A Memory Cartridge plugs vertically into the Buffer Module immediately behind the microcomputer enclosure to require a minimum of area in desktop applications. A recessed label area on the Memory Cartridge cover allows configuration information to be neatly added in an area visible to the operator. Address decoding required by the different cartridges is accomplished automatically without user intervention.

A 16K Battery Backed CMOS RAM Cartridge retains program and data in memory when the AIM 65 Microcomputer power is turned off. Critical information can thus be preserved during AC power transients or outages and during normal turn-off cycles.

FEATURES

- Preconfigured Memory Cartridges
 - AIM 65 high level languages and support firmware
 - Up to 16K bytes additional RAM (volatile or non-volatile)
 - Up to 32K byte additional PROM/ROM
 - Combination RAM and PROM/ROM
- Permanent Buffer Module installation
- Convenient Memory Cartridge plug-in installation
- Use with any AIM 65 500 Series Desktop Microcomputer
- Compatible with A65-006 enclosure and power supply
- Cartridges are fully assembled, tested and warranted

ORDERING INFORMATION

Part No.	Description
A65-905-00	Buffer Module
A65-905-01	BASIC Interpreter, Assembler, 8K CMOS RAM & 4K User PROM Socket
A65-905-02	PL/65 Compiler, Assembler, 8K CMOS RAM & 4K User PROM Socket
A65-905-03	FORTH, Math Package, 8K CMOS RAM & 4K User PROM Socket
A65-905-04	Instant PASCAL & 6K CMOS RAM
A65-905-05	32K PROM/ROM (1)
A65-905-06	16K CMOS RAM
A65-905-07	16K CMOS RAM (unpopulated)
A65-905-08	8K CMOS RAM & 16K PROM/ROM (1)
A65-905-09	16K Battery Backed CMOS RAM
(1) PROMs not included.	



AIM 65 Desktop Microcomputer with Memory Cartridge

FUNCTIONAL DESCRIPTION

BUFFER MODULE

The Buffer Module interfaces the AIM 65 Expansion Connector to a Memory Cartridge as illustrated. Non-inverting circuits buffer the data and address lines. Data direction is controlled by the BR/W signal. During a write operation, data from the AIM 65 Master Module is directed towards the cartridge. During a read operation, data from the cartridge is directed towards the AIM 65 Master Module. The RAM R/W signal is routed through the Buffer Module to the cartridge interface to control the Memory Cartridge device read/write operation.

Address decoding is accomplished by a factory programmed 256×4 PROM which drives a 3-to-8 decoder. An interlock signal (PE) ensures the PROM is enabled only when a cartridge is installed. Three address straps within the cartridge (S1, S2, and S3) identify the cartridge type installed by selecting the appropriate address decoding section in the PROM. The five most significant buffered address lines address one of the 32 bytes within the selected section. A valid address for the installed cartridge results in a low level signal on the most significant PROM output pin. This signal in turn enables both the 3-to-8 decoder and the data transceiver. The remaining three PROM outputs (O1, O2, and O3) provide the selection input to the

decoder and drive the appropriate decoder output to the low state. The eight decoder outputs form the eight active low chip select signals for the cartridge.

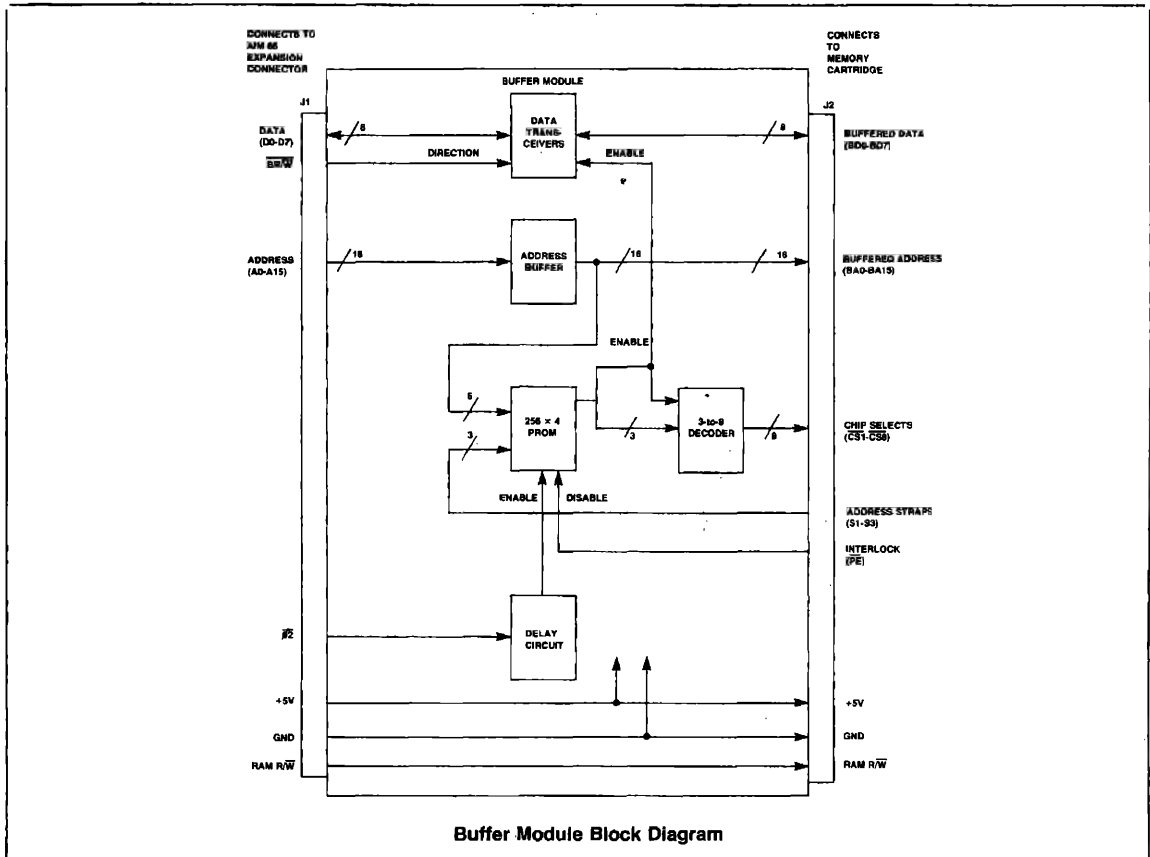
PROM timing is controlled by a delay circuit implemented with a mono-stable multivibrator. This circuit delays the turn-on of the address decode PROM to prevent bus contentions at the beginning of each cycle.

Power for the Buffer Module is derived from the AIM 65 power supply through the Expansion Connector. Power for the cartridge is routed through the Buffer Module.

MEMORY CARTRIDGE

The Memory Cartridge has eight 24-pin sockets which can accept 2K RAMs, 4K PROMs or 4K ROMs. In models -01, -02, -03, -05, and -08, sockets are available for user supplied PROMs. In model -07, sockets are provided for user supplied RAMs.

Variations in socket functions are accomplished by routing selected signals through factory installed jumpers. The eight sockets are arranged into three groups as illustrated in the block diagram. All sockets in each group are configured to accept the same memory device type.



INSTALLATION

BUFFER MODULE

1. Before installing the Buffer Module, turn off power to the AIM 65 Microcomputer.
2. Align the Buffer Module Connector J1 pin 1 with the AIM 65 Expansion Connector J3 pin 1.
3. Carefully slide the Buffer Module under the AIM 65 Master Module, plugging the Buffer Module onto the Expansion Connector. Press in firmly on the end of the module assembly until all pins are securely seated.
4. If your AIM 65 Microcomputer is installed in an AIM 65 Enclosure, fasten the Buffer Module Assembly bottom plate to the base plate of the enclosure using the screws provided with the Buffer Module.

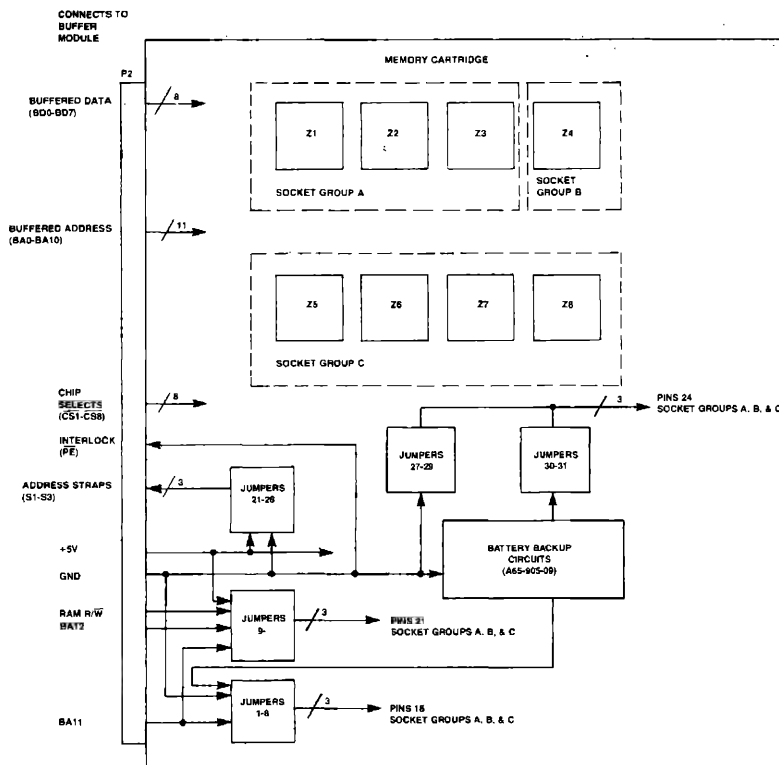
2. There is no on/off switch for the battery. Remove the battery to prevent draining the battery when the cartridge is not powered.
3. The battery will last six months in battery back-up mode. Therefore, replace the battery after six months of use. The replacement battery should be either a GE or Sanyo CR2032.
4. A potentiometer in the cartridge sets the voltage threshold level at which the cartridge switches from V_{CC} mode to battery back-up mode. The factory set levels are approximately +4.5 Vdc for battery back-up and +4.7 Vdc for V_{CC} power. Adjust this potentiometer while monitoring the voltage on pin 4 of Z9 to raise or lower these levels. When pin 4 goes high (about +5 Vdc), the cartridge is in battery back-up.

MEMORY CARTRIDGE

1. Before installing or removing a Memory Cartridge, turn off power to the AIM 65 Microcomputer.
2. To install the cartridge, align the cartridge with the label side towards the microcomputer and plug the cartridge into the Buffer Module receptacle (the cartridge is keyed to prevent improper insertion). Press down firmly on the top of the cartridge until all pins are securely seated.

MEMORY CARTRIDGE BATTERY INSTALLATION (A65-905-09 only)

1. The battery is NOT factory installed. Install the battery by sliding it into the holder plus side (+) up.



Memory Cartridge Block Diagram

Memory Cartridge Memory Map

Block Starting Address	Cartridge Model (A65-905-XX)								
	-01	-02	-03	-04	-05	-06	-07	-08	-09
0000 (1)	AIM 65 Master Module RAM								
1000	8K RAM	8K RAM	8K RAM	6K RAM	32K PROM	16K RAM	16K RAM	8K RAM	16K Battery Backed RAM
2000									
3000									
4000	4K PROM	4K PROM	4K PROM	PASCAL				16K PROM	
5000									
6000									
7000									
8000									
9000									
A000	AIM 65 Master Module I/O								
B000	BASIC	PL65	FORTH	PASCAL					
C000									
D000									
E000	AIM 65 Monitor	AIM 65 Monitor	AIM 65 Monitor	AIM 65 Monitor	AIM 65 Monitor	AIM 65 Monitor	AIM 65 Monitor	AIM 65 Monitor	
F000									

Notes:

(1) Master Module only.

(2) These blocks are addressed on the AIM 65 Master Module in addition to the cartridges. Components must be removed from AIM 65 Master Module sockets Z24, Z25, and Z26 prior to installing the memory cartridge model -01, -02, or -03. Component must be removed from AIM 65 Master Module socket Z26 prior to installing cartridge module -04.

Memory Cartridge Component Summary

Socket	Cartridge Model No. (A65-905-XX)								
	-01	-02	-03	-04	-05	-06	-07	-08	-09
Function	BASIC	PL/65	FORTH	PASCAL	PROM/ROM	RAM	User RAM	RAM and PROM/ROM	Battery Backed RAM
Z1	RAM	RAM	RAM	RAM	PROM	RAM	RAM	RAM	RAM
Z2	RAM	RAM	RAM	RAM	PROM	RAM	RAM	RAM	RAM
Z3	RAM	RAM	RAM	RAM	PROM	RAM	RAM	RAM	RAM
Z4	RAM	RAM	RAM	R32P2-11 ROM	PROM	RAM	RAM	RAM	RAM
Z5	(1) PROM	(1) PROM	(1) PROM	R32P3-11 ROM	PROM	RAM	RAM	PROM	RAM
Z6	R3226-11 ROM	R3299-11 ROM	R32J1-11 ROM	R32P4-11 ROM	PROM	RAM	RAM	PROM	RAM
Z7	R3225-11 ROM	R3298-21 ROM	R32J2-11 ROM	R32P5-11 ROM	PROM	RAM	RAM	PROM	RAM
Z8	R3224-11 ROM	R3224-11 ROM	R32L3-11 ROM	R32P6-11 ROM	PROM	RAM	RAM	PROM	RAM

Notes:

1. All PROM is user provided TI2532 or equivalent.

2. All RAM is Toshiba TC5516AP, Toshiba TC5516APL or Suwa Seikosha SRM2018C.

Buffer Module to AIM 65 Expansion Connector Pin Assignments

Top (Component Side)				Bottom (Solder Side)			
Pin	Signal Mnemonic	Signal Name	Input/ Output**	Pin	Signal Mnemonic	Signal Name	Input/ Output**
1	SYNC	*SYNC		A	A0	Address Bit 0	I
2	RDY	*Ready		B	A1	Address Bit 1	I
3	$\phi 1$	*Phase 1 Clock		C	A2	Address Bit 2	I
4	IRQ	*Interrupt Request		D	A3	Address Bit 3	I
5	S.O.	*Set Overflow		E	A4	Address Bit 4	I
6	NMI	*Non-Maskable Interrupt		F	A5	Address Bit 5	I
7	RES	*Reset		H	A6	Address Bit 6	I
8	D7	Data Bit 7	I/O	J	A7	Address Bit 7	I
9	D6	Data Bit 6	I/O	K	A8	Address Bit 8	I
10	D5	Data Bit 5	I/O	L	A9	Address Bit 9	I
11	D4	Data Bit 4	I/O	M	A10	Address Bit 10	I
12	D3	Data Bit 3	I/O	N	A11	Address Bit 11	I
13	D2	Data Bit 2	I/O	P	A12	Address Bit 12	I
14	D1	Data Bit 1	I/O	R	A13	Address Bit 13	I
15	D0	Data Bit 0	I/O	S	A14	Address Bit 14	I
16	-12V	*-12 Vdc		T	A15	Address Bit 15	I
17	+12V	*+12 Vdc		U	SYS $\phi 2$	System Phase 2 Clock	
18	CS8	*Chip Select 8		V	SYS R/W	*System Read/Write	
19	CS9	*Chip Select 9		W	R/W	Read/Write "Not"	I
20	CSA	*Chip Select A		X	TEST	*Test	
21	+5V	+5 Vdc		Y	$\phi 2$	Phase 2 Clock "Not"	I
22	GND	Ground		Z	RAM R/W	RAM Read/Write	I

Note:
 * = Not used on this module.
 ** = With respect to the Buffer Module.

Memory Cartridge to Buffer Module Connector Pin Assignments

Front (Label Side)				Rear			
Pin	Signal Mnemonic	Signal Name	Input/ Output**	Pin	Signal Mnemonic	Signal Name	Input/ Output**
2	BA3	Address Bit 3	I	1	BA2	Address Bit 2	I
4	BA1	Address Bit 1	I	3	BA0	Address Bit 0	I
6	BA7	Address Bit 7	I	5	BA6	Address Bit 6	I
8	BA4	Address Bit 4	I	7	BA5	Address Bit 5	I
10	BA15	Address Bit 15	I	9		Not Used	
12	BA14	Address Bit 14	I	11	PE	PROM Enable	O
14	BA12	Address Bit 12	I	13	BA13	Address Bit 13	I
16	BA9	Address Bit 9	I	15	BA8	Address Bit 8	I
18	BA11	Address Bit 11	I	17	BA10	Address Bit 10	I
20	BD1	Data Bit 1	I/O	19	BD0	Data Bit 0	I/O
22	BD3	Data Bit 3	I/O	21	BD2	Data Bit 2	I/O
24	BD5	Data Bit 5	I/O	23	BD4	Data Bit 4	I/O
26	BD7	Data Bit 7	I/O	25	BD6	Data Bit 6	I/O
28	CS2	Chip Select 2	I	27	CS1	Chip Select 1	I
30	CS4	Chip Select 4	I	29	CS3	Chip Select 3	I
32	CS6	Chip Select 6	I	31	CS5	Chip Select 5	I
34	CS8	Chip Select 8	I	33	CS7	Chip Select 7	I
36	RAM R/W	RAM Read/Write	I	35	S3	Address Strap 3	O
38	S2	Address Strap 2	O	37	S1	Address Strap 1	O
40		Not Used		39		Not Used	
42	+5V	+5 Vdc		41	+5V	+5 Vdc	
44	GND	Ground		43	GND	Ground	

Note:
 **With respect to Memory Cartridge.

SPECIFICATIONS

Parameter	Value	
	Memory Cartridge	Buffer Module
Dimensions		
Width	5.25 in. (133 mm)	4.75 in. (121 mm)
Length	4.85 in. (123 mm)	4.69 in. (119 mm)
Height	0.88 in. (22 mm)	1.48 in. (38 mm)
Power	$+5V \pm 5\%$ -01, -02, -03 550 ma—Typical -04 550 ma—Typical -05 870 ma—Typical -06, -07, -09 380 ma—Typical -08 620 ma—Typical	$+5V \pm 5\%$ 250 ma—Typical
Environment		
Operating Temperature	0°C to 50°C	0°C to 70°C
Storage Temperature	–40°C to 85°C (except A65-905-09) –20°C to 50°C (A65-905-09)*	–40°C to 85°C
Relative Humidity	0% to 85% (without condensation)	0% to 85% (without condensation)
Interface Connections		
AIM 65 Expansion Connector		44 pin-edge receptacle (0.156 in. centers)
Buffer Module to Cartridge	44 pin-edge connector (0.100 in. centers)	44 pin-edge receptacle (0.100 in. centers)
Note: * –40°C to 85°C if the battery is not present.		

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SECTION 8

AIM 65/40 MICROCOMPUTER FAMILY

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AIM 65/40 MICROCOMPUTER FAMILY

Modular Microcomputer Family With Wide OEM, Control Capabilities

The AIM 65/40 modular microcomputer system allows functional steps up from the AIM 65 microcomputer in hard working blue collar applications, at very competitive prices. It also offers an extremely wide range of languages, controller options and an operating system for even greater application flexibility.

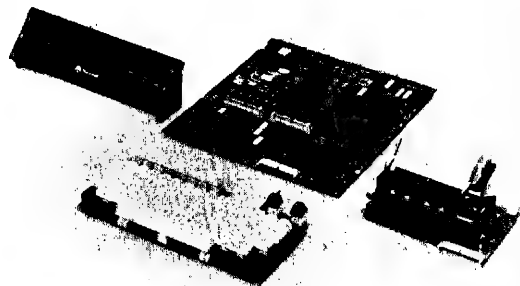
The four basic modules of an AIM 65/40 include an R6502 based single board computer, an intelligent printer with 40 column alphanumerics and graphics capabilities, a 40-character intelligent alphanumeric VF display, and a full ASCII keyboard. It may be purchased as a complete set for end users or as separate modules for OEM users. The printer and display modules may be mounted remotely from the single board computer.

Language ROMs include BASIC interpreter and compiler, FORTH firmware and compiler. An assembler ROM, debug monitor and text editor ROMs, math package ROM add to the versatility. There are even disk operating systems.

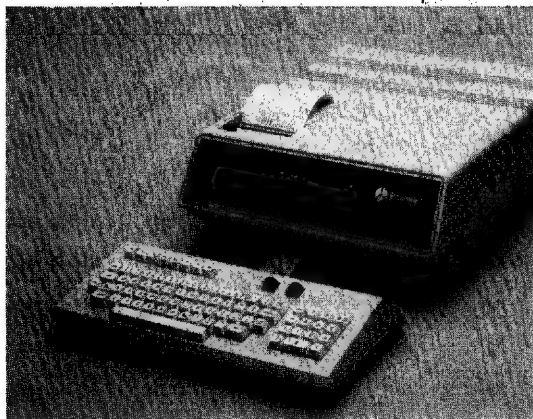
A video controller module can be pre-configured onto the AIM 65/40 or can be used stand alone with other microprocessor based systems. It gives the AIM 65/40 the ability to command screen formatting, text handling and screen editing, plus full graphics drawing and data display functions. When pre-configured, the AIM 65/40 comes with an extended keyboard that includes cursor movement controls and a numeric keypad.

For desk top use, the AIM 65/40 comes in an attractive enclosure, including power supply and an expansion card cage which can accept any RM 65 Eurocard module. With its built-in features and expansion capabilities, the desk top AIM 65/40 can be any type of microcomputer system you might need.

In the blue collar family, the AIM 65/40 microcomputer provides more power, greater flexibility, for more applications.



AIM 65/40 MICROCOMPUTER
BOARD-LEVEL VERSION



AIM 65/40 MICROCOMPUTER
PACKAGED VERSION

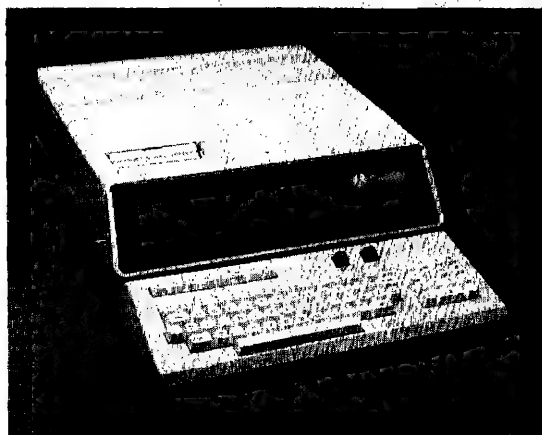


A65/40-8X15 AIM 65/40 SERIES 8000 MICROCOMPUTER SYSTEM

OVERVIEW

The AIM 65/40 Series 8000 Microcomputer System is a powerful, 8-bit R6502 CPU based microcomputer with a complete complement of RAM, ROM and I/O capacity—packaged in an attractive professional desk-top enclosure and ready for use in a wide range of OEM and end-user applications. Four models offer either a built-in 40-character single line display or an 80-character × 25 line video display controller with each display model available with an internal graphics printer or a Centronics type printer interface.

ROM-based disk operating system, input/output functions, debug monitor, text editor, R6500 assembler, and BASIC interpreter provide both standalone software development capability and run-time environment. Application programs developed and/or executed on a Series 8000 microcomputer can meet requirements for low cost, high performance applications such as data acquisition and logging, instrumentation, medical analysis, environmental monitor, scientific calculation, and automatic test equipment in office, laboratory, or light industrial environments.



A65/40-8515 Microcomputer System

FEATURES

- Integrated, complete and expandable microcomputer system
 - AIM 65/40 single board microcomputer with all its features and populated with 48K bytes RAM and 24K bytes ROM
 - AIM 65/40 extended keyboard with 57-key main keyboard, 15-key numeric and cursor control keyboard, 8 function keys and separate RESET and ATTN keys
 - RM 65 card cage with two available slots for user expansion
 - RM 65 floppy disk controller for interfacing with up to four 5¼" double-density floppy disk drives
 - Internal power supply with user expansion capacity
- Four models to choose from
 - Optional single line display or video display controller (VDC)
 - Optional graphics printer or Centronics printer interface
- Fully contained in attractive, professional enclosure
 - Attractive, stylized two-piece design
 - Strong, injection molded ABS plastic construction
 - Complementary two-tone color (sand with brown trim)
 - Swing-open top for easy access to internal components
 - Separate floating keyboard assembly
- Hardware and software expansion options
 - RM 65 input/output, controller and memory modules
 - Disk- and ROM-based language assemblers, compilers and/or interpreters
- ROM-resident firmware for immediate operation
 - Bootstrap disk operating system (BDOS 1.0)
 - User accessible I/O subroutines
 - Debug monitor/text editor
 - R6500 assembler
 - 8K BASIC interpreter

ORDERING INFORMATION

Part No.	Description
A65/40-8215	AIM 65/40 with VDC, Extended Keyboard, 48K RAM, BASIC Interpreter, Assembler, BDOS 1.0, FDC & 2 Expansion Slots
A65/40-8315	Same as A65/40-8215 with Graphics Printer
A65/40-8415	AIM 65/40 with 40-Character Display, Extended Keyboard, 48K RAM, BASIC Interpreter, Assembler, BDOS 1.0, FDC & 2 Expansion Slots
A65/40-8515	Same as A65/40-8415 with Graphics Printer

HARDWARE DESCRIPTION

The AIM 65/40 Series 8000 Microcomputer System is fully packaged in a two-unit injection-molded ABS plastic enclosure. The Main Unit houses the Single Board Computer (SBC) module, power supply, RM 65 4-Slot Card Cage and adapter, Single Line Display or Video Display Controller (VDC) module, Graphics Printer or Centronics Printer Interface adapter, and interconnect cabling. The hinged front panel swings forward revealing internal components thus allowing convenient switch setting and PROM/ROM installation for custom applications. The rear section is easily removed to access the RM 65 Card Cage for installation of RM 65 expansion modules. Cables from external peripherals and equipment connect directly to connectors mounted on the back panel.

The detached Keyboard Unit houses the AIM 65/40 Extended Keyboard and is connected to the Main Unit by a retractable cable for flexible positioning on the work surface.

SBC Module

The SBC module contains an R6502 CPU, a 1 MHz clock circuit, on-board device decoders, Interrupt request priority circuit, reset conditioning, 32K bytes PROM/ROM sockets and 48K bytes RAM. 24K bytes of ROM are installed with two 4K-byte sockets available for user PROM/ROM installation. All on-board memory may be enabled in 4K-byte blocks, yielding an optimal mix of on-board/off-board memory and I/O to be addressed. The RAM may also be write-protected in 8K-byte segments. Dual bank addressing allows an additional 56K bytes of memory or I/O to be accessed off-board.

Video Display Controller (Models -8215 and -8315)

The Video Display Controller (VDC) interfaces the SBC module to a CRT monitor by generating a composite video output signal which is routed to a BNC connector on the back panel. Controlled by a separate microprocessor, built-in commands in

either text or graphics mode provide flexible text handling and screen editing as well as full graphics line drawing and display functions.

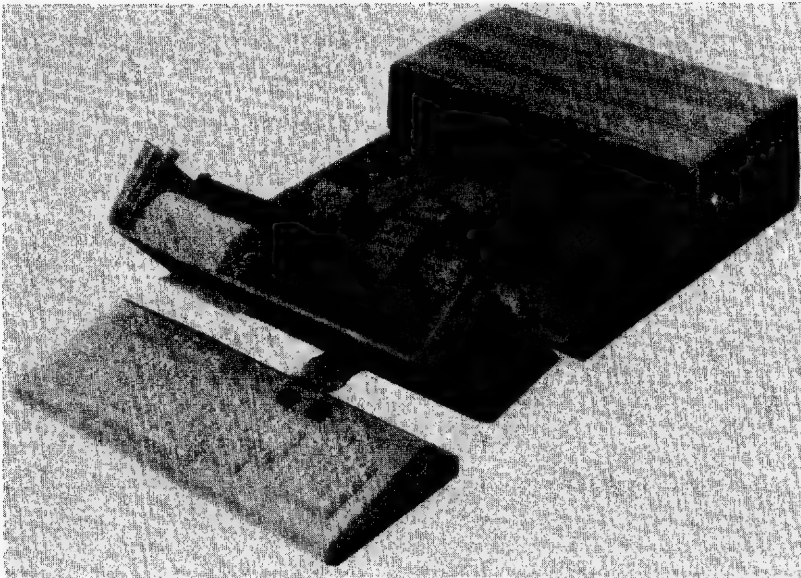
In the text mode, a screen format of 80 characters × 24 lines is automatically selected. A 40 × 24 format is also available and other formats are user programmable. Eight pages of text are available in the 80 × 24 format with automatic page sizing for other formats. A 4K-byte character generator ROM contains bit patterns for 256 different characters in a 7 × 10 dot matrix field. Standard characters include upper- and lower-case alphabets, numerals (including subscripts and superscripts), math and Greek symbols, common European letters, and semigraphic characters.

The full graphics mode incorporates bit mapping of 280 × 224 pixels, which is compatible with the Graphics Printer. Line drawing commands move a pen and draw or erase lines using either relative or absolute position reference. Data byte capability allows individual dots to be controlled using a 40 bytes per dot line format (seven dots per byte).

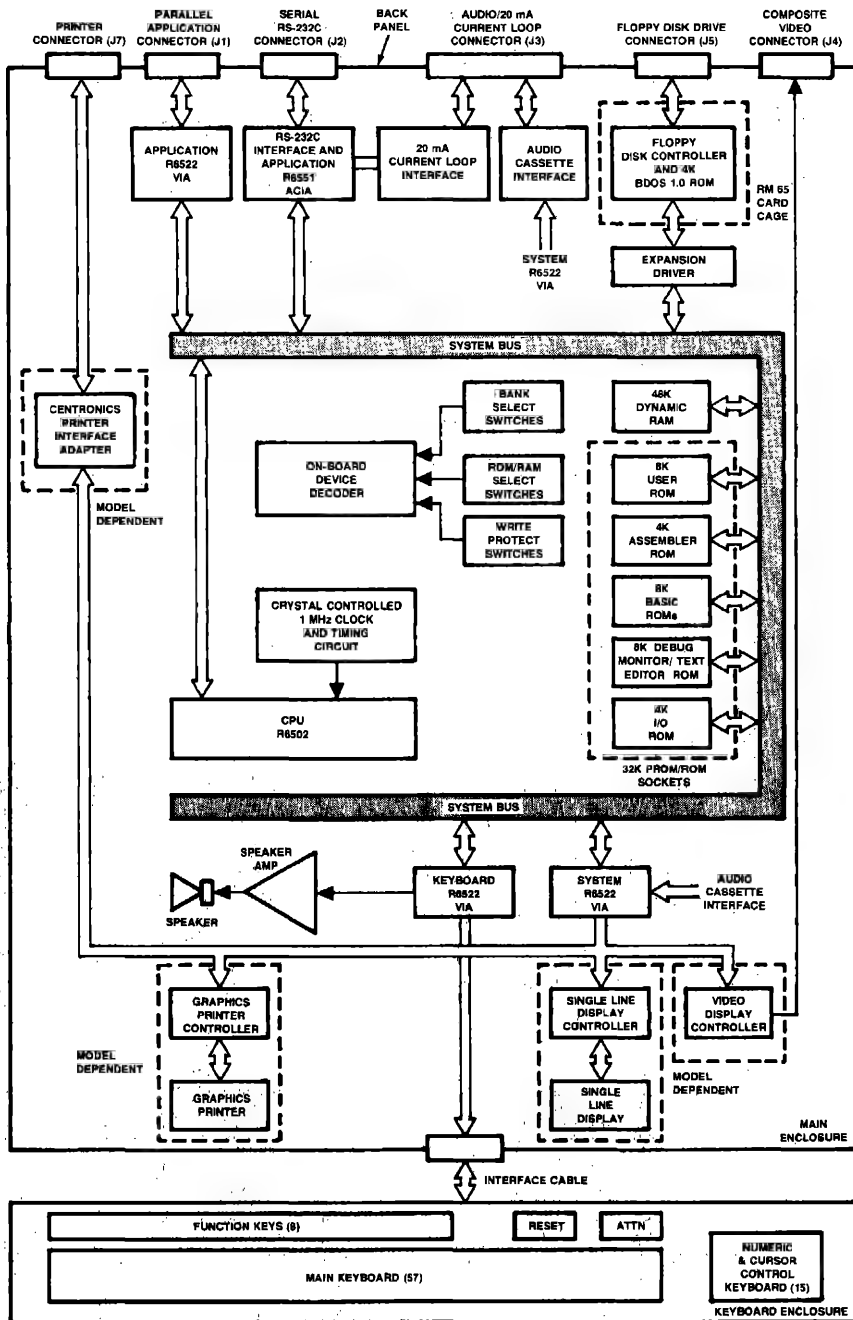
Graphics Printer (Models -8315 and -8515)

The Graphics Printer is a dot matrix thermal printer with two modes operation: text and graphics. In the text mode, up to 40 characters per line can be printed using 7 × 8 dot matrix characters. 256 pre-defined upper and lower case letters, numbers including superscripts and subscripts, math symbols, and common European and Greek letters are included in the controller ROM. Text is printed at a fast 240 lines per minute. In the graphics mode, all 280 horizontal dots in a row are individually controlled, and any number of rows may be printed.

The printer includes a dedicated microprocessor-based controller which operates the printer motor and thermal head timing and control functions independently from the SBC module thus relieving the SBC module from time consuming peripheral control functions.



A65/40-8515 Microcomputer System—Front Cover Open



AIM 65/40 Series 8000 Microcomputer System Block Diagram

Parallel Application Connector (J1) Pin Assignments

Pin	Signal	I/O	Type	Pin	Signal	Type
1	CB2	I/O	NMOS	2	NC/+5V*	Power
3	CB1	I/O	NMOS	4	GND	Power
5	PB7	I/O	NMOS	6	GND	Power
7	PB6	I/O	NMOS	8	GND	Power
9	PB5	I/O	NMOS	10	GND	Power
11	PB4	I/O	NMOS	12	GND	Power
13	PB3	I/O	NMOS	14	GND	Power
15	PB2	I/O	NMOS	16	GND	Power
17	PB1	I/O	NMOS	18	GND	Power
19	PB0	I/O	NMOS	20	GND	Power
21	PA7	I/O	NMOS	22	GND	Power
23	PA6	I/O	NMOS	24	GND	Power
25	PA5	I/O	NMOS	26	GND	Power
27	PA4	I/O	NMOS	28	GND	Power
29	PA3	I/O	NMOS	30	GND	Power
31	PA2	I/O	NMOS	32	GND	Power
33	PA1	I/O	NMOS	34	GND	Power
35	PA0	I/O	NMOS	36	GND	Power
37	CA2	I/O	NMOS	38	GND	Power
39	CA1	I	NMOS	40	NC/+5V*	Power

Note: *Pins 2 and 40 can be optionally jumpered to +5V (maximum current through each pin should not exceed 200 mA).

Serial RS-232C Application Connector (J2) Pin Assignments

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
1	GND		Power	2	TD	O	RS-232C
3	RD	I	RS-232C	4	RTS	I/O	RS-232C
5	CTS	I/O	RS-232C	6	DSR	I/O	RS-232C
7	GND		Power	8	DCD	I/O	RS-232C
9	NC			10	NC		RS-232C
11	NC			12	NC		
13	NC			14	NC		
15	NC			16	NC		
17	NC			18	NC		
19	NC			20	DTR	I/O	
21	NC			22	NC		RS-232C
23	NC			24	NC		
25	NC			26	NC		

Audio/20 mA Current Loop Connector (J3) Pin Assignments

Pin	Signal	I/O	Type	Pin	Signal	Type
1	TTY RTS	I	TTY	2	GND	Power
3	TTY TD	O	TTY	4	GND	Power
5	TTY RD	I	TTY	6	GND	Power
7	TTY RTN		Power	8	GND	Power
9	AUDIO OUT	I	TTL	10	GND	Power
11	AUDIO IN	O	TTL	12	GND	Power
13	CTRL 2 RTN	O	Relay	14	GND	Power
15	CTRL 2	I	Relay	16	GND	Power
17	CTRL 1 RTN	O	Relay	18	GND	Power
19	CTRL 1	I	Relay	20	GND	Power

Floppy Disk Drive Connector (J5) Pin Assignments⁽¹⁾

Pin	Signal	I/O	Pin	Signal	I/O
2	NC ⁽²⁾		20	STEP PULSE	O
4	NC		22	WRITE DATA	O
6	DRIVE SELECT #4	O	24	WRITE GATE	O
8	INDEX	I	26	TRACK ZERO	O
10	DRIVE SELECT #1	O	28	WRITE PROTECTED	I
12	DRIVE SELECT #2	O	30	READ DATA	O
14	DRIVE SELECT #3	O	32	2ND SIDE SELECT	O
16	MOTOR ON	O	34	NC	
18	DIRECTION IN	O			

Notes: 1. 5¼" floppy disk drive interface.
2. NC = No connection.

Printer Connector (J7) Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	STROBE	O	6	DATA 5	O
2	DATA 1	O	7	DATA 6	O
3	DATA 2	O	8	DATA 7	O
4	DATA 3	O	10	ACK	I
5	DATA 4	O	9, 11-18	NC	
			19-2	GND	

**Centronics Printer Interface
(Models -8215 and -8415)**

The Centronics Printer Interface connector adapter buffers the external printer output signals from the SBC module and routes the signals to the Printer connector on the back panel.

40-Character Display (Models -8415 and -8515)

The 40-Character Display includes a vacuum fluorescent display and a dedicated microprocessor-based controller. The vacuum fluorescent display is a single sealed unit containing 40 separately controllable digits. Each digit is composed of a 16-segment font which illuminates a full set of upper case alphabets, numerics, and special characters. In the semi-graphics mode, the 16 segments for each digit are individually controlled. In addition, each digit includes a separate decimal point. When energized, the digits form bright, crisp characters in a blue-green color.

Extended Keyboard

The Extended Keyboard contains a 57-key full-size terminal style alphanumeric keyboard with locking SHIFT key, a 15-key numeric and cursor control keyboard, eight function keys, and separate RESET and ATTN keys.

SOFTWARE DESCRIPTION

Standard ROM-based software in the Series 8000 Microcomputer System provides either immediate development capability in BASIC and R6500 assembly language or automatic application program startup in a run-time environment. Program initiation can be performed either in a PROM/ROM-based application program or in RAM after an automatically initiated load of the application program from floppy disk. The ROMs installed in each Series 8000 systems are:

- AIM 65/40 I/O ROM
- AIM 65/40 Bootstrap Disk Operating System Version 1.0 (BDOS 1.0)
- AIM 65/40 Debug Monitor/Text Editor
- AIM 65/40 BASIC Interpreter
- AIM 65/40 Assembler

I/O ROM

The I/O ROM includes preprogrammed auto-start initialization, interrupt, input/output and utility functions which support user-defined programs as well as Series 8000 standard firmware and optional firmware/software. Auto-start initialization jumps to pre-determined PROM/ROM addresses during RESET processing. The application program can assume direct control of the system for continued operation, or it can just initialize required functions, then return control back to the I/O ROM for continued auto-start of other functions. I/O drivers directly support intelligent display and printer peripherals. Other drivers support the RS-232C/20MA interfaces and the audio cassette ports, and control the on-board speakers.

BDOS 1.0

The BDOS 1.0 ROM provides disk and file management functions as well as automatic loading of a bootstrap loader from

disk for load and go program execution. BDOS functions open, close, read and write program and data files under operator or program control. User-friendly prompts, displayed at the Debug Monitor, Text Editor, BASIC, and Assembler command level messages, simplify operator initiation and monitoring of disk and file operations. Disk-oriented functions include format a disk and list the directory for all files on the disk. File-oriented functions include list, delete and recover a named file.

When the BASIC ROMs are installed, the microcomputer automatically initializes to the BASIC command level unless overridden by an application program auto-start sequence. Easy entry to the Debug Monitor and Text Editor command levels allow machine level debugging, assembler selection and text entry/editing.

Debug Monitor/Text Editor ROMs

The Debug Monitor/Text Editor includes a wide selection of functions to simplify computer program entry and checkout. Text can be easily entered, edited, saved and retrieved using either line- or screen-oriented commands in the Text Editor. A character cursor can be positioned left, right, up, or down to aid character insertion, addition, and deletion. Automatic and selective character string change capability makes block changes as desired. Multiple text buffers can easily be maintained for separate program and data files.

The Debug Monitor controls program execution in single step and run modes and allows convenient examination and altering of memory and registers. Single step mode disassembles instructions and traces register contents upon command for detail examination of program operation. Symbol level debugging reduces dependence on absolute addresses and simplifies program checkout. Command string capability allows command sequences to be chained and easily repeated.

BASIC ROMs

The 8K Microsoft-developed BASIC Interpreter implements an industry standard high level language which is simple but powerful and is commonly used in industry, science and schools.

BASIC operates in one of two modes, development and run-time. In the development mode, BASIC statements are entered and executed as either direct or indirect commands. Direct commands are executed upon entry to provide immediate results, however, the statements are not stored for subsequent execution. Indirect commands are entered along with an associated line number and are executed upon RUN command entry or application program auto-start initialization. Indirect statements can also be loaded into the Text Editor for entry into BASIC to simplify program editing. The microcomputer peripherals, i.e., keyboard, 40-character single line display/video display and printer, are used in the development mode to enter statements, to list entered indirect statements and to display/print execution results.

Assembler ROM

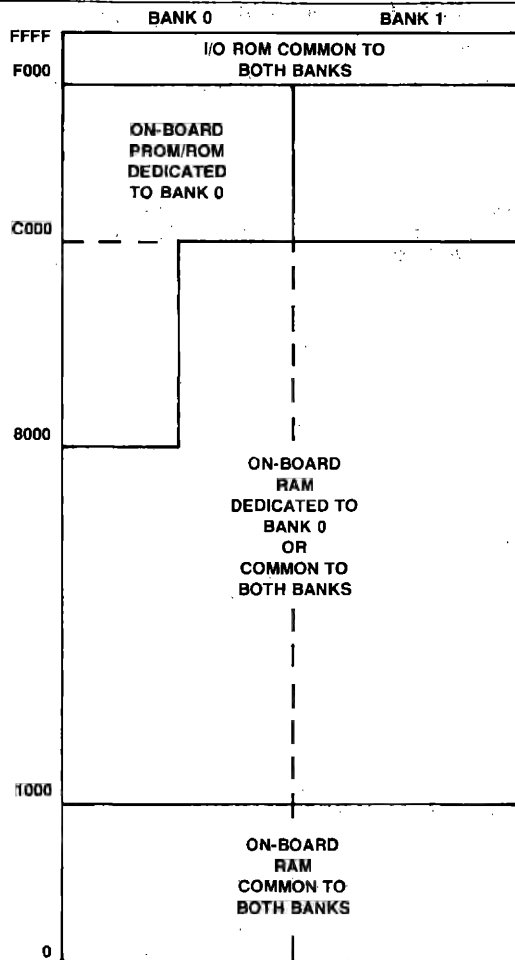
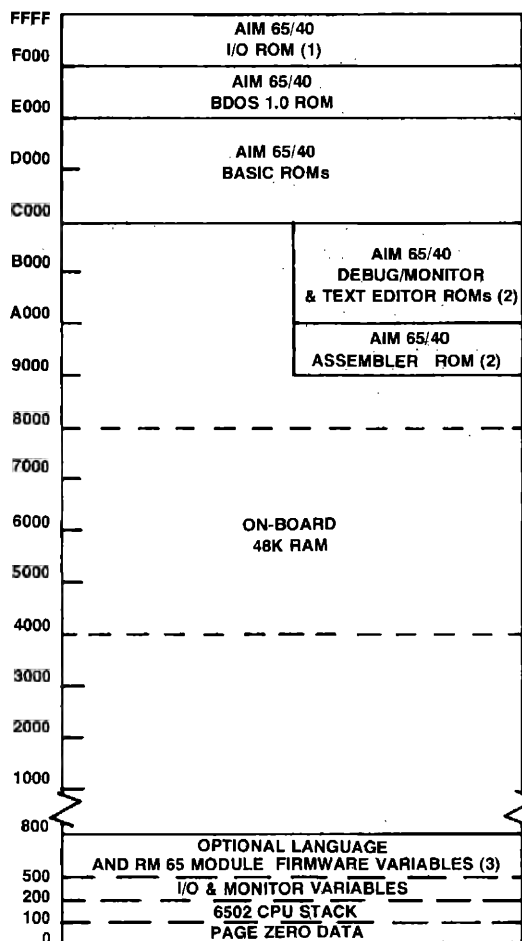
The assembler translates computer program instructions written in R6500 assembly language for the 6502 microprocessor into machine code that will operate either in the Series 8000 Microcomputer System or in any 65XX CPU-based microcomputer. Operating options are selected interactively by the operator

upon assembly command. These options specify source code device, object code device, symbol table location, full assembly or errors only output listing and output listing device. A repeat command invokes the assembly according to previously commanded options for rapid setup during program debugging, editing and reassembly. Memory to memory assembly is supported to speed program generation.

SOFTWARE OPTIONS

Part No.	Description
Disk-Based ⁽¹⁾	
A65/40-7012	AIM 65/40 Macro Assembler and Linking Loader
A65/40-7024	AIM 65/40 BASIC Compiler
A65/40-7052	AIM 65/40 FORTH Compiler
ROM-Based	
A65/40-7040	AIM 65/40 Math Package ROM
A65/40-7050	AIM 65/40 FORTH ROMs
Note: Provided a 5¼-inch double-density floppy disk compatible with AIM 65/40 BDOS 1.0.	

MEMORY MAP



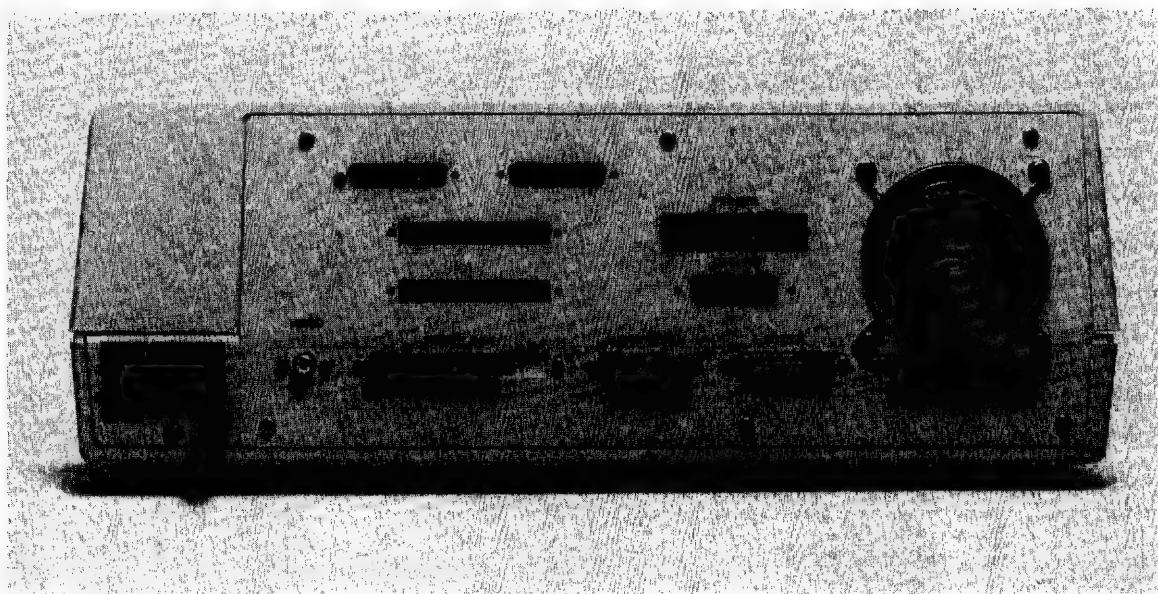
Notes: (1) AIM 65/40 System peripheral I/O addresses are assigned to FF80-FFDF.

(2) User available during application program operation.

(3) User available if the optional language and the RM 65 expansion module ROMs are not used.

SPECIFICATIONS

Parameter	Value	Parameter	Value
Dimensions		Electrical (cont.)	
Main Enclosure		J3 (Audio/20 mA Current Loop)	20-pin mass terminated connector (3M#3421-7020 or equivalent)
Width	17.00 in. (43.2 cm)	J4 (Composite Video)	RCA BNC type (Allied#60BB or equivalent)
Length	7.75 in. (19.7 cm)	J5 (Floppy Disk Drive)	34-pin mass terminated connector (3M#3414-8034 or equivalent)
Height	2.26 in. (5.8 cm)	J7 (Printer)	36-pin mass terminated connector (3M#3386-1001 or equivalent)
Keyboard Enclosure		AC Power Connection	
Width	17.00 in. (43.2 cm)	Power Connector	3-Prong Recessed Grounding Plug (NEMA 5-15P)
Length	17.68 in. (44.9 cm)	Power Cord	
Height	6.00 in. (15.2 cm)	Type	Detachable, 3-Conductor
Environment		Length	6 Feet
Operating Temperature		Rating	125 Vac, 15A Service
With Printer	0°C to 50°C	Line End	Molded Vinyl Grounding Plug (NEMA 5-15P)
Without Printer	0°C to 70°C	Microcomputer End	Molded Vinyl Grounding Receptacle
Storage Temperature		AC Power Requirement	
With Printer	0°C to 70°C	Input Voltage	115 Vac \pm 10%, 47-63 Hz
Without Printer	-25°C to 85°C	Fuse	230 Vac, 3A, Slo-Blo
Relative Humidity	0% to 85% (without condensation)		
Electrical			
Interface Connectors (Back Panel)			
J1 (Parallel Application)	40-pin mass terminated connector (3M#3417-7040 or equivalent)		
J2 (Serial RS-232C Application)	25-pin Delta connector (3M#3482-1000 or equivalent)		



A65/40-8515 Microcomputer System—Back Panel



A65/40-2000, -3000, -4000 and -5000 AIM 65/40 MICROCOMPUTER

OVERVIEW

The AIM 65/40 microcomputer integrates the AIM 65/40 modular components—Single Board Computer (SBC), 40-Character Display or Video Display Controller (VDC) module, Graphics Printer, and a Standard or Extended Keyboard—into a complete self-contained system including an application-oriented I/O ROM and a ROM resident operator-oriented Debug Monitor/Text Editor. The display and printer modules are mounted onto the SBC while the keyboard is detached—all peripherals are connected through removable 40-conductor ribbon cables. The peripherals can easily be relocated to other positions to satisfy unique installation requirements.

In its integrated form, a desk-top installation of the AIM 65/40 microcomputer system can perform a wide range of specialized data acquisition, data reduction, control, and monitor functions in either OEM or end-user configurations. As a development tool, the system can support software developed in either assembly or high level language for operation in AIM 65/40 or RM 65 based microcomputers at a fraction of the cost of other systems.

As an advanced generation of the popular AIM 65 microcomputer, the separate AIM 65/40 assemblies provide increased processing throughput, improved keyboard, display and printer modules, and expanded application interfaces. The 6502 CPU-based AIM 65 Single Board Computer, with a full address complement of memory capacity on-board, extremely flexible I/O, and interrupt driven I/O handlers in firmware, is the heart of the AIM 65/40 microcomputer system. The AIM 65 Graphics Printer, with its separate microcomputer controller, prints 40 columns of characters using a complete set of upper and lower case alphabetic, numeric, semi-graphic, and special characters in the text mode at 240 lines per minute, and also provides a full graphics mode of 280 dots by 16 rows. The AIM 65/40-Character Display, with its own microprocessor-based controller, features an easy-to-read fluorescent display, and provides a full complement of alphanumeric and special characters as well as internal editing, scrolling, and blinking functions. The terminal-style AIM 65 Standard Keyboard contains a full-size main keyboard plus a separate row of eight dedicated function keys and isolated RESET and ATTN keys.

The system comes with a 4K-byte I/O ROM and an 8K-byte interactive debug monitor and text editor. Optional assembler and common high level language compilers/interpreters improve programmer productivity, increase program reliability, and simplify program maintenance. ROM-based firmware includes a disk operating system, symbolic assembler, universally accepted BASIC interpreter, and a highly efficient FORTH system with resident compiler, interpreter, and macro assembler. Optional disk-based software includes a macro assembler, BASIC compiler and FORTH target compiler.

FEATURES

- Single Board Computer with extensive memory and I/O
 - 6502 CPU
 - 131K addressing, in Two 65K-byte banks
 - Up to 48K-bytes of on-board RAM, with write-protect
 - Up to 32K-bytes of on-board PROM or ROM
 - User-Prioritized Interrupts, up to six levels
 - User-Dedicated parallel I/O interface
 - User-Dedicated RS-232C serial interface
 - Audio cassette/TTY (20 mA current) interface
 - RM 65 bus expansion interface
- Graphics Printer
 - Text mode provides upper/lower case alphanumerics, Math, and Special Characters at 240 lines/minute
 - Full graphics mode provides 280-dot resolution
 - Quiet, reliable thermal operation
- 40-Character Display
 - Full upper case alphanumeric and special characters
 - Bright, crisp vacuum fluorescent display
 - Display, edit, auto-scroll, and character blinking functions
- Full-Size Terminal-Style Standard Keyboard
 - 57 keys, including locking ALL CAPS key
 - Eight user function keys, plus ATTN and RESET
- I/O ROM
 - Auto-start initialization
 - Interrupt-driven peripheral I/O handling
 - RAM vectored I/O with expansion hooks
 - General purpose I/O and utility subroutines
- ROM-Resident Interactive Debug Monitor
 - Accepts instructions in mnemonic form
 - Machine level debug functions
 - Command file for automatic command execution
- ROM-Resident Text Editor
 - Line and screen oriented commands
 - Read, list, insert, delete functions
 - Cursor control functions
 - Automatic and manual block change functions
- Extensive Documentation
 - Comprehensive user's manual
 - I/O ROM and Monitor/Editor assembly listings
 - Programming and hardware manual
 - Summary booklet and wall schematic



A65/40-5000 AIM 65/40 Microcomputer

ORDERING INFORMATION

Microcomputers

Part No.	Description
A65/40-2000	AIM 65/40 SBC with 32K RAM, Monitor ROMs, Extended Keyboard, and VDC Module
A65/40-3000	AIM 65/40 SBC with 32K RAM, Monitor ROMs, Extended Keyboard, VDC Module & Graphics Printer
A65/40-4000	AIM 65/40 SBC with 32K RAM Monitor ROMs, Standard Keyboard and 40 Char. Display
A65/40-5000	AIM 65/40 with 32K RAM Monitor ROMs, Standard Keyboard, 40 Char. Display and Graphics Printer

Firmware Options

Part No.	Description
A65/40-7010	AIM 65/40 Assembler ROM
A65/40-7020	AIM 65/40 BASIC Interpreter ROMs
A65/40-7040	AIM 65/40 Math Package ROM
A65/40-7050	AIM 65/40 FORTH ROMs
A65/40-7090	AIM 65/40 Disk Operating System Version 1.0 (DOS 1.0) ROM
A65/40-7092	AIM 65/40 Bootstrap Disk Operating System Version 1.0 (BDOS 1.0) ROM

Software Options (5¼" Disks)

Part No.	Description
A65/40-7012	AIM 65/40 Macro Assembler and Linking Loader ⁽¹⁾
A65/40-7024	AIM 65/40 BASIC Compiler Disk ⁽²⁾
A65/40-7052	AIM 65/40 FORTH Target Compiler ⁽²⁾

Notes:

- Requires RM 65 FDC Module (RM65-5101E) and A65/40-7092 BDOS 1.0 ROM.
- Requires RM 65 FDC Module (RM65-5101E) and either A65/40-7090 DOS 1.0 or A65/40-7092 BDOS 1.0 ROM.

FUNCTIONAL DESCRIPTION

SINGLE BOARD COMPUTER (SBC) MODULE

The A65/40-1000 SBC Module contains an R6502 CPU, a 1 MHz clock circuit, on-board device decoders, interrupt request priority circuit, reset conditioning, and both PROM/ROM and RAM memory. On-board sockets accept up to 65K bytes of read-only and read/write memory. Up to 32K bytes of PROM/ROM and up to 48K bytes of RAM may be installed. All on-board memory may be enabled in 4K-byte blocks, yielding an optimal mix of on-board/off-board memory and I/O to be addressed. The RAM may also be write-protected in 8K-byte segments. Dual bank addressing allows an additional 56K bytes of memory or I/O to be accessed off-board.

The SBC module is connected by removable cables to the 40-Character Display and the Graphics Printer over identical Centronics type parallel handshaking interfaces. The SBC is also connected to the Standard Keyboard through a removable interface cable. These peripheral ports may be also used as general purpose bi-directional data ports with parallel, serial, interrupt, and timer capabilities controlled by user programming of two on-board R6522 Versatile Interface Adapter (VIA) devices.

A separate user-dedicated R6522 VIA interfaces with the Parallel I/O Connector. The high current drive capacity of the VIA's eight "B" port lines can directly drive many industry-standard devices, such as solid state relays. The RS-232C connector provides an interface that allows the SBC to function as a data set or data terminal. An Audio/TTY Connector interfaces to one or two audio cassette recorders and to a 20 mA current loop serial interface.

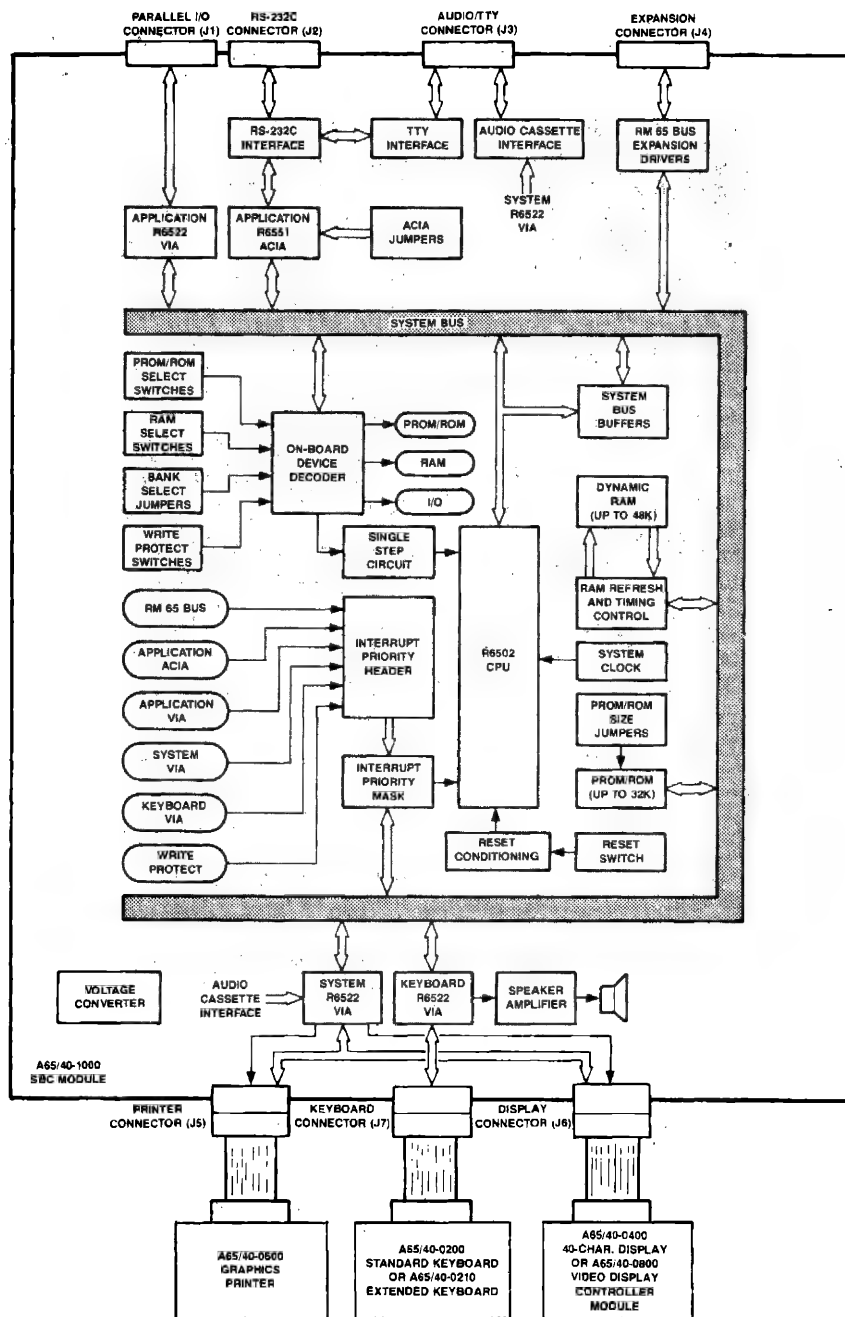
An Expansion Connector extends the system bus to Rockwell RM 65 bus compatible memory, I/O, or peripheral controller modules. Up to six levels of interrupt priority may be assigned to on-board and off-board peripherals.

STANDARD KEYBOARD

The A65/40-0200 Standard Keyboard is a full-size terminal style alphanumeric keyboard containing 66 momentary contact single pole single throw (SPST) keys and one locking SPST key. The keyboard has a complement of 63 momentary contact keys in an 8 x 9 matrix with nine positions unused. An ALL CAPS locking key is also in this matrix. Nine strobe and eight return lines are used to determine which key is pressed. Three momentary contact keys—RESET, ATTN, and PAPER FEED are outside of the keyboard matrix. These key switches have dedicated returns.

EXTENDED KEYBOARD

The A65/40-0210 Extended Keyboard has the added features of an industry standard numeric keyboard and cursor control keys.



AIM 65/40 System Block Diagram

GRAPHICS PRINTER

The A65/40-0600 Graphics Printer includes a dot matrix thermal printer mechanism, a microcomputer controller, thermal head drivers, and motor/strobe timing circuitry.

The printer mechanism includes a thermal head, platen, motor drive linkage, and associated wiring. There are 40 thermal elements on the thermal head, each of which spans seven dot fields; each element is a discrete point which rides against heat sensitive paper. Control logic turns on the thermal head drivers to heat the sensitized paper when a dot is to be printed. During a print cycle, the thermal head moves horizontally across the paper; when an entire row of dots has been printed, the printer motor advances the platen by one horizontal row of dots.

The printer controller includes an R6504 CPU, 4K-byte ROM, RAM, I/O, timer, clock, and reset circuitry. The ROM contains both the CPU instructions and the individual character bit patterns. The controller performs printer motor and thermal head timing and control functions to enable the printer to operate independently from the SBC module.

Data and control commands are transmitted to the printer over the Centronics type parallel handshake interface. An internal buffer accepts up to 80 bytes for printing. The controller automatically prints the first 40 7 x 8 dot-matrix characters in the text mode or after receiving a row of 280 dots in the graphics mode. The paper can also be advanced with a paper feed command, or manually using the paper feed switch.

40-CHARACTER DISPLAY

The A65/40-0400 40-Character Display contains a vacuum fluorescent display, a microprocessor-based controller, a 2K-byte character font/program ROM, character and segment drivers, and a DC/DC power converter. The vacuum fluorescent display is a single sealed unit containing 40 separately controllable digits. Each digit is composed of a 16-segment font which allows a full set of upper case alphabets, numerics, and special characters to be displayed. In the semi-graphics mode, the 16 segments of each digit are individually controlled. In addition, each digit includes a separate decimal point. When energized, the digits form bright, crisp characters in a blue-green color.

VIDEO DISPLAY CONTROLLER (VDC) MODULE

The A65/40-0800 Video Display Controller (VDC) module interfaces the AIM 65/40 microcomputer to either a CRT monitor or TV receiver. The module connects to the AIM 65/40 SBC module display connector (J5) and interfaces to the display through either the composite video output or the separate HSYNC, VSYNC, and VIDEO output TTL compatible signals. With its integral microcomputer controller, built-in commands provide selectable and programmable screen formatting, flexible text handling and editing, and full graphics drawing and data display functions. In the text mode, preprogrammed formats of 80 characters x 24 lines or 40 characters x 24 lines are selectable. Other formats are user programmable. The full graphics mode incorporates bit mapping of 280 x 224 pixels, which is compatible with the Graphics Printer.

I/O ROM

The I/O ROM includes preprogrammed auto-start initialization, interrupt, input/output and utility functions which support user-defined programs as well as AIM 65/40 optional firmware/software. Auto-start initialization jumps to predetermined PROM/ROM addresses during RESET processing. The application program can assume direct control of the system for continued operation, or it can just initialize required functions, then return control back to the I/O ROM for continued auto-start of other functions.

I/O drivers directly support AIM 65/40 intelligent display and printer peripherals. Other drivers support the RS-232C/TTY interfaces, the audio cassette ports and control the on-board speaker.

DEBUG MONITOR/TEXT EDITOR

The Debug Monitor/Text Editor includes a wide selection of functions to simplify computer program entry and checkout. Text can be easily entered, edited, saved, and retrieved using either line or screen oriented commands in the Text Editor. A character cursor can be positioned left, right, up, or down to aid character insertion, addition, and deletion. Automatic and selective character string change capability makes block-changes as desired. Multiple text buffers can easily be maintained for separate program and data files.

The Debug Monitor controls program execution in single step and run modes and allows convenient examination and altering of memory and registers. Single step operation allows instruction and register trace for detail examination of executed instructions. Symbol level debugging reduces dependence on absolute addresses and simplifies program checkout.

DEBUG MONITOR COMMANDS**Monitor Control Commands**

CTRL RESET	Enter and Initialize Monitor (Cold Reset)
RESET	Enter Monitor (Warm Reset)
ATTN	Non-Maskable Interrupt
ESC	Escape to Monitor Command Level
E	Initialize Text Buffer and Enter Text Editor
C	Recover Text Buffer and Enter Text Editor
T	Reenter Text Editor
F1 - F8	Enter Function 1 - Function 8
+	Repeat Last Command
&	Execute Command String
O	Toggle Memory Bank
CTRL Z	Direct Peripheral Control
CTRL Z CTRL Z	SBC Module RAM Self Test
CTRL C	Clear Display And Home Cursor
CTRL N	Home Cursor

Display/Alter Registers

R	Display Register Contents
A	Display/Alter Accumulator
P	Display/Alter Processor Status
S	Display/Alter Stack Pointer
X	Display/Alter X Register
Y	Display/Alter Y Register
*	Display/Alter Program Counter

Display/Alter Memory

M	Display Selected Memory Contents
SPACE	Display Higher Memory Locations
-	Display Lower Memory Locations
/	Alter Current Memory Contents

Enter/Disassemble Instructions

I	Enter Mnemonic Instruction
K	Disassemble Memory
:	Enter Symbolic Address

Execution/Trace

G	Execute Program
Z	Toggle Instruction Trace
J	Display Register Heading
H	Display Jump and Branch History
V	Toggle Symbol Table On/Off

Breakpoint Manipulation

?	Display Breakpoints
#	Clear Breakpoints
4	Toggle Breakpoint Enable On/Off
B	Set Breakpoint

Load/Dump Memory

L	Load Memory
D	Dump Memory
F	Verify Memory

Peripheral Control

CTRL P	Toggle Auto-Print On/Off
PRINT	Print Display Contents
1	Toggle Recorder 1 Control On/Off
2	Toggle Recorder 2 Control On/Off
3	Verify Tape Checksum

Screen Oriented Commands

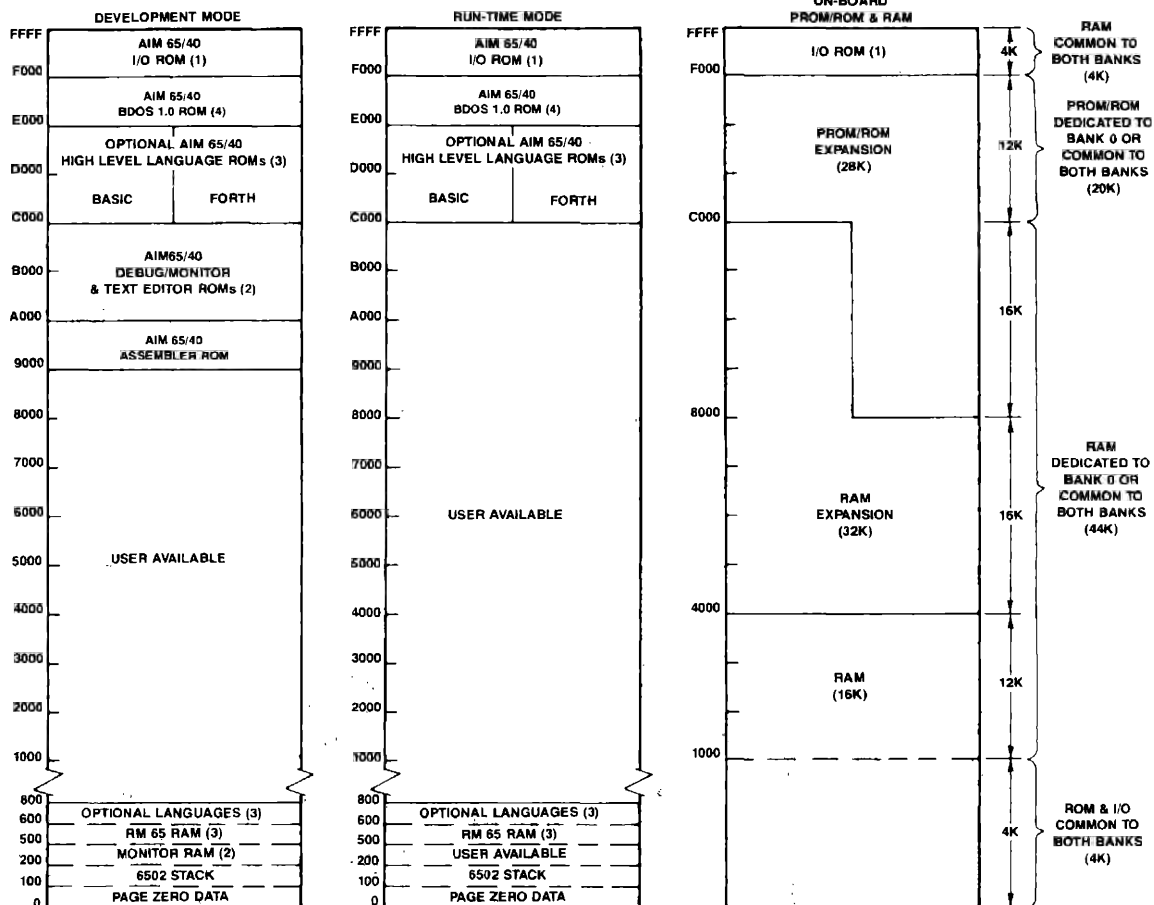
F1 (or CTRL Q)	Home Cursor on Line
F2 (or CTRL R)	Clear Line to Right
F3 (or CTRL S)	Toggle Insert Mode On/Off
F4 (or CTRL T)	Delete Character Under Cursor
F5 (or CTRL U)	Move Cursor Left (Left Arrow)
F6 (or CTRL V)	Move Cursor Right (Right Arrow)
F7 (or CTRL W)	Move Line/Cursor Down (Down Arrow)
F8 (or CTRL X)	Move Line/Cursor Up (Up Arrow)
CTRL A	Add (Insert) a Line
CTRL B	Break a Line
CTRL D	Delete a Line

TEXT EDITOR COMMANDS**Editor Control Commands**

S	Enter Screen Edit Mode
Q	Quit Editor and Enter Monitor
ESC	Return to Editor Command Level
+	Repeat Last Command
CTRL C	Clear Display and Home Cursor
CTRL N	Home Cursor

Line Oriented Commands

L	List Multiple Lines
R	Read Multiple Lines
I	Insert One Line
O	Overlay Current Line
K	Delete Multiple Lines
(SPACE)	Display Current Line
?	Display Current and Last Line Addresses
G	Go to Line Number
U	Go up Multiple Lines
D	Go down Multiple Lines
T	Go to Top Line
B	Go to Bottom Line
F7 (or CTRL W)	Go Down One Line
F8 (or CTRL X)	Go Up One Line



Notes

- (1) AIM 65/40 System peripheral I/O addresses are assigned to FF80-FFDF
- (2) User available during application program operation if the debug and text editor functions are not used.
- (3) User available if the optional language and the RM 65 expansion module ROMs are not used
- (4) Requires RM65-5101E Floppy Disk Controller (FDC) module
- (5) 56K bytes of RAM (0 - \$DFFF) is available for disk-based assembler compilers and user programs. I/O ROM and BDOS 1.0 ROM require 8K bytes (\$E000-\$FFFF)

AIM 65/40 SBC Memory Map

SBC Module Connector J1 (Parallel Application) Pin Assignments

Pin	Signal	I/O	Type	Pin	Signal	Type
1	CB2	I/O	NMOS	2	NC/+5V*	Power
3	CB1	I/O	NMOS	4	GND	Power
5	PB7	I/O	NMOS	6	GND	Power
7	PB6	I/O	NMOS	8	GND	Power
9	PB5	I/O	NMOS	10	GND	Power
11	PB4	I/O	NMOS	12	GND	Power
13	PB3	I/O	NMOS	14	GND	Power
15	PB2	I/O	NMOS	16	GND	Power
17	PB1	I/O	NMOS	18	GND	Power
19	PB0	I/O	NMOS	20	GND	Power
21	PA7	I/O	NMOS	22	GND	Power
23	PA6	I/O	NMOS	24	GND	Power
25	PA5	I/O	NMOS	26	GND	Power
27	PA4	I/O	NMOS	28	GND	Power
29	PA3	I/O	NMOS	30	GND	Power
31	PA2	I/O	NMOS	32	GND	Power
33	PA1	I/O	NMOS	34	GND	Power
35	PA0	I/O	NMOS	36	GND	Power
37	CA2	I/O	NMOS	38	GND	Power
39	CA1	I	NMOS	40	NC/+5V*	Power

Note: *Pins 2 and 40 can be optionally jumpered to +5V (maximum current through each pin should not exceed 200 mA).

SBC Module Connector J2
(Serial Application) Pin Assignment

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
1	GND		Power	2	$\overline{\text{TD}}$	O	RS-232C
3	$\overline{\text{RD}}$	I	RS-232C	4	RTS	I/O	RS-232C
5	CTS	I/O	RS-232C	6	DSR	I/O	RS-232C
7	GND		Power	8	DCD	I/O	RS-232C
9	NC			10	NC		
11	NC			12	NC		
13	NC			14	NC		
15	NC			16	NC		
17	NC			18	NC		
19	NC			20	DTR	I/O	RS-232C
21	NC			22	NC		
23	NC			24	NC		
25	NC			26	NC		

SBC Module Connector J3
(Audio/TTY) Pin Assignments

Pin	Signal	I/O	Type	Pin	Signal	Type
1	TTY RTS	I	TTY	2	GND	Power
3	TTY TD	O	TTY	4	GND	Power
5	TTY RD	I	TTY	6	GND	Power
7	TTY RTN		Power	8	GND	Power
9	AUDIO OUT	I	TTL	10	GND	Power
11	AUDIO IN	O	TTL	12	GND	Power
13	CTRL 2 RTN	O	Relay	14	GND	Power
15	CTRL 2	I	Relay	16	GND	Power
17	CTRL 1 RTN	O	Relay	18	GND	Power
19	CTRL 1	I	Relay	20	GND	Power

SBC Module Connector J4 (RM 65 Bus) Pin Assignments

Bottom (Solder Side)					Top (Component Side)				
Pin	Signal Mnemonic	Signal Name	I/O	Type	Pin	Signal Mnemonic	Signal Name	I/O	Type
W _a		Not Connected		—	W _c		Not Connected		—
X _a	+5V	+5 Vdc Line (See Note)		Power	X _c	+5V	+5 Vdc (See Note)		Power
1 _a	GND	Ground		Power	1 _c	+5V	+5 Vdc		Power
2 _a	BADR/	Buffered Bank Address	O	3S TTL	2 _c	BA15/	Buffered Address Bit 15	O	3S TTL
3 _a	GND	Ground		Power	3 _c	BA14/	Buffered Address Bit 14	O	3S TTL
4 _a	BA13/	Buffered Address Bit 13	O	3S TTL	4 _c	BA12/	Buffered Address Bit 12	O	3S TTL
5 _a	BA11/	Buffered Address Bit 11	O	3S TTL	5 _c	GND	Ground		3S TTL
6 _a	BA10/	Buffered Address Bit 10	O	3S TTL	6 _c	BA9/	Buffered Address Bit 9	O	3S TTL
7 _a	BA8/	Buffered Address Bit 8	O	3S TTL	7 _c	BA7/	Buffered Address Bit 7	O	3S TTL
8 _a	GND	Ground		Power	8 _c	BA6/	Buffered Address Bit 6	O	3S TTL
9 _a	BA5/	Buffered Address Bit 5	O	3S TTL	9 _c	BA4/	Buffered Address Bit 4	O	3S TTL
10 _a	BA3/	Buffered Address Bit 3	O	3S TTL	10 _c	GND	Ground		Power
11 _a	BA2/	Buffered Address Bit 2	O	3S TTL	11 _c	BA1/	Buffered Address Bit 1	O	3S TTL
12 _a	BA0/	Buffered Address Bit 0	O	3S TTL	12 _c	B ϕ 1	Buffered Phase 1 Clock	O	TP TTL
13 _a	GND	Ground		Power	13 _c	BSYNC	Buffered Sync		3S TTL
14 _a	BSO	Buffered Set Overflow	I	OC TTL	14 _c	BDRQ1/	*Buffered DMA Request 1		
15 _a	BRDY	Buffered Ready	I	OC TTL	15 _c	GND	Ground		Power
16 _a		*User Spare 1			16 _c	-12V/-V	*-12 Vdc/-V		
17 _a	+12V/+V	*+12 Vdc/+V			17 _c		*User Spare 2		
18 _a	GND	Ground Line		Power	18 _c	BFLT/	Buffered Bus Float	I	OC TTL
19 _a	BDMT/	*Buffered DMA Terminate			19 _c	B ϕ 0	*Buffered External Phase 0 Clock		
20 _a		*User Spare 3			20 _c	GND	Ground		Power
21 _a	BR/ \bar{W} /	Buffered Read/Write "Not"	O	3S TTL	21 _c	BDRQ2/	*Buffered DMA Request 2		
22 _a		*System Spare			22 _c	BR/ \bar{W}	Buffered Read/Write	O	3S TTL
23 _a	GND	Ground		Power	23 _c	BACT/	Buffered Bus Active	I	OC TTL
24 _a	BIRQ/	Buffered Interrupt Request	I	OC TTL	24 _c	BNMI/	Buffered Non-Maskable Interrupt	I	OC TTL
25 _a	B ϕ 2/	Buffered Phase 2 "Not" Clock	O	3S TTL	25 _c	GND	Ground		Power
26 _a	B ϕ 2	Buffered Phase 2 Clock	O	3S TTL	26 _c	BRES/	Buffered Reset	O	OC TTL
27 _a	BD7/	Buffered Data Bit 7	I/O	3S TTL	27 _c	BD6/	Buffered Data Bit 6	I/O	3S TTL
28 _a	GND	Ground		Power	28 _c	BD5/	Buffered Data Bit 5	I/O	3S TTL
29 _a	BD4/	Buffered Data Bit 4	I/O	3S TTL	29 _c	BD3/	Buffered Data Bit 3	I/O	3S TTL
30 _a	BD2/	Buffered Data Bit 2	I/O	3S TTL	30 _c	GND	Ground		Power
31 _a	BD1/	Buffered Data Bit 1	I/O	3S TTL	31 _c	BD0/	Buffered Data Bit 0	I/O	3S TTL
32 _a	+5V	+5 Vdc		Power	32 _c	GND	Ground		Power
Y _a	+5V	+5 Vdc (See Note)		Power	Y _c	+5V	+5 Vdc (See Note)		Power
Z _a		Not Connected		—	Z _c		Not Connected		—

Note: *Not used on the SBC. Signal name reflects RM 65 Bus reserved function.

SBC Module Connector J5 (Printer) Pin Assignments

Pin	R6522		Printer		Type	Pin	Signal	Type
	Signal	I/O	Signal	I/O				
1 (1)	+5V		+5V	O	Power	2	GND	Power
3	NC		NC		—	4	GND	Power
5	NC		NC		—	6	GND	Power
7	NC		NC		—	8	GND	Power
9	NC		NC		—	10	GND	Power
11	NC		NC		—	12	GND	Power
13	NC		NC		—	14	GND	Power
15	PAPER FEED (2)		PAPER FEED (2)		TTL	16	GND	Power
17	RES	O	RES	O	TTL	18	GND	Power
19	PB1	I/O	STROBE	O	NMOS	20	GND	Power
21	PA7	I/O	Data 7	O	NMOS	22	GND	Power
23	PA6	I/O	Data 6	O	NMOS	24	GND	Power
25	PA5	I/O	Data 5	O	NMOS	26	GND	Power
27	PA4	I/O	Data 4	O	NMOS	28	GND	Power
29	PA3	I/O	Data 3	O	NMOS	30	GND	Power
31	PA2	I/O	Data 2	O	NMOS	32	GND	Power
33	PA1	I/O	Data 1	O	NMOS	34	GND	Power
35	PA0	I/O	Data 0	O	NMOS	36	GND	Power
37			NC		—	38	GND	Power
39	CA2	I/O	ACK	I	NMOS	40 (1)	+5V	Power

Notes: (1) Maximum +5V current through J5 should not exceed 200 mA per pin.
 (2) Connected to J7-39 through jumper W3.

SBC Module Connector J6 (Display) Pin Assignments

Pin	R6522		Printer		Type	Pin	Signal	Type
	Signal	I/O	Signal	I/O				
1 (1)	+5V		+5V		Power	2	GND	Power
3	NC		NC		—	4	GND	Power
5	NC		NC		—	6	GND	Power
7	NC		NC		—	8	GND	Power
9	NC		NC		—	10	GND	Power
11	NC		NC		—	12	GND	Power
13	NC		NC		—	14	GND	Power
15	PAPER FEED (2)		PAPER FEED (2)	O	TTL	16	GND	Power
17	RES		RES	O	TTL	18	GND	Power
19	PB0	I/O	STROBE	O	NMOS	20	GND	Power
21	PA7	I/O	Data 7	O	NMOS	22	GND	Power
23	PA6	I/O	Data 6	O	NMOS	24	GND	Power
25	PA5	I/O	Data 5	O	NMOS	26	GND	Power
27	PA4	I/O	Data 4	O	NMOS	28	GND	Power
29	PA3	I/O	Data 3	O	NMOS	30	GND	Power
31	PA2	I/O	Data 2	O	NMOS	32	GND	Power
33	PA1	I/O	Data 1	O	NMOS	34	GND	Power
35	PA0	I/O	Data 0	O	NMOS	36	GND	Power
37			NC		—	38	GND	Power
39	CB2	I/O	ACK	I	NMOS	40	+5V	Power

Notes: (1) Maximum +5V current through J6 should not exceed 200 mA per pin.
 (2) Connected to J7-39 through jumper W3.

SBC Module Connector J7 (Keyboard) Pin Assignments

Pin	R6522		Keyboard		Type	Pin	Signal	Type
	Signal	I/O	Signal	I/O				
1 (2)	CB2	I/O	RES	I	TTL	2 (1)	NC/+5V	Power
3 (3)	CB1	I/O	ATTN	I	TTL	4	GND	Power
5	PB7	I/O	MSB7	O	NMOS	6	GND	Power
7	PB6	I/O	MSB6	O	NMOS	8	GND	Power
9	PB5	I/O	MSB5	O	NMOS	10	GND	Power
11	PB4	I/O	MSB4	O	NMOS	12	GND	Power
13	PB3	I/O	MSB3	O	NMOS	14	GND	Power
15	PB2	I/O	MSB2	O	NMOS	16	GND	Power
17	PB1	I/O	MSB1	O	NMOS	18	GND	Power
19	PB0	I/O	MSB0	O	NMOS	20	GND	Power
21	PA7	I/O	MRT7	I	NMOS	22	GND	Power
23	PA6	I/O	MRT6	I	NMOS	24	GND	Power
25	PA5	I/O	MRT5	I	NMOS	26	GND	Power
27	PA4	I/O	MRT4	I	NMOS	28	GND	Power
29	PA3	I/O	MRT3	I	NMOS	30	GND	Power
31	PA2	I/O	MRT2	I	NMOS	32	GND	Power
33	PA1	I/O	MRT1	I	NMOS	34	GND	Power
35	PA0	I/O	MRT0	I	NMOS	36	GND	Power
37	CA2	I/O	MSB8	I	NMOS	38	GND	Power
39 (4)	CA1	I	PAPER FEED	I	NMOS	40 (1)	NC/+5V	Power

Notes: (1) Pins 2 and 40 can be optionally jumpered to +5V (maximum current through each pin should not exceed 200 mA).

(2) Pin 1 can be optionally jumpered to the RESET circuit or to CB2.

(3) Pin 3 can be optionally jumpered to the NMI circuit or to CB1.

(4) Pin 39 can be optionally jumpered as PAPER FEED or to CA1.

NMOS INTERFACE (Input Voltage = +5.0V, TA = 25°C)

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input High Voltage	2.4	5.0	V
V_{IL}	Input Low Voltage	-0.3	+0.4	V
I_{IH}	Input High Current ($V_{IH} = 2.4V$)	-100	-300	μA
I_{IL}	Input Low Current ($V_{IL} = 0.4V$)	-1.0	-1.6	mA
V_{OH}	Output High Voltage ($I_{LOAD} \leq -100A$)	2.4	5.0	V
V_{OL}	Output Low Voltage ($I_{LOAD} \leq -3 mA$)	—	0.4	V
I_{OH}	Output High Current (Sourcing) ($V_{OH} \geq 2.4V$) ($V_{OH} \geq 1.5V$, VIA PB0-PB7 only)	-100 -1.0	—	μA mA
I_{OL}	Output Low Current (Sinking) ($V_{OL} \leq 0.4V$)	1.6	—	mA
TTL — Industry standard LS TTL. 3S TTL — Industry standard Tri-State LS TTL. OC TTL — Industry standard Open Collector LS TTL. TP TTL — Industry standard Totem Pole LS TTL.				

SPECIFICATIONS

Parameter	Value
Dimensions	
Width	11.85 in. (301 mm)
Length ⁽¹⁾	19.75 in. (502 mm)
Height ⁽²⁾	4.6 in. (117 mm)
Shipping	
Size	12.5 in. (320 mm) × 16.5 in. (420 mm) × 15 in. (385 mm)
Weight	13.3 lb. (6 kg)
Weight	
With Printer	4 lb. 4 oz. (1.58 kg)
Without Printer	3 lb. 4 oz. (1.21 kg)
Environment	
Operating Temperature	
With Printer	0°C to 50°C
Without Printer	0°C to 70°C
Storage Temperature	
With Printer	0°C to 70°C
Without Printer	-25°C to 85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	
With Printer	+5V ±5% regulated @ 2.6A (typ); 3.4A (max.); 3.4A (peak) ⁽³⁾ +24V (+3.6V, -2.6V) unregulated @ 2.5A (typ); 4.0A (max.); 6.3A (peak) ⁽⁴⁾
Without Printer	+5V ±5% regulated @ 1.8A (typ); 2.4A (max); 2.4A (peak) ⁽³⁾
Interface Connector	
J1 (Parallel Application)	40-pin edge connector (0.100 in. centers). Pre-drilled holes for installation of 40-pin 3M #3432-1002, or equivalent, mass terminated connector.
J2 (Serial Application)	26-pin edge connector (0.100 in. centers). Pre-drilled holes for installation of 25-pin AMP #206584-1, or equivalent, mass terminated connector.
J3 (Audio/TTY)	20-pin edge connector (0.100 in. centers). Pre-drilled holes for installation of 20-pin 3M #3492-1002, or equivalent, mass terminated connector.
J4 (RM 65 Expansion)	72-pin edge connector (0.100 in. centers). Pre-drilled holes for installation of a 64-pin DIN 41612 Euroconnector or 72-pin TI H42-51-11-36, or equivalent, connector to directly mate to one Rockwell RM 65 module.
J7 (Keyboard)	40-pin 3M #3495-1002, or equivalent. Mates with 3M #3418-0000T, or equivalent, ribbon cable connector.
J5 (Printer) and J6 (Keyboard)	40-pin 3M #3495-2002, or equivalent. Mates with 3M #3418-0000T, or equivalent, ribbon cable connector.
Notes: 1. Specified for 2 in. separation between keyboard and SBC modules. The length may be reduced if keyboard and SBC modules are overlapped/canted or may be extended by installation of a longer interface cable. A cable up to four feet in length may be installed. 2. Specified for the printer mounted to the SBC module on 1 in. standoffs. The printer may be mounted up to 2.5 in. above the SBC module using the installed 3 in. cable or may be installed to operate with a cable up to four feet in length. 3. Power requirements are specified for 8 PROM/ROM devices (32K bytes) 0.6A (typical) and 1.2A (maximum) total, and for 16 RAM devices (32K bytes) with 0.9A (typical) and 1.7A (maximum) total, installed. 4. +24V peak current specified as worst case with printer duty cycle of 75%. For most cases, a +24V 4A power supply is sufficient.	

REFERENCE DOCUMENTS

The following product literature is available for further product information.

Order Number	Document Title
D74	A65/40-0200, A65/40-0210 Standard and Extended Keyboard Data Sheet
D76	A65/40-0400 40-Character Display Data Sheet
D75	A65/40-0600 Graphic Printer Data Sheet
D86	A65/40-0800 Video Display Controller Module Data Sheet
D77	A65/40-1000 Single Board Computer Module Data Sheet
D123	A65/40-7010 Assembler ROM
D128	A65/40-7012 Macro Assembler and Linking Loader
D120	A65/40-7020 BASIC Interpreter ROMs
D118	A65/40-7024 BASIC Compiler
D130	A65/40-7040 Math Package ROMs
D122	A65/40-7050 FORTH ROMs
D119	A65/40-7052 FORTH Target Compiler
D116	A65/40-7090 Disk Operating System Version 1.0 ROM
D129	A65/40-7092 Bootstrap Disk Operating System Version 1.0 ROM



A65/40-1000 AIM 65/40 SINGLE BOARD COMPUTER

OVERVIEW

The A65/40-1000 Single Board Computer (SBC) is one of the hardware options available for the AIM 65/40 Microcomputer family.

The SBC is an extremely flexible and adaptable microcomputer on a single board. Memory sockets accept up to 65K bytes of read-only and read/write memory on the board. Three installed peripheral ribbon cable connectors, as well as three user dedicated application edge connectors, provide extensive and versatile parallel and serial interfaces for use in industrial, scientific and educational installations. The RM 65 Bus compatible expansion connector allows additional memory, I/O, peripheral controller and application modules to be easily connected.

Up to 32K bytes of PROM/ROM and up to 48K bytes of RAM may be installed on-board. All on-board memory may be enabled in 4K-byte blocks, yielding an optimal mix of on-board/off-board memory and I/O to be addressed. The RAM may also be write-protected in 8K-byte segments. Dual bank addressing allows an additional 56K bytes of memory or I/O to be accessed off-board.

The display and printer interfaces connect through interface cables to the A65/40-0400 40-Character Display and the A65/40-0600 Graphics Printer over identical Centronics type parallel handshaking interfaces. The keyboard interface connects to the A65/40-0200 Standard Keyboard through an interface cable. These peripheral ports may be used as general purpose bidirectional data ports with parallel, serial, interrupt and timer capabilities controlled by user programming of two on-board R6522 Versatile Interface Adapter (VIA) devices.

In addition, a separate user-dedicated R6522 VIA interfaces with the Parallel Application connector. The high current drive capacity of the VIA's eight "B" port lines can directly drive many industry-standard devices, such as solid state relays. The RS-232C Connector provides an interface that allows the SBC to function as a data set or data terminal. An Audio/TTY Connector can be used to attach one or two audio cassette recorders, for program or data storage, and a 20 mA current loop teletypewriter.

The A65/40-1000 SBC comes with a 4K-byte I/O ROM installed. Preprogrammed auto-start initialization, interrupt, input/output and utility functions support user-defined programs as well as AIM 65/40 optional firmware/software. Auto-start initialization jumps to predetermined PROM/ROM addresses during RESET processing. The application program can assume direct control of the SBC for continued operation, or it can just initialize required functions, then return control back to the I/O ROM for continued auto-start of other functions. I/O drivers directly support AIM 65/40 intelligent display and printer peripherals.

FEATURES

- Popular and Powerful 6502 CPU
- Extensive On-Board Memory
 - Up to 48K bytes of RAM, with write-protect
 - up to 32K bytes of PROM or ROM
- Extended and Flexible Addressing
 - 131K addressing, in two 65K-byte banks
 - Dedicated or shared bank addressing
 - On-board/off-board memory select
- User-Prioritized Interrupts—Up to six levels
- Installed I/O Driver ROM
 - Interrupt driven AIM 65/40 peripheral I/O handlers
 - User program auto-start initialization
 - Utility subroutines and user I/O driver linkage
- Two System Display/Printer Connectors
 - Centronics type parallel handshake
 - AIM 65/40 40-character display compatible
 - AIM 65/40 graphics printer compatible
- Full-Size Keyboard Interface
 - General purpose parallel interface
 - AIM 65/40 keyboard compatible
- Parallel Application Interface
 - R6522 Versatile Interface Adapter (VIA)
 - Two 8-bit parallel bidirectional data ports
 - Two 2-bit handshake control ports
 - Two programmable 16-bit counter/timers
 - 8-bit serial interface
- RS-232C Serial Application Interface
 - R6551 Asynchronous Communications Interface Adapter (ACIA) with programmable data rate to 19,200 baud
 - Configurable as data set or data terminal
- 20 mA Current Loop Serial Interface
- Interface to Low Cost Audio Cassette Recorders
 - Remote on/off control through on-board relays
 - AIM 65 format compatible
- On-Board Piezo-Electric Speaker
 - Programmable tone and duration
- +5V Operation

FUNCTIONAL DESCRIPTION

CENTRAL PROCESSING AND CONTROL

The A65/40-1000 SBC contains a central processing unit (CPU), decoders, read/write memory, read-only memory, peripheral interface devices, application interface circuits, expansion bus drivers and support circuitry—all connected together by an internal system bus.

The R6502 CPU, with its advanced pipeline architecture and 13 addressing modes for fast execution and memory efficiency, performs the central processing. A 1 MHz system operating frequency is derived from a clock circuit employing a 16 MHz reference crystal.

The RESET conditioning circuit shapes the RESET signal received from the on-board RESET switch or the Keyboard Connector and generates the system reset (\overline{RES}) for the CPU, on-board I/O devices, the off-board peripherals and the expansion bus. It also generates the \overline{RES} signal at power turn-on.

The Single Step circuit, enabled under software control, allows CPU monitored single instruction execution through user programs located below \$A000. When enabled, a Non-Maskable Interrupt (NMI) is generated upon execution of each instruction to allow an interrupt subroutine to perform debug functions, such as disassembly of the instruction and display of register contents.

The Interrupt Request Priority circuitry prioritizes individual interrupt requests (IRQ) from six sources—the System R6522 VIA, the Keyboard R6522 VIA, the Application R6522 VIA, the Application R6551 ACIA, the RM 65 Bus, and the on-board RAM Write Protect circuitry—into a system \overline{IRQ} . Each \overline{IRQ} can be assigned any priority relative to the others by wiring the Interrupt Request Priority Header. The Interrupt Request Priority Mask inhibits generation of the System \overline{IRQ} to the CPU for individual interrupt requests assigned below a software selected priority level.

The On-board Device Decoder generates device select signals for all on-board RAM, ROM or I/O access. The PROM/ROM and RAM select switches allow independent on-board/off-board selection of each 4K-byte block.

Programmable Bank Addressing creates two 65K-byte banks, for an effective addressing range of 131K bytes with the RM 65 Bus Expansion Connector. The upper 4K bytes containing the I/O ROM, and the lower 4K bytes containing the R6502 stack RAM, are always common to both Bank 0 and Bank 1. An additional 20K bytes of PROM/ROM may be assigned common to both banks, or dedicated to Bank 0, on 4K-byte boundaries with the Bank Selection jumpers. The remaining PROM/ROM and RAM is dedicated to Bank 0.

MEMORY

Eight 24-pin PROM/ROM sockets allow installation of up to 32K bytes of PROM/ROM. PROM/ROM size jumpers set up the sockets to accept 8K- or 4K-byte devices. The on-board RAM can be expanded up to 48K bytes using industry standard 16K \times 1 dynamic RAM devices in 24 16-pin sockets.

The RAM Refresh and Timing Control circuitry controls address and data timing for RAM memory access, and provides transparent refreshing of the dynamic RAM devices. Write protect switches allow the RAM to be selected for read-only access, with independent protection of 8K byte sections (except for the lowest 8K which contains page 0 and page 1). An attempted write into any protected RAM location will generate a write protect interrupt request (\overline{IRQ}).

I/O HARDWARE

Two system R6522 VIA devices support three peripheral ports—display, printer and keyboard. Common I/O data lines and separate control lines are routed from the System VIA to the Display and Printer Connectors. Both common or unique data can easily be transferred through the System VIA to the interfacing peripherals since the handshaking control lines are separately handled. The System VIA also controls data transferred to and from audio cassette recorders as well as on-board relays to remotely turn the recorders on and off. Each VIA provides two 16-bit timer/counters and an 8-bit serial shift register.

A separate R6522 VIA interfaces with the Keyboard Connector and the on-board speaker amplifier. Nine keyboard strobe lines are output from the keyboard VIA to the keyboard and another eight return lines are input. The eight return lines are also or'ed together and connected to the VIA to cause a keyboard \overline{IRQ} when a key is depressed.

The third R6522 VIA is dedicated to user functions. All 16 data and 4 control lines are routed directly to the Parallel Application Connector. The Application VIA provides two 8-bit bidirectional data ports with handshake control and allows the data direction of each port bit to be individually assigned. One of the data lines may be configured as a serial line to an 8-bit shift register with three input and four output modes. Two independent 16-bit timer/counters in the R6522 with four modes in Timer 1 and three modes in Timer 2 support numerous internal and external timing and clock functions. Two data ports associated with the timers allow various input/output functions to be programmed such as rectangular wave form generation and sampling.

In addition to the parallel interfaces, a user dedicated serial interface is provided in both RS-232C and 20 mA forms. An R6551 Asynchronous Communication Interface Adapter (ACIA) device connects to RS-232C and 20 mA current loop interface circuits. On-board jumpers configure the R6551 ACIA to operate as either a data set or a data terminal. The R6551 ACIA, with its internal data rate generator, may be programmed to one of the 16 rates (from 50 to 19,200 baud). Additional program control of word length (5, 6, 7 or 8 bits), number of stop bits (1, 1½ or 2) and parity (odd, even or none) is also provided.

The RS-232C interface circuit converts the TTL level signals to RS-232C voltage levels and routes the signals to the RS-232C Connector. The TTY Interface circuit converts TTL level signals to 20 mA current signals and routes the signals to the Audio/TTY Connector. The TTY receive data and transmit data lines operate in parallel with the RS-232C lines.

Line driver and tri-state circuitry interface with the on-board address, data and control lines to interface with the Expansion Connector. Both the address lines and data lines are inverted

to be compatible with the Rockwell RM 65 Bus. Data and control lines are connected to the Bus Control line from the Expansion Connector so they can be disconnected from the bus during off-board DMA operations.

INTERFACE CONNECTORS

The two identical 40-pin Display and Printer connectors allow display and printer functions to be easily interchanged, or duplicated if two displays or two printers are connected. These connectors are directly compatible with the A65/40-0400 40-Character Display and the A65/40-0600 Graphics Printer—or they may be connected to other Centronics type interface compatible equipment. +5V is routed to the connectors for use by the interfacing peripherals. The display and printer connectors are mounted vertically on the front half of the SBC to conveniently connect to the printer and display interface cables.

The 40-pin Keyboard Connector connects the 17 I/O lines from the Keyboard VIA to the keyboard interface cable. Keyboard RESET and Non-Maskable Interrupt (NMI) lines are routed from the connector to the Reset Conditioning and Single Step circuits respectively. The Paper Feed signal from the keyboard may be routed directly to the display and printer connectors, or to the Keyboard VIA. Mounted horizontally on the front of the SBC, the connector allows easy connection to an interfacing cable from the A65/40 Keyboard, or from any other compatible equipment.

The application, audio/TTY and expansion bus signals are routed to four edge connectors. The pins on each connector are spaced at standard 0.100 inch separation for direct connection to mass terminated cable connectors. Mounting holes are also provided to allow installation of other connectors.

The 40-pin Parallel Application Connector connects to I/O lines routed directly to the Application R6522 VIA. In addition, +5V can be supplied to the interfacing equipment through an on-board jumper.

The 26-pin RS-232C Connector connects to lines from the RS-232C Interface circuitry. A standard 25-pin D-type connector can be installed. The 20-pin Audio/TTY Connector interfaces with audio data and control lines from the Audio Cassette Interface circuitry and 20 mA current loop lines from the TTY Interface circuitry.

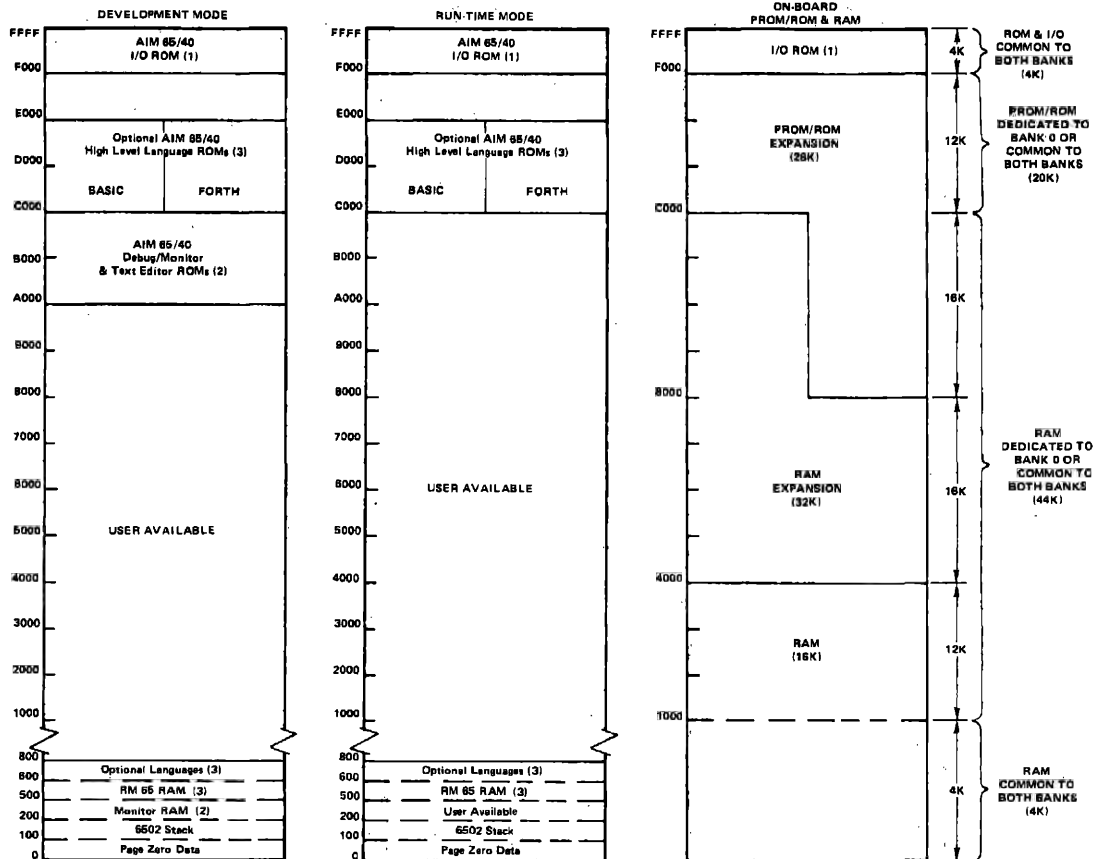
The 72-pin Expansion Connector interfaces to lines from the RM 65 Bus interface. An RM 65-AIM 65/40 Buffer Module; P/N RM65-7140(E) can be connected to the Expansion Connector to interface with a Rockwell RM 65 card cage/motherboard.

VOLTAGE CONVERTER

The DC-DC Voltage Converter generates all required on-board voltages from the +5 volt supply. The +12V and -12V are used by the RS-232C Interface Circuit, while +12V and -5V are required by the dynamic RAMs.

NMOS Interface (Input Voltage = +5.0V, TA = 25°C)

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input High Voltage	2.4	5.0	V
V_{IL}	Input Low Voltage	-0.3	+0.4	V
I_{IH}	Input High Current ($V_{IH} = 2.4V$)	-100	-300	
I_{IL}	Input Low Current ($V_{IL} = 0.4A$)	-1.0	-1.6	mA
V_{OH}	Output High Voltage ($I_{LOAD} \leq -100 A$)	2.4	5.0	V
V_{OL}	Output Low Voltage ($I_{LOAD} \leq -3 mA$)	—	0.4	V
I_{OH}	Output High Current (Sourcing) ($V_{OH} \geq 2.4V$)	-100	—	μA
	($V_{OH} \geq 1.5V$, VIA PB0-PB7 only)	-1.0	—	mA
I_{OL}	Output Low Current (Sinking) ($V_{OL} \leq 0.4V$)	1.6	—	mA
Notes: TTL — Industry standard LS TTL. 3S TTL — Industry standard Tri-State LS TTL. OC TTL — Industry standard Open Collector LS TTL. TP TTL — Industry standard Totem Pole LS TTL.				



- Notes: (1) AIM 65/40 System peripheral I/O addresses are assigned to FF80 - FFDF.
 (2) User available during application program operation if the debug and text editor functions are not used.
 (3) User available if the optional language and the RM 65 expansion module ROMs are not used.

Connector J1 (Parallel Application) Pin Assignments

Pin	Signal	I/O	Type	Pin	Signal	Type
1	CB2	I/O	NMOS	2	NC/+5V*	Power
3	CB1	I/O	NMOS	4	GND	Power
5	PB7	I/O	NMOS	6	GND	Power
7	PB6	I/O	NMOS	8	GND	Power
9	PB5	I/O	NMOS	10	GND	Power
11	PB4	I/O	NMOS	12	GND	Power
13	PB3	I/O	NMOS	14	GND	Power
15	PB2	I/O	NMOS	16	GND	Power
17	PB1	I/O	NMOS	18	GND	Power
19	PB0	I/O	NMOS	20	GND	Power
21	PA7	I/O	NMOS	22	GND	Power
23	PA6	I/O	NMOS	24	GND	Power
25	PA5	I/O	NMOS	26	GND	Power
27	PA4	I/O	NMOS	28	GND	Power
29	PA3	I/O	NMOS	30	GND	Power
31	PA2	I/O	NMOS	32	GND	Power
33	PA1	I/O	NMOS	34	GND	Power
35	PA0	I/O	NMOS	36	GND	Power
37	CA2	I/O	NMOS	38	GND	Power
39	CA1	I	NMOS	40	NC/+5V*	Power

Note: *Pins 2 and 40 can be optionally jumpered to +5V (maximum current through each pin should not exceed 200 mA).

Connector J2 (Serial Application) Pin Assignments

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
1	GND		Power	2	TD	O	RS-232C
3	RD	I	RS-232C	4	RTS	I/O	RS-232C
5	CTS	I/O	RS-232C	6	DSR	I/O	RS-232C
7	GND		Power	8	DCD	I/O	RS-232C
9	NC			10	NC		
11	NC			12	NC		
13	NC			14	NC		
15	NC			16	NC		
17	NC			18	NC		
19	NC			20	DTR	I/O	RS-232C
21	NC			22	NC		
23	NC			24	NC		
25	NC			26	NC		

Connector J3 (Audio/TTY) Pin Assignments

Pin	Signal	I/O	Type	Pin	Signal	Type
1	TTY RTS	I	TTY	2	GND	Power
3	TTY TD	O	TTY	4	GND	Power
5	TTY RD	I	TTY	6	GND	Power
7	TTY RTN		Power	8	GND	Power
9	AUDIO OUT	I	TTL	10	GND	Power
11	AUDIO IN	O	TTL	12	GND	Power
13	CTRL 2 RTN	O	Relay	14	GND	Power
15	CTRL 2	I	Relay	16	GND	Power
17	CTRL 1 RTN	O	Relay	18	GND	Power
19	CTRL 1	I	Relay	20	GND	Power

Connector J4 (RM 65 Bus) Pin Assignments

Bottom (Solder Side)					Top (Component Side)				
Pin	Signal Mnemonic	Signal Name	I/O	Type	Pin	Signal Mnemonic	Signal Name	I/O	Type
Wa		Not Connected		—	Wc		Not Connected		—
Xa	+5V	+5 Vdc Line (See Note)		Power	Xc	+5V	+5 Vdc (See Note)		Power
1a	GND	Ground		Power	1c	+5V	+5 Vdc		Power
2a	BADR/	Buffered Bank Address	O	3S TTL	2c	BA15/	Buffered Address Bit 15	O	3S TTL
3a	GND	Ground		Power	3c	BA14/	Buffered Address Bit 14	O	3S TTL
4a	BA13/	Buffered Address Bit 13	O	3S TTL	4c	BA12/	Buffered Address Bit 12	O	3S TTL
5a	BA11/	Buffered Address Bit 11	O	3S TTL	5c	GND	Ground		3S TTL
6a	BA10/	Buffered Address Bit 10	O	3S TTL	6c	BA9/	Buffered Address Bit 9	O	3S TTL
7a	BA8/	Buffered Address Bit 8	O	3S TTL	7c	BA7/	Buffered Address Bit 7	O	3S TTL
8a	GND	Ground		Power	8c	BA6/	Buffered Address Bit 6	O	3S TTL
9a	BA5/	Buffered Address Bit 5	O	3S TTL	9c	BA4/	Buffered Address Bit 4	O	3S TTL
10a	BA3/	Buffered Address Bit 3	O	3S TTL	10c	GND	Ground		Power
11a	BA2/	Buffered Address Bit 2	O	3S TTL	11c	BA1/	Buffered Address Bit 1	O	3S TTL
12a	BA0/	Buffered Address Bit 0	O	3S TTL	12c	Bφ1	Buffered Phase 1 Clock	O	TP TTL
13a	GND	Ground		Power	13c	BSYNC	Buffered Sync		3S TTL
14a	BSO	Buffered Set Overflow	I	OC TTL	14c	BDRQ1/	*Buffered DMA Request 1		
15a	BRDY	Buffered Ready	I	OC TTL	15c	GND	Ground		Power
16a		*User Spare 1			16c	-12 V/-V	*-12 Vdc/-V		
17a	+12 V/+V	*+12 Vdc/+V			17c		*User Spare 2		
18a	GND	Ground Line		Power	18c	BFLT/	Buffered Bus Float	I	OC TTL
19a	BDMT/	*Buffered DMA Terminate			19c	Bφ0	*Buffered External Phase 0 Clock		
20a		*User Spare 3			20c	GND	Ground		Power
21a	BRW/	Buffered Read/Write "Not"	O	3S TTL	21c	BDRQ2/	*Buffered DMA Request 2		
22a		*System Spare			22c	BRW/	Buffered Read/Write	O	3S TTL
23a	GND	Ground		Power	23c	BACT/	Buffered Bus Active	I	OC TTL
24a	BIRQ/	Buffered Interrupt Request	I	OC TTL	24c	BNMI/	Buffered Non-Maskable Interrupt	I	OC TTL
25a	Bφ2/	Buffered Phase 2 "Not" Clock	O	3S TTL	25c	GND	Ground		Power
26a	Bφ2	Buffered Phase 2 Clock	O	3S TTL	26c	BRES/	Buffered Reset	O	OC TTL
27a	BD7/	Buffered Data Bit 7	I/O	3S TTL	27c	BD6/	Buffered Data Bit 6	I/O	3S TTL
28a	GND	Ground		Power	28c	BD5/	Buffered Data Bit 5	I/O	3S TTL
29a	BD4/	Buffered Data Bit 4	I/O	3S TTL	29c	BD3/	Buffered Data Bit 3	I/O	3S TTL
30a	BD2/	Buffered Data Bit 2	I/O	3S TTL	30c	GND	Ground		Power
31a	BD1/	Buffered Data Bit 1	I/O	3S TTL	31c	BD0/	Buffered Data Bit 0	I/O	3S TTL
32a	+5V	+5 Vdc		Power	32c	GND	Ground		Power
Ya	+5V	+5 Vdc (See Note)		Power	Yc	+5V	+5 Vdc (See Note)		Power
Za		Not Connected		—	Zc		Not Connected		—

Note: *Not used on the SBC. Signal name reflects RM 65 Bus reserved function.

Connector J5 (Printer) Pin Assignments

Pin	R6522		Printer		Type	Pin	Signal	Type
	Signal	I/O	Signal	I/O				
1 (1)	+5V	O	+5V	O	Power	2	GND	Power
3	NC		NC		—	4	GND	Power
5	NC		NC		—	6	GND	Power
7	NC		NC		—	8	GND	Power
9	NC		NC		—	10	GND	Power
11	NC		NC		—	12	GND	Power
13	NC		NC		—	14	GND	Power
15	PAPERFEED (2)		PAPERFEED (2)		TTL	16	GND	Power
17	RES	O	RES	O	TTL	18	GND	Power
19	PB1	I/O	STROBE	O	NMOS	20	GND	Power
21	PA7	I/O	Data 7	O	NMOS	22	GND	Power
23	PA6	I/O	Data 6	O	NMOS	24	GND	Power
25	PA5	I/O	Data 5	O	NMOS	26	GND	Power
27	PA4	I/O	Data 4	O	NMOS	28	GND	Power
29	PA3	I/O	Data 3	O	NMOS	30	GND	Power
31	PA2	I/O	Data 2	O	NMOS	32	GND	Power
33	PA1	I/O	Data 1	O	NMOS	34	GND	Power
35	PA0	I/O	Data 0	O	NMOS	36	GND	Power
37			NC		—	38	GND	Power
39	CA2	I/O	ACK	I	NMOS	40(1)	+5V	Power

Notes: (1) Maximum +5V current through J5 should not exceed 200 mA per pin. (2) Connected to J7-39 through jumper W3.

Connector J6 (Display) Pin Assignments

Pin	R6522		Display		Type	Pin	Signal	Type
	Signal	I/O	Signal	I/O				
1 (1)	+5V		+5V		Power	2	GND	Power
3	NC		NC		—	4	GND	Power
5	NC		NC		—	6	GND	Power
7	NC		NC		—	8	GND	Power
9	NC		NC		—	10	GND	Power
11	NC		NC		—	12	GND	Power
13	NC		NC		—	14	GND	Power
15	PAPERFEED (2)		PAPERFEED (2)	O	TTL	16	GND	Power
17	RES		RES	O	TTL	18	GND	Power
19	PB0	I/O	STROBE	O	NMOS	20	GND	Power
21	PA7	I/O	Data 7	O	NMOS	22	GND	Power
23	PA6	I/O	Data 6	O	NMOS	24	GND	Power
25	PA5	I/O	Data 5	O	NMOS	26	GND	Power
27	PA4	I/O	Data 4	O	NMOS	28	GND	Power
29	PA3	I/O	Data 3	O	NMOS	30	GND	Power
31	PA2	I/O	Data 2	O	NMOS	32	GND	Power
33	PA1	I/O	Data 1	O	NMOS	34	GND	Power
35	PA0	I/O	Data 0	O	NMOS	36	GND	Power
37			NC		—	38	GND	Power
39	CB2	I/O	ACK	I	NMOS	40	+5V	Power

Notes: (1) Maximum +5V current through J6 should not exceed 200 mA per pin. (2) Connected to J7-39 through jumper W3.

Connector J7 (Keyboard) Pin Assignments

Pin	R6522		Keyboard		Type	Pin	Signal	Type
	Signal	I/O	Signal	I/O				
1 (2)	CB2	I/O	RES	I	TTL	2 (1)	NC/+5V	Power
3 (3)	CB1	I/O	ATTN	I	TTL	4	GND	Power
5	PB7	I/O	MSB7	O	NMOS	6	GND	Power
7	PB6	I/O	MSB6	O	NMOS	8	GND	Power
9	PB5	I/O	MSB5	O	NMOS	10	GND	Power
11	PB4	I/O	MSB4	O	NMOS	12	GND	Power
13	PB3	I/O	MSB3	O	NMOS	14	GND	Power
15	PB2	I/O	MSB2	O	NMOS	18	GND	Power
17	PB1	I/O	MSB1	O	NMOS	18	GND	Power
19	PB0	I/O	MSB0	O	NMOS	20	GND	Power
21	PA7	I/O	MRT7	I	NMOS	22	GND	Power
23	PA6	I/O	MRT6	I	NMOS	24	GND	Power
25	PA5	I/O	MRT5	I	NMOS	26	GND	Power
27	PA4	I/O	MRT4	I	NMOS	28	GND	Power
29	PA3	I/O	MRT3	I	NMOS	30	GND	Power
31	PA2	I/O	MRT2	I	NMOS	32	GND	Power
33	PA1	I/O	MRT1	I	NMOS	34	GND	Power
35	PA0	I/O	MRT0	I	NMOS	36	GND	Power
37	CA2	I/O	MSB8	I	NMOS	38	GND	Power
39	CA1	I	PAPERFEED	I	NMOS	40 (1)	NC/+5V	Power

Notes: (1) Pins 2 and 40 can be optionally jumpered to +5V (maximum current through each pin should not exceed 200 mA).

(2) Pin 1 can be optionally jumpered to the RESET circuit or to CB2.

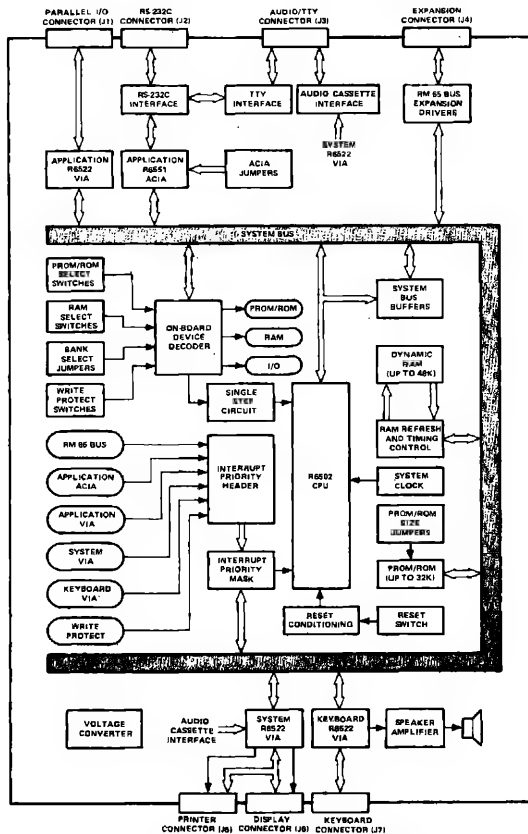
(3) Pin 3 can be optionally jumpered to the NMI circuit or to CB1.

(4) Pin 39 can be optionally jumpered as PAPERFEED or to CA1.

SPECIFICATIONS

Parameter	Value
Dimensions	
Width	11.85 in. (301 mm)
Length	12.5 in. (318 mm)
Height	0.75 (19 mm)
Weight	1.0 lb. (373 g)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	+5V ±5% Regulated; 2.5A (typical); 3.5A (max.)
Power Connector	2 Post Terminal Block
Interface Connector	
J1 (Parallel Application)	40-pin edge connector (0.100 in. centers). Pre-drilled holes for installation of 40-pin 3M #3432-1002, or equivalent, mass terminated connector.
J2 (Serial Application)	26-pin edge connector (0.100 in. centers). Pre-drilled holes for installation of 25-pin AMP #206584-1, or equivalent, mass terminated connector.
J3 (Audio/TTY)	20-pin edge connector (0.100 in. centers). Pre-drilled holes for installation of 20-pin 3M #3492-1002 or equivalent, mass terminated connector.
J4 (RM 65 Expansion)	72-pin edge connector (0.100 in. centers). Pre-drilled holes for installation of a 64-pin DIN 41612 Euroconnector or 72-pin TI H42-51-11-36, or equivalent, connector to directly mate to one Rockwell RM 65 module.
J7 (Keyboard)	40-pin 3M #3495-1002, or equivalent. Mates with 3M #3418-0000T, or equivalent, ribbon cable connector.
J5 (Printer) and J6 (Keyboard)	40-pin 3M #3495-2002, or equivalent. Mates with 3M #3418-0000T, or equivalent, ribbon cable connector.

Note: Power requirements are specified for 8 PROM/ROM devices (32K bytes) 0.6A (typical) and 1.2A (maximum), and for 16 RAM devices (32K bytes) with total 0.9A and 1.7A (maximum) total, installed.



A65/40-1000 Single Board Computer (SBC) Diagram



A65/40-0004

AIM 65/40 POWER SUPPLY AND CABLE

DESCRIPTION

The AIM 65/40 Power Supply and Cable is an open frame DC power supply with output cable for connection to an AIM 65/40 Microcomputer. The power supply provides sufficient power for full on-board RAM and PROM/ROM expansion as well as off-board RM 65 expansion modules, e.g., RM 65 Floppy Disk Controller (FDC) module (RM65-5101E) and RM 65 Multifunction Peripheral Interface (MPI) module (RM65-5223E). The +24V/4A output supplies power to the AIM 65/40 Graphics Printer. The $\pm 12V$ and $-5V$ outputs are not used by the AIM 65/40 Microcomputer, but are available for expansion module use.

AC power connects to an input terminal strip. A jumper on the power supply can be positioned for either 115 or 230 Vac input. An input fuse (5A for 115 Vac or 3A for 230 Vac) provides line protection. The 3-wire DC output cable, factory connected to the power supply output terminals, allows direct connection to the AIM 65/40 input power terminals.

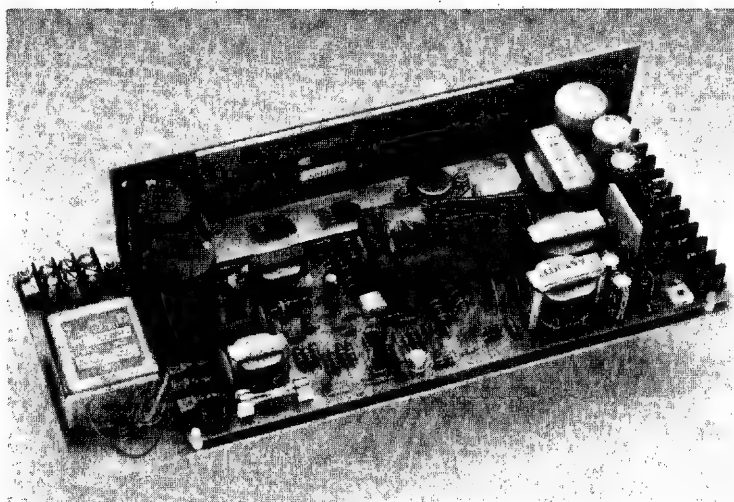
All outputs are current limited to prevent damage to the power supply if the outputs are overloaded or accidentally shorted together. Full power output is provided from 0° to 50°C.

FEATURES

- Dual AC input voltage
 - 115 Vac @ 47-63 Hz or
 - 230 Vac @ 47-63 Hz
- Five DC output voltages
 - +5V for AIM 65/40 Microcomputer logic
 - +24V for AIM 65/40 Graphics Printer
 - +12V, -12V and -5V for expansion modules
- Fused input
- 75% minimum efficiency
- All outputs current limited
- No 60 Hz EMI
- Meets FCC/VDE RFI requirements
- Soft start—Minimizes input current surge at turn-on
- No turn on or turn off overshoot
- DC output cable included

ORDERING INFORMATION

Part No.	Description
A65/40-0004	AIM 65/40 Power Supply and Cable



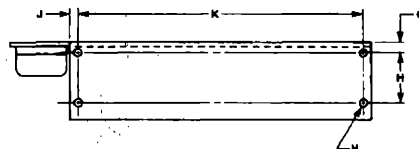
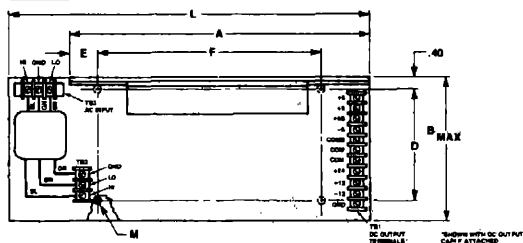
A65/40-0004 Power Supply

SPECIFICATIONS

Parameter	Value	Parameter	Value
AC Input	115/230 Vac \pm 10%, 47-63 Hz	Hold Up Time	16 ms min. at nominal line input with full load output
DC Output		Temperature Range	0°C to 50°C full rating, derated 2% per °C linearly from 50°C to 70°C.
Total Output Power	150 W max.	Dimensions	
+5 Vdc	20.0A max.	A	10.50 in. (266.7 mm)
+24 Vdc	4.0A ave. max., 8.0A peak	B	5.00 in. (127.0 mm)
+12 Vdc	1.5A max.	C	2.50 in. (63.5 mm)
-12 Vdc	1.0A max.	D	3.90 in. (99.0 mm)
-5 Vdc	0.5A max.	E	0.30 in. (7.6 mm)
Output Accuracy*		F	8.90 in. (226.0 mm)
+5V output	Adjustable \pm 5%	G	0.38 in. (9.6 mm)
Other outputs	\pm 5% max.	H	1.62 in. (41.1 mm)
Static Regulation		J	0.25 in. (6.4 mm)
Line	\pm 1% all output	K	10.00 in. (254.0 mm)
Load	20% to 100% max. rated load	L	12.5 in. (317.5 mm)
+5V output	\pm 1% max.	M	8-32 THD. (4)
Other outputs	\pm 3% max.	N	0.156 in. (3.96 mm) DIA. (4)
Ripple and Noise	0.2% RMS	Output Cable	
Temperature Coefficients	0.02%/°C	Length	12 in. (304.8 mm)
Overshoot	No turn on or turn off overshoot	Type	3-wire jacketed with internal balun
Overload Protection	Current limit protection on all outputs	Gauge	20 AWG
Overvoltage Protection	All outputs protected against power supply induced overvoltage.	Termination	Tinned leads
Brownout Protection	Holds full rated regulation to 85/170 Vac	Routed Outputs	+5V, +24V and COM

Note:

*Referenced to nominal input voltage at 60% load on all outputs with +5V output set to +5.00V.





A65/40-0200 AND A65/40-0210 AIM 65/40 STANDARD AND EXTENDED KEYBOARDS

OVERVIEW

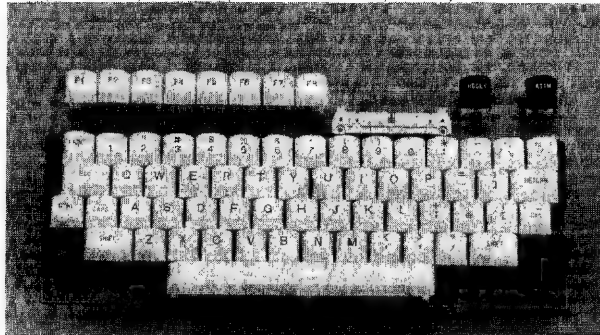
The A65/40-0200 and A65/40-0210 keyboard subassemblies are one of the hardware options available for the AIM 65/40 Microcomputer family.

The A65/40-0200 Standard Keyboard is a full-size ASCII keyboard. The 57 main keys provide the complete set of 128 ASCII printable and control characters. Eight separate function keys, located above the main keyboard, support user-defined processes. Separate ATTN and RESET keys allow user-defined interrupt processing and computer initialization. An industry standard, NMOS parallel interface can be used to connect the keyboard to a Rockwell AIM 65/40 Single-Board Computer (SBC), Rockwell RM 65 board-level products, or to other computers.

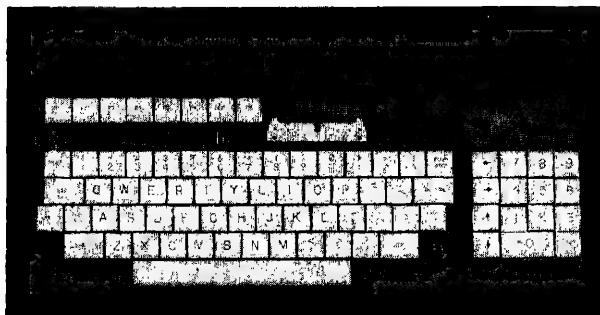
The A65/40-0210 Extended Keyboard has all of the above features, plus an industry standard numeric keyboard and cursor control key:

FEATURES

- Full-size, terminal-style keyboard
- 64 keys within an 8 × 9 matrix support the ASCII character set:
 - Alphanumerics
 - Punctuation
 - Special symbols
 - PRINT
 - Eight special functions
 - Locking ALL CAPS
- Separate RESET, ATTN, and PAPER FEED keys
- Extended keyboard has 15 additional keys; 10 numeric, decimal point and 4 cursor control keys
- No active components ensures long life
- Keyboard interface connector compatible with AIM 65/40 SBC or RM 65 Parallel Application connectors



A65/40-0200 Standard Keyboard



A65/40-0210 Extended Keyboard

FUNCTIONAL DESCRIPTION

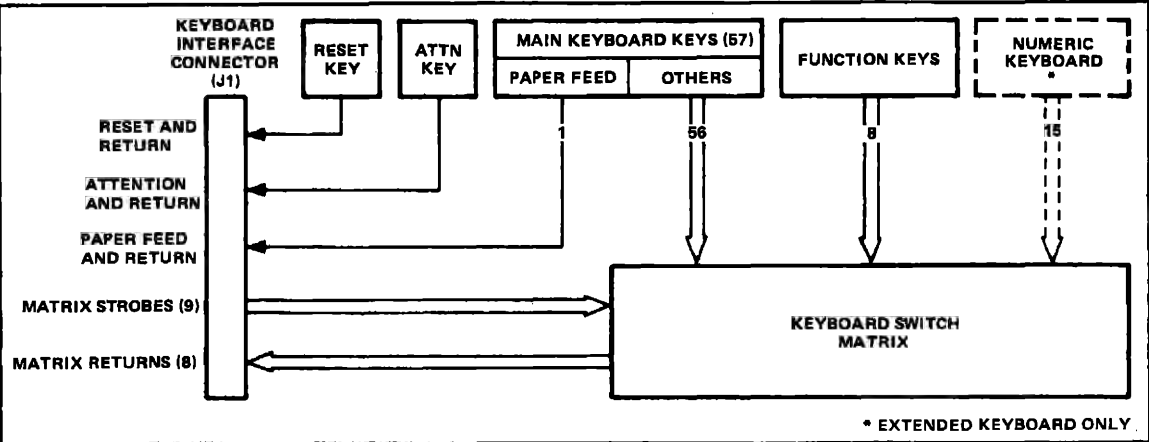
The AIM 65/40 Keyboard assembly is a terminal-style alphanumeric keyboard which interfaces to a host computer through a parallel interface. The keyboard contains 66 momentary contact single pole single throw (SPST) keys and one locking SPST key.

The keyboard has a complement of 63 momentary contact keys in an 8 x 9 matrix; with nine positions unused. An ALL CAPS locking key is also in this matrix. To decode keys within the matrix, the AIM 65/40 software places a logic 0 on one of the nine strobe lines of the matrix. By reading the eight return lines, any key(s) down on that strobe row can be distinguished. Repeating this process for each of the nine strobe rows gives

an image of the entire keyboard matrix. Three momentary contact keys—RESET, ATTN, and PAPER FEED are outside of the keyboard matrix.

All keyboard strobe and return lines are brought out to a 40-pin keyboard interface connector, which allows direct connection to an AIM 65/40 SBC or any RM 65 modules with the parallel peripheral connector.

The added keys on the Extended Keyboard control 15 additional momentary contact SPST switches, which are included in the 8 x 9 switch matrix. The 11 numeric and decimal switches are connected in parallel with their counterparts on the main keyboard. The four cursor control switches are added positions in the matrix which are not included in the Standard Keyboard.

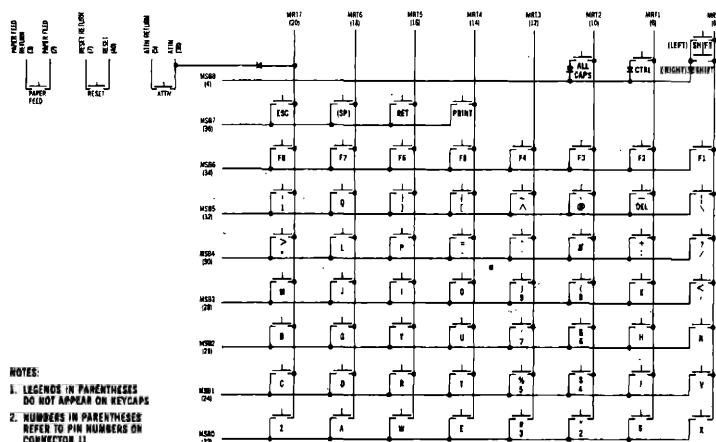


Keyboard Functional Block Diagram

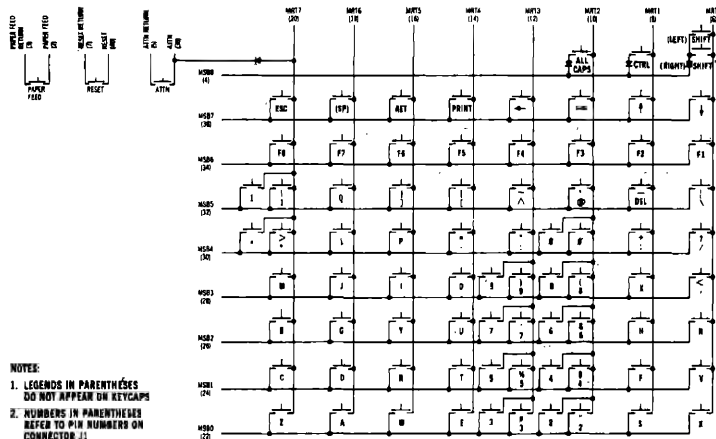
Connector P1 (System Interface) Pin Assignments

Pin	Signal	Pin	Signal
40	RES	39	NC
38	ATTN	37	GND (1)
36	MSB7	35	GND (1)
34	MSB6	33	GND (1)
32	MSB5	31	GND (1)
30	MSB4	29	GND (1)
28	MSB3	27	GND (1)
26	MSB2	25	GND (1)
24	MSB1	23	GND (1)
22	MSB0	21	GND (1)
20	MRT7	19	GND (1)
18	MRT6	17	GND (1)
16	MRT5	15	GND (1)
14	MRT4	13	GND (1)
12	MRT3	11	GND (1)
10	MRT2	9	GND (1)
8	MRT1	7	RES RET
6	MRT0	5	ATTN RET
4	MSB8	3	PAPER FEED RET
2	PAPER FEED	1	NC

Notes:
(1) Odd-numbered pins 9 through 37 are connected together on the keyboard and should be connected to GND on the interfacing equipment.
(2) The pin number assignments are reversed from the AIM 65/40 SBC, to provide a one-to-one signal routing through a 40-conductor ribbon cable.



Standard

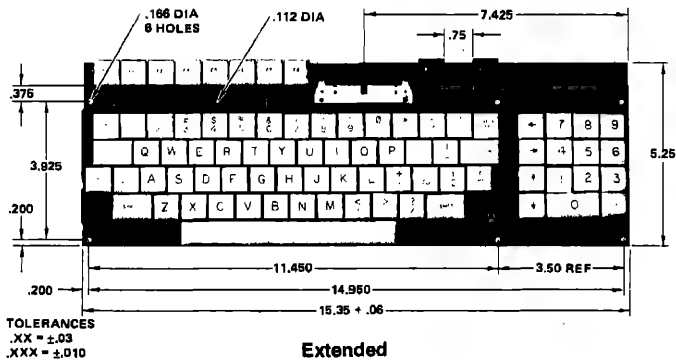
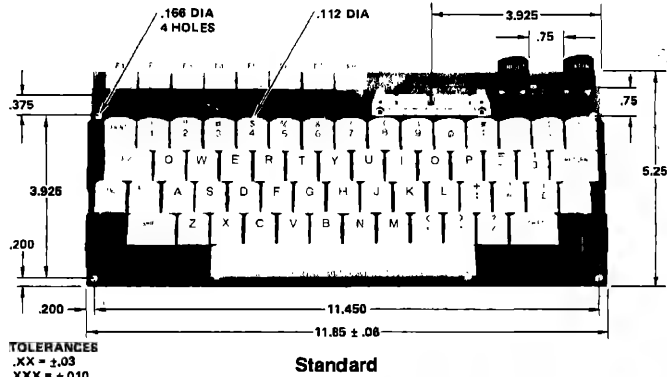


Extended

Keyboard Schematic

SPECIFICATIONS

Parameter	Value		
Dimensions	Standard	Extended	
	Width	11.85 in. (301 mm)	15.35 in. (390 mm)
	Length	5.25 in. (133 mm)	5.25 in. (133 mm)
	Height	1.25 in. (32 mm)	1.25 in. (32 mm)
Weight	1 lb. 8 oz.	1 lb. 12 oz.	
Environment			
	Operating Temperature	0°C to 50°C	
	Storage Temperature	−40°C to 55°C	
	Relative Humidity	0% to 95% (without condensation)	
Interface Connector	40-pin 3M #3495-1002, or equivalent, receptacle. Mates with 3M #3418-0000T, or equivalent ribbon cable connector.		



Keyboard Dimensions



A65/40-0400

AIM 65/40 40-CHARACTER DISPLAY

OVERVIEW

The A65/40-0400 40-Character Display is one of the hardware options available for the AIM 65/40 Microcomputer family.

The 40-Character Alphanumeric Display is a free-standing subassembly consisting of a vacuum fluorescent display and a microprocessor based controller. With its integral controller, operation is completely automatic—including display refresh. Connecting to a host computer over parallel interface with Centronics-compatible protocol, command and data are transferred in a handshaking manner.

The sealed vacuum fluorescent display includes 40 bright, crisp, 16-segment digits. The blue-green characters are easily readable in almost any working environment—from office to factory.

Firmware functions in the controller augment basic communication and display updating with a variety of editing functions and display enhancements to increase its usability. The full 40-characters, coupled with programmable eye-catching techniques, such as variable rate character blinking and auto-scrolling, allow meaningful and important messages to be displayed, detected and understood—in factory, office, laboratory and classroom applications.

Installation in a wide variety of racks, cabinets, enclosures, and front panels is easy due to its straightforward construction and standard interface. The display can be connected directly to the Rockwell A65/40-1000 Single Board Computer (SBC), to Rockwell RM 65-1000E SBC module or RM65-5222E GPIO and Timer module, or other compatible equipment, through an interconnecting cable.

FEATURES

- Intelligent controller
 - Independent operation
 - Centronics type handshake interface
 - Separate character font/program ROM
- 40-character display
 - Vacuum fluorescent
 - Easy-to-read 16-segment digits
 - Clear, bright blue-green color
 - Fast response
 - Long life
- 196 characters
 - Upper case alphabets with lower case notation
 - Numbers
 - Math symbols
 - Special characters
- Variable display parameters
 - Auto-scroll rate
 - Character blinking
 - Character blink rate
 - Cursor blink rate
- Internal editing functions
 - 80-character line buffer
 - Insert/delete character
 - Right/left cursor control
 - Transmit edited line to host
- Display self-test
- +5V operation



A65/40-0400 40-Character Display

FUNCTIONAL DESCRIPTION

The 40-Character Display contains a vacuum fluorescent display, a microprocessor based controller, clock, a 2K-byte character font/program ROM, character and segment drivers, and a DC/DC power converter.

The vacuum fluorescent display is a single sealed unit containing 40 separately controllable digits. Each digit is composed of a 16-segment font which allows a full set of upper case alphabets, numerics, and special characters to be displayed. In the semi-graphics mode, the 16 segments of each digit are individually controlled. In addition, each digit includes a separate decimal point. When energized, the digits form blue-green color characters. The unit comes with a smoked, neutral filter lens cover the display, but other custom lens filters can be used to change the display color to meet unique installation requirements.

The display controller includes an R6504 CPU, RAM, I/O, timer, clock and reset circuitry. The 2K byte ROM contains both the CPU controller instructions and the individual character segment patterns. This ROM can be replaced by another PROM or ROM

to provide a custom character set. The controller performs all communications interfacing, display refreshing, and control functions—enabling the display to operate independently from the host computer.

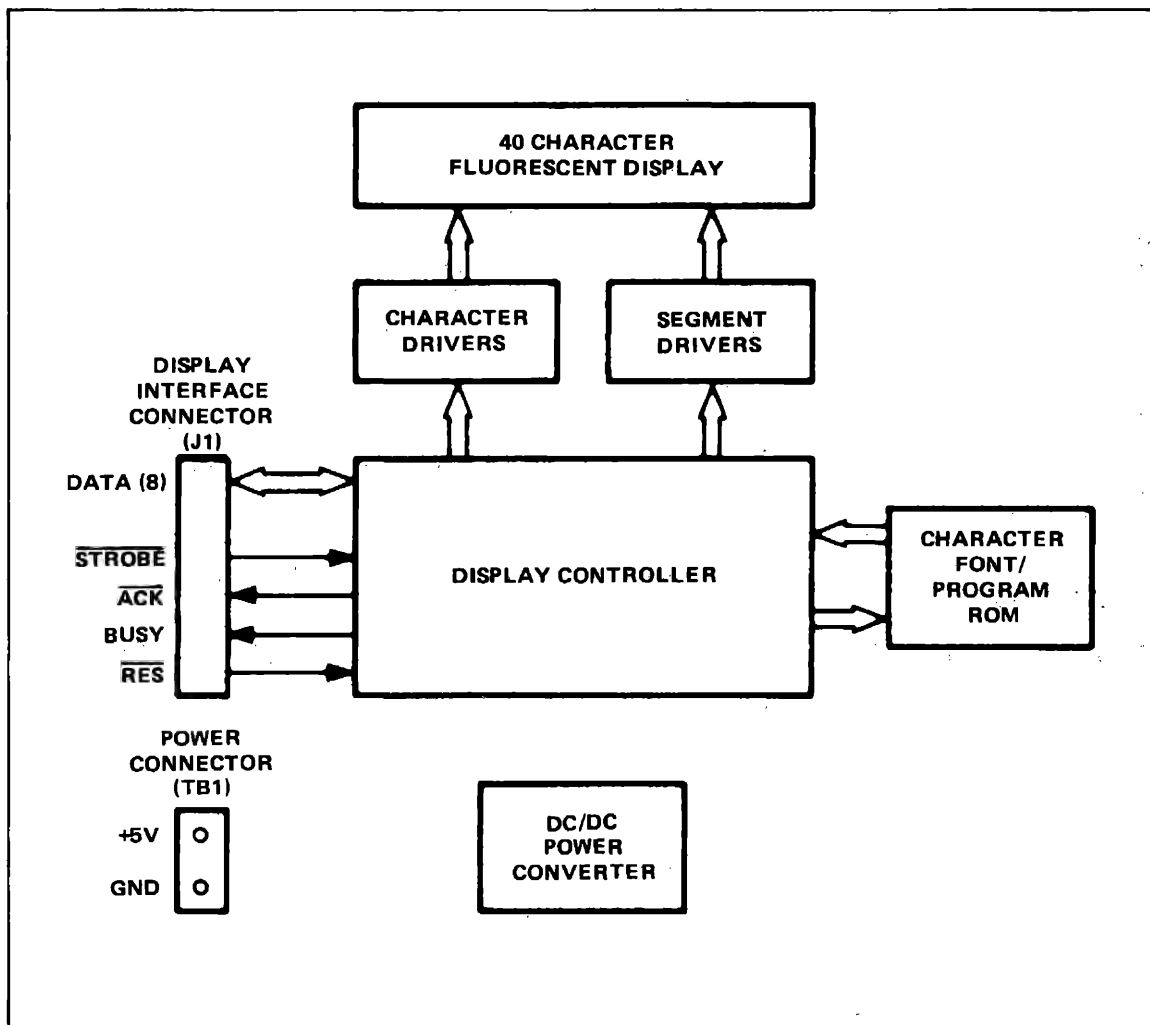
All data and control commands are transmitted to the display over the Centronics-type parallel handshake interface. An internal buffer allows up to 80 characters to be received by the display; the display scrolls after the 40th character is received. There are character editing commands such as insert and delete, as well as transmit buffer, which sends an edited line back to the host computer. There are also display enhancement features such as auto-scroll which allows the display buffer to be continuously circulated, at a selected rate, and blinking characters.

The two-post terminal block provides +5V for the controller and for the on-board DC/DC Converter, which generates the additional voltages required by the fluorescent display. The +5V can, alternatively, be routed through the interface connector.

Display Control Commands

Hex Code	Control Character	Description	Hex Code	Control Character	Description
00	CTRL @	*	10	CTRL P	Pass Through Next Character
01	CTRL A	Clear Line	11	CTRL Q	*
02	CTRL B	Clear to End of Line	12	CTRL R	*
03	CTRL C	Clear Line	13	CTRL S	Toggle Insert Character Mode
04	CTRL D	Clear to End of Line	14	CTRL T	Delete One Character
05	CTRL E	Clear Line	15	CTRL U	*
06	CTRL F	Clear to End of Line	16	CTRL V	*
07	CTRL G	*	17	CTRL W	Display Cursor
08	CTRL H	Backspace (←)	18	CTRL X	Blank Cursor
09	CTRL I	Horizontal Tab (→)	19	CTRL Y	Warm Reset
0A	CTRL J	Warm Reset	1A	CTRL Z	Cold Reset
0B	CTRL K	Warm Reset	1B	CTRL [Escape Command (ESC)
0C	CTRL L	Warm Reset	1C	CTRL \	*
0D	CTRL M	(Home on Line)	1D	CTRL]	*
0E	CTRL N	(Home on Line)	1E	CTRL ^	*
0F	CTRL O	Carriage Return (Home on Line)	1F	CTRL _	*

*Characters with no indicated function are acknowledged, but do not otherwise affect display operation.



40-Character Display Block Diagram

Display Escape Commands

Hex Code	Character Sequence	Function
1B 41	ESC A	Auto-Scroll Display
1B 45	ESC E x y z	Set Environment (1)
1B 47	ESC G	Enter Graphics Mode
1B 49	ESC I	Select/Deselect Display (toggle)
1B 54	ESC T	Perform Self-Test
1B 58 4C	ESC X L	Transmit Line
1B 3D	ESC = x y	Position Cursor (2)
1B 57	ESC W	Set Window Position
1B 58	ESC X	Transmit Display Line

Notes:

(1) Set Environment Sequence:

Hex Code	Character Sequence	Function
41 XX	A (Attribute)	Set Bit-7 Attributes
42 YY ZZ	B (On) (Off)	Set Blinking Character Rate
43 YY ZZ	C (On) (Off)	Set Blinking Cursor Rate
52 XX	R (Rate)	Set Auto-Scroll Rate
53 XX	S (Character)	Set the Cursor Character

(2) The Position Cursor sequence requires two additional characters. The first (y) is ignored. The second (x) becomes the new cursor position.

Connector J1 (Interface) Pin Assignments

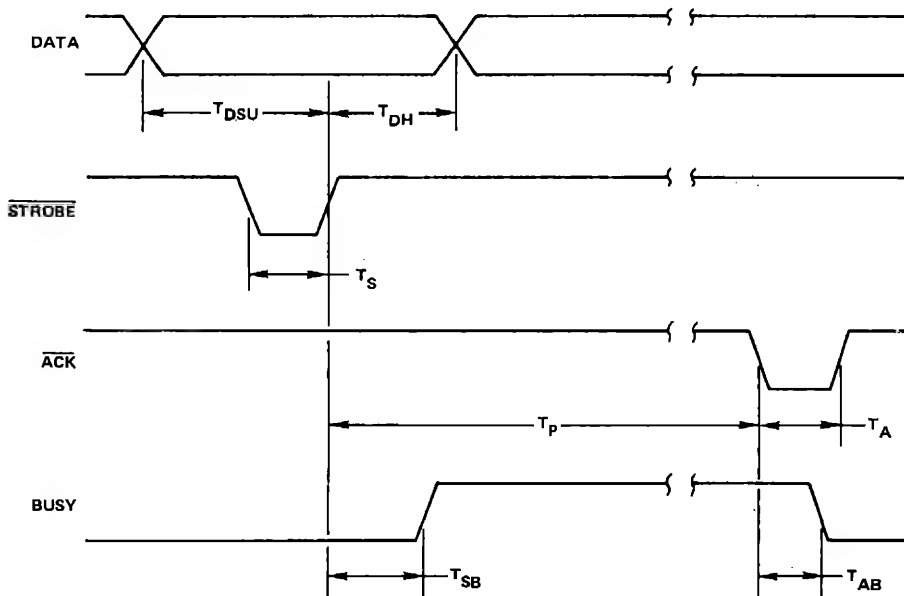
Pin	Signal	I/O	Type	Pin	Signal	Type
1	+5V*		Power	2	NC	—
3	NC		—	4	GND	Power
5	NC		—	6	GND	Power
7	NC		—	8	GND	Power
9	NC		—	10	GND	Power
11	NC		—	12	GND	Power
13	BUSY		TTL	14	GND	Power
15	NC		—	16	GND	Power
17	RES	I	NMOS	18	GND	Power
19	STROBE	I	NMOS	20	GND	Power
21	DATA 7	I	NMOS	22	GND	Power
23	DATA 6	I	NMOS	24	GND	Power
25	DATA 5	I	NMOS	26	GND	Power
27	DATA 4	I	NMOS	28	GND	Power
29	DATA 3	I	NMOS	30	GND	Power
31	DATA 2	I	NMOS	32	GND	Power
33	DATA 1	I	NMOS	34	GND	Power
35	DATA 0	I	NMOS	36	NC	—
37	NC		—	38	NC	—
39	ACK	O	NMOS	40	+5V*	Power

Note: *+5V on pins 1 and 40 can be disconnected by a jumper.

Data Transfer Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{DSU}	Data Set-Up Time	0	—	—	μs
T_{DH}	Data Hold Time	25	—	—	μs
T_S	Strobe Pulse Width Time	50	—	—	ns
T_P	Processing Time	—	500	—	μs
T_A	Acknowledge Width	—	5	—	μs
T_{SB}	Strobe-to-Busy Time	—	14	25	ns
T_{AB}	Acknowledge-to-Busy Time	—	20	40	ns

Note: t_r , t_f = 10 to 30 ns



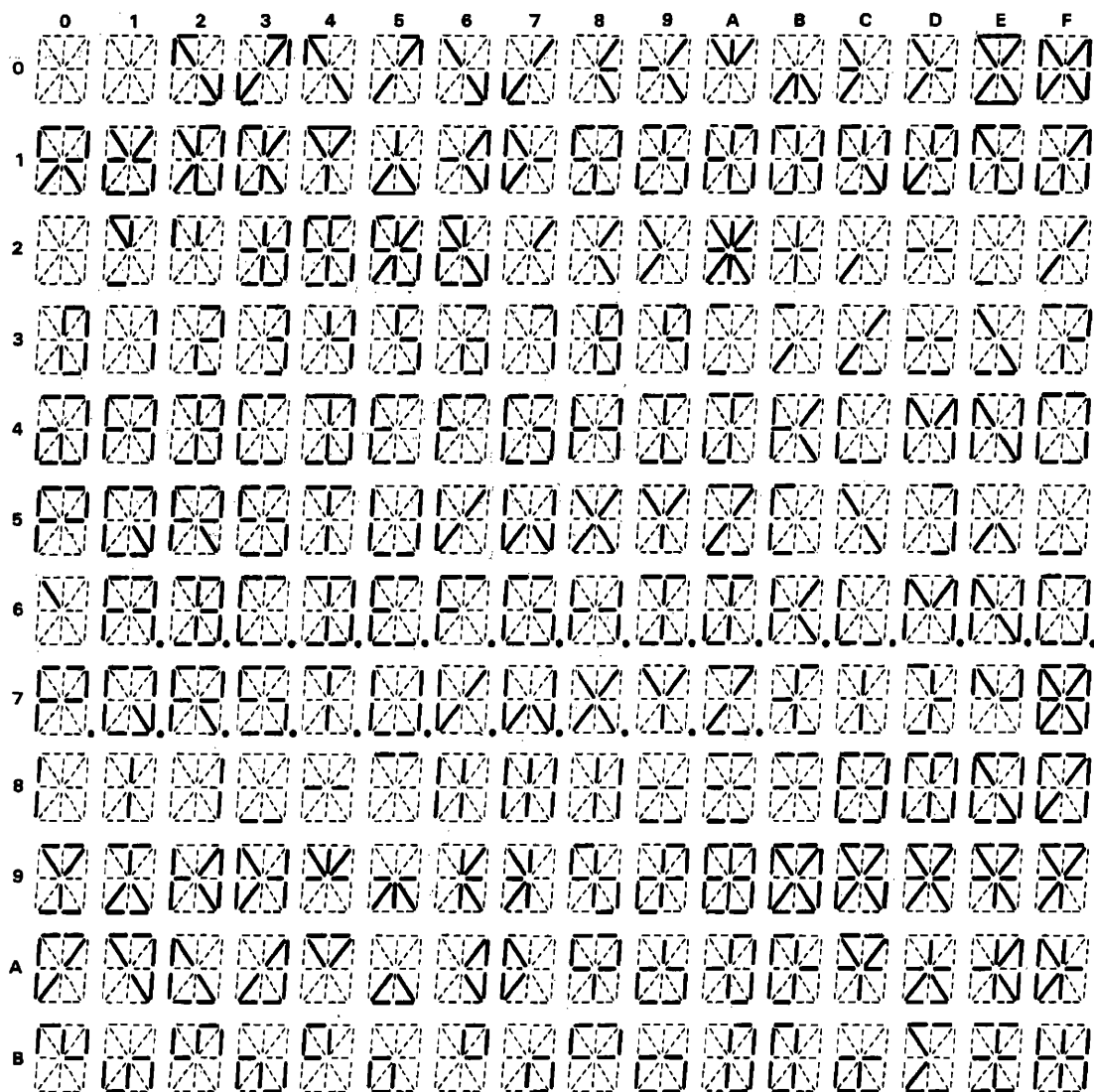
Data Transfer Waveforms

SPECIFICATIONS

Parameter	Value
Dimensions	
Width	11.85 in. (301 mm)
Height*	3.6 in. (91 mm)
Depth*	1.5 in. (38 mm)
Weight	8 oz.
Digit Dimensions	
Height	0.24 in. (6 mm)
Width	0.12 in. (3 mm)
Power Requirements	+5V \pm 5% Regulated, 0.8A (typical), 1.0A (max.)
Environment	
Operating Temperature	0°C to 50°C
Storage Temperature	-55°C to +80°C
Relative Humidity	0% to 95% (without condensation)
Interface Connector	40-pin 3M #3495-1002, or equivalent, connector. Mates with 3M #3418-0000T, or equivalent, ribbon cable connector.
Power Connector	Two-post terminal block
Note: *Dimensions do not include mounting brackets.	

NMOS Interface (Input Voltage = +5.0V, TA = 25°C)

Symbol	Parameter	Min	Max	Unit
V _{IH}	Input High Voltage	2.4	5.0	V
V _{IL}	Input Low Voltage	-0.3	+0.4	V
I _{IH}	Input High Current (V _{IH} = 2.4V)	-100	-300	μ A
I _{IL}	Input Low Current (V _{IL} = 0.4V)	-1.0	-1.6	mA
V _{OH}	Output High Voltage (I _{LOAD} \leq -100A)	2.4	5.0	V
V _{OL}	Output Low Voltage (I _{LOAD} \leq -3 mA)	—	0.4	V
I _{OH}	Output High Current (Sourcing) (V _{OH} \geq 2.4V)	-100	—	μ A
I _{OL}	Output Low Current (Sinking) (V _{OL} \leq 0.4V)	1.6	—	mA



Character Display



A65/40-0600 AIM 65/40 GRAPHICS PRINTER

OVERVIEW

The A65/40-0600 Graphics Printer is one of the hardware options available for the AIM 65/40 Microcomputer Family.

The Graphics Printer is a microprocessor-controlled dot matrix thermal printer, with a 4K byte character font/program ROM, and a paper feed switch. In the test mode, up to 40 characters can be printed using 7 × 8 dot matrix characters. In the graphics mode, all 280 horizontal dot positions on a row are individually controlled, and any number of rows may be printed.

The printer mechanism includes a thermal head, platen, motor, drive linkage and associated wiring. There are 40 thermal elements on the thermal head, each of which spans seven dot fields. Each element is a discrete point which rides against heat sensitive paper. During a print cycle, the thermal head moves horizontally across the paper. Control logic turns on the thermal head drivers to heat the sensitized paper when a dot is to be printed. When an entire row of dots has been printed, the printer motor advances the platen by one horizontal row of dots.

The printer controller includes an R6504 CPU, RAM, I/O, timer, clock and reset circuitry. The 4K byte ROM contains both the CPU instructions and the individual character bit patterns. The ROM is socketed, and can be replaced by a user-supplied PROM or ROM, to provide a custom character set. The con-

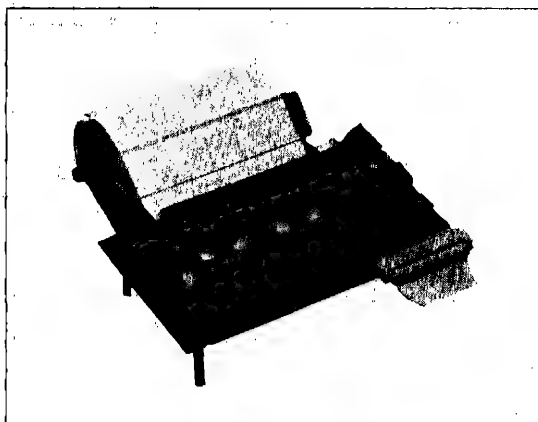
troller performs printer motor and thermal head timing and control functions, to enable the printer to operate independently from the host computer. Further, the controller handles the communications interface, and processes the commands and data to be printed.

Data and control commands are transmitted to the printer over the Centronics type parallel handshake interface. An internal buffer accepts up to 80 characters for printing. The controller automatically prints the first 40 characters in the text mode or after receiving each row of 280 dots in the graphics mode. The paper can also be advanced with a paper feed command, or manually, using the paper feed switch.

A three-post terminal block connects to +5V, +24V and GND. The +5V supplies the control circuitry while the +24V powers the motor and thermal head drivers. On-board potentiometers allow motor speed and dot print intensity to be manually adjusted.

FEATURES

- Intelligent controller
 - Independent operation
 - User command flexibility
 - Centronics type handshake interface
 - Separate character font/program ROM
- 40-column text/semi-graphics
 - 256 character set
 - Upper and lower case alphabets
 - Numbers including superscripts and subscripts
 - Math symbols
 - European and Greek characters
- Full graphics capability
 - 280 dot × n
 - Individual dot control
 - Print complex wave forms and digitized photographs
- Fast—240 lines per minute
- Quiet, thermal operation
- User alterable dot timing
- Printer self-test
- Requires only +5V and +24V



A65/40-0600 Graphics Printer

Printer Control Commands

Hex Code	Character	Description	Hex Code	Character	Description
00	CTRL @	*	10	CTRL P	Pass Through Next Character
01	CTRL A	Clear Line	11	CTRL Q	*
02	CTRL B	Clear to End of Line	12	CTRL R	*
03	CTRL C	Clear Line	13	CTRL S	Toggle Insert Character Mode
04	CTRL D	Clear to End of Line	14	CTRL T	Delete One Character
05	CTRL E	Clear Line	15	CTRL U	*
06	CTRL F	Clear to End of Line	16	CTRL V	*
07	CTRL G	*	17	CTRL W	Turn Cursor On
08	CTRL H	Backspace (←)	18	CTRL X	Turn Cursor Off
09	CTRL I	Horizontal Tab (→)	19	CTRL Y	Cold Reset
0A	CTRL J	Line Feed (↓)	1A	CTRL Z	Warm Reset
0B	CTRL K	Line Feed (↓)	1B	CTRL [Escape Command (ESC)
0C	CTRL L	Form Feed	1C	CTRL /	Print Buffer Without Clear
0D	CTRL M	(Home on Line)	1D	CTRL]	Print Display Image (Window)
0E	CTRL N	(Home on Line)	1E	CTRL ^	Paper Feed
0F	CTRL O	Carriage Return (Home on Line)	1F	CTRL _	*

Note: *These characters are acknowledged, but do not otherwise affect printer operation.

Printer Escape Commands

Hex Code	Character Sequence	Function
1B 3D	ESC = y x	Position Cursor (1)
1B 45	ESC E x	Set Environment (2)
1B 47	ESC G	Enter Graphics Mode
1B 53	ESC S	Transmit Character Definition
1B 54	ESC T	Perform Self-Test

Notes:

(1) The Position Cursor sequence requires two additional characters. The first (y) is ignored. The second (x) becomes the new cursor position.

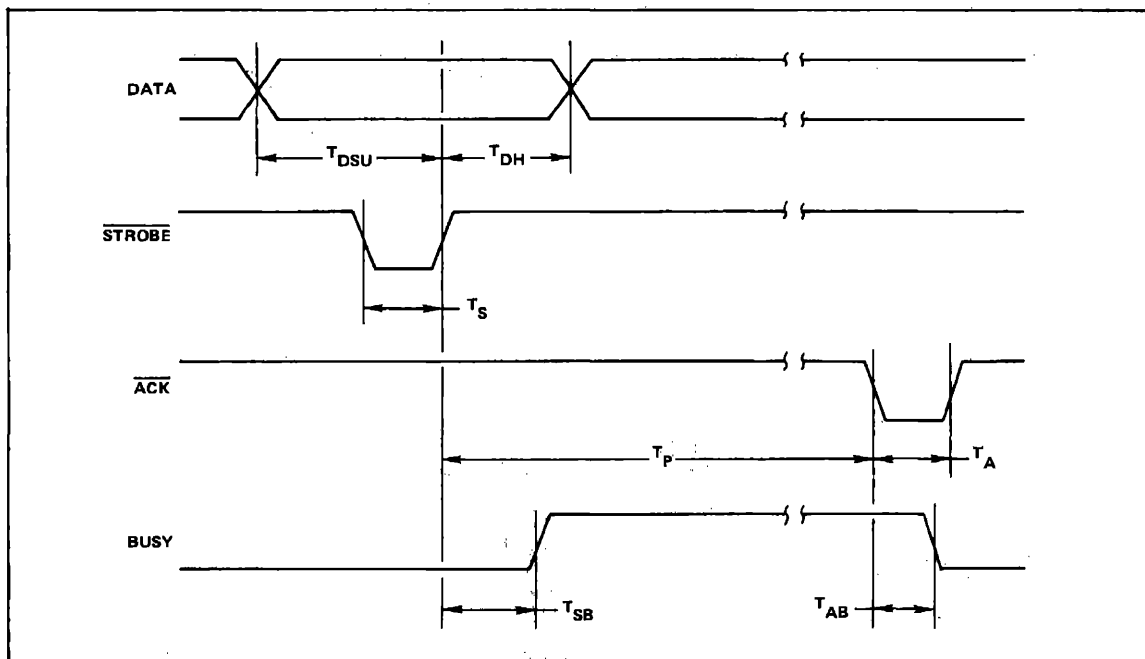
(2) Set Environment Sequence:

Hex Code	Character Sequence	Function
41 XX	A (Attribute)	Set Bit 7 Attributes
47 XX	G (Length)	Set Gap Between Pages
50 XX	P (Length)	Set Page Length
54 XX	T (Time)	Set Dot Print Time

Data Transfer Timing

Symbol	Parameter	Min	Typ	Max	Unit
T_{DSU}	Data Set-up Time	0	—	—	μ S
T_{DH}	Data Hold Time	25	—	—	μ S
T_S	Strobe Pulse Width Time	50	—	—	ns
T_P	Processing Time (non-printing)	0.13	0.15	12	ms
T_P	Processing Time (printing)	0.25	—	0.5	S
T_A	Acknowledge Pulse Width Time	—	5	—	μ S
T_{SB}	Strobe-to-Busy Time	—	14	25	ns
T_{AB}	Acknowledge-to-Busy Time	—	20	40	ns

Note: t_r , t_f = 10 to 30 ns



Data Transfer Waveforms

SPECIFICATIONS

Parameter	Value
Dimensions	
Width	7.6 in. (193 mm)
Length	6.3 in. (160 mm)
Height	3.0 in. (77 mm)
Weight	1.0 lb. (0.45 kg)
Environment	
Operating Temperature	0°C to 50°C
Storage Temperature	0° to 70°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	+5V \pm 5% Regulated, 0.3A (typical); 0.4A (max.); 0.4 (peak) +24V (+3.6V, -2.6V) Unregulated, 2.5A (typical); 4.0A (max.); 6.3" (peak)
Interface Connector	40-pin 3M#3495-1002, or equivalent, receptacle. Mates with 3M #3418-0000T, or equivalent, ribbon cable connector.
Power Connector	3-post terminal block

Note: *+24V peak current specified as worst case with printer duty cycle of 75%. For most cases, a +24V 4A power supply is sufficient.

Connector J4 (System Interface) Pin Assignments

Pin	Signal	I/O	Type	Pin	Signal	Type
1*	+5V		Power	2	NC	—
3	NC		—	4	GND	Power
5	NC		—	6	GND	Power
7	NC		—	8	GND	Power
9	NC		—	10	GND	Power
11	NC		—	12	GND	Power
13	BUSY		TTL	14	GND	Power
15	PAPER FEED	I	—	16	GND	Power
17	RES	I	TTL	18	GND	Power
19	STROBE	I	TTL	20	GND	Power
21	Data 7	I	NMOS	22	GND	Power
23	Data 6	I	NMOS	24	GND	Power
25	Data 5	I	NMOS	26	GND	Power
27	Data 4	I	NMOS	28	GND	Power
29	Data 3	I	NMOS	30	GND	Power
31	Data 2	I	NMOS	32	GND	Power
33	Data 1	I	NMOS	34	GND	Power
35	Data 0	I	NMOS	36	GND	Power
37	NC		—	38	GND	Power
39	ACK	O	NMOS	40*	+5V	Power

Note: *Power on pin 1 and 40 can be disconnected from this connector with on-board jumpers.

[illegible]

Character Set



AIM 65/40-0800 VIDEO DISPLAY CONTROLLER (VDC) MODULE

OVERVIEW

The A65/40-0800 Video Display Controller (VDC) module interfaces the A65/40-1000 Rockwell AIM 65/40 Single Board Computer, RM65-1000 Single Board Computer or RM65-5223 Multi-Function Peripheral Interface module, or any other host computer with an industry compatible Centronics-type parallel interface, to a CRT monitor or TV receiver. The VDC module outputs an NTSC compatible composite video on one connector and separate HSYNC, VSYNC and VIDEO signals at TTL levels on another connector for convenient CRT interfacing.

With its integral microcomputer controller, built-in commands provide selectable and programmable screen formatting, flexible text handling and editing, and full graphics drawing and data display functions. These CRT-oriented functions extend the use of the AIM 65/40 microcomputer into new man-machine applications in the factory, office, laboratory and classroom.

In the text mode, preprogrammed formats of 80 characters \times 24 lines or 40 characters \times 24 lines are selectable. Other formats are user programmable. Eight pages of text are available (in the 80 \times 24 format) with automatic page sizing for other formats. The 4K-byte character generator ROM contains bit patterns for 256 different characters in a 7 \times 10 dot matrix field. Standard characters include upper- and lower-case alphabets, numerals (including subscripts and superscripts), math and Greek symbols, common European letters, and semigraphic characters.

The full graphics mode incorporates bit mapping of 280 \times 224 pixels, which is compatible with the Rockwell AIM 65/40 Graphics Printer (A65/40-0600). Line drawing commands move a pen and draw or erase lines using either relative or absolute position reference. Data byte capability allows individual dots to be controlled using a 40 bytes per dot line format (seven dots per byte). In addition, the entire screen display data can be transmitted to the host computer.



A65/40-0800 VDC Module

FEATURES

- Independent Intelligent Controller
 - 6502 CPU Based
 - Centronics-type Parallel Handshake Interface
 - 4K-byte Program ROM
 - 4K-byte Character ROM
 - 16K-bytes of Refresh RAM
- Flexible Text Mode Operation
 - Selectable 80 or 40 Columns \times 24 Lines
 - Other Screen Formats Programmable
 - Multiple Text Pages
 - Cursor Movement and Positioning
 - Character and Line Editing
 - Line, Page, and Buffer Control
 - Inverse Video on a Character Basis
- 256 Character ROM
 - Upper- and Lower-case Alphabets
 - Numerals Including Subscripts and Superscripts
 - Math Symbols
 - European and Greek Letters
 - Semigraphic Symbols
- Full Graphics Mode
 - 280 \times 224 Pixels Resolution
 - Line Drawing Functions
 - Individual Bit Map Control
 - Transmit Screen to Host
- Two Video Output Formats
 - Separate VIDEO, HSYNC and VSYNC TTL Signals
 - NTSC or European Compatible Composite VIDEO Signal
- Self-Test
- +5V Operation

SELF-TEST

A self-test function tests the microcomputer RAM, calculates and displays the program ROM check-sum, and displays all the characters generated by the Character Generator ROM.

FUNCTIONAL DESCRIPTION

The A65/40-0800 VDC module consists of four major sections:

- Microcomputer Section
- CRT Section
- Oscillator
- DC/DC Power Converter

The microcomputer section consists of a R6502 Central Processing Unit (CPU), R6532 RAM, Input/Output and Timer (RIOT), a 4K-byte R2332 program ROM, address decoder, reset timer and associated support circuitry. The CPU also has major interfaces with the R6545-1 CRT Controller (CRTC) and the refresh RAM (through address multiplexers) in the CRT section. Internal data, address and control bus lines interconnect these devices within the VDC module.

The CPU controls the transfer of data received from the host computer on data lines D0-D7 through the RIOT onto internal data bus lines. If the data is a command, the CPU performs the associated processing and sends appropriate commands to the R6545-1 CRTC. Display data is passed from the CPU onto the refresh RAM for subsequent display as text or graphics.

The 4K-byte Program ROM contains the CPU program instructions which implement the control and escape commands. This ROM can be replaced with a compatible 4K- or 8K-byte PROM/ROM device for custom applications.

The R6532 RIOT supplies the RAM and I/O required for CPU control. Eight of the 16 I/O port lines interface the data I/O lines while two lines service the STROBE and ACK signals at the connector J1 interface. Five other lines (80/40 characters/line, normal/inverse video, display mode, blanking and DISPLAY ENABLE) interface with the CRT section.

The CRT section consists of the R6545-1 CRTC and other logic to generate, combine and output the video signal. The R6545-1 CRTC provides the interface between the CPU and the rest of the CRT section. The CRTC generates refresh RAM addresses and character generator row addresses to allow text or graphics data to be accessed from the refresh RAM for converting to video format.

The CRTC operation is controlled by the contents of 16 internal registers which specify such screen format characteristics as the number of total and displayed horizontal characters, horizontal sync position, VSYNC and HSYNC pulse widths, number of total and displayed vertical rows, and the number of scan lines per character. In addition, the cursor position address and the display start address in the refresh RAM are programmable as are the cursor character start and stop scan lines.

Eight 4116 16K \times 1 dynamic RAM devices comprise the 16K-byte refresh RAM. This RAM is accessed by both the CPU and the CRTC through address multiplexers. Separate address lines from the CPU and from the CRTC are connected to the multiplexers which in turn output the RAM address lines to access the refresh RAM. An additional 16K \times 1 RAM device stores the normal/inverse status for each text character.

During the display trace, the CRT addresses the refresh RAM to output the text characters or graphics data on the RAM data output lines. DATA is retrieved from the RAM at the 1.714 MHz clock rate during 80 column text mode and at 0.857 MHz in the 40 column text mode and in the graphics mode. The data from the RAM is latched for text or graphics output.

In the text mode, the ASCII character codes on the latched refresh RAM data output lines form the character address to the character generator ROM. During text display, the bit patterns corresponding the ASCII characters are output on ROM data lines to the text parallel-to-serial converter which then shifts the data out serially to the video combining circuit.

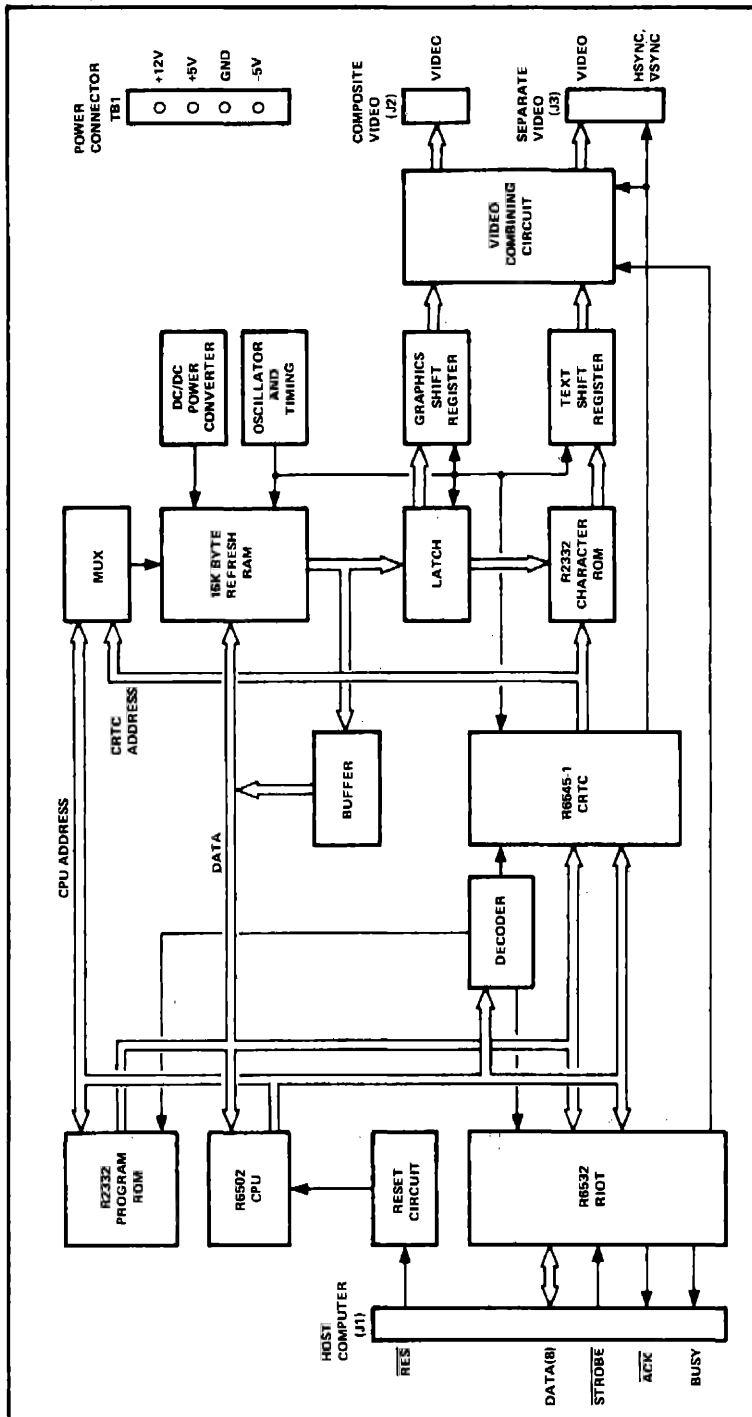
In the graphics mode, each byte in the refresh RAM contains a dot pattern rather than a character ASCII code. The bit patterns on the latched refresh RAM output data are loaded directly into the graphics parallel-to-serial converter which then shifts the data out serially to the video combining circuit.

The selected text or graphics serial data is combined with the CURSOR signal, the BLANK signal and the character INVERSE signal.

This merged video signal is then converted to TTL level and routed to connector J3 as the separate video signal. The VSYNC and HSYNC outputs from the CRTC are routed through drivers to the same connector.

The driven VSYNC and HSYNC signals are nor'ed to produce the combined SYNC signal. The SYNC signal is then combined with the merged video signal, converted to NTSC format and routed to connector J2 as the composite video signal. Trimmer potentiometers allow adjustment of the contrast and brightness levels.

The VDC module operates on +5V provided either from the host computer through connector J1 or from a terminal block (TB1) connection. +12V and -5V are generated on-board by a DC/DC power converter. Optional connections on TB1 also allow +12V and -5V to be provided externally.



A65/40-0800 VDC Module Block Diagram

SPECIFICATIONS

Parameter	Value
Outside Dimensions	
Width	11.85 in. (301 mm)
Height*	4.9 in. (124 mm)
Depth*	0.6 in. (14 mm)
Component Height	0.4 in. (10 mm)
Lead Protrusion	0.1 in. (2.5 mm)
Weight	9.5 oz. (270 g)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	
Internally Generated +12V and -5V	+5V $\pm 5\%$ Regulated—0.85 A (typical); 1.5A (max.)
Externally Supplied +12V and -5V	+5V $\pm 5\%$ Regulated—0.5 A (typical); 1.2A (max.) +12V $\pm 5\%$ Regulated—200 mA (typical); 315 mA (max.) -5V $\pm 5\%$ Regulated—1.4 mA (typical); 1.8 mA (max.)
Interface Connection	
Host Computer	40-pin 3M #3495-1002, or equivalent, connector. Mates with 3M #3417-6040, or equivalent, ribbon cable connector
Separate Video	6-pin right angle connector. Mates with AMP 87159-6, or equivalent, connector (supplied with module)
Composite Video	Single conductor screw-on right angle coaxial connector. Mates with Sealectro 50-024-0000, or equivalent, connector (supplied with module)
Power Connector	Four-post terminal block (+5V, +12V, -5V, and GND)
Note: *Dimensions do not include mounting brackets.	

NMOS Interface (Input Voltage = +5.0V, TA = 25°C)

Symbol	Parameter	Min	Max	Unit
V _{IH}	Input High Voltage	2.4	5.0	V
V _{IL}	Input Low Voltage	-0.3	+0.4	V
I _{IH}	Input High Current (V _{IH} = 2.4V)	100	300	μ A
I _{IL}	Input Low Current (V _{IL} = 0.4V)	-1.0	-1.6	mA
V _{OH}	Output High Voltage (I _{LOAD} \leq -100 μ A)	2.4	5.0	V
	(I _{LOAD} \leq -3 mA)	1.5	5.0	V
V _{OL}	Output Low Voltage (I _{LOAD} \leq 1.6 mA)	0	0.4	V
I _{OH}	Output High Current (Sourcing) (V _{OH} \geq 2.4V)	-100	-1000	μ A
I _{OL}	Output Low Current (Sinking) (V _{OL} \leq 0.4V)	1.6	—	mA

Connector J1 (Interface) Pin Assignments

Pin	Signal	I/O	Type	Pin	Signal	Power
1	+5V*		Power	2	NC	—
3	NC		—	4	GND	Power
5	NC		—	6	GND	Power
7	NC		—	8	GND	Power
9	NC		—	10	GND	Power
11	NC		—	12	GND	Power
13	BUSY	O	TTL	14	GND	Power
15	NC		—	16	GND	Power
17	$\overline{\text{RES}}$	I	NMOS	18	GND	Power
19	STROBE	I	TTL	20	GND	Power
21	DATA 7	I/O	NMOS	22	GND	Power
23	DATA 6	I/O	NMOS	24	GND	Power
25	DATA 5	I/O	NMOS	26	GND	Power
27	DATA 4	I/O	NMOS	28	GND	Power
29	DATA 3	I/O	NMOS	30	GND	Power
31	DATA 2	I/O	NMOS	32	GND	Power
33	DATA 1	I/O	NMOS	34	GND	Power
35	DATA 0	I/O	NMOS	36	NC	—
37	NC		—	38	NC	—
39	ACK	O	NMOS	40	+5V*	Power

Note: *+5V on pins 1 and 40 can be disconnected by a jumper.

Connector J2 (Composite Video) Pin Assignments

Pin	Signal	I/O	Type
Center Shield	Composite Video	O	NTSC
	GND	—	—

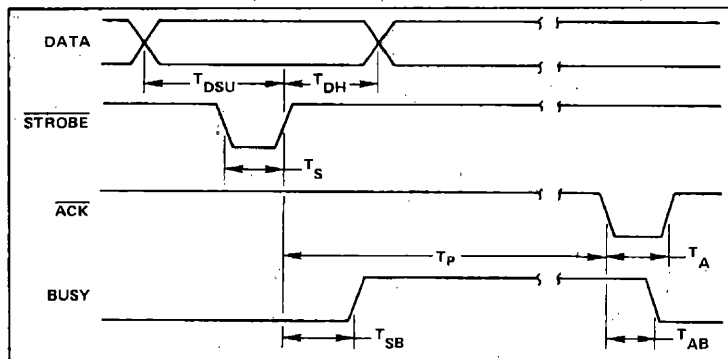
Connector J3 (Separate Video) Pin Assignments

Pin	Signal	I/O	Type
1	Video	O	TTL
2	GND	—	—
3	VSYNC	O	TTL
4	GND	—	—
5	HSYNC	O	TTL
6	GND	—	—

Data Transfer Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{DSU}	Data Set-Up Time	0	—	—	μs
T_{DH}	Data Hold Time	25	—	—	μs
T_S	Strobe Pulse Width Time	50	—	—	ns
T_P	Processing Time	0.1	—	500	ms
T_A	Acknowledge Width	—	5	—	μs
T_{SB}	Strobe-to-Busy Time	—	14	25	ns
T_{AB}	Acknowledge-to-Busy Time	—	20	40	ns

Note: $t_r, t_f = 10$ to 30 ns



Data Transfer Waveforms

Video Display Control Commands

Hex Code	Control Character	Description	Hex Code	Control Character	Description
00	CTRL @	*	10	CTRL P	Pass Through Next Character
01	CTRL A	Clear Line	11	CTRL Q	Next Page
02	CTRL B	Clear to End of Line	12	CTRL R	Previous Page
03	CTRL C	Clear Page	13	CTRL S	Toggle Insert Character Mode
04	CTRL D	Clear to End of Page	14	CTRL T	Delete One Character
05	CTRL E	Clear Buffer	15	CTRL U	Insert One Line
06	CTRL F	Clear to End of Buffer	16	CTRL V	Delete One Line
07	CTRL G	*	17	CTRL W	Display Cursor
08	CTRL H	Cursor Left (Backspace)	18	CTRL X	Blank Cursor
09	CTRL I	Cursor Right (Horizontal Tab)	19	CTRL Y	Cold Reset
0A	CTRL J	Cursor Down (Line Feed)	1A	CTRL Z	Warm Reset
0B	CTRL K	Cursor Up (Vertical Tab)	1B	CTRL [Escape Command (ESC)
0C	CTRL L	Next Page (Form Feed)	1C	CTRL \	Cursor Down (Line Feed)
0D	CTRL M	Home on Line (Carriage Return)	1D	CTRL]	Home Cursor on Last Line
0E	CTRL N	Home on Page	1E	CTRL ^	Cursor Up (Vertical Tab)
0F	CTRL O	Home on Buffer	1F	CTRL _	*

Note: *Characters with no indicated function are acknowledged, but do not otherwise affect display operation.

Video Display Escape Commands

Hex Code	Character Sequence	Function
1B 3D	ESC = Y X	Position Cursor
1B 45	ESC E X Y Z	Set Environment
1B 45 44 XX	ESC E D (Character)	Set Blanking Character
1B 45 45 XX YY	ESC E E (Register) (Value)	Set CRTC Register
1B 45 4D XX	ESC E M (Mode)	Set Display Mode
1B 47	ESC G	Enter Graphics Mode
1B 49	ESC I	Select/Deselect Display
1B 4C 42	ESC L B	Lock Buffer Bottom
1B 4C 54	ESC L T	Lock Buffer Top
1B 52	ESC R	Toggle Reverse Video
1B 54	ESC T	Perform Self Test
1B 55 42	ESC U B	Unlock Buffer Bottom
1B 55 54	ESC U T	Unlock Buffer Top
1B 58 4C	ESC X L	Transmit Line
1B 58 50	ESC X P	Transmit Page
1B 58 42	ESC X B	Transmit Buffer

Video Display Graphics Commands

Control Character	ASCII Code	Function
CTRL A	01	Move Absolute
CTRL C	03	Draw Absolute
CTRL E	05	Erase Absolute
CTRL G	07	Move Relative
CTRL I	09	Draw Relative
CTRL K	0B	Erase Relative
CTRL M	0D	Clear Screen
CTRL O	0F	Home Pen
CTRL Q	11	Dump Graphics Buffer
CTRL S	13	Position Byte Cursor
CTRL U	15	Exit Graphics
CTRL W	17	Send Graphics Byte
CTRL Y	19	*
CTRL [1B	*
CTRL]	1D	*
CTRL _	1F	*

Note: *Characters with no indicated function are acknowledged but do not otherwise affect the display.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
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7																
8																
9																
A																
B																
C																
D																
E																
F																

Character Set



A65/40-7010

AIM 65/40 ASSEMBLER ROM

ASSEMBLY LANGUAGE

An assembler translates microprocessor instructions and data statements written in symbolic form (the source program) into machine executable code (the object program). The AIM 65/40 Assembler translates one instruction, consisting of a label (if required), a mnemonic operation code, an operand (if required) and arithmetic operator (if required) into a machine instruction consisting of from one to three bytes of memory. Constants comprising one or more bytes of memory are generated from data statements while one or more bytes of memory are assigned to variables. The assembler operates in two passes. Pass 1 checks for syntax errors and assigns values to symbols in a symbol table. Pass 2 generates the actual machine code and outputs the assembly listing which lists the source code and the corresponding machine code.

The source code is usually entered and edited using the AIM 65/40 Text Editor then assembled to generate the machine code for program execution and debugging. Program changes to the source program can easily be edited then the program reassembled to generate the new machine code thus eliminating the need for the programmer to code and recode the program in machine code—a time consuming and laborious process.

PRODUCT OVERVIEW

The AIM 65/40 Assembler is a 4K-byte ROM-resident, two-pass symbolic assembler that plugs into socket Z64 on the AIM 65/40 Microcomputer Single Board Computer (SBC) module and operates in conjunction with the AIM 65/40 I/O ROM and the AIM 65/40 Debug Monitor/Text Editor ROMs. The assembler translates computer program instructions written in standard assembly language for the 6502 microprocessor into machine code that will operate in any 6502 or 65XX CPU. Operating options are selected interactively by the operator upon assembly command. These options specify source code device, object code device, symbol table location, full assembly or errors only output listing and output listing device. A repeat command invokes the assembly according to previously commanded options for rapid setup during program debugging, editing and reassembly. Memory to memory assembly is supported to speed program generation. Compatibility with the RM 65 Floppy Disk Controller (FDC) module (RM65-5101NE) and AIM 65/40 DOS 1.0 (A65/40-7090) and AIM 65/40 BDOS 1.0 (A65/40-7092) allows source code to be input from one or more files on a floppy disk and object code to be output to a floppy disk file to assemble very large programs and to permanently save source and object code.

FEATURES

- AIM 65/40 Microcomputer host
- 6502 machine code generation
- ROM-resident for immediate operation
- Symbolic linkage—operands and labels
- Interactive assembler operation setup
- Operator selected input device
 - Memory (text buffer in RAM)
 - Floppy disk
 - Audio tape
 - Serial
 - User defined (interactive and non-interactive)
- Operator selected object code output device
 - Memory (RAM)
 - Floppy disk
 - Audio tape
 - Serial
 - User-defined (interactive and non-interactive)
 - Display/printer
 - Printer
- Operator selected assembly/error listing output device
 - Display/printer
 - Printer
 - Serial
 - User-defined (interactive and non-interactive)
- Assembler directives
- AIM 65/40 DOS 1.0 and BDOS 1.0 compatible

MEMORY MAP

Address (Hex)	Contents
\$9000-\$9FFF	Assembler Program
\$0-\$D6	Assembler Variables

ORDERING INFORMATION

Part No.	Description
A65/40-7010	AIM 65/40 Assembler ROM
Order No.	Description
297	AIM 65/40 Assembler User's Manual ⁽¹⁾
Note:	
(1) Included with A65/40-7010.	

R6502 CPU INSTRUCTIONS

Mnemonic	Instruction	Mnemonic	Instruction
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	AND Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
BCC	Branch on Carry Clear	LSR	Shift Right One Bit (Memory or Accumulator)
BCS	Branch on Carry Set	NOP	No Operation
BEQ	Branch on Result Zero	ORA	OR Memory with Accumulator
BIT	Test Bits in Memory with Accumulator	PHA	Push Accumulator on Stack
BMI	Branch on Result Minus	PHP	Push Processor Status on Stack
BNE	Branch on Result Not Zero	PLA	Pull Accumulator from Stack
BPL	Branch on Result Plus	PLP	Pull Processor Status from Stack
BRK	Force Break	ROL	Rotate One Bit Left (Memory or Accumulator)
BVC	Branch on Overflow Clear	ROR	Rotate One Bit Right (Memory or Accumulator)
BVS	Branch on Overflow Set	RTI	Return from Interrupt
CLC	Clear Carry Flag	RTS	Return from Subroutine
CLD	Clear Decimal Mode	SBC	Subtract Memory from Accumulator with Borrow
CLI	Clear Interrupt Disable Bit	SEC	Set Carry Flag
CLV	Clear Overflow Flag	SED	Set Decimal Mode
CMP	Compare Memory and Accumulator	SEI	Set Interrupt Disable Status
CPX	Compare Memory and Index X	STA	Store Accumulator in Memory
CPY	Compare Memory and Index Y	STX	Store Index X in Memory
DEC	Decrement Memory by One	STY	Store Index Y in Memory
DEX	Decrement Index X by One	TAX	Transfer Accumulator to Index X
DEY	Decrement Index Y by One	TAY	Transfer Accumulator to Index Y
EOR	Exclusive-OR Memory with Accumulator	TSX	Transfer Stack Pointer to Index X
INC	Increment Memory by One	TXA	Transfer Index X to Accumulator
INX	Increment Index X by One	TXS	Transfer Index X to Stack Pointer
INY	Increment Index Y by One	TYA	Transfer Index Y to Accumulator
JMP	Jump to New Location		
JSR	Jump to New Location Saving Return Address		

AIM 65/40 ASSEMBLER DIRECTIVES

Command	Function	Command	Function
=	Equate	.OPT	Listing control option
.BYTE	Byte constant	LIS/NOL	Assembly listing generation
.WORD	Word constant	GEN/NOG	Object code question
.DBYTE	Double-byte constant	ERR/NOE	Error listing generation
.PAG	Page heading	.FILE	Source code file linkage
.SKIP	Skip line(s)	.END	Last statement/first source code file linkage



A65/40-7012 AIM 65/40 MACRO ASSEMBLER & LINKING LOADER

DESCRIPTION

The AIM 65/40 Macro Assembler and Linking loader is a disk-based computer program that generates computer program absolute machine code or relocatable object code and links relocatable object code into absolute machine code. The assembler/loader operates on the AIM 65/40 Microcomputer and generates code for execution by any central processing unit (CPU) in the Rockwell R6500 NMOS microprocessor, R6500/* NMOS one-chip microcomputer and R65C00 CMOS microprocessor device families.

MACRO ASSEMBLER

The macro assembler translates CPU instructions and data statements written in symbolic form (the source program), into absolute or relocatable code. Instructions, consisting of a label (if included), a mnemonic operation code, an operand (if required) and an arithmetic operator (if included), are assembled one-at-a-time into one- to three-byte machine instructions (with absolute or relocatable address information). Constants comprising one or more bytes of memory are generated from data statements while one or more bytes of memory are assigned to variables. The macro capability allows sequences of instructions, to be pre-defined for in-line code inclusion by specifying only the macro name. Conditional assembly allows portions of instruction sequences or macros to be included in (or excluded from) in-line code. The combination of the macro and conditional assembly capability speeds program development by eliminating duplicate coding efforts for similar processing tasks and increases program flexibility and reliability by allowing one source program to generate different computer programs based on specified control parameters.

LINKING LOADER

The linking loader combines independently assembled modules of absolute and/or relocatable object code into a single executable object file. This allows a large program to be developed in manageable size modules and integrated by the linking process. This also allows program changes to be made to one module without affecting any of the other modules—a key requirement in many program validation and certification procedures.

Small programs can still be assembled into absolute executable code without using the linking loader, however, to simplify development.

The assembler/loader operates in conjunction with the AIM 65/40 BDOS 1.0 Upgrade Kit (A65/40-7092).

MACRO ASSEMBLER FEATURES

- Supports three CPU families
 - R6500 NMOS Microprocessor
 - R6500/* NMOS Microcomputer
 - R65C00 CMOS Microprocessor
- Flexible code generation
 - Absolute executable code
 - Relocatable linkable code
- Macro definition includes
 - Multiple parameters
 - Other macros
 - Assembler
- Macro call includes
 - Macro name
 - Argument list
- Condition assembly
 - IF condition
 - ELSE complementary condition
 - 12 conditional operators
- Symbol cross reference table
 - Lists defined and used symbols
 - Alphanumeric order

LINKING LOADER FEATURES

- Resolves inter-module symbol linkage
- Assigns absolute addresses
- Generates absolute executable code
- Produces reports
 - Load map of module locations
 - Symbolic debug table
 - Symbol table
- Interactive or command file setup

ORDERING INFORMATION

Part No.	Description
A65/40-7012	AIM 65/40 Macro Assembler and Linking Loader ⁽¹⁾
Order No.	Description
2153	AIM 65/40 Macro Assembler and Linking Loader User Manual ⁽²⁾
Notes: 1. Requires RM 65 Floppy Disk Controller (FDC) module (RM65-5101NE) and AIM 65/40 BDOS 1.0 Upgrade Kit (A65/40-7092). 2. Included with A65/40-7012.	



A65/40-7020

AIM 65/40 BASIC INTERPRETER ROMS

BASIC LANGUAGE

BASIC is a simple but powerful computer program language. Originally developed at Dartmouth University, BASIC has gained universal acceptance and is commonly used world-wide in schools, industry, and science.

The heart of BASIC is a set of easily learned English words which are used as commands. Complex and powerful statements can be constructed by adding operands and operators to the commands. Equations involving complex formulas and multiple variables can easily be solved. Internal floating point arithmetic handles a wide range of numeric values (2.93873588E-39 to 1.70141183E+38) and provides nine-digit accuracy to most calculations. In addition to addition, subtraction, multiplication and division, a full set of transcendental functions support trigonometric, exponential, square, square root, polynomial and logarithmic operations.

PRODUCT OVERVIEW

The AIM 65/40 BASIC Interpreter, consisting of input formatter, lister, floating point functions, interpreter and input/output functions, is contained in two 4K-byte ROMs that plug into sockets Z70 and Z71 on the AIM 65/40 Microcomputer Single Board Computer (SBC) Module. AIM 65/40 BASIC operates in one of two modes, development and run-time. In the development mode, BASIC statements are entered and executed as either direct or indirect commands. Direct commands are executed upon entry to provide immediate results, however, the statements are not stored for subsequent execution. Indirect commands are entered along with an associated line number and are executed upon RUN command entry. The AIM 65/40 Text Editor can be conveniently used to load indirect statements into the Text Buffer for entry into BASIC to simplify program editing. The AIM 65/40 microcomputer peripherals, i.e., keyboard, 40-character single line display/video display controller module and graphics printer, are used in the development mode to enter statements, to list entered indirect statements and to display/print execution results.

In the run-time mode, BASIC begins execution of the application program (i.e., previously entered indirect statements) without entering the BASIC command level. The AIM 65/40 peripherals are not required in their mode unless used in the application. The AIM 65/40 I/O ROM must be resident (but not the Debug Monitor/Text Editor ROMs) for run-time support. A short user-provided driver program initializes BASIC upon power turn-on or RESET via the AIM 65/40 I/O ROM auto-start linkage.

LANGUAGE FEATURES

- BASIC is easy to learn
- Microsoft BASIC is universally accepted
- BASIC is widely used
- Supports simple and complex statements
- Floating point arithmetic functions
 - Add, subtract, multiply, divide
 - Trigonometric (sine, cosine, tangent, arctangent)
 - Exponential, square, square root
 - Natural logarithm
- String variables and arrays
- Integer variables
- Subroutine calls
- Conditional expressions
- User function

INTERPRETER FEATURES

- AIM 65/40 Microcomputer or RM 65 Single Board Computer (SBC) module host
- ROM resident for immediate operation
- Operates in development and run-time modes
- Fast execution (reference Microsoft 6502 BASIC interpretation)
- Executes application program from RAM or PROM
- Develops programs for execution in either AIM 65 Microcomputer or in RM 65 SBC module based system with AIM 65/40 BASIC ROMs installed.

ORDERING INFORMATION

Part No.	Description
A65/40-7020	AIM 65/40 BASIC ROMs
Order No.	Description
299	AIM 65/40 BASIC User's Manual*
2100	AIM 65/40 BASIC Reference Card*
NOTES:	
*Included with A65/40-7020.	

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MEMORY MAP

Address (Hex)	Contents
\$C000-\$DFFF	AIM 65/40 BASIC Program
\$700-\$7D8	AIM 65/40 BASIC Variables and Vectors
\$0-\$6D	AIM 65/40 BASIC Variables

PROGRAMMING

The application program can easily be programmed into a PROM for operation in an OEM or end-user environment using an RM 65 PROM Programmer module (RM65-2901E) connected to an AIM 65/40 Microcomputer.

The AIM 65/40 BASIC Interpreter ROMs can also be used in an RM 65 environment in either development or run-time mode. When installed in an RM 65 SBC module based system along with the RM 65 I/O ROM, AIM 65/40 peripherals can be used to support development as well as run-time operation.

AIM 65/40 BASIC STATEMENTS

Program Statements	Commands	String Functions
DEF FN	CLEAR	ASC
DIM	CONT	CHR\$
END	FRE	LEFT\$
FOR	LIST	LEN
GOSUB	LOAD	MID\$
GOTO	NEW	RIGHT\$
IF ... GOTO	PEEK	STR\$
IF ... THEN	POKE	VAL
LET	RUN	
NEXT	SAVE	
ON ... GOSUB		Arithmetic Functions
ON ... GOTO		ABS
REM	Input/Output	ATN
RESTORE	DATA	COS
RETURN	GET	EXP
STOP	INPUT	INT
USR	READ	LOG
WAIT	PRINT	RND
	SPC	SIN
	TAB	SGN
	POS	SQR
	FILE*	TAN

*Links to user-defined function.



A65/40-7024 AIM 65/40 BASIC COMPILER

BASIC LANGUAGE

BASIC is a simple but powerful computer program language. Originally developed at Dartmouth University, BASIC has gained universal acceptance and is commonly used world-wide in schools, industry, and science.

The heart of BASIC is a set of easily learned English words which are used as commands. Complex and powerful statements can be constructed by adding operands and operators to the commands. Equations involving complex formulas and multiple variables can easily be solved. Internal floating point arithmetic handles a wide range of numeric values (2.93873588E-39 to 1.70141183E+38) and provides nine-digit accuracy to most calculations. In addition to addition, subtraction, multiplication and division, a full set of transcendental functions support trigonometric, exponential, square, square root, polynomial and logarithmic operations.

PRODUCT OVERVIEW

The AIM 65/40 BASIC Compiler, consisting of the BASIC Compiler and BASIC run-time library, is contained on an AIM 65/40 diskette. The BASIC Compiler, in conjunction with the BASIC run-time library, compiles a program written in the BASIC language into a 6500 assembly language source file and an optimized run-time library file. The BASIC source code file is made up of indirect BASIC commands and statements. The two output files, assembly source file and optimized run-time file, are then assembled using the AIM 65/40 assembler to create a BASIC object code file for execution.

The AIM 65/40 Text Editor can be used to create and edit the application program source code. The AIM 65/40 peripherals, i.e., keyboard, 40-character single line display/video display controller module and graphic printer, are used to enter and list BASIC statements and to display/print execution results.

The disk-based compiler operates on the AIM 65/40 Microcomputer in conjunction with the RM65 Floppy Disk Controller (FDC) module and the AIM 65/40 DOS 1.0 or BDOS 1.0 firmware. The AIM 65/40 Assembler (Part No. A65/40-7010) or the AIM 65/40 Macro Assembler (Part No. A65/40-7012) option is required to support the BASIC Compiler on the AIM 65/40 Microcomputer. The AIM 65/40 I/O ROM must be resident for BASIC I/O support during application program execution, i.e., to run the program after compilation and assembly.

LANGUAGE FEATURES

- BASIC is easy to learn
- Microsoft BASIC is universally accepted
- BASIC is widely used
- Supports simple and complex statements
- Floating point arithmetic functions
 - Add, subtract, multiply, divide
 - Trigonometric (sine, cosine, tangent, arctangent)
 - Exponential, square, square root
 - Natural logarithm
- String variables and arrays
- Integer variables
- Subroutine calls
- Conditional expressions
- User function

COMPILER FEATURES

- AIM 65/40 Microcomputer or RM 65 Single Board Computer (SBC) module host
- Generates standalone code
- Compiles to 6500 assembly language easing optimization
- Fast execution
- Executes application program from RAM or PROM
- Develops programs for execution in either AIM 65 Microcomputer or in RM 65 SBC module based system without AIM 65/40 BASIC ROMs installed.

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ORDERING INFORMATION

Part No.	Description
A65/40-7024	AIM 65/40 BASIC Compiler
Order No.	Description
2160	AIM 65/40 BASIC User's Manual*
2100	AIM 65/40 BASIC Reference Card*
Note: *Included with A65/40-7024.	

MEMORY MAP

Address (Hex)	Contents
\$1000-\$3C00	AIM 65/40 BASIC Compiler
\$0-\$100	AIM 65/40 BASIC Variables

PROGRAMMING

The application program can easily be programmed into a PROM for operation in an OEM or end-user environment using an RM 65 PROM Programmer module (RM65-2901E) connected to an AIM 65/40 Microcomputer.

When used in an RM 65 SBC module based system along with the RM 65 I/O ROM, AIM 65/40 peripherals can be used to support the BASIC Compiler operation.

AIM 65/40 BASIC STATEMENTS

Program Statements	Commands	String Functions
DEF FN	PEEK	ASC
DIM	POKE	CHR\$
END		LEFT\$
FOR	Input/Output	LEN
GOSUB	DATA	MID\$
GOTO	GET	RIGHT\$
IF... GOTO	INPUT	STR\$
IF... THEN	READ	VAL
LET	PRINT	
NEXT	SPC	Arithmetic Functions
ON... GOSUB	TAB	ABS
ON... GOTO	POS	ATN
REM	FILE*	COS
RESTORE		EXP
RETURN		INT
STOP		LOG
USR		RND
WAIT		SIN
		SGN
		SQR
		TAN

*Links to user-defined function.



A65/40-7040 AIM 65/40 MATH PACKAGE ROM

FLOATING POINT ARITHMETIC

Floating point arithmetic is often desired to perform mathematical operations in calculation intensive applications such as scientific computation, industrial data acquisition and reduction, process control, and laboratory measurements. In the AIM 65/40 Math Package, a number is represented in floating point form as an unsigned exponent, a normalized mantissa and an arithmetic sign. The magnitude of the number is equal to two raised to the exponent power times the fractional mantissa, where the exponent may range from -127 to $+127$. The mantissa is a 32-bit number normalized such that the most significant bit (MSB) is always equal to "1". Operating on floating point numbers alleviates programming difficulty and additional development time usually associated with fixed point scaling and minimizes uncertainties when performing calculations involving both very large and very small numbers. Numbers in magnitude from $2.93873588\text{E}-39$ to $1.70141183\text{E}+38$ can be handled in the AIM 65/40 Math Package. In addition, nine digit accuracy is provided in most calculations.

PRODUCT OVERVIEW

The AIM 65/40 Math Package contains a full complement of floating point arithmetic, conversion, trigonometric, utility and other transcendental functions as user-callable subroutines in a 4K-byte ROM. Programmed in 6502 machine language for fast execution, these functions support calculation intensive applications. These functions are host computer independent and may be installed in any 6502 CPU based microcomputer supporting the memory map requirements. The math package is located at \$8000-\$8FFF to allow direct installation in an AIM 65/40 Microcomputer, an RM 65 Single Board Computer (SBC) module or in an RM 65 PROM/ROM module.

In addition to the machine language interface, direct linkage to AIM 65/40 FORTH provides floating point processing in the FORTH language. When installed in an AIM 65/40 Microcomputer with AIM 65/40 FORTH also installed, the floating point words can be automatically linked to the FORTH vocabulary during FORTH initialization. Application programs written in FORTH can thus be both developed and executed on the AIM 65/40 Microcomputer. For OEM or end user installation in an RM 65 system with user-provided input/output functions, such programs can be developed on an AIM 65/40 Microcomputer then transferred to an RM 65 SBC based system with AIM 65/40 FORTH installed for execution in the RM 65 environment.

FEATURES

- Floating point arithmetic
 - Addition and subtraction
 - Multiplication and division
- Integer arithmetic
 - Multiplication
 - Division
- Comparison ($<$, $=$, $>$)
- Trigonometric
 - Sine and cosine
 - Tangent and arctangent
- Conversion
 - Degrees to radians
 - Radians to degrees
- Polynomials
 - Consecutive power
 - Odd power
- Logarithmic
 - Natural log
 - Common log
- Square root, power, exponential
- Absolute value, integer and floating point sign, greatest integer
- 6502 CPU machine instruction linkage
- Host computer independent
- AIM 65/40 FORTH compatible
- 4K-byte ROM based
- Nine digit accuracy
- Wide range ($2.93873588\text{E}-39$ to $1.70141183\text{E}+38$)

ORDERING INFORMATION

Part No.	Description
A65/40-7040	AIM 65/40 Math Package ROM
A65/40-7050	AIM 65/40 FORTH ROMs
Order No.	Description
2113	AIM 65/40 Math Package User's Manual ⁽¹⁾
2103	AIM 65/40 FORTH User's Manual ⁽²⁾
Notes:	
1. Included with A65/40-7040.	
2. Included with A65/40-7050.	

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MEMORY MAP

Address(Hex)	Contents
\$8000-\$8FFF	AIM 65/40 Math Package Program
\$AB-\$C4	AIM 65/40 Math Package Variables
\$110-\$132	AIM 65/40 Math Package Variables

MATH PACKAGE FUNCTIONS

Assembly Language Label	FORTH Word	Function	Assembly Language Label	FORTH Word	Function
INIT		Initialize Math Package	SIN	SIN	Sine
FADDT	F+	Floating Point Add	COS	COS	Cosine
FADD		Floating Point Add (Memory)	TAN	TAN	Tangent
FSUBT	F-	Floating Point Subtract	ARCTAN	ARCTAN	Arc Tangent
FSUB		Floating Point Subtract (Memory)	DEGRE	DEGREES	Convert Radians to Degrees
FMULTT	F*	Floating Point Multiply	RADS	RADIANS	Convert Degrees to Radians
FMULT		Floating Point Multiply (Memory)	POLYX	POLYODD	Odd Exponent Polynomial
FDIVT	F/	Floating Point Divide	POLY	POLY	Consecutive Exponent Polynomial
FDIV		Floating Point Divide (Memory)	MOVFM	M>F	Move Number from Memory to FAC
IMULT		Integer Multiply	MOVMF	F>M	Move Number from FAC to Memory
IDIVID		Integer Divide	MOVFA		Move Number from ARG to FAC
FTOD		Convert Floating Point to Integer	MOVAF		Move Number from FAC to ARG
DTOD		Convert Integer to Floating Point	CONUPK	M>A	Move Number from Memory to ARG
NEGFAC		Negate Floating Point Number		S>A	Move Number from Stack to ARG
ABS	FABS	Absolute Value of Floating Point Number		S>F	Move Number from Stack to FAC
INT	INT	Truncate Floating Point Number		F>S	Move Number from FAC to Stack
SGN	SGN	Sign of FAC to FAC	FIN	FIN	Convert ASCII to Floating Point
SIGN	FSIGN	Sign of FAC to ARG	FOUT	FOUT	Convert Floating Point to ASCII
FCOMP	FCOMP	Compare Floating Point Number	MINLN	MIN-WIDTH	FOUT Minimum Field Width Variable
SQR	SQR	Square Root	DECLN	DEC-LENGTH	FOUT No. of Places to the Right of the Decimal Point Variable
FPWRT	↑	Raise to a Power			
EXP	EXP	Exponential			
LOG10	LOG	Common Log			
LOG	LN	Natural Log			



A65/40-7050 AIM 65/40 FORTH ROMS

FORTH LANGUAGE

FORTH is a unique programming language well suited to a variety of applications. Because it was originally developed for real-time control applications, FORTH is ideal for machine and process control, energy managements, data acquisition, automatic testing, robotics and other applications where assembly language was previously the only possible language choice.

FORTH actually provides the best of two worlds. It has the looping and branching constructs of high-level languages (DO . . . LOOP, BEGIN . . . END, IF . . . THEN and IF . . . ELSE . . . THEN) and the code efficiency of machine and assembly languages. And programmers will be pleased to know that FORTH allows you to specify addresses, operands and data in hexadecimal, octal, binary or any other number base from two to 40—a distinct advantage over languages like BASIC, where all information must be in decimal.

In most time-critical applications, at least part of the program must be written in assembly language. FORTH has a built in 6502 macro assembler, and lets you drop into assembly language at almost any point in your program, without perarate assembly and load steps or awkward machine level linkage. FORTH programs typically run up to ten times faster than other interpretive languages, and can even approach the speed of machine language programs for some applications.

FEATURES

- AIM 65/40 Microcomputer host and target
- RM 65 SBC module based system compatible
- ROM resident for Immediate operation
- Application oriented
- Extensible language
- Over 200 pre-defined functions
- Interactive compilation
- Reverse polish notation
- Compact memory usage
- Fast execution
- Easy debugging
- Stack implementation
- 16-bit words
- Built-in structured macro assembler
- Shortens software development time

PRODUCT OVERVIEW

The AIM 65/40 FORTH system, consisting of primitives, interpreter, macro assembler and input/output functions, is contained in two 4K-byte ROMs. These ROMs plug into sockets Z70 and Z71 on the AIM 65/40 Microcomputer Single Board Computer (SBC) module. Linkage to the AIM 65/40 I/O ROM interfaces FORTH to the AIM 65/40 peripherals (keyboard, single-line display/video display controller and graphics printer) and to user-defined functions. Interface with the AIM 65/40 Debug Monitor and Text Editor ROMs supports machine level debugging and editing of application programs written in FORTH. Both interactive and batch modes of operation are supported. Interaction operation allows FORTH words to be compiled and/or executed as they are entered for immediate debugging and operation. In the batch mode, FORTH words can be entered into the Text Buffer then input to FORTH to be compiled and/or executed. Batch mode allows an application program to be easily edited using Text Editor line- and screen-oriented commands.

The AIM 65/40 FORTH ROMs can also be installed in an RM 65 Single Board Computer (SBC) module based system for either development or runtime operation. This is especially attractive in OEM or end-user applications requiring a compact RM 65 modular computer assembly. The RM 65 I/O ROM, when also installed in this configuration, supports FORTH input/output operation with AIM 65/40 peripherals connected to RM 65 input/output modules. Vectored input/output functions support user-defined interface functions, as well, in an RM 65 installation.

ORDERING INFORMATION

Part No.	Description
A65/40-7050	AIM 65/40 FORTH ROMs
A65/40-7040	AIM 65/40 Math Package ROM
Order No.	Description
2103	AIM 65/40 FORTH User's Manual ⁽¹⁾
2104	AIM 65/40 FORTH Reference Card ⁽¹⁾
2113	AIM 65/40 Math Package User's Manual ⁽²⁾
NOTES:	
1. Included with A65/40-7050.	
2. Included with A65/40-7040.	

DEVELOPING FORTH PROGRAMS

FORTH is built on subroutine-like functions, called "words." These words are linked together to form a "dictionary," which is the central core of the language. Writing a program in FORTH consists of using several predefined words to define each new word. Once the new word has been added to the system dictionary, it becomes as much a part of the language as any other word that has been previously defined. In this way new features and extensions can be added by simply defining one or more new words. Adding new features to conventional languages like BASIC or Pascal requires the language system to be completely reassembled or recompiled.

FORTH is a stack-oriented language, and is programmed in Reverse Polish Notation (RPN), the notation that is used in Hewlett-Packard scientific calculators. Using a data stack is an extremely efficient way of passing variables back and forth between operations. A data stack eliminates the need to tie up memory locations with variable tables, and allows you to use only as much memory as you need.

FORTH programs are developed using "top-down/bottom-up" techniques. That is, the programmer begins by defining the program in very general terms, then systematically breaks these definitions down into more and more detailed sub-modules. When the lowest levels of sub-modules have been defined, he starts coding, in FORTH, at those levels, working back up toward the top of the program, in pyramid fashion. Each sub-module is a stand-alone component of the program, and can be completely debugged without having the complete program in the system. This type of software development is difficult, if not impossible, to do with most other high-level languages.

FLOATING POINT FUNCTIONS

AIM 65/40 FORTH contains both a single- (16-bit) and double- (32-bit) precision integer arithmetic capability. In AIM 65/40 or RM 65 applications where floating point arithmetic is desired, the AIM 65/40 Math Package may be used in conjunction with the FORTH ROMs. These floating point functions may be called using FORTH words included in the math package ROM. When this ROM is installed in socket Z63 on the AIM 65/40 SBC Module, the floating point math words can be automatically linked to the FORTH dictionary during FORTH initialization. The AIM 65/40 Math Package can also be installed in either an RM 65 SBC module based system for operation in the RM 65 environment.

MEMORY MAP

Address (Hex)	Contents
\$C000-\$DFFF	FORTH Program
\$8000-\$8FFF	Math Package Program
\$780-\$7FF	Terminal Input Buffer
\$760-\$77F	User Variables
\$700-\$75F	FORTH User Variables
\$AB-\$C4	Math Package Variables
\$10-\$A8	FORTH Variables

FORTH WORDS

STACK MANIPULATION

DUP	Duplicate top of stack.
2DUP	Duplicate top two stack items.
DROP	Delete top of stack.
2DROP	Delete top two stack items.
SWAP	Exchange top two stack items.
OVER	Copy second item to top.
ROT	Rotate third item on top.
- DUP	Duplicate only if non-zero
>R	Move top item to return stack.
R>	Retrieve item from return stack.
R	Copy top of return stack onto stack.
PICK	Copy the nth item to top.
SP@	Return address of stack position
RP@	Return address of return stack pointer.
BOUNDS	Convert "address count" to "end-address start-address."
.S	Print contents of stack.

DEFINING WORDS

:<name>	Begin colon definition of <name>.
	End colon definition.
VARIABLE <name>	Create a variable <name> with initial value n; returns address when executed.
CONSTANT <name>	Create a constant <name> with value n; returns value when executed.
CODE <name>	Begin definition of assembly-language primitive operation <name>.
:CODE	Used to create a new defining word, with execution-time "code routine" for this data type in assembly.
<BUILDS ... DOES>	Used to create a new defining word, with execution-time routine for this data type in higher-level FORTH.
USER	Create a user variable.

MEMORY

@	Fetch value addressed by top of stack.
!	Store n1 at address n2.
C@	Fetch one byte only.
C!	Store one byte only.
?	Print contents of address.
+	Add second number on stack to contents of address on top.
CMOVE	Move n3 bytes starting at address n1 to area starting at address n2.
FILL	Put byte n3 into n2 bytes starting at address n1.
ERASE	Fill n2 bytes in memory with zeroes, beginning at address n1.
BLANKS	Fill n2 bytes in memory with blanks, beginning at address n1.
TOGGLE	Mask memory with bit pattern.

NUMERIC REPRESENTATION

DECIMAL	Set decimal base.
HEX	Set hexadecimal base.
BASE	Set number base.
DIGIT	Convert ASCII to binary.
0	The number zero.
1	The number one.
2	The number two.
3	The number three.
4	The number four.

FORTH WORDS (CONT'D)

ARITHMETIC AND LOGICAL

+	Add.
D+	Add double-precision numbers.
-	Subtract (n1 - n2)
.	Multiply.
/	Divide (n1/n2).
MOD	Modulo (i.e., remainder from division).
/MOD	Divide, giving remainder and quotient.
-/MOD	Multiply, then divide (n1*n2/n3), with double intermediate.
./	Like -/MOD, but give quotient only.
U.	Unsigned multiply leaving double product.
U/	Unsigned divide.
M*	Signed multiplication leaving double product.
M/	Signed remainder and quotient from double dividend.
M/MOD	Unsigned divide leaving double quotient and remainder from double dividend and single divisor.
MAX	Maximum.
MIN	Minimum.
+ -	Set sign.
D+ -	Set sign of double-precision number.
ABS	Absolute value.
DABS	Absolute value of double-precision number.
NEGATE	Change sign.
DNEGATE	Change sign of double-precision number.
S- >D	Sign extend to double-precision number.
1 +	Increment value on top of stack by 1.
2 +	Increment value on top of stack by 2.
1 -	Decrement value on top of stack by 1.
2 -	Decrement value on top of stack by 2.
AND	Logical AND (bitwise).
OR	Logical OR (bitwise).
XOR	Logical exclusive OR (bitwise).

COMPARISON OPERATORS

<	True if n1 less than n2.
>	True if n1 greater than n2.
=	True if top two numbers are equal.
0<	True if top number negative.
0=	True if top number zero.
U<	True if u1 less than u2.
NOT	Same as 0=.

MISCELLANEOUS AND SYSTEM

(<comment>)	Begin comment (terminate by right parentheses on same line).
CFA	Alter PFA to CFA.
NFA	Alter PFA to NFA.
PFA	Alter NFA to PFA.
LFA	Alter PFA to LFA.
LIMIT	Top of memory.
QUIT	Clear return stack and return to terminal.

CONTROL STRUCTURES

DO ... LOOP	Set up loop, given index range.
DO ... +LOOP	Like DO ... LOOP, but adds stack value to index.
I	Place current index value on stack.
LEAVE	Terminate loop at next LOOP or +LOOP.
BEGIN ... UNTIL	Loop back to BEGIN until true at UNTIL.
BEGIN ... WHILE ... REPEAT	Loop while true at WHILE, REPEAT loops unconditionally to BEGIN.
BEGIN ... AGAIN	Unconditional loop.
IF ... THEN	If top of stack true, execute following clause THEN continue; otherwise continue at THEN.
IF ... ELSE ... THEN	If top of stack true, execute ELSE clause THEN continue; otherwise execute following clause, THEN continue.
END	Alias for UNTIL.
ENDIF	Alias for THEN.

COMPILER-TEXT INTERPRETER

[COMPILE]	Force compilation of IMMEDIATE word.
COMPILE	Compile following <name> into dictionary.
LITERAL	Compile a number into a literal.
DLITERAL	Compile a double-precision number into a literal.
EXECUTE	Execute the definition on top of stack.
[Suspend compilation, enter execution.
]	Resume compilation.

DICTIONARY CONTROL

CREATE	Create a dictionary header.
FORGET	FORGET all definitions from <name> on.
HERE	Returns address of next unused byte in the dictionary.
ALLOT	Leave a gap of n bytes in the dictionary.
TASK	A dictionary marker.
- FIND	Find the address of <name> in the dictionary.
DP	Search dictionary for <name>.
	User variable containing the dictionary pointer.
C,	Store byte into dictionary.
	Compile a number into the dictionary.
PAD	Pointer to temporary buffer.
IMMEDIATE	Force execution when compiling.
INTERPRET	The Text Interpreter executes or compiles.
LATEST	Leave name field address (NFA) of top word in CURRENT.
LIT	Place 16-bit literal on the stack.
CLIT	Place byte literal on the stack.
LITERAL	Compile a 16-bit literal.
SMUDGE	Toggle name SMUDGE bit.
STATE	User variable containing compilation state.

FORTH WORDS (CONT'D)

USER VARIABLES

U?IN	User variable for ?IN.
U?OUT	User variable for ?OUT.
U?TERMINAL	User variable for ?TERMINAL.
U-CR	User variable for -CR.
UABORT	User variable for ABORT.
UB/BUF	User variable for B/BUF.
UB/SCR	User variable for B/SCR.
UC/L	User variable for C/L.
UCLOSE	User variable for CLOSE.
UCR	User variable for CR.
UEMIT	User variable for EMIT.
UFIRST	User variable for FIRST.
UKEY	User variable for KEY.
ULIMIT	User variable for LIMIT.

MONITOR & CASSETTE I/O

COLD	AIM 65/40 FORTH cold start.
MON	Exit to AIM 65/40 Monitor.
CLOSE	Close tape file.
?IN	Set to active input device (AID).
?OUT	Set to active output device (AOD).
GET	Input a character from the AID.
PUT	Output a character to the AOD.
READ	Input n2 characters from AID to address n1.
WRITE	Output n2 characters to AOD at address n1.
SOURCE	Compile from the AID.
FINIS	Terminate compile from SOURCE.

INPUT-OUTPUT

- CR	Output CR to printer only.
CR	Carriage return.
SPACE	Type one space.
SPACES	Type n spaces.
CLRLINE	Output a CTRL B.
"	Print text string (terminated by ").
DUMP	Dump n2 words starting at address.
TYPE	Type string of n1 characters starting at address n2.
?TERMINAL	True if terminal break request present.
KEY	Read key, put ASCII value on stack.
EMIT	Output ASCII value from stack.
EXPECT	Read n1 characters from input to address n2.
WORD	Read one word from input stream, until delimiter.
IN	User variable contained within TIB.
BAUD	Set BAUD rate. (See Note 1)
BL	Output a SPACE character.
C/L	Number of characters/line.
TIB	Pointer to terminal input buffer start address.
QUERY	Input text from terminal.
ID.	Print <name> from name # field address (nfa).
HANG	Wait for keystroke.

OUTPUT FORMATTING

NUMBER	Convert string at address to double-precision number.
<#	Start output string.

OUTPUT FORMATTING (CONT'D)

#	Convert next digit of double-precision number and add character to output string.
#S	Convert all significant digits of double-precision number to output string.
SIGN	Insert sign of n into output string.
#>	Terminate output string (ready for TYPE).
HOLD	Insert ASCII character into output string.
HOL	Hold pointer, user variable.
- TRAILING	Suppress trailing blanks.
.LINE	Display line of text from mass storage.
COUNT	Change length of byte string to type form.
.R	Print number on top of stack.
D.	Print number n1 right justified n2 places.
D.R	Print double-precision number n2 n2.
DPL	Print double-precision number n2 n1 right justified n3 places.
	Number of digits to the right of decimal point.

VOCABULARIES

CONTEXT	Returns address of pointer to CONTEXT vocabulary.
CURRENT	Returns address of pointer to CURRENT vocabulary.
FORTH	Main FORTH vocabulary.
ASSEMBLER	Assembler vocabulary.
DEFINITIONS	Set CURRENT vocabulary to CONTEXT.
VOCABULARY <name>	Create new vocabulary.
VLIST	Print names of all words in CONTEXT vocabulary.
VOC-LINK	Most recently defined vocabulary.

VIRTUAL STORAGE

LOAD	Load mass storage screen (compile or execute).
BLOCK	Read mass storage block to memory address.
B/BUF	System constant giving mass storage block size in bytes.
B/SCR	Number of blocks/editing screen.
BLK	System variable containing current block number.
SCR	System variable containing current screen number.
UPDATE	Mark last buffer accessed as updated.
FLUSH	Write all updated buffers to mass storage.
EMPTY-BUFFERS	Erase all buffers.
+BUF	Increment buffer address.
BUFFER	Fetch next memory buffer.
RW	User read write linkage.
USE	Variable containing address of next buffer.
PREV	Variable containing address of latest buffer.
FIRST	Leaves address of first block buffer.
OFFSET	User variable block offset to mass storage.
- ->	Interpret next screen.
;S	Stop interpretation.

FORTH WORDS (CONT'D)

PRIMITIVES

OBRANCH	Run-time conditional branch.
BRANCH	Run-time unconditional branch.
ENCLOSE	Text scanning primitive used by WORD.
R0	Location of Return Stack.
S0	Location of Parameter Stack.
RP!	Initialize Return Stack.
SP!	Initialize Parameter Stack.
NEXT	The FORTH virtual machine.

SECURITY

ICSP	Store stack position in check stack pointer.
?COMP	Error if not compiling.
?CSP	Check stack position.
?ERROR	Output error message.
?EXEC	Not executing error.
?PAIRS	Conditional not paired error.
?STACK	Stack out of bounds error.
ABORT	Error; operation terminates.
ERROR	Execute error notification and restart system.
MESSAGE	Displays message.
WARNING	Pointer to message routine.
FENCE	Prevents forgetting below this point.
WIDTH	Controls significant characters of <name>.

MATH PACKAGE FORTH WORDS (A65/40-7040)*

FLOATING POINT ARITHMETIC

F+	Adds two floating point numbers.
F-	Subtracts one floating point number from another floating point number.
F*	Multiplies two floating point numbers.
F/	Divides one floating point number by another floating point number.

UTILITY, SIGN AND COMPARISONS

FABS	Takes the absolute value of a floating point number.
INT	Truncates a floating point number to an integer.
SGN	Converts the sign of a floating point number to a floating point number.
FSIGN	Gets a value corresponding to the sign of a floating point number.
FCOMP	Compares the value of a compacted number in memory to a floating point number.

POLYNOMIAL

POLY	Evaluates a polynomial with consecutive exponents.
POLYODD	Evaluates a polynomial with odd exponents.

EXPONENTIAL AND LOGARITHMIC

SQR	Takes the square root of a floating point number.
>	Raises one floating point number to the power of another floating point number.
EXP	Raises the transcendental number e to the power of a floating point number.
LOG	Computes the logarithm to the base 10 (i.e., common log) of a floating point number.
LN	Computes the logarithm to the base e (i.e., natural log) of a floating point number.

USER VARIABLE

MIN-WIDTH	Specifies the minimum field width to be output.
DEC-LENGTH	Specifies the number of places to the right of the decimal point to be output.

ASCII/FLOATING POINT CONVERSIONS

FIN	Converts a number in memory from ASCII to floating point format.
FOUT	Converts a number from floating point to ASCII.

FORMAT CONVERSION AND DATA MOVING

M>F	Unpacks the compacted number in memory to floating point.
F>M	Packs the floating point number to compacted format and stores the result in memory.
M>A	Unpacks the floating point number in memory.
S>A	Converts an integer to floating point format.
S>F	Converts an integer to floating point format.
F>S	Converts a number from floating point to an integer.

TRIGONOMETRIC AND UNITS CONVERSION

SIN	Calculates the sine of a floating point number (in radians).
COS	Calculates the cosine of a floating point number (in radians).
TAN	Calculates the tangent of a floating point number (in radians).
ARCTAN	Calculates the arc tangent of a floating point number.
DEGREES	Converts a floating point number from radians to degrees.
RADIANS	Converts a floating point number from degrees to radians.

*Requires AIM 65/40 FORTH ROMs be resident.



A65/40-7052

AIM 65/40 FORTH TARGET COMPILER

FORTH LANGUAGE

FORTH is a unique programming language well suited to a variety of applications. Originally developed for real-time control applications, FORTH has features that make it ideal for machine and process control, energy management, data acquisition, automatic testing, robotics and other input/output intensive applications where assembly language was previously considered to be the only possible language choice.

FORTH actually provides the best of two worlds. It has the looping and branching constructs of high-level languages (DO ... LOOP, BEGIN ... END, IF ... THEN and IF ... ELSE ... THEN) and the code efficiency of machine and assembly languages. FORTH allows programmers to specify addresses, operands and data in hexadecimal, octal, binary or any other number base from two to 40—a distinct advantage over languages like BASIC, where all information must be in decimal.

FORTH TARGET COMPILER

The FORTH Target Compiler generates object code from application programs written in FORTH. The object code is a compiled composite of the user's application vocabulary and those portions of the Target Compiler nucleus necessary to support the application vocabulary. The disk-based FORTH Target Compiler operates on the AIM 65/40 Microcomputer in conjunction with the AIM 65/40 FORTH Interpreter ROMs, the RM 65 Floppy Disk Controller (FDC) module and the AIM 65/40 BDOS 1.0 Upgrade Kit.

The compiled object code, located at a user-specified origin with optional auto-start vectors, will execute in any 6502 CPU-based microcomputer system supporting the runtime nucleus memory map requirements. Application programs can also be developed to run on AIM 65/40 or RM 65 SBC module-based systems with supporting RM 65 memory and input/output modules, e.g., Analog Input/Output, IEEE-488 Interface, and Multi-function Peripheral Interface. Linkage to RM 65 Floppy Disk Controller, CRT Controller, and IEEE-488 module, as well as the AIM 65/40 I/O and Math Package, firmware can also be included for expanded application systems.

FEATURES

- Fully compatible with FORTH programs developed with AIM 65 or AIM 65/40 FORTH Interpreter ROMs
- Disk-based compiler operation with vocabulary overlays for
 - Text Editing
 - Disk Interfacing
 - Serial Input/Output
 - Compiling
 - Special Utilities
- Easy compiler operation
 - Load screen direction
 - Compile tracing (mapping)
 - Compiles to RAM and/or disk
- Includes 6502 Macro Assembler with
 - Forward references
 - Symbolic labels
 - Relative branches
- Efficient object code generation
 - ROMable object code
 - Standalone operation
 - Minimum runtime nucleus
 - Optimized FORTH compiled vocabulary
 - User-specified origin
- Flexible target computer installation
 - System independent (runs on any 6502 CPU-based system with minimal runtime memory map requirements) or
 - AIM 65/40 or RM 65 I/O ROM autostart capability

ORDERING INFORMATION

Part No.	Description
AIM 65/40-7052	AIM 65/40 FORTH Target Compiler
AIM 65/40-7050	AIM 65/40 FORTH Interpreter ROMs ⁽¹⁾
AIM 65/40-7092	AIM 65/40 BDOS 1.0 Upgrade Kit ^(1,2)
AIM 65/40-7040	AIM 65/40 Math Package ROM ⁽⁶⁾
Order No.	Description
2105	AIM 65 and AIM 65/40 FORTH Target Compiler User's Manual ⁽³⁾
2103	AIM 65/40 FORTH User's Manual ⁽⁴⁾
2113	AIM 65/40 Math Package User's Manual ⁽⁵⁾
Notes:	
(1) Required for FORTH Target Compiler operation.	
(2) Requires RM65-5101NE FDC module.	
(3) Included with A65/40-7052.	
(4) Included with A65/40-7050.	
(5) Included with A65/40-7040.	
(6) Optional	

DEVELOPING FORTH PROGRAMS

FORTH is built on subroutine-like functions, called "words." These words are linked together to form a "dictionary," which is the central core of the language. Writing a program in FORTH consists of using the dictionary words to define each new word. Once the new word has been defined it is added to the system dictionary and it becomes as much a part of the language as any other word that has been previously defined. In this way new features and extensions can be added by simply defining one or more new words.

FORTH is a stack-oriented language, and is programmed in Reverse Polish Notation (RPN), the notation that is used in Hewlett-Packard scientific calculators. A data stack is an extremely efficient way of passing variables back and forth between operations and eliminates the need to tie up memory locations with variable tables.

FORTH programs are developed using "top-down/bottom-up" techniques. That is, the programmer begins by defining the program in very general terms, then systematically breaks these definitions down into more and more detailed sub-modules. When the lowest levels of sub-modules have been defined, FORTH coding begins with those levels, working back up toward the top of the program, in pyramid fashion. Each sub-module is a stand-alone component of the program, and can be debugged without having the complete program in the system. The interactive nature of FORTH supports this time efficient development technique.

In most time-critical applications, at least part of the program must be written in assembly languages. FORTH has a built-in 6502 macro assembler, and allows assembly language coding at almost any point in your program, without separate assembly and load steps or special machine level linkage. FORTH programs typically run up to ten times faster than other interpretive languages, and can even approach the speed of machine language programs for some applications.

The application program is developed, debugged and integrated with the user interface using the ROM-based FORTH Interpreter. After program validation, the application is compiled into stand-alone object code with only required portions of the Target

Nucleus. The compiled byte count will generally be less than the separate application/interpreter byte count.

FORTH TARGET COMPILER OPERATION

The disk-based, two-pass, FORTH Target Compiler compiles object code in one of two modes: BIG.COMPILE or QUICK.COMPILE. The QUICK.COMPILE mode compiles the entire object code directly to RAM then saves the compiled code on disk. The BIG.COMPILE mode compiles to 1K-byte buffer areas in RAM. When the buffer is full, the buffer contents are transferred to disk then compilation continues. The BIG.COMPILE mode optimizes object code RAM requirements although it compiles slower than the QUICK.COMPILE mode.

Operation of the compiler is directed by one or more LOAD SCREENS. This technique provides the user with complete control of compiler variables, origin statements, cold start vectors and utility routines. The LOAD-SCREEN(s) then specify which user screens to compile and in what order.

FLOATING POINT OPERATION

The FORTH Target Compiler provides both single-precision (16-bit) and double-precision (32-bit) single integer arithmetic functions. If floating point arithmetic is desired, code words can easily be defined within the application program to link to external floating point subroutines. The AIM 65/40 Math Package ROM, located at address \$8000-\$8FFF can be installed in the application system. Alternatively, user-defined floating point functions may be linked to or even provided within the code definitions.

SYSTEM REQUIREMENTS

The AIM 65/40 FORTH Target Compiler operates in an AIM 65/40 Microcomputer with 32K bytes RAM in conjunction with an RM 65 FDC module with an AIM 65/40 DOS 1.0 or BDOS 1.0 ROM installed on the FDC module. The following table lists two configurations of AIM 65/40 and RM 65 hardware and firmware which may be used. Other configurations can be easily composed depending on the user's development and application requirements.

Required Peripherals/ Firmware		Host Computer	
		AIM 65/40-2000 (AIM 65/40 SBC Module with 32K RAM, Monitor ROMS, Extended Keyboard, and VDC Module)	A65/40-8315 (AIM 65/40 Microcomputer System — Series 8000)
RM65-7141E	RM 65 Cable Adapter & Buffer Module for AIM 65/40	X	
RM65-7004E	RM 65 4-Slot Card Cage	X	
RM65-5101NE	RM 65 Floppy Disk Controller (FDC) Module (Without ROM)	X	X
A65/40-7090	AIM 65/40 DOS 1.0 ROM, or	X	X
A65/40-7092	AIM 65/40 BDOS 1.0 Upgrade Kit	X	X
A65-40-7040	AIM 65/40 Math Package ROM	optional	optional
A65/40-7050	AIM 65/40 FORTH ROMs	X	X
	Floppy Disk Drives (2)	X	X
	CRT Monitor	X	X

Notes: X = Required in addition to host microcomputer.

FORTH WORDS

GENERAL PURPOSE VOCABULARY

The following FORTH words are provided in addition to those provided in the A65/40-7050 FORTH Interpreter ROMs (refer to Data Sheet No. D122).

ABORT"	Prints TEXT if a run-time error occurs.
ASCII	During compile time, places a CLIT and the literal value of CHAR in the dictionary. In immediate mode, returns the ASCII value on the stack.
COMBINE	Combines low byte of l and high byte of h to form n.
COMPILING	Activates the Compiler Vocabulary Overlay.
DISKING	Activates the Disk Vocabulary Overlay.
EDITOR	Activates the Editor Overlay.
EXTERNAL	Execution only. NFA of next word to be defined.
FALSE	Returns a false flag.
H.	Prints n as an unsigned hexadecimal value.
HI	Returns the high byte of n.
IFEND	Marks a place.
IFTRUE	Compiles the following input if f=1, otherwise skips.
INTERNAL	Returns the NFA of the latest word defined.
LO	Returns the low byte of n.
LOADER	Creates word NAME that loads screen no. n.
MODULE	Execution only. Places NFA1 into LFA of NFA2.
OFF	Stores a 0 in ADDR.
ON	Stores a 1 in ADDR.
ROLL	Rotates the nth number to the top of the stack.
ROOM	n = RAM space left.
SET	Places value n in variable or constant NAME.
SPLIT	Returns low and high byte of n.
THRU	Performs sequential LOAD's beginning at screen no. n and continuing through screen no. n.
TRUE	Returns a true flag.
U.	Outputs n as a double-precision number.
UNRAVEL	Back traces the return stack.
Y/N?	Asks the question YES? or NO?, depending on $f_1 = 1$ or 0. Returns f_2 as true or false depending on input match to f_1 .
2ROT	Rotates double-precision numbers d_1 , d_2 , d_3 .
2*	Returns $d_3 = d_1 * d_2$.

2OVER	Double-precision OVER.
2SWAP	Double-precision SWAP.
==	Execution only. Creates a constant NAME with value n.
-TEXT	Compares strings at ADDR1 and ADDR2 for n bytes. Returns f=1 if same.
?DEF	IF NAME is defined, returns f=1.
?RANGE	Returns f=1 if $n2 < n1 < n3$ for signed numbers.
?URANGE	Returns f=1 if $u2 < u1 < u3$ for unsigned numbers.

DISK VOCABULARY OVERLAY

BACKUP	Copies all of drive 0 to drive 1.
BLOCKS	Copies block b1 through b1+n to block b2 through b2+n.
COPY	Copies block b1 to block b2.
DOWN	Beginning at block b and continuing for n blocks, copies from drive 1 to drive 0.
MASSACRE	Clears n blocks beginning at block b, DR0.
SCREENS	Copies screens S1 through S1+n to screens S2 through S2+n.
SLATE	WRITES blanks (\$20) to block b relative to DRIVE 0.
SWEEP	READS blocks b through b+n searching for disk errors.
UP	Beginning at block b, copies n blocks from drive 0 to drive 1.
VERIFY	Compares blocks beginning at b1 to those beginning at b2 for n blocks and displays errors.
VOLUME	Returns the block number of the block 0 of drive 2 relative to drive 0.
?WRONG	If $b1 = b2$, then sets f=1, else sets f=0.

FORTH WORDS (Continued)

EDITOR VOCABULARY OVERLAY

BUFFERS

INSERT-BUF An 80-byte buffer beginning at PAD + 80.

FIND-BUF An 80-byte buffer beginning at PAD + 160.

LINE ORIENTED COMMANDS:

K Swaps the contents of the INSERT-BUF and FIND-BUF.

LINE On current screen, returns the RAM address of the beginning of the line#.

M Replaces INSERT-BUF and line# in block# with current referenced line.

NEW Beginning at line#, clears each line and allows a NEW line to be typed in. Input is terminated by a null line entry (CR CR). Clears remaining lines on the current screen.

P Copies text into the INSERT-BUF and the current line until the delimiter (CR) is encountered.

TILL Beginning at the current cursor address, deletes text UNTILL the end of the matching text string is encountered. The text is held in FIND-BUF.

T Moves cursor to beginning of line# in current screen. Shows the line.

U Copies text into the INSERT-BUF and the line on the current screen under the cursor.

X Copies the current line into INSERT-BUF. Then deletes the line and scrolls the screen up. The last line becomes a blank.

>LINE# Returns the current cursor line#.

(DELETE) Referring to the current cursor position, deletes n preceding characters and calls UPDATE.

(HOLD) Copies the referenced line number into INSERT-BUF and UPDATE.

(KILL) Blanks line# and UPDATE.

(PUT) Replaces the current line with contents of INSERT-BUF.

? Prints the current line with the cursor at current cursor position and the line number at the end of the line.

1LINE Searches the current line after cursor position for a match to contents of FIND-BUF. Repositions cursor to it if a match is found and sets f=1. If no match is found, sets f=0 and positions the cursor to the next line.

STRING ORIENTED COMMANDS:

D Finds the text, deletes it and shows the line.

F Finds the text, positions the cursor at the end of the text string and shows the line.

I Inserts the contents of INSERT-BUF into line at cursor position.

MATCH Searches the memory space beginning at ADDR2 for CNT2 for a match of the data beginning at ADDR1 for CNT1. If no match is found, sets f=1 and ADDR3=ADDR1 + CNT1. If a match is found, sets f=0 and ADDR3=address of the next byte after the matching string.

(F) Locates the text in the buffer (a subpart of the F command).

#LAG Returns the address of the character following the cursor and then counts to the end of the line.

#LEAD Returns the address of the character preceding the cursor and the count to the beginning of the line.

SCREEN COMMANDS

B Moves to last block.

L Lists current screen.

N Moves to next block.

TOP Moves cursor to the top line of the text.

WIFE Clears the entire screen.

MISCELLANEOUS COMMANDS

BUF-MOVE Move non-null contents of PAD to ADDR.

E Erases the string in front of the cursor for a length equal to the string in FIND-BUFF.

R Replaces string identified by FIND-BUFF with TEXT.

S Beginning at current screen and continuing through screen #n, searches for a string match to TEXT and displays match occurrences.

CURSOR COMMANDS

R# Returns the cursor position (n).

#LOCATE Returns byte position of cursor and line number.

>> Adds n to cursor position and displays the line.

FORTH WORDS (Continued)

TEXT	Takes text from input stream until DLimit character is encountered (65 characters maximum). Moves text to PAD and fills to 65 characters with blanks (\$20).
USE	Displays CHAR as the cursor.
WHERE	Displays where an error in LOADING occurred. Also shows context and current.

ORIGIN	Compiler's target dictionary.
FAST.COMPILE	Target space will be RAM only, based on WINDOW.LO and WINDOW.HI.
BIG.COMPILE	Target space maybe virtual data space on disk.
CLEAR.TARGET	Fills the target area with zeros.
READY	Initializes internal variables to their default value.
START	Begins the compilation. Everything following this command will be interpreted or compiled in the simulated target machine environment.

TARGET COMPILER VOCABULARY OVERLAY

LISTS

SYMBOLS	Defines names in the object code.
LOCALS	Defines words at compile time only.

MAGICS	Immediate words.
--------	------------------

SWITCHES & FLAG WORDS (directives active during compile)

ON	Changes switch state to ON.
OFF	Changes switch state to OFF.
MAPPING	Prints or displays the name and CFA of each WORD when created.
GAG	Suppresses most non-fatal error messages.

AUTO.FORWARD	Automatic forward reference for undefined words.
--------------	--------------------------------------------------

NUMERIC	Values must be preceded by a valid decimal character to be a valid number.
---------	----------------------------------------------------------------------------

ROMABLE	Generates read-only code.
---------	---------------------------

CONTROL WORDS

FORWARD	Forces forward reference of the name immediately following.
WIDE	Name field length (headerless code).
SET	Changes the value of FORTH user constants.
WINDOW.LO WINDOW.HI	Defines the Target address space boundaries.
DESTINATION	Defines the target buffer block number.
RAM.LO } RAM.HI }	Identifies nucleus RAM boundaries. Extends from RAM.LO for USER.SIZE bytes.
USER.SIZE	Number of bytes reserved beginning at RAM.LO. RAM between RAM.LO + USER.SIZE and RAM.HI is used for work buffers (PAD, etc.) when ROMABLE flag is set.

DEFINING WORDS

= =	Generates an equate type statement.
LABEL	For use in assembly language to provide flexibility and allow code sharing.
VARIABLE	If ROMABLE is true, VARIABLE becomes a USER variable, otherwise variable is identical to ROM-based FORTH.
BYTES	Sets aside bytes in RAM area (like ALLOT).
RAM	Equivalent to ROM command HERE. Returns current RAM address.
BCC, BCS, BNE, BEQ, BPL, BMI, BVC, BVS,	Relative branch opcodes for assembly operation.

MAGIC WORDS

DLITERAL	Compiles a double number in line.
ASCII	Compiles CLIT of following ASCII character.
DOES>	Immediate word to separate <BUILDS DOES> into TARGET NUCLEUS and Target Compiler.
;CODE	Identical to CODE but also sets a pointer for LOCATE.
LOCATE	Informs the compiler where the execution time CODE is located.
REVEAL	Similar to SMUDGE.
HIDE	Sets the SMUDGE bit on the last target word.



A65/40-7090

AIM 65/40 DISK OPERATING SYSTEM VERSION 1.0 (DOS 1.0) ROM

DISK OPERATING SYSTEM

A disk operating system (DOS) provides a standard interface between the user and one or more floppy disk drives, floppy disk control (FDC) hardware and executive level software. The DOS, implemented in software, allows program and data files to be opened, closed, read and written under operator or program control. In an interactive environment, commands are usually initiated by the operator from the keyboard in response to user friendly prompts displayed by the system.

PRODUCT OVERVIEW

The AIM 65/40 Disk Operating System Version 1.0 (DOS 1.0) provides disk and file management functions for the AIM 65/40 Microcomputer in conjunction with an RM 65 Floppy Disk Controller (FDC) module. With this configuration, mass storage files can be easily manipulated when connected to one to four 5¼" or 8" floppy disk drives. DOS 1.0 functions, contained on a 4K-byte ROM that plugs into the FDC module, are available immediately upon computer power turn-on without waiting for separate loading of a disk-based DOS into RAM.

DOS 1.0 functions are operator commandable through interactive AIM 65/40 Debug Monitor/Text Editor operation as well as language (assembler, compiler and/or interpreter) operation. Text and program source code may be written to, and read from, disk with the Editor List and Read commands, respectively. Binary data and program object code may be written to, and loaded from, disk using the Debug Monitor Dump and Load commands, respectively. Files containing source and object code for application programs written in AIM 65/40 Assembler, BASIC, and FORTH languages are therefore supported. In addition, utility functions format a disk, list the contents of the disk directory, delete a file, recover a file and backup a disk upon command. The DOS functions may also be called under program control by the application program into order to read and write data files.

Disk read or write errors, both at the DOS and FDC hardware level, are reported upon detection. User-alterable variables allow changing of default values to application unique values.

Disks formatted by AIM 65/40 DOS 1.0 are compatible with AIM 65 DOS 1.0 and AIM 65/40 BDOS 1.0. Files written by any of these DOS programs may therefore be read by either microcomputer.

FEATURES

- AIM 65/40 Microcomputer compatible
- ROM resident for immediate operation
- Installs on-board RM 65 Floppy Disk Controller (FDC) module
- Provides mass storage of programs and data
- Compatible with AIM 65 high level language and Assembler ROMs
- Disk oriented commands (format, list, backup)
- File oriented commands (list, delete, recover)
- Input/Output commands
 - Read and write text and object code
 - Automatic file open and close
- User-alterable variables
 - Utility function and error handling vectors (before and after DOS functions)
 - Error handling vectors (before and after DOS functions)
 - Input/output vectors
- Extensive error detection and reporting

MEMORY MAP

Address (Hex)	Contents
\$8F00-\$8FFF	RM 65 FDC Module I/O
\$8000-\$8EFF	DOS 1.0 Program
\$3E00-\$3FFF	DOS 1.0 I/O Buffer (default location)
\$500-\$563	DOS 1.0 Variables
\$4A0-\$4FA	DOS 1.0 Variables
\$D7-\$DE	DOS 1.0 Variables

ORDERING INFORMATION

Part No.	Description
A65/40-7090 RM65-5101NE	AIM 65/40 DOS 1.0 ROM RM 65 FDC Module (without ROM containing primitive subroutines ⁽²⁾)
Order No.	Description
802	RM 65 FDC Module User's Manual ⁽¹⁾

NOTES:

1. Describes user's instructions for AIM 65/40 DOS 1.0. Included with A65/40-7090 and RM65-5101NE.
2. The DOS 1.0 ROM includes primitive subroutines in addition to DOS functions.



A65/40-7092

AIM 65/40 BOOTSTRAP DISK OPERATING SYSTEM VERSION 1.0 UPGRADE KIT

DISK OPERATING SYSTEM

A disk operating system (DOS) provides a standard interface between the user and one or more floppy disk drives, floppy disk control (FDC) hardware and executive level software. The DOS, implemented in software, allows program and data files to be opened, closed, read and written under operator or program control. In an interactive environment, commands are usually initiated by the operator from the keyboard in response to user friendly prompts displayed by the system.

PRODUCT OVERVIEW

The AIM 65/40 Bootstrap Disk Operating System Version 1.0 (BDOS 1.0) provides disk and file management functions for the AIM 65/40 Microcomputer in conjunction with an RM 65 Floppy Disk Controller (FDC) module. With this configuration, mass storage files can be easily manipulated when connected to one to four 5¼" or 8" floppy disk drives. BDOS 1.0 functions, contained on a 4K-byte ROM that plugs into the FDC module, are available immediately upon computer power turn-on without waiting for separate loading of a disk-based DOS into RAM.

The AIM 65/40 BDOS 1.0 provides a bootstrap and autostart capability in addition to the same functions as AIM 65/40 DOS 1.0 (A65/40-7090). It is also located higher in memory than AIM 65/40 DOS 1.0 to allocate RAM at \$8XXX to disk-resident system or application software. If neither AIM 65/40 Debug Monitor nor BASIC Interpreter ROMs are installed, a bootstrap function can be read from the disk and executed to load and autostart an application program. The BASIC or Debug Monitor command level will be entered if the AIM 65/40 BASIC or Debug Monitor ROMs are installed (BASIC overrides the Debug Monitor) unless overridden by an application autostart via the AIM 65/40 I/O ROM. AIM 65 BDOS 1.0 does not contain DMA routines, however, indirect vectors are provided for user addition.

Disks formatted by AIM 65/40 BDOS 1.0 are compatible with AIM 65 DOS 1.0 and AIM 65/40 DOS 1.0. Files written by any of these DOS programs may therefore be read by either microcomputer.

The upgrade kit includes:

For installation on RM 65 FDC Module

AIM 65/40 BDOS 1.0 ROM
FDC Module addressing PLA (495R23-003)

For installation on the AIM65/40 SBC Module

AIM 65/40 I/O ROM V1.1 (R32T3-14)
AIM 65/40 Monitor/Editor ROMs V1.1
(R32U5-13 and R32U6-13)

FEATURES

- AIM 65/40 Microcomputer compatible
- ROM resident for immediate operation
- Installs on-board RM 65 Floppy Disk Controller (FDC) module
- Provides mass storage of programs and data
- Compatible with AIM 65 high level language and Assembler ROMs
- Disk oriented commands (format, list, backup)
- File oriented commands (list, delete, recover)
- Input/Output commands
 - Read and write text and object code
 - Automatic file open and close
- User-alterable variables
 - Utility function and error handling vectors (before and after DOS functions)
 - Input/output vectors
 - I/O buffer vectors
- Extensive error detection and reporting

MEMORY MAP

Address (Hex)	Contents
\$E000-\$EFFF	DOS 1.0 Program
TOP OF RAM	DOS 1.0 I/O Buffer
\$500-\$563	DOS 1.0 Variables
\$4A0-\$4FA	DOS 1.0 Variables
\$D7-\$DE	DOS 1.0 Variables

ORDERING INFORMATION

Part No.	Description
A65/40-7092	AIM 65/40 BDOS 1.0 Upgrade Kit
RM65-5101NE	RM 65 FDC Module (without ROM containing primitive subroutines ⁽¹⁾)
Order No.	Description
2152	AIM 65/40 BDOS, 1.0 User's Manual ⁽²⁾
288	AIM 65 Monitor/Editor Program Listing
280	AIM 65/40 System User's Manual
262	AIM 65/40 I/O ROM Program Listing
Notes:	
1. BDOS 1.0 ROM in upgrade kit includes primitive subroutines in addition to DOS functions.	
2. Included with A65/40-7092	

SECTION 9

RM 65 MICROCOMPUTER MODULE FAMILY

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RM 65 MICROCOMPUTER MODULE FAMILY

Standard Boards Cut Design Costs, Offer Flexibility

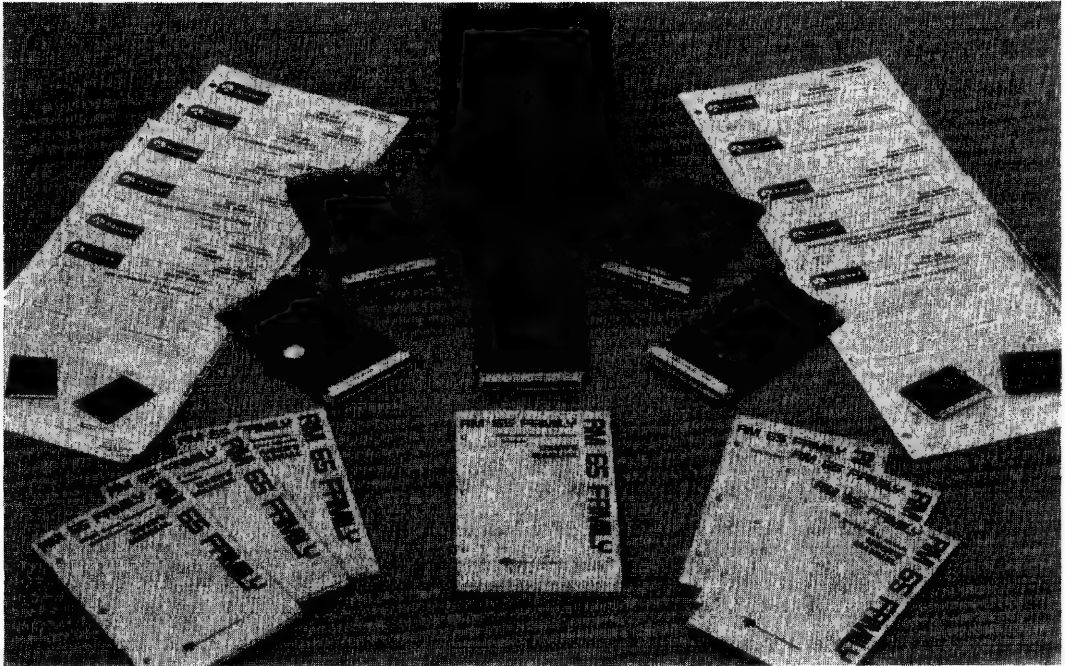
RM 65 microcomputer modules offer a simple solution to designing hard working blue collar microcomputer systems. You start with an R6502 based single board Eurocard-sized computer. Then you add functions, exactly as required, with additional Eurocards. Program your system in either FORTH or BASIC, control essentially any peripherals the system may need. There's no more optimum way to quickly and economically put together prototype and small to medium run systems.

The RM 65 family includes a single board computer, memory, general purpose I/O, intelligent peripheral controllers and accessory modules. Silicon software supports the family with BASIC, FORTH and peripheral drivers. Plus, the family includes card cages, buffers, adapters, cabling, extender module, everything needed for complete system implementation.

The RM 65 microcomputer modules are all Eurocard sized, 100 mm x 160 mm. Memory modules include 8K static RAM, 32K dynamic RAM, 16K PROM/ROM and a PROM programmer. ROMs include I/O, BASIC and FORTH. There is an IEEE-488 module, general purpose I/O and timer module, ACIA module, and a multifunction peripheral controller module.

An analog input/output module allows an RM 65 system to interface with thermocouples, strain gages, pressure sensors and similar analog devices. Floppy disk and CRT controller modules allow RM 65 systems to drive displays and removable memory. A direct memory access controller allows RM 65 systems to have high data transfer rates when needed.

Since the RM 65 blue collar family is designed around the R6500 family, systems can be readily redesigned into R6500 devices as volume or application warrant. RM 65 lets you design custom systems with standard boards, buying only what you need, when you need it.





RM65-1000E RM65 SINGLE BOARD COMPUTER (SBC) MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-1000E Single Board Computer Module is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Modules are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 Microcomputer Modules use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desk-top microcomputer applications.

PRODUCT OVERVIEW

The RM65-1000E Single Board Computer (SBC) Module allows users to design their products into compact modular stacks. The SBC module plugs into a single slot in an RM 65 card cage/motherboard and controls other memory and I/O modules. The heart of the SBC module is an R6502 CPU, which is capable of addressing 65K bytes of memory. In addition, the SBC module contains bank address logic which allows addressing of one or two 65K byte memory banks. Sockets on the module accept up to 16K bytes of PROM/ROM. 2K bytes of static RAM are also provided.

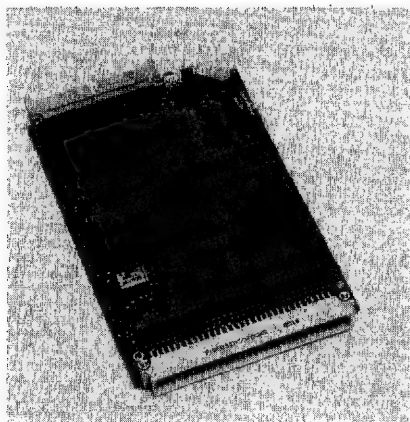
An R6522 Versatile Interface Adapter (VIA) provides two 8-bit parallel I/O data lines, two 2-bit control lines, two counter-timers and an 8-bit shift register. On-board switches assign memory sections to 4K byte blocks. All address, data and control lines are buffered.

ORDERING INFORMATION

Part No.	Description
RM65-1000E	Single Board Computer (SBC) Module
Order No.	Description
809	Single Board Computer (SBC) Module User's Manual (included with RM65-1000E)

FEATURES

- Compact size—about 4" × 6½" (100 mm × 160 mm)
- Pin and socket bus connection
- On-board R6502 CPU
- 2K of 2114 static RAM
- Two sockets for up to 16K PROM/ROM
- Supports the following PROM/ROM or equivalents
 - TI TMS 2516, TMS 2532 and Motorola MCM 68764 PROMs
 - Rockwell R2316, R2332, or R2364 ROMs
- R6522 Versatile Interface Adapter (VIA) and I/O interface
- Fully Buffered Address, Data, and Control lines for RM 65 Bus
- Separate switches allow RAM, PROM/ROM, and VIA to be individually dedicated to one or two 65K byte memory banks
- Jumpers allow selection of the following
 - 2K, 4K or 8K PROM/ROMs
 - RAM, PROM/ROM and I/O starting address to 4K byte boundary
 - On-board or External bank addressing source
 - Programmable DMA Terminate
 - On-board or external clock source
- +5V operation
- Fully assembled, tested and warranted



RM65-1000E Single Board Computer (SBC) Module

FUNCTIONAL DESCRIPTION

The Clock Circuit uses a crystal-controlled oscillator to provide a stable 1-MHz clock reference. A jumper selects between the internal clock reference or an external clock (to 1 MHz) as the source for the R6502 and the derived system clock.

The Reset Control circuit conditions the Reset signal to drive the R6502 Reset line. A reset can be generated by either the on-board reset pushbutton or an external switch. This circuitry also generates a reset automatically, upon power-up.

The R6502 Central Processing Unit (CPU) is the heart of the SBC Module and any interfacing Modules connected to the RM 65 Bus. The R6502 controls all program execution by means of the address, data, control, and timing lines. All internal R6502 operations are synchronized to the clock source.

The Bank Select Control circuit detects when the SBC Module's assigned memory bank is addressed, by comparing the Bank Address signal to the Bank Select Enable and Bank Select switches. The Bank Select Enable Switches allow all on-board PROM/ROM, RAM, & VIA to be independently assigned common to both Bank 0 (lower 65K) and Bank 1 (upper 65K) or dedicated to either Bank 0 or Bank 1, depending on the Bank Select switches. A jumper allows the Bank Address signal to be driven by the on-board R6522 VIA or from another module.

The Base Address Decoder uses the six most-significant address bits and the Base Address Jumpers to generate chip selects for the on-board PROM/ROM, RAM, and VIA. The RAM and VIA can be independently mapped into any 4K block of the selected 65K bank. The PROM/ROMs may be mapped into any 4K or 8K block of the selected bank.

The 16K PROM/ROM section has two sockets which can accept 2K, 4K or 8K PROM/ROM devices. The size and type of PROM

or ROM is specified by the Base Address selection jumpers and the PROM/ROM type jumpers.

The 2K RAM section uses four 1K \times 4 RAM devices to provide on-board read/write memory.

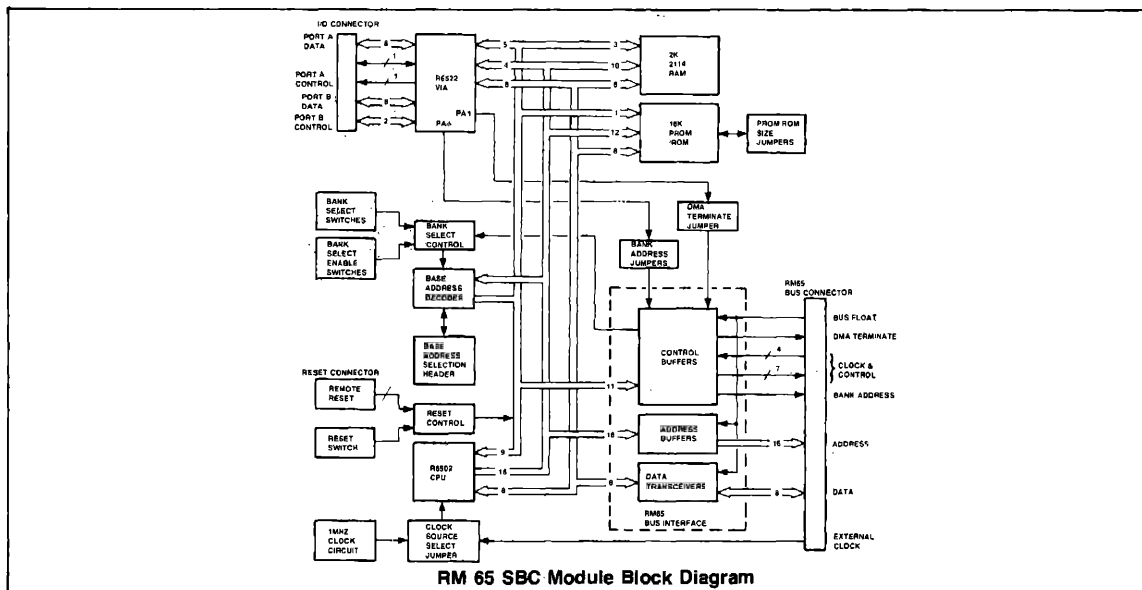
The R6522 Versatile Interface Adapter (VIA) provides input-output capability to the SBC Module. The VIA provides two 8-bit I/O ports each with two control lines. Both ports and control lines are brought out to a connector for user applications.

The SBC Module can control up to 15 additional support modules by means of the RM 65 Bus. There are three groups of signals on the RM 65 Bus: data, address, and control.

The Data Transceivers invert and transfer eight bits of parallel data between the SBC Module and the RM 65 bus. The direction of the transceivers is controlled by the read/write signal from the R6502. The transceivers are disabled when the on-board PROM/ROM, RAM, or VIA is addressed or when the Bus Float signal from the RM 65 Bus is active.

The Address Buffers invert and transfer 16 parallel address bits from the SBC Module to the RM 65 bus:

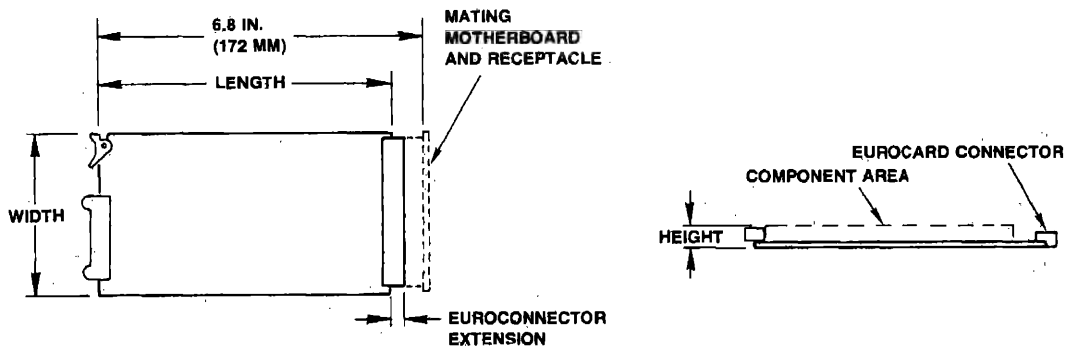
The Control Buffers buffer all control and clock signals between the SBC Module and the RM 65 bus. The Non-Maskable Interrupt, Interrupt Request, Set Overflow, External Clock ($\phi 0$), Ready and Bus Float input lines are buffered coming from the RM 65 bus into the SBC Module. The DMA Terminate, Reset and Phase 1 Clock ($\phi 1$) output lines are always driven from the SBC Module onto the RM 65 Bus. The other six output lines for Read/Write, Phase 2 Clock, sync, and Bank Address are also buffered, but are tri-stated (disabled) when the Bus Float signal is active.



RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	Bφ1	Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	Buffered Sync
14a	BSO	Buffered Set Overflow	14c	BDRQ1/	*Buffered DMA Request 1
15a	BRDY	Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	-12V/-V	*-12 Vdc/-V
17a	+12V/+V	*+12 Vdc/+V	17c		*User Spare 2
18a	GND	Ground line	18c	BFLT/	Buffered Bus Float
19a	BDMT/	Buffered DMA Terminate	19c	Bφ0	Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR/W/	Buffered Read/Write "Not"	21c	BDRQ2/	*Buffered DMA Request 2
22a		*System Spare	22c	BR/W/	Buffered Read/Write
23a	GND	Ground	23c	BACT/	*Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request	24c	BNMI/	Buffered Non-Maskable Interrupt
25a	Bφ2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	Bφ2	Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note:
*Not used on this module.



RM 65 SBC Module Dimensional Outline

SPECIFICATIONS

Parameter	Value
Dimensions (See Notes)	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	5.6 oz. (160 g)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C
Relative Humidity	0% to 85% (without condensation)
Electrical	
Power Requirements	+5 Vdc $\pm 5\%$, 0.75 A (3.5 W)—Typical 1.2 A (6.0 W)—Maximum
Interface	
RM 65 Bus Interface	64-pin plug (0.100 in. centers) per DIN 41612 (Row B not installed)
I/O Connector	40-pin 3M mass termination (0.100 in. centers)
RESET Switch Connector	2 vertical pins (0.3 in. high) on 0.200 in. center
Notes: 1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.). 2. Length does not include extensions beyond the edge of the module due to connectors or the module ejector. 3. Dimensions conform to DIN 41612.	



RM65-0110

RM 65 INPUT/OUTPUT (I/O) ROM

INPUT/OUTPUT FUNCTIONS

The input/output (I/O) functions in a microcomputer performs interface processing between an application program and peripheral devices, e.g., display, printer and keyboard. These functions are usually implemented as closed subroutines that may be called by the application program or as part of an operating system that operates on passed parameters. The I/O functions normally issue operating commands to the peripherals, monitor status from the peripherals and transfer data to and from the peripherals. Data formatting and message protocol stripping is also usually performed. In addition, general purpose utility functions supporting I/O operations are often provided.

PRODUCT OVERVIEW

The RM 65 I/O ROM contains initialization, interrupt and I/O processing functions to interface AIM 65/40 peripherals to an RM 65 Single Board Computer (SBC) based microcomputer system. The processing and entry points, in most cases, are identical to the AIM 65/40 I/O ROM, to enable an application program developed on the AIM 65/40 Microcomputer to be easily transferred to the RM 65 environment for final validation and production operation. Source code entry, editing, compilation and/or assembly, and debugging can be performed on the AIM 65/40 Microcomputer with its extensive development aids using the AIM 65/40 Debug Monitor/Text Editor and the desired language. The AIM 65/40 peripherals connected to the AIM 65/40 SBC module can support development as well as application checkout in this configuration.

In a minimum RM 65 module installation consisting of only the RM 65 SBC module (RM65-1000E), the 4K-byte RM 65 I/O ROM in one SBC module socket supports an application program in the other SBC module socket for user-defined I/O over the SBC module parallel I/O port. The addition of one RM 65 Multifunction Peripheral Interface (MPI) module (RM65-5223E) allows interface to an AIM 65/40 Keyboard and either the AIM 65/40 40-Character Display or AIM 65/40 Video Display Controller in one configuration, or the AIM 65/40 Graphics Printer and a user-defined interface in the other configuration. Installation of two RM 65 MPI modules supports both configurations.

MEMORY MAP

Address (Hex)	Contents
\$FFFA-\$FFFF	NMI, RES and IRQ Vectors
\$F000-\$FFF9	I/O ROM Program
\$1000-\$1FFF	System I/O
\$200-\$49F	I/O ROM Vectors, Constants and Variable
\$F0-\$FF	I/O ROM Variables

FEATURES

- RM 65 SBC module compatible
- AIM 65/40 I/O ROM interface compatible
- ROM resident for immediate operation
- Supports AIM 65/40 Peripherals
 - 40-Character Display (A65/40-0400)
 - Video Display Controller Module (A65/40-0800)
 - Graphics Printers (A65/40-0600)
 - Standard Keyboard (A65/40-0200)
 - Expanded Keyboard (A65/40-0210)
- Interrupt Handlers
 - Interrupt Request (IRQ) with before and after user linkage
 - Non-Maskable Interrupt (NMI) with before and after user linkage
 - Reset (RES)
 - Break instruction linkage
- Initialization Functions
 - Cold and warm start variable initialization
 - Autostart linkage to application programs
- Provide input/output handlers for
 - Keyboard (system terminal) input
 - Display/printer (system terminal) output
 - Memory input/output
 - Floppy disk (RM65-5101E)
 - Printer output
 - Interactive user-defined input/output
 - Non-interactive user-defined input/output
 - Null output
- User-alterable variables
 - Input/output vectors
 - Interrupt vectors

ORDERING INFORMATION

Part No.	Description
RM65-0110	RM 65 I/O ROM
Order No.	Description
821	RM 65 I/O ROM User's Manual*
Note:	
*Included with RM65-0110.	



RM 65-0122

RM 65 RUN-TIME BASIC INTERPRETER ROM

BASIC LANGUAGE

BASIC is a simple but powerful computer program language. Originally developed at Dartmouth University, BASIC has gained universal acceptance and is commonly used world-wide in schools, industry, and science.

The heart of BASIC is a set of easily learned English words which are used as commands. Complex and powerful statements can be constructed by adding operands and operators to the commands. Equations involving complex formulas and multiple variables can easily be solved. Internal floating point arithmetic handles a wide range of numeric values (2.93873588E-39 to 1.70141183E+38) and provides nine-digit accuracy to most calculations. In addition to addition, subtraction, multiplication and division, a full set of transcendental functions support trigonometric, exponential, square, square root, polynomial and logarithmic operations.

PRODUCT OVERVIEW

RM 65 Run-Time BASIC, consisting of input formatter, lister, interpreter, floating point functions and input/output linkage, is contained in an 8K-byte ROM that plugs into an RM65-1000 Single Board Computer (SBC) or RM65-3216 PROM/ROM module for development or run-time operation in the RM 65 environment. This run-time package allows an application program written in BASIC to be developed on an AIM 65 Microcomputer using its on-board peripherals (keyboard, single line display and printer) and ROM resident Debug Monitor and Text Editor and then transferred to the RM 65 module for run-time operation.

All input/output functions for use with RM 65 Run-Time BASIC are user-provided and link to the application program through one or more of the 10 I/O vectors provided in the run-time ROM. BASIC words such as LOAD, SAVE, PRINT, INPUT, READ and GET link through these vectors to the I/O functions.

The RM 65 Run-Time BASIC can be used in the development mode by user-provided AIM 65 equivalent input/output functions. In fact, the RM 65 Run-Time BASIC ROM can be installed on an RM 65 PROM/ROM module, the module connected to an AIM 65 Microcomputer, the I/O vectors loaded to point to AIM 65 Monitor ROM functions, then development and/or final program validation performed on the AIM 65 Microcomputer before transferring the application program object code to PROM/ROM.

LANGUAGE FEATURES

- BASIC is easy to learn
- Microsoft BASIC is universally accepted
- BASIC is widely used
- Supports simple and complex statements
- Floating point arithmetic functions
 - Add, subtract, multiply, divide
 - Trigonometric (sine, cosine, tangent, arctangent)
 - Exponential, square, square root
 - Natural logarithm
- String variables and arrays
- Integer variables
- Subroutine calls
- Conditional expressions
- User function

INTERPRETER FEATURES

- RM 65 Single Board Computer (SBC) module host and/or target
- ROM resident for immediate operation
- Compatible with indirect statements entered on AIM 65 Microcomputer with AIM 65 BASIC
- I/O vectors link to user-provided peripheral drivers

ORDERING INFORMATION

Part No.	Description
RM65-0122 A65-020	RM 65 Run-time BASIC ROM AIM 65 BASIC ROMs
Order No.	Description
810 221	RM 65 Run-time BASIC User's Manual ⁽¹⁾ AIM 65 BASIC User's Manual ⁽²⁾
Notes:	
1. Included with RM65-0122.	
2. Included with A65-020.	

MEMORY MAP

Address (Hex)	Contents
\$B000-\$CFFF	BASIC Program
\$248-\$2DC	BASIC Input/Output Buffers
\$218-\$247	BASIC Variables
\$200-\$217	BASIC I/O Vectors
	BASIC Variables

PROM PROGRAMMING

The application program object code can be programmed into a PROM for operation in an OEM or end-user environment using an AIM 65 PROM Programmer & CO-ED module (A65-901) or an RM 65 PROM Programmer module (RM65-2901E) connected to the AIM 65 Microcomputer.

STATEMENTS

Program Statements	Commands	String Functions
DEF FN	CLEAR	ASC
DIM	CONT	CHR\$
END	FRE	LEFT\$
FOR	LIST	LEN
GOSUB	LOAD	MID\$
GOTO	NEW	RIGHT\$
IF ... GOTO	PEEK	STR\$
IF ... THEN	POKE	VAL
LET	RUN	
NEXT	SAVE	
ON ... GOSUB		Arithmetic Functions
ON ... GOTO	Input/Output*	ABS
REM	DATA	ATN
RESTORE	GET	COS
RETURN	INPUT	EXP
STOP	READ	INT
USR	PRINT	LOG
WAIT	SPC	RND
	TAB	SIN
	POS	SGN
		SQR
		TAN

*Input/output functions link through I/O vectors to user-defined functions.



RM65-0152

RM 65 RUN-TIME FORTH ROM

FORTH LANGUAGE

FORTH is a unique programming language well suited to a variety of applications. Because it was originally developed for real-time control applications, FORTH is ideal for machine and process control, energy management, data acquisition, automatic testing, robotics and other applications where assembly language was previously the only possible language choice.

FORTH actually provides the best of two worlds. It has the looping and branching constructs of high-level languages (DO ... LOOP, BEGIN ... END, IF ... THEN and IF ... ELSE ... THEN) and the code efficiency of machine and assembly languages. And programmers will be pleased to know that FORTH allows you to specify addresses, operands and data in hexadecimal, octal, binary or any other number base from two to 40—a distinct advantage over languages like BASIC, where all information must be in decimal.

In most time-critical applications, at least part of the program must be written in assembly language. FORTH has a built-in 6502 macro assembler, and lets you drop into assembly language at almost any point in your program, without separate assembly and load steps or awkward machine level linkage. FORTH programs typically run up to ten times faster than other interpretive languages, and can even approach the speed of machine language programs for some applications.

FEATURES

- RM 65 SBC module compatible
- ROM resident for immediate operation
- Application oriented
- Extensible language
- Over 200 pre-defined functions
- Interactive compilation
- Reverse polish notation
- Compact memory usage
- Fast execution
- Easy debugging
- Stack implementation
- 16-bit words
- Built-in structured macro assembler
- Shortens software development time
- AIM 65 FORTH compatible

PRODUCT OVERVIEW

RM 65 Run-Time FORTH, consisting of primitives, interpreter, macro assembler and input/output linkage, is contained in an 8K-byte ROM that plugs into an RM65-1000E Single Board Computer (SBC) or RM65-3216E PROM/ROM module for development or run-time operation in the RM 65 environment. This run-time package allows an application program written in FORTH to be developed on an AIM 65 Microcomputer with its on-board peripherals (keyboard, single line display and printer) and ROM-resident Debug Monitor and Text Editor and then transferred to the RM 65 module for run-time operation. The application program object code can be programmed into a PROM using an A65-901 AIM 65 PROM Programmer & CO-ED module or an RM65-2901E PROM Programmer module.

All input/output functions for use with RM 65 Run-Time FORTH are user-provided and link to the application program through one or more of the 11 I/O vectors provided in the run-time ROM. FORTH words such as KEY, EXPECT, EMIT, GET, READ, and ?IN link through these vectors to the I/O functions.

The RM 65 Run-Time FORTH can be used in the development mode by user-provided AIM 65 equivalent input/output functions. In fact, the RM 65 Run-Time FORTH ROM can be installed on an RM 65 PROM/ROM module, the module connected to an AIM 65 Microcomputer, the I/O vectors loaded to point to AIM 65 Monitor ROM functions, then development and/or final program validation performed on the AIM 65 Microcomputer before transferring the application program object code to PROM/ROM.

ORDERING INFORMATION

Part No.	Description
RM65-0152	RM 65 Run-Time FORTH ROM
A65-050	AIM 65 FORTH ROMs
A65-040	AIM 65 Math Package ROM
Order No.	Description
812	RM 65 Run-Time FORTH User's Manual ⁽¹⁾
265	AIM 65 FORTH User's Manual ⁽²⁾
2118	AIM 65 Math Package User's Manual ⁽³⁾
Notes:	
1. Included with RM65-0152	
2. Included with A65-050.	
3. Included with A65-040.	

DEVELOPING FORTH PROGRAMS

FORTH is built on subroutine-like functions, called "words." These words are linked together to form a "dictionary," which is the central core of the language. Writing a program in FORTH consists of using several predefined words to define each new word. Once the new word has been added to the system dictionary, it becomes as much a part of the language as any other word that has been previously defined. In this way new features and extensions can be added by simply defining one or more new words. Adding new features to conventional languages like BASIC or Pascal requires the language system to be completely reassembled or recompiled.

FORTH is a stack-oriented language, and is programmed in Reverse Polish Notation (RPN), the notation that is used in Hewlett-Packard scientific calculators. Using a data stack is an extremely efficient way of passing variables back and forth between operations. A data stack eliminates the need to tie up memory locations with variable tables, and allows you to use only as much memory as you need.

FORTH programs are developed using "top-down/bottom-up" techniques. That is, the programmer begins by defining the program in very general terms, then systematically breaks these definitions down into more and more detailed sub-modules. When the lowest levels of sub-modules have been defined, he starts coding, in FORTH, at those levels, working back up toward the top of the program, in pyramid fashion. Each sub-module is a stand-alone component of the program, and can be completely debugged without having the complete program in the system.

FLOATING POINT FUNCTIONS

The RM 65 Run-Time FORTH ROM contains both a single- (16-bit) and double- (32-bit) precision integer arithmetic capability. In RM 65 applications where floating point arithmetic is desired, the AIM 65 Math Package ROM may be used in conjunction with the run-time FORTH ROM. The application program can be developed on an AIM 65 Micro-computer with both AIM 65 FORTH and AIM 65 Math Package ROMs installed. A math package ROM must then be installed in the RM 65 SBC or PROM/ROM module for run-time operation of the application program along with the RM 65 Run-Time FORTH ROM.

MEMORY MAP

Address (Hex)	Description
\$D000-\$DFFF	Math Package Program
\$B000-\$CFFF	FORTH Program
\$300-\$31E	I/O Vectors
\$280-\$2FF	Terminal Input Buffer
\$25C-\$27F	Math Package Variables
\$200-\$257	FORTH User Variables
\$AB-\$CA	Math Package Variables
\$10-\$AA	FORTH Variables

FORTH WORDS

STACK MANIPULATION

DUP	Duplicate top of stack.
2DUP	Duplicate top two stack items.
DROP	Delete top of stack.
2DROP	Delete top two stack items.
SWAP	Exchange top two stack items.
OVER	Copy second item to top.
ROT	Rotate third item on top.
- DUP	Duplicate only if non-zero
>R	Move top item to return stack.
R>	Retrieve item from return stack.
R	Copy top of return stack onto stack.
PICK	Copy the nth item to top.
SP@	Return address of stack position
RP@	Return address of return stack pointer.
BOUNDS	Convert "address count" to "end-address start-address."
.S	Print contents of stack.

DEFINING WORDS

:<name>	Begin colon definition of <name>.
:	End colon definition.
VARIABLE <name>	Create a variable <name> with initial value n; returns address when executed.
CONSTANT <name>	Create a constant <name> with value n; returns value when executed.
CODE <name>	Begin definition of assembly-language primitive operation <name>.
:CODE	Used to create a new defining word, with execution-time "code routine" for this data type in assembly.
<BUILDS ... DOES>	Used to create a new defining word, with execution-time routine for this data type in higher-level FORTH.
USER	Create a user variable.

MEMORY

@	Fetch value addressed by top of stack.
!	Store n1 at address n2.
C@	Fetch one byte only.
C!	Store one byte only.
?	Print contents of address.
+!	Add second number on stack to contents of address on top.
CMOVE	Move n3 bytes starting at address n1 to area starting at address n2.
FILL	Put byte n3 into n2 bytes starting at address n1.
ERASE	Fill n2 bytes in memory with zeroes, beginning at address n1.
BLANKS	Fill n2 bytes in memory with blanks, beginning at address n1.
TOGGLE	Mask memory with bit pattern.

NUMERIC REPRESENTATION

DECIMAL	Set decimal base.
HEX	Set hexadecimal base.
BASE	Set number base.
DIGIT	Convert ASCII to binary.
0	The number zero.
1	The number one.
2	The number two.
3	The number three.

FORTH WORDS (CONT'D)

ARITHMETIC AND LOGICAL

+	Add.
D+	Add double-precision numbers.
-	Subtract ($n1 - n2$)
*	Multiply.
/	Divide ($n1/n2$).
MOD	Modulo (i.e., remainder from division).
/MOD	Divide, giving remainder and quotient.
./MOD	Multiply, then divide ($n1 \cdot n2 / n3$), with double intermediate.
./	Like ./MOD, but give quotient only.
U-	Unsigned multiply leaving double product.
U/	Unsigned divide.
M*	Signed multiplication leaving double product.
M/	Signed remainder and quotient from double dividend.
M/MOD	Unsigned divide leaving double quotient and remainder from double dividend and single divisor.
MAX	Maximum.
MIN	Minimum.
+ -	Set sign.
D+ -	Set sign of double-precision number.
ABS	Absolute value.
DABS	Absolute value of double-precision number.
NEGATE	Change sign.
DNEGATE	Change sign of double-precision number.
S- >D	Sign extend to double-precision number.
1 +	Increment value on top of stack by 1.
2 +	Increment value on top of stack by 2.
1 -	Decrement value on top of stack by 1.
2 -	Decrement value on top of stack by 2.
AND	Logical AND (bitwise).
OR	Logical OR (bitwise).
XOR	Logical exclusive OR (bitwise).

COMPARISON OPERATORS

<	True if $n1$ less than $n2$.
>	True if $n1$ greater than $n2$.
=	True if top two numbers are equal.
0<	True if top number negative.
0=	True if top number zero.
U<	True if $u1$ less than $u2$.
NOT	Same as 0=.

MISCELLANEOUS AND SYSTEM

(<comment>)	Begin comment (terminate by right parentheses on same line).
CFA	Alter PFA to CFA.
NFA	Alter PFA to NFA.
PFA	Alter NFA to PFA.
LFA	Alter PFA to LFA.
LIMIT	Top of memory.
QUIT	Clear return stack and return to terminal.

CONTROL STRUCTURES

DO ... LOOP	Set up loop, given index range.
DO ... +LOOP	Like DO ... LOOP, but adds stack value to index.
I	Place current index value on stack.
LEAVE	Terminate loop at next LOOP or +LOOP.
BEGIN ... UNTIL	Loop back to BEGIN until true at UNTIL.
BEGIN ... WHILE ... REPEAT	Loop while true at WHILE, REPEAT loops unconditionally to BEGIN.
BEGIN ... AGAIN	Unconditional loop.
IF ... THEN	If top of stack true, execute following clause THEN continue; otherwise continue at THEN.
IF ... ELSE ... THEN	If top of stack true, execute ELSE clause THEN continue; otherwise execute following clause, THEN continue.
END	Alias for UNTIL.
ENDIF	Alias for THEN.

COMPILER-TEXT INTERPRETER

[COMPILE]	Force compilation of IMMEDIATE word.
COMPILE	Compile following <name> into dictionary.
LITERAL	Compile a number into a literal.
DLITERAL	Compile a double-precision number into a literal.
EXECUTE	Execute the definition on top of stack.
[Suspend compilation, enter execution.
]	Resume compilation.

DICTIONARY CONTROL

CREATE	Create a dictionary header.
FORGET	FORGET all definitions from <name> on.
HERE	Return address of next unused byte in the dictionary.
ALLOT	Leave a gap of n bytes in the dictionary.
TASK	A dictionary marker.
'	Find the address of <name> in the dictionary.
- FIND	Search dictionary for <name>.
DP	User variable containing the dictionary pointer.
C,	Store byte into dictionary.
,	Compile a number into the dictionary.
PAD	Pointer to temporary buffer.
IMMEDIATE	Force execution when compiling.
INTERPRET	The Text Interpreter executes or compiles.
LATEST	Leave name field address (NFA) of top word in CURRENT.
LIT	Place 16-bit literal on the stack.
CLIT	Place byte literal on the stack.
LITERAL	Compile a 16-bit literal.
SMUDGE	Toggle name SMUDGE bit.
STATE	User variable containing compilation state.

FORTH WORDS (CONT'D)

USER VARIABLES (See Note 1)

U?TERMINAL	User variable for ?TERMINAL. (See Note 2.)
UABORT	User variable for ABORT.
UB/BUF	User variable for B/BUF.
UB/SCR	User variable for B/SCR.
UC/L	User variable for C/L.
UEMIT	User variable for EMIT.
UFIRST	User variable for FIRST.
UKEY	User variable for KEY.
ULIMIT	User variable for LIMIT.

MONITOR & CASSETTE I/O (See Note 1)

COLD	AIM 65 FORTH cold start. (See Note 2.)
MON	Exit to AIM 65 Monitor. (See Note 2.)
CHAIN	Chain tape file.
CLOSE	Close tape file.
?IN	Set to active input device (AID).
?OUT	Set to active output device (AOD).
GET	Input a character from the AID.
PUT	Output a character to the AOD.
READ	Input n2 characters from AID to address n1.
WRITE	Output n2 characters to AOD at address n1.
SOURCE	Compile from the AID.
FINIS	Terminate complete from SOURCE.

INPUT-OUTPUT (See Note 1).

- CR	Output CR to printer only.
CR	Carriage return.
SPACE	Type one space.
SPACES	Type n spaces.
CLRLINE	Output a CTRL B.
"	Print text string (terminated by ").
DUMP	Dump n2 words starting at address.
TYPE	Type string of n1 characters starting at address n2.
?TERMINAL	True if terminal break request present.
KEY	Read key, put ASCII value on stack.
EMIT	Output ASCII value from stack.
EXPECT	Read n1 characters from input to address n2.
WORD	Read one word from input stream, until delimiter.
IN	User variable contained within TIB.
BAUD	Set BAUD rate.
BL	Output a SPACE character.
C/L	Number of characters/line.
TIB	Pointer to terminal input buffer start address.
QUERY	Input text from terminal.
ID.	Print <name> from name # field address (nfa).
HANG	Wait for keystroke.

OUTPUT FORMATTING (See Note 1)

NUMBER	Convert string at address to double-precision number.
<#	Start output string.

- NOTES: 1. Requires user-provided I/O function.
2. Requires AIM 65 Monitor ROM be installed.

OUTPUT FORMATTING (CONT'D)

#	Convert next digit of double-precision number and add character to output string.
#S	Convert all significant digits of double-precision number to output string. Insert sign of n into output string.
SIGN	Terminate output string (ready for TYPE).
#>	Insert ASCII character into output string.
HOLD	Hold pointer, user variable.
HDL	Suppress trailing blanks.
- TRAILING	Display line of text from mass storage.
.LINE	Change length of byte string to type form.
COUNT	Print number on top of stack.
.R	Print number n1 right justified n2 places.
D.	Print double-precision number n2 n2.
D.R	Print double-precision number n2 n1 right justified n3 places.
DPL	Number of digits to the right of decimal point.

VOCABULARIES

CONTEXT	Returns address of pointer to CONTEXT vocabulary.
CURRENT	Returns address of pointer to CURRENT vocabulary.
FORTH	Main FORTH vocabulary.
ASSEMBLER	Assembler vocabulary.
DEFINITIONS	Set CURRENT vocabulary to CONTEXT.
VOCABULARY <name>	Create new vocabulary.
VLIST	Print names of all words in CONTEXT vocabulary.
VOC-LINK	Most recently defined vocabulary.

VIRTUAL STORAGE

LOAD	Load mass storage screen (compile or execute).
BLOCK	Read mass storage block to memory address.
B/BUF	System constant giving mass storage block size in bytes.
B/SCR	Number of blocks/editing screen.
BLK	System variable containing current block number.
SCR	System variable containing current screen number.
UPDATE	Mark last buffer accessed as updated.
FLUSH	Write all updated buffers to mass storage.
EMPTY-BUFFERS	Erase all buffers.
+BUF	Increment buffer address.
BUFFER	Fetch next memory buffer.
RW	User read write linkage.
USE	Variable containing address of next buffer.
PREV	Variable containing address of latest buffer.
FIRST	Leaves address of first block buffer.
OFFSET	User variable block offset to mass storage.
->	Interpret next screen.
;S	Stop interpretation.

FORTH WORDS (CONT'D)

PRIMITIVES

0BRANCH	Run-time conditional branch.
BRANCH	Run-time unconditional branch.
ENCLOSE	Text scanning primitive used by WORD.
R0	Location of Return Stack.
S0	Location of Parameter Stack.
RP!	Initialize Return Stack.
SP!	Initialize Parameter Stack.
NEXT	The FORTH virtual machine.

SECURITY

!CSP	Store stack position in check stack pointer.
?COMP	Error if not compiling.
?CSP	Check stack position.
?ERROR	Output error message.
?EXEC	Not executing error.
?PAIRS	Conditional not paired error.
?STACK	Stack out of bounds error.
ABORT	Error; operation terminates.
ERROR	Execute error notification and restart system.
MESSAGE	Displays message.
WARNING	Pointer to message routine.
FENCE	Prevents forgetting below this point.
WIDTH	Controls significant characters of <name>.

MATH PACKAGE FORTH WORDS (A65-040)*

FLOATING POINT ARITHMETIC

F+	Adds two floating point numbers.
F-	Subtracts one floating point number from another floating point number.
F*	Multiplies two floating point numbers.
F/	Divides one floating point number by another floating point number.

UTILITY, SIGN AND COMPARISONS

FABS	Takes the absolute value of a floating point number.
INT	Truncates a floating point number to an integer.
SGN	Converts the sign of a floating point number to a floating point number.
FSIGN	Gets a value corresponding to the sign of a floating point number.
FCOMP	Compares the value of a compacted number in memory to a floating point number.

POLYNOMIAL

POLY	Evaluates a polynomial with consecutive exponents.
POLYODD	Evaluates a polynomial with odd exponents.

EXPONENTIAL AND LOGARITHMIC

SQR	Takes the square root of a floating point number.
>	Raises one floating point number to the power of another floating point number.
EXP	Raises the transcendental number e to the power of a floating point number.
LOG	Computes the logarithm to the base 10 (i.e., common log) of a floating point number.
LN	Computes the logarithm to the base e (i.e., natural log) of a floating point number.

USER VARIABLE

MIN-WIDTH	Specifies the minimum field width to be output.
DEC-LENGTH	Specifies the number of places to the right of the decimal point to be output.

ASCII/FLOATING POINT CONVERSIONS

FIN	Converts a number in memory from ASCII to floating point format.
FOUT	Converts a number from floating point to ASCII.

FORMAT CONVERSION AND DATA MOVING

M>F	Unpacks the compacted number in memory to floating point.
F>M	Packs the floating point number to compacted format and stores the result in memory.
M>A	Unpacks the floating point number in memory.
S>A	Converts an integer to floating point format.
S>F	Converts an integer to floating point format.
F>S	Converts a number from floating point to an integer.

TRIGONOMETRIC AND UNITS CONVERSION

SIN	Calculates the sine of a floating point number (in radians).
COS	Calculates the cosine of a floating point number (in radians).
TAN	Calculates the tangent of a floating point number (in radians).
ARCTAN	Calculates the arc tangent of a floating point number.
DEGREES	Converts a floating point number from radians to degrees.
RADIANS	Converts a floating point number from degrees to radians.

*Requires AIM 65 FORTH or RM 65 Run-Time FORTH be resident.



RM65-2901E

RM 65 PROM PROGRAMMER MODULE

RM 65 MICROCOMPUTER MODULES

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC, and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

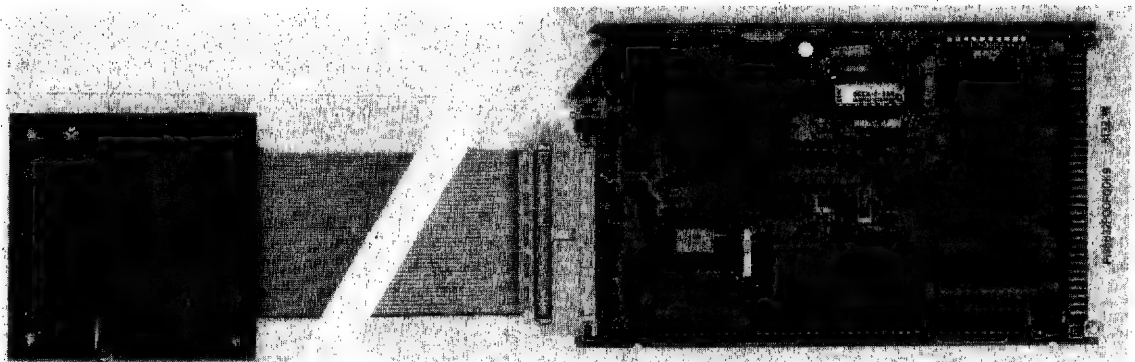
RM 65 Module products use a motherboard interconnect concept in which any card can be inserted in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, provides high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages allows packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The RM 65 PROM Programmer module in conjunction with an AIM 65 or AIM 65/40 Microcomputer, programs industry standard 1K-, 2K-, 4K- and 8K-byte EPROMs (ultra-violet light erasable programmable read-only memories) and 2K-byte EEROMs (electrically erasable programmable read-only memories). The module consists of an RM 65 module and a PROM socket module connected together by a 24-inch ribbon cable. A 28-pin Zero Insertion Force (ZIF) socket mounted on the PROM socket module allows installation of a 28-pin or 24-pin PROM. The PROM socket module may be installed in various desk-top enclosure or front panel arrangements for development, end-user or OEM installation.

FEATURES

- RM 65 bus compatible
- Compact size RM 65 module—about 100 mm × 160 mm (4 in. × 6¼ in.)
- Separate PROM socket module with
 - 28-pin Zero Insertion Force (ZIF) socket
 - Mounting holes for enclosure or panel installation
 - Connecting 24-inch cable to RM 65 module
- Programs 1K-byte to 8K-byte UV EPROMs
 - 1K-byte: 2508, 2758
 - 2K-byte: 2516, 2716
 - 4K-byte: 2532, 2732, 2732A
 - 8K-byte: 2564, 2764, 68764
- Erases and programs 2K-byte EEROMs
 - 2K-byte: R5213/2816, 5213, 2816, 48016
- On-board 8K-byte ROM contains programming functions compatible with both
 - AIM 65 Microcomputer Monitor
 - AIM 65/40 Microcomputer I/O and Monitor
- Easy-to-use interactive commands
 - PROM interface (check, program, read, verify)
 - RAM preparation (fill and invert)
 - Utility functions (command and PROM type menu, PROM type selection, toggle verify mode, etc.)
- Verify during or after programming
- +5V only operation (on-board DC/DC converter)
- Fully assembled and tested with one year warranty



RM65-2901E PROM Programmer Module

ORDERING INFORMATION

Part No.	Description
RM65-2901E	PROM Programmer Module
Order No.	Description
820	PROM Programmer Module User's Manual*
Note: *Included with RM65-2901E.	

FUNCTIONAL DESCRIPTION

RM 65 Module

The Data Transceivers invert and transfer 8-bits of parallel data between the PROM Programmer module and the RM 65 data bus when enabled by the Chip Select Decoder. The read/write line from the RM 65 bus determines the direction of data flow. During a write operation, data is transferred from the bus to the module; during a read operation, data is transferred from the module to the RM 65 bus.

The Control Signal Buffers invert and transfer the phase 2, read/write, bank address and reset signals from the RM 65 bus to the module. The bus active signal is also driven to the RM 65 bus when data is being transferred between the RM 65 bus and the module.

Address Signal Buffers invert and transfer signals from 13 address lines from the RM 65 bus to the module.

The Chip Select Decoder, in conjunction with Base Address Select, Bank Select and Bank Select Enable switches and the ROM Range Select jumper decodes the address from the RM 65 bus and generates enable signals to other major on-board circuits. When the address matches the I/O Base Address switch positions, one of two Octal Latches, the on-board R6522 Versatile Interface Adapter (VIA), the Digital-to-Analog Converter (DAC) and/or the Data Bus Transfers are enabled. When the address matches the ROM Base Address switch positions and ROM Range Selection jumper position, the on-board program ROM is enabled along with the Data Bus Transceivers.

Bank Select and Bank Select Enable switches assign the module to one or two 65K-byte memory banks. The Bank Select Enable switch assigns the module to be active in common memory (both Bank 0 and 1) or in the bank selected by the Bank Select switch (either Bank 0 or 1).

There are eight Base Address switches; four switches assign the on-board ROM base address to a 4K-byte boundary and five assign the I/O base address to a page (256 bytes) within the ROM base address.

The ROM Range Select jumper indicates that no ROM, a 4K-byte ROM or an 8K-byte ROM, is installed on-board.

An 8K-byte ROM containing the PROM Programmer computer program instructions is installed on the module. One-half of the ROM contains programming functions; memory mapped at \$7100-\$7FFF, which operate in conjunction with the AIM 65 Monitor firmware. The other half of the ROM is memory mapped at \$D100-\$DFFF and contains programming functions compatible with the AIM 65/40 I/O and Monitor ROMs. A jumper selects which 4K-bytes (upper or lower), or if the entire 8K-bytes, of the ROM socket are to be addressed.

The R6522 VIA transfers 8-bit data between the RM 65 data bus and the PROM data lines and controls programming voltage levels. During PROM programming, the VIA transfers data from the Data Transceivers for writing into the PROM and during a PROM read, verify or check function, the VIA reads data from the PROM. During PROM programming, the VIA issues control signals to the Power Multiplexer, the Misplaced PROM Detector, and the Vpp Rise/Fall Time Controller.

The Programmable Voltage Regulator, consisting of the 8-bit DAC, a Vpp Rise/Fall Time Controller, a DC/DC Converter and an Analog Buffer, generates the Vpp programming voltage. The DAC outputs a voltage proportional to Vpp for the selected PROM type as controlled by 8-bit data received from the RM 65 data bus. The DAC output voltage is amplified to the full Vpp level, mixed with the rise or fall time control signal, clamped to minimum Vpp level, and output to the Analog Buffer. The +5 to +32V DC/DC Converter provides the high voltage used in the second stage of amplification. The Analog Buffer amplifies the Vpp current for use by the Power Multiplexer.

The Power Multiplexer selects the proper voltage level to output to the PROM during a programming or read operation as controlled by signals from the VIA and Octal Latch A. The output voltage is selected from TTL high, TTL low, Vcc and the Vpp output from the Analog Buffer. The correct voltage is selected by VIA output control lines.

The Misplaced PROM Detector determines if a 24-pin PROM has been offset by one or two pin positions when installed in the 28-pin ZIF socket on the PROM module. The detected state is input to the VIA and sampled by the programming firmware to prevent application of programming voltage to a misplaced PROM.

The two Octal Latches, A and B, transfer addresses from the Address Buffers to the PROM during PROM access operations. The levels of three programming voltages output by the Power Multiplexer to the PROM are also controlled by Octal Latch A.

PROM Socket Module and Interface Cable

A 28-pin Zero Insertion Force (ZIF) socket is mounted on a 3-inch x 3-inch PROM socket module and connected to the RM 65 module by a 24-inch ribbon cable. The socket module has mounting holes and may be installed in any orientation. The 28-pin ZIF socket allows installation of 24-pin PROMs as well as 28-pin PROMs.

PROM PROGRAM COMMANDS

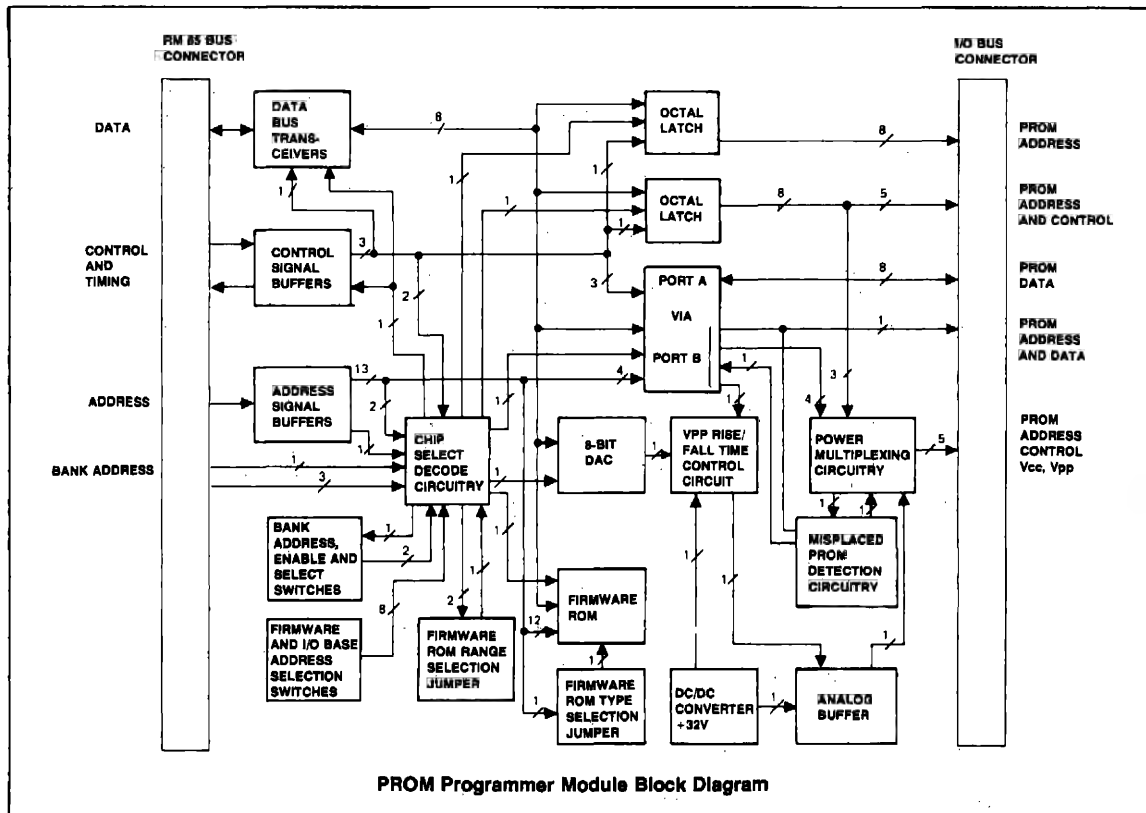
Computer program routines to operate the PROM Programmer module are provided in an 8K-byte ROM installed on the RM 65 module. One of the two versions of the resident firmware is jumper selectable upon installation to operate with either the AIM 65 or the AIM 65/40 I/O and Monitor firmware. Easy-to-use interactive commands perform PROM interface functions (check, program, read and verify), RAM preparation functions (fill and invert) and utility functions (e.g., command and PROM type menus, toggle verification mode, and change PROM type). Many Monitor commands are directly linked to the PROM Programmer command level for ease of operation.

PROM Programmer commands are invoked from a command entry level mode similar to the AIM 65 and 65/40 Debug Monitor operation. Initial entry and re-entry functions from the Debug Monitor provide operator initialization flexibility. The commands listed below can then be selected by single keystrokes. Sub-prompts displayed upon command selection request entry of information pertinent to the specific function. Once initiated, each function operates automatically until successful completion or upon termination due to a detected error.

PROM PROGRAMMER FUNCTIONS

Command	Function
C	Check PROM
P	Program PROM
R	Read PROM
V	Verify PROM
S	Check Memory
A	Alter Memory
I	Invert Memory
?	Display Menu
E	Erase EEROM
N	Change PROM Type
T	Toggle Verify Mode
X	Exit
L	Load with Offset
D	Dump with Offset

The RM 65 Floppy Disk Controller (FDC) Module and DOS 1.0 functions may also be used in conjunction with the PROM Programmer to simplify file handling during PROM programming or read operations.



PROM Socket Pin Assignment

Connector J1 (P2) Pin No.	28-pin PROM Socket Pin Number	Signal Symbol	Signal Name	Connector J1 (P2) Pin No.	28-pin PROM Socket Pin Number	Signal Symbol	Signal Name
3, 5, 10, 15, 24, 26, 28, 30, 32, 35, 37, 39	14	GND	Ground	16	11	Q0	Data Bit 0
1, 40	28	VCC	PROM Supply Voltage	17	12	Q1	Data Bit 1
2	1	VPP	Programming Voltage	18	13	Q2	Data Bit 2
4	2	A12	Address Bit 12	19	15	Q3	Data Bit 3
6	3	A7	Address Bit 7	20	16	Q4	Data Bit 4
7	4	A6	Address Bit 6	21	17	Q5	Data Bit 5
8	5	A5	Address Bit 5	22	18	Q6	Data Bit 6
9	6	A4	Address Bit 4	23	19	Q7	Data Bit 7
11	7	A3	Address Bit 3	25	20	CE	Chip Enable
12	8	A2	Address Bit 2	27	21	A10	Address Bit 10
13	9	A1	Address Bit 1	29	22	OE	Output Enable
14	10	A0	Address Bit 0	31	23	A11	Address Bit 11
				33	24	A9	Address Bit 9
				34	25	A8	Address Bit 8
				36	26	A13	Address Bit 13
				38	27	PGM	Program

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Signal Mnemonic	Signal Name	Pin	Pin	Signal Mnemonic	Signal Name
GND	Ground	1a	1c	+5V	+5 Vdc
BADR/	Buffered Bank Address	2a	2c	BA15/	Buffered Address Bit 15
GND	Ground	3a	3c	BA14/	Buffered Address Bit 14
BA13/	Buffered Address Bit 13	4a	4c	BA12/	Buffered Address Bit 12
BA11/	Buffered Address Bit 11	5a	5c	GND	Ground
BA10/	Buffered Address Bit 10	6a	6c	BA9/	Buffered Address Bit 9
BA8/	Buffered Address Bit 8	7a	7c	BA7/	Buffered Address Bit 7
GND	Ground	8a	8c	BA6/	Buffered Address Bit 6
BA5/	Buffered Address Bit 5	9a	9c	BA4/	Buffered Address Bit 4
BA3/	Buffered Address Bit 3	10a	10c	GND	Ground
BA2/	Buffered Address Bit 2	11a	11c	BA1/	Buffered Address Bit 1
BA0/	Buffered Address Bit 0	12a	12c	Bφ1	*Buffered Phase 1 Clock
GND	Ground	13a	13c	BSYNC	*Buffered Sync
BSO	*Buffered Set Overflow	14a	14c	BDRQ1/	*Buffered DMA Request 1
BRDY	*Buffered Ready	15a	15c	GND	Ground
	*User Spare 1	16a	16c	-12V/-V	*- 12 Vdc/-V
+12V/+V	*+12 Vdc	17a	17c		*User Spare 2
GND	Ground	18a	18c	BFLT/	*Buffered Bus Float
BDMT/	*Buffered DMA Terminate	19a	19c	Bφ0	*Buffered External Phase 0 Clock
	*User Spare 3	20a	20c	GND	Ground
BR/W/	Buffered Read/Write "Not"	21a	21c	BDRQ2/	*Buffered DMA Request 2
	*System Spare	22a	22c	BR/W/	*Buffered Read/Write
GND	Ground	23a	23c	BACT/	Buffered Bus Active
BIRQ/	*Buffered Interrupt Request	24a	24c	BNMI/	*Buffered Non-Maskable Interrupt
Bφ2/	Buffered Phase 2 "Not" Clock	25a	25c	GND	Ground
Bφ2	*Buffered Phase 2 Clock	26a	26c	BRES/	Buffered Reset
BD7/	Buffered Data Bit 7	27a	27c	BD6/	Buffered Data Bit 6
GND	Ground	28a	28c	BD5/	Buffered Data Bit 5
BD4/	Buffered Data Bit 4	29a	29c	BD3/	Buffered Data Bit 3
BD2/	Buffered Data Bit 2	30a	30c	GND	Ground
BD1/	Buffered Data Bit 1	31a	31c	BD0/	Buffered Data Bit 0
+5V	+5 Vdc	32a	32c	GND	Ground

Note:

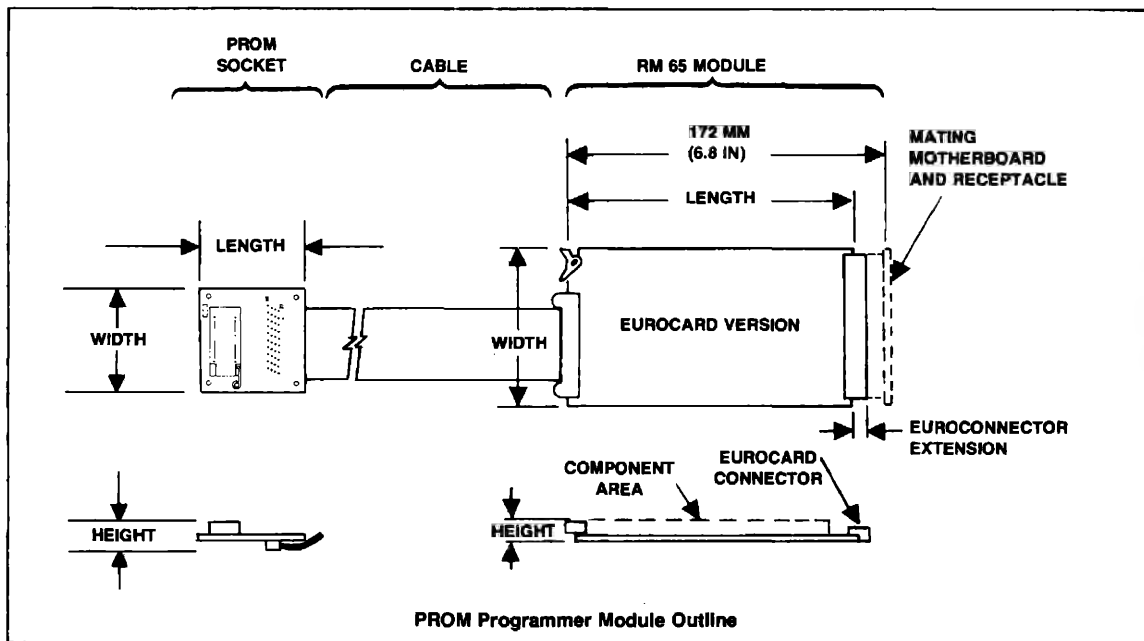
*Not used on this module

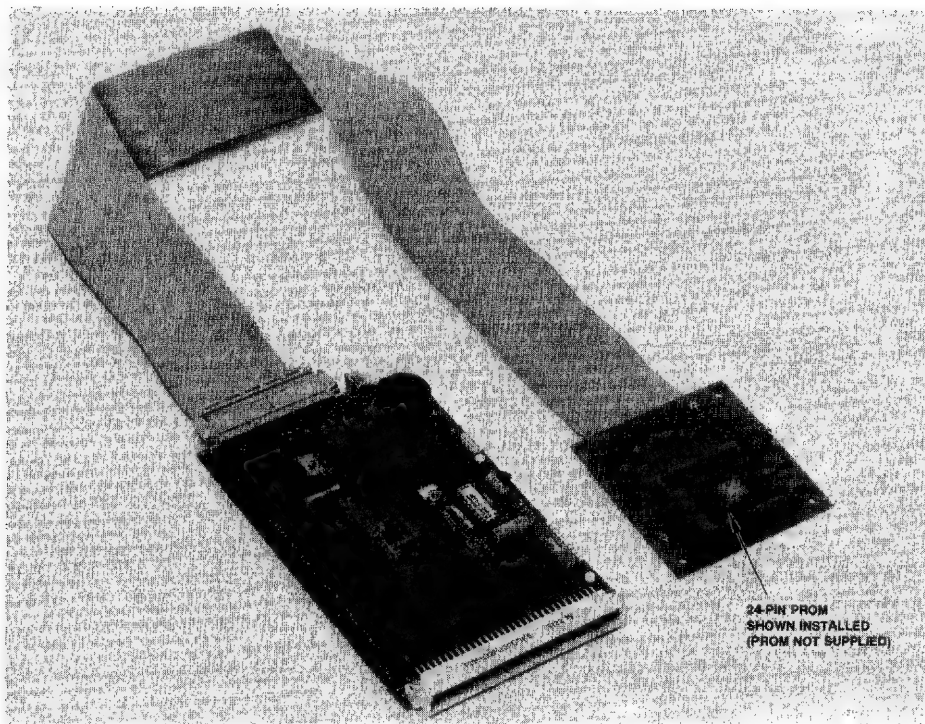
SPECIFICATIONS

Characteristics	Values
Dimensions	
PROM Programmer Module	
Width	100 mm (3.94 in.)
Length	167 mm (6.58 in.)
Height ⁽¹⁾	14 mm (0.56 in.)
Weight ⁽³⁾	184 g (6.5 oz.)
PROM Socket Module	
Length	76 mm (3.0 in.)
Height ⁽²⁾	35 mm (1.38 in.)
Weight (with cable) ⁽³⁾	99 g (3.5 oz.)
PROM Programmer Cable	
Length	610 mm (24 in.)
Environment	
Operating Temperature	0° to 70°C
Storage Temperature	-40°C to 85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	
	+5V \pm 5% at 1.1 A typical
	2.0 A maximum (average)
	2.9 A maximum (peak)
Connectors/Sockets	
RM 65 Bus Connector (P1)	64-pin plug per DIN 41612 (Rows a and b with c not installed)
Socket Module Cable Connector (J1)	40-pin plug (0.100 in. centers) per DIN 41612, mates with 3417-7040 (3M) or equivalent
PROM Socket	28-pin, 213R27-010 or equivalent

Notes:

1. Height value includes the maximum values for component height above the board surface (0.4 in.), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. Height value includes height of Zero Insertion Force Socket lever and cable connector plug thickness.
3. Total weight of PROM Programmer Module (including PROM Programmer Cable with attached PROM Socket Module) 284 g (10 oz.).



**RM65-2901E PROM Programmer Module**



RM65-3108E RM 65 8K STATIC RAM MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-3108E 8K Static RAM Module is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 module products use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

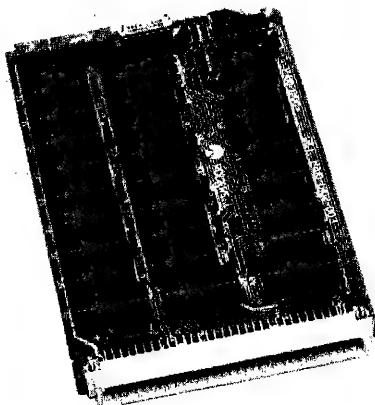
The RM65-3108E 8K Static RAM Module contains 8192 8-bit bytes of Random Access Memory (RAM), in sixteen 2114 static RAM devices. The memory is arranged as two separately addressable 4K memory sections. The starting address of each 4K section is selectable by on-board address switches. A Bank Select switch allows the RAM module to be assigned to one of two 64K memory banks.

FEATURES

- Compact size—about 4" × 6¼" (100 mm × 160 mm)
- Pin and socket bus connectors
- RM 65 Bus compatible
- Buffered address, data and control lines
- Two separately addressable 4K byte sections
- 16 socketed 2114 static RAM devices
- Write-protect switch for each memory section
- Bank Select and Enable switches
- +5V operation
- Fully assembled, tested and warranted.

ORDERING INFORMATION

Part No.	Description
RM65-3108E	8K Static RAM Module
RM65-3108NE	8K Static RAM Module (without RAM devices installed)
Order No.	Description
805	8K Static RAM Module User's Manual (included with RM65-3108E and RM65-3108NE)



RM65-3108E 8K Static RAM Module

FUNCTIONAL DESCRIPTION

8K bytes of static 2114 RAM are divided into two separately addressable 4K blocks. Two devices per 1K bytes are required since each device is $1K \times 4$ bits.

The Data Transceivers invert and transfer 8-bits of parallel data between the RAM devices and the RM 65 Bus, based on data direction signals from the Data Transceiver Control Circuit.

The Address Buffers invert and transfer 16 address bits from the RM 65 Bus to the RAM devices, to the Base Address Decoders and to the Chip Select Decoder.

The Control Buffers invert and transfer phase 2 clock and read/write control signals from the RM 65 Bus onto the RAM module, and drive the bus active signal onto the RM 65 Bus.

The Bank Select Controller detects when the RAM module's assigned memory bank is addressed, by comparing the bank address signal from the RM 65 Bus to the settings of the Bank Select and Bank Select Enable switches. If the addressed bank is the same as the selected memory bank, an enable signal is sent to the Chip Select Decoder.

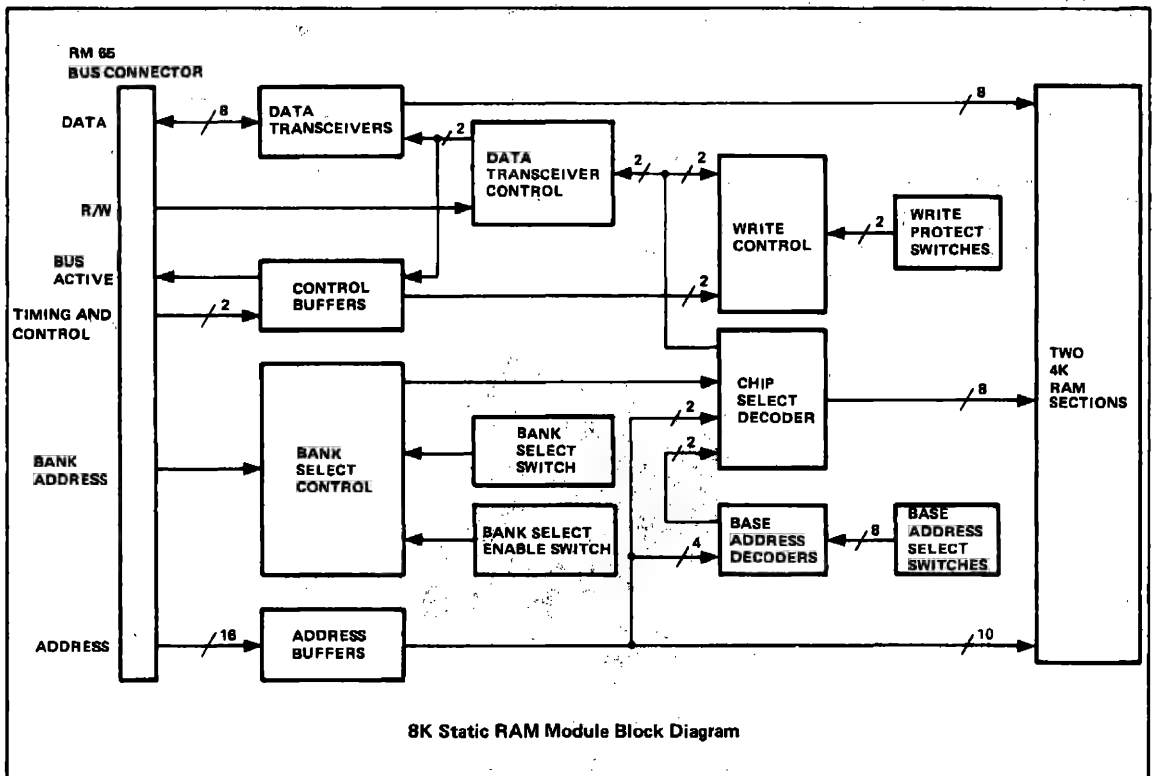
Two Base Address Decoders detect when either 4K RAM Section (1 or 2) is addressed, by comparing the address lines to

Base Address Select **switch** settings. When a match occurs, an enable signal is sent to the Chip Select Decoder.

The Chip Select Decoder uses outputs from the Bank Select Control circuit, the Base Address Decoders, and the PROM/ROM size jumpers as well as address lines A11 and A10 to generate one of eight chip select lines to the RAM devices. A signal indicating that a chip select line is active is also sent to the Write Control and Data Transceiver Control circuits.

The Write Control circuit generates the write enable signals to the RAM devices and to the Data Transceiver Control circuit. If the corresponding write protect switch is off, the write enable signal is activated. If the Write Protect switch is on, the Data Transceivers are disabled.

The Data Transceiver Control circuit determines whether a valid read or write operation is in progress, and provides transceiver enable and data direction signals to the Data Transceivers. The Data Transceivers are enabled if both the bank address and the address lines correspond to the selected bank and a selected base address, respectively.

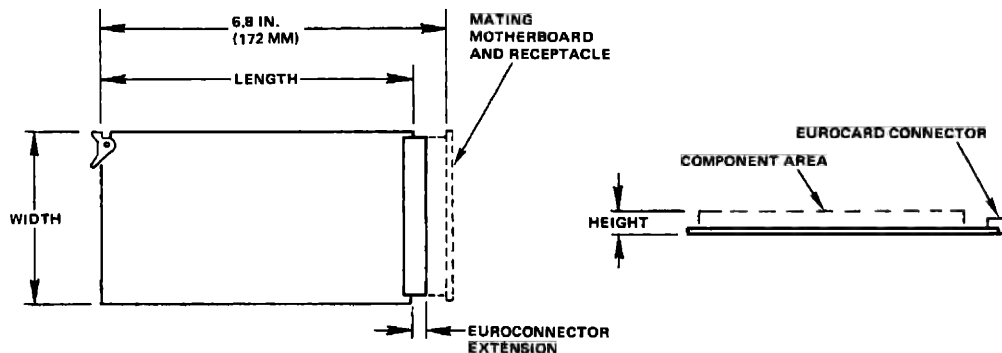


RM 65 Bus Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Pin	Signal Mnemonic	Signal Name	Input/Output	Pin	Signal Mnemonic	Signal Name	Input/Output
1a	GND	Ground		1c	+5V	+5 Vdc	
2a	BADR/	Buffered Bank Address	I	2c	BA15/	Buffered Address Bit 15	I
3a	GND	Ground		3c	BA14/	Buffered Address Bit 14	I
4a	BA13/	Buffered Address Bit 13	I	4c	BA12/	Buffered Address Bit 12	I
5a	BA11/	Buffered Address Bit 11	I	5c	GND	Ground	
6a	BA10/	Buffered Address Bit 10	I	6c	BA9/	Buffered Address Bit 9	I
7a	BA8/	Buffered Address Bit 8	I	7c	BA7/	Buffered Address Bit 7	I
8a	GND	Ground		8c	BA6/	Buffered Address Bit 6	I
9a	BA5/	Buffered Address Bit 5	I	9c	BA4/	Buffered Address Bit 4	I
10a	BA3/	Buffered Address Bit 3	I	10c	GND	Ground	
11a	BA2/	Buffered Address Bit 2	I	11c	BA1/	Buffered Address Bit 1	I
12a	BA0/	Buffered Address Bit 0	I	12c	B ϕ 1	*Buffered Phase 1 Clock	
13a	GND	Ground		13c	BSYNC	*Buffered Sync	
14a	BSO	*Buffered Set Overflow		14c	BDRQ1/	*Buffered DMA Request 1	
15a	BRDY	*Buffered Ready		15c	GND	Ground	
16a		*User Spare 1		16c	-12V/-V	*-12 Vdc/-V	
17a	+12V/+V	*+12 Vdc/+V		17c		*User Spare 2	
18a	GND	Ground Line		18c	BFLT/	*Buffered Bus Float	
19a	BDMT/	*Buffered DMA Terminate		19c	B ϕ 0	*Buffered External Phase 0 Clock	
20a		*User Spare 3		20c	GND	Ground	
21a	BR/W	Buffered Read/Write "Not"	I	21c	BDRQ2/	*Buffered DMA Request 2	
22a		*System Spare		22c	BR/W	Buffered Read/Write	I
23a	GND	Ground		23c	BACT/	Buffered Bus Active	O
24a	BIRQ/	*Buffered Interrupt Request		24c	BNM/	*Buffered Non-Maskable Interrupt	
25a	B ϕ 2/	Buffered Phase 2 "Not" Clock	I	25c	GND	Ground	
26a	B ϕ 2	*Buffered Phase 2 Clock		26c	BRES/	*Buffered Reset	
27a	BD7/	Buffered Data Bit 7	I/O	27c	BD6/	Buffered Data Bit 6	I/O
28a	GND	Ground		28c	BD5/	Buffered Data Bit 5	I/O
29a	BD4/	Buffered Data Bit 4	I/O	29c	BD3/	Buffered Data Bit 3	I/O
30a	BD2/	Buffered Data Bit 2	I/O	30c	GND	Ground	
31a	BD1/	Buffered Data Bit 1	I/O	31c	BD0/	Buffered Data Bit 0	I/O
32a	+5V	+5 Vdc		32c	GND	Ground	

Note:

*Not used on this module.



Module Dimensions

SPECIFICATIONS

Parameter	Value
Dimensions (See Notes)	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	5.3 oz. (145 g)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C
Relative Humidity	0% to 85% (Without condensation)
Power Requirements	+5 Vdc $\pm 5\%$ @ 1.0A (5.0W)—Typical 1.9A (9.5W)—Maximum
Access Time	450 ns—Maximum
RM 65 Bus Interface	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)
Notes: 1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.). 2. Length does not include the added extension due to the module ejector. 3. Dimensions conform to DIN 41612.	



RM65-3132E

RM 65 32K DYNAMIC RAM MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-3132E 32K Dynamic RAM Module is one of the hardware options available for the RM 65 Microcomputer Module Family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 module products use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The 32K Dynamic RAM module provides 32K bytes of read/write memory using 16 16K bit \times 1 dynamic RAM (DRAM) devices. Two bank select switches allow the board to be dedicated to either one of two 65K Banks, or to be assigned common to both banks. A 24-pin DIP header allows each of the eight 4K sections to be independently mapped into any 4K block of the selected 65K bank. The independent addressing of blocks provide flexibility with system memory maps. An on-board switch allows the entire board to be write-protected.

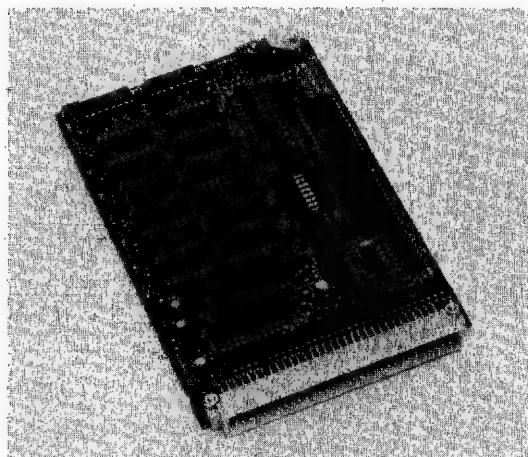
All refreshing of the dynamic RAM chips is automatic and completely transparent to the RM 65 Bus, thus providing low power performance at no loss of bus speed.

FEATURES

- Compact size—about 4" \times 6 $\frac{1}{4}$ " (100 mm \times 160 mm)
- Pin and socket bus connection
- RM 65 bus compatible
- Buffered data, address, and control lines
- Internal Refresh controller is completely transparent to the RM 65 bus
- On-board switch allows write protection
- Base Address Header allows each 4K memory section to be assigned to any 4K block as a selected bank
- Bank select switches allow the entire board to be mapped into either or both 65K banks
- On-board DC-DC converter for -5 volt power supply
- Requires +5 and +12 volt power from the RM 65 bus
- Fully assembled, tested, and warranted.

ORDERING INFORMATION

Part No.	Description
RM65-3132E	32K Dynamic RAM Module
RM65-3132NE	32K Dynamic RAM Module (without RAM devices installed)
Order No.	Description
808	32K Dynamic RAM Module User's Manual (included with RM65-3132E and RM65-3132NE)



RM65-3132E 32K Dynamic RAM Module

FUNCTIONAL DESCRIPTION

The Data Transceivers invert and transfer 8-bit parallel data between the selected DRAMs to the RM 65 bus. During a read operation, data from the DRAMs are latched and driven by the transceivers onto the RM 65 bus. During a write operation, data from the RM 65 bus drives the DRAMs. The transceivers are disabled when the module is not addressed.

The Address Buffers invert and transfer 16-bit parallel address lines from the RM 65 bus into the DRAM Module.

The Bank Select Control circuit detects when the DRAM module's assigned memory bank is addressed by comparing the bank address signal from the RM 65 bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch allows the board to reside in common memory (both Bank 0 and Bank 1) or only in the Bank set by the Bank Select switch (either Bank 0 or Bank 1).

The Control Buffers buffer the control and timing signals used from the RM 65 bus.

The DRAM devices require 3 voltages. Two of these (+5 and +12 volts) are available directly from the RM 65 bus. The third voltage (-5 volts) is generated on board with a DC/DC converter.

The Address Decoder uses the four MSB address lines to decode and enable one of 16 lines, each of which correspond to 4K blocks. The Base Address Selection Jumpers are placed in a 28 pin socket which consists of 16 lines from the Address Decoder, four lines from +5 volts, and 8 lines to the Base Address Encoder. The Base Address Selection is made by connecting each of the eight encoder inputs to any one of the 16 decoder outputs or to +5 volts. This allows each 4K block to be addressed anywhere in the selected 65K memory bank or dis-

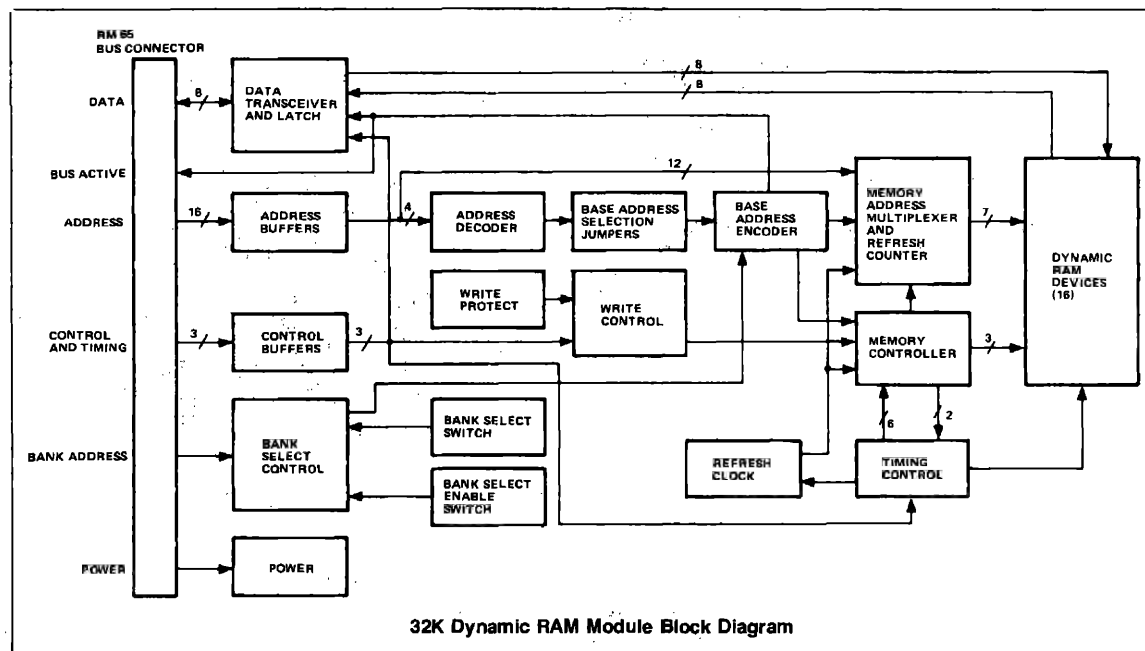
abled. The Base Address Encoder produces a 3 bit code for the enabled line and an additional signal for any line active (Board Select). The 3 bit code from the encoder becomes the 3 MSB address bits for the Memory Address Multiplexer. The Board Select line and a valid Bank Select signal are used to enable the Memory Controller and Data Transceivers, as well as create a Data Bus Active Signal.

The Write Control logic uses the Write Protect switch and the Read/Write line to enable writing into the DRAMs. If the Write Protect switch is off, the Read/Write signal is transferred directly to the Memory Controller. If the Write Protect switch is on, the Memory Controller forces a read operation so that the contents of the DRAMs will not be altered.

The Timing Control generates all the clocks required by the Memory Controller, Memory Address Multiplexer, and the Refresh Clock. The Refresh Clock generates a refresh cycle for every seven RM 65 clock cycles.

The Memory Controller uses the clocks derived in the timing control to sequence the signals to the DRAM devices. During normal read or write cycles, the Memory Controller allows Row Address, then Column Address information to be applied to the addressed DRAMs and generates the read/write signal. When a refresh is required, the timing is controlled so that the refresh is transparent to the RM 65 bus.

The Memory Address Multiplexer and Refresh Counter multiplexes Row, Column, or Refresh Addresses onto the DRAM address lines in response to the Memory Controller. There is also a Refresh Counter which is incremented by the Refresh Clock.



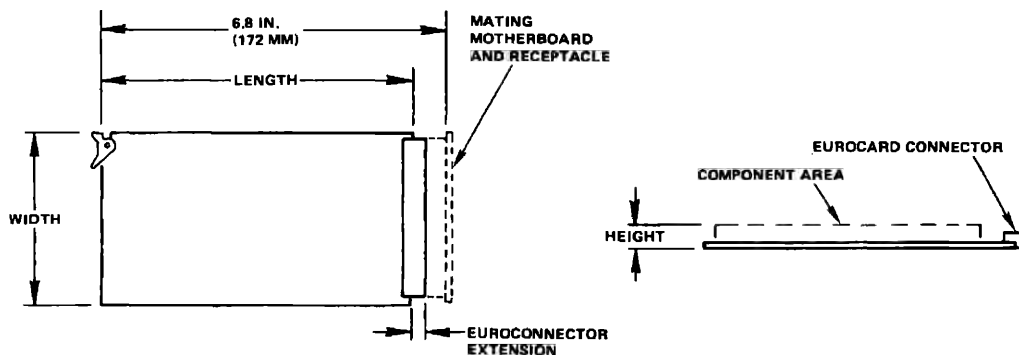
32K Dynamic RAM Module Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	B ϕ 1	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	*Buffered DMA Request 1
15a	BRDY	*Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	-12V/-V	*-12 Vdc/-V
17a	+12V/+V	+12 Vdc/+V	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	B ϕ 0	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR \overline{W} /	Buffered Read/Write "Not"	21c	BDRQ2/	*Buffered DMA Request 2
22a		*System Spare	22c	BR \overline{W}	Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	*Buffered Interrupt Request	24c	BNMI/	*Buffered Non-Maskable Interrupt
25a	B ϕ 2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	B ϕ 2	*Buffered Phase 2 Clock	26c	BRES/	*Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note:

*Not used on this module.



Module Dimensions

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3) Width Length Height	3.9 in. (100 mm) 6.3 in. (160 mm) 0.56 in. (14 mm)
Weight	4.5 oz. (140 g)
Environment Operating Temperature Storage Temperature Relative Humidity	0°C to 70°C -40°C to +85°C 0% to 85% (without condensation)
Power Requirements	+5 Vdc $\pm 5\%$ 1.4 A (7.0 W)—Maximum +12 Vdc $\pm 5\%$ 170 mA (2.1W)—Maximum
RM 65 Bus Interface	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)
Notes: 1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.). 2. Length does not include extensions beyond the edge of the module due to connectors or the module ejector. 3. Dimensions conform to DIN 41612.	



RM65-3216E

RM 65 16K PROM/ROM MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-3216E 16K PROM/ROM Module is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 module products use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

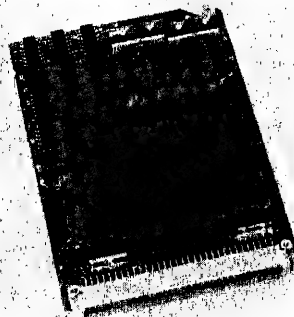
The RM 65 16K PROM/ROM Module has eight, 24-pin sockets to accept up to 16K bytes of either programmable read-only memory (PROM) or masked read-only memory (ROM) devices. On-board jumpers permit selection of 2K, 4K or 8K byte PROM/ROM devices. Switches allow setting of the starting address for independent 4K byte blocks of memory. All 16K bytes can be assigned to two memory banks, or 8K can be assigned to common memory while the other 8K can be dedicated to one or two 65K memory banks. Low power operation is jumper selectable for PROMs that have this option.

FEATURES

- Compact size—about 4" × 6¼" (100 mm × 160 mm)
- Pin and socket bus connection
- RM 65 Bus compatible
- Buffered address, data and control lines
- Supports the following PROMs/ROMs or equivalents:
Intel 2716 or 2732 PROMs
TI TMS 2516 or 2532 PROMs
Rockwell R2316, R2332 or R2364 ROMs
- Low-power PROM operation selectable by individual socket jumpers
- Jumpers allow selection of 2K, 4K or 8K byte devices
- Starting address selectable for each of four 4K memory blocks
- Separate switch allows 8K to be dedicated to one or two memory bank operation
- +5V operation
- Fully assembled, tested and warranted

ORDERING INFORMATION

Part No.	Description
RM65-3216E	16K PROM/ROM Module
Order No.	Description
806	16K PROM/ROM Module User's Manual (included with RM65-3216E)



RM65-3216E 16K PROM/ROM Module

FUNCTIONAL DESCRIPTION

The PROM/ROM module has eight 24-pin sockets which can accept up to 16K of either 2K, 4K, or 8K PROM or ROM.

The Data Buffers invert and transfer 8-bits of parallel data from the selected PROM/ROM devices to the RM 65 Bus during read operations.

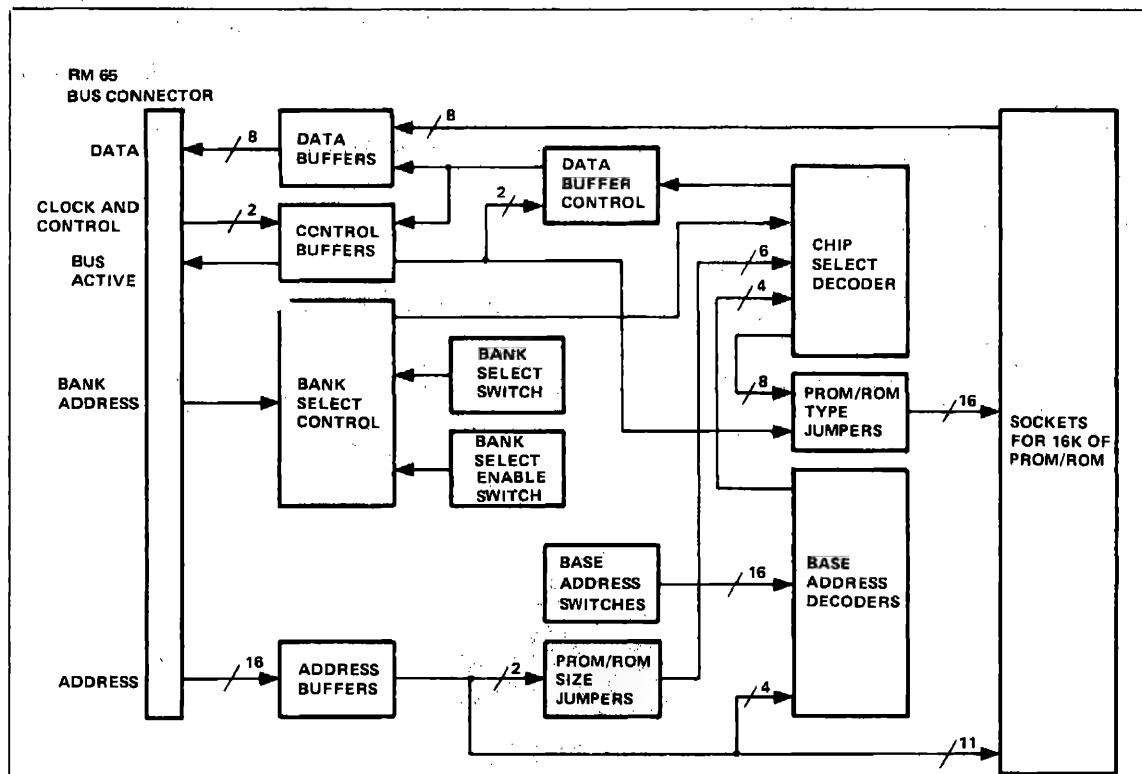
The Control Buffers invert and transfer phase 2 clock, and read/write control signals from the RM 65 Bus onto the PROM/ROM module, and drive the bus active signal onto the RM 65 Bus.

The Bank Select control circuit detects when the PROM/ROM module's assigned memory bank is addressed, by comparing the bank address signal from the RM 65 Bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch allows 8K of the PROM/ROM to be common memory (addressable in both Bank 0 and Bank 1) while the remaining 8K is assigned either to Bank 0 or Bank 1, as determined by the Bank Select switch.

Four Base Address Decoders allow 4K PROM/ROM sections to be independently addressed on any 4K boundary within the selected bank. When an address falls within any section (per the Base Address switches), an enable signal is sent to the Chip Select Decoder.

The Chip Select Decoder uses outputs from the Bank Select Control circuit, the Base Address Decoders, and the PROM/ROM size jumpers as well as the address lines to generate chip selects to the PROM/ROM devices. The PROM/ROM type jumpers route the chip select lines to the correct pins on the PROM/ROM sockets.

The Data Buffer Control circuit enables the Data Buffers during a read operation when an address corresponding to a selected base address is decoded and the selected PROM/ROM memory bank is addressed.



16K PROM/ROM Module Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Signal Mnemonic	Signal Name	Input/Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/Output
GND	Ground		1a	1c	+5V	+5 Vdc	
BADR/	Buffered Bank Address	I	2a	2c	BA15/	Buffered Address Bit 15	I
GND	Ground		3a	3c	BA14/	Buffered Address Bit 14	I
BA13/	Buffered Address Bit 13	I	4a	4c	BA12/	Buffered Address Bit 12	I
BA11/	Buffered Address Bit 11	I	5a	5c	GND	Ground	
BA10/	Buffered Address Bit 10	I	6a	6c	BA9/	Buffered Address Bit 9	I
BA8/	Buffered Address Bit 8	I	7a	7c	BA7/	Buffered Address Bit 7	I
GND	Ground		8a	8c	BA6/	Buffered Address Bit 6	I
BA5/	Buffered Address Bit 5	I	9a	9c	BA4/	Buffered Address Bit 4	I
BA3/	Buffered Address Bit 3	I	10a	10c	GND	Ground	
BA2/	Buffered Address Bit 2	I	11a	11c	BA1/	Buffered Address Bit 1	I
BA0/	Buffered Address Bit 0	I	12a	12c	Bφ1	*Buffered Phase 1 Clock	
GND	Ground		13a	13c	BSYNC	*Buffered Sync	
BSO	*Buffered Set Overflow		14a	14c	BDRQ1/	*Buffered DMA Request 1	
BRDY	*Buffered Ready		15a	15c	GND	Ground	
	*User Spare 1		16a	16c	-12V/-V	*-12 Vdc/-V	
+12V/+V	*+12 Vdc/+V		17a	17c		*User Spare 2	
GND	Ground Line		18a	18c	BFLT/	*Buffered Bus Float	
BDMT/	*Buffered DMA Terminate		19a	19c	Bφ0	*Buffered External Phase 0 Clock	
	*User Spare 3		20a	20c	GND	Ground	
BR/W/	*Buffered Read/Write "Not"	I	21a	21c	BDRQ2/	*Buffered DMA Request 2	
	*System Spare		22a	22c	BR/W/	Buffered Read/Write	I
GND	Ground		23a	23c	BACT/	Buffered Bus Active	O
BIRQ/	*Buffered Interrupt Request		24a	24c	BNMI/	*Buffered Non-Maskable Interrupt	
Bφ2/	*Buffered Phase 2 "Not" Clock		25a	25c	GND	Ground	
Bφ2	*Buffered Phase 2 Clock		26a	26c	BRES/	*Buffered Reset	
BD7/	Buffered Data Bit 7	O	27a	27c	BD6/	Buffered Data Bit 6	O
GND	Ground		28a	28c	BD5/	Buffered Data Bit 5	O
BD4/	Buffered Data Bit 4	O	29a	29c	BD3/	Buffered Data Bit 3	O
BD2/	Buffered Data Bit 2	O	30a	30c	GND	Ground	
BD1/	Buffered Data Bit 1	O	31a	31c	BD0/	Buffered Data Bit 0	O
	Not Connected (See Note)		Za	Zc		Not Connected (See Note)	

Note:

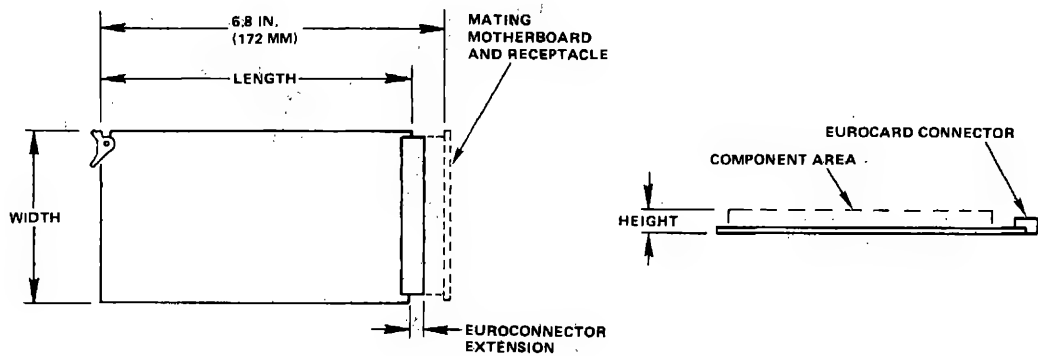
*Not used on the 16K PROM/ROM module.

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3)	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	5.0 oz. (140 g)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	
w/o PROM/ROM Devices	+5 Vdc $\pm 5\%$ 0.17A (0.85W)—Typical 0.27A (1.35W)—Maximum
Access Time	450 nanoseconds (max)
RM 65 Bus Interface	
Edge Connector Version	72-pin edge connector (0.100 in. centers)
Eurocard Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)

Notes:

- Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
- Length does not include the added extension due to the module ejector.
- Dimensions conform to DIN 41612.



Module Dimensions



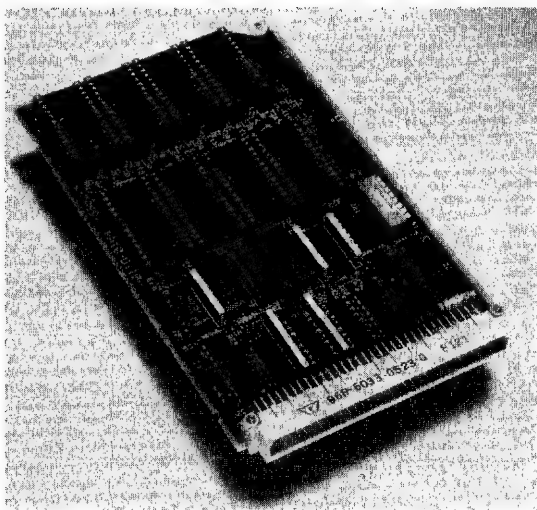
RM65-3264NE UNIVERSAL MEMORY MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-3264NE Universal Memory Module (16K-128K) is one of the hardware options available for the RM 65 Microcomputer Module Family.

RM 65 Microcomputer Modules are designed for OEM and end user microcomputer applications when state-of-the-art performance, compact size, modular design, and low cost are required. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC, and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 Modules plug into a motherboard designed to accept any card in any slot. The 64-line RM 65 Bus accommodates memory addressing up to 128K bytes, provides high immunity to electrical noise, and includes growth provisions for user functions. A selection of card cages permit packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 or AIM 65/40 Microcomputers for product development and for portable or desktop microcomputer applications.



RM65-3264NE Universal Memory Module

FEATURES

- In the high speed mode, supports Rockwell Design Center 4 MHz RAM operations
- In the universal memory mode, supports 2K, 4K, 8K, and 16K byte-wide memory devices
- On-board header and shunt configure the module into a 2K to 128K memory space
- Each half (four device sockets) independently configurable in the universal memory mode
- On-board memory bank select switches assign each half of the module to either one or both of two 64K memory banks
- On-board ROM select switches serve as write-protect switches for each half of the memory in universal memory mode
- Rockwell RM 65 Bus compatible
- Compact size—100 mm × 167 mm (approximately 4 in. × 6.3 in.)
- Operates from a single +5V power source
- Fully assembled (except for user-supplied memory devices), tested and warranted
- Supports 16K of 2K devices, 32K of 4K devices, 64K of 8K devices, and 128K of 16K devices in universal memory mode
- Supports 64K of 8K devices in high speed mode (refer to Devices Supported for part numbers)

OVERVIEW

Two major capabilities are provided in the Universal Memory Module: the flexibility of using 2K, 4K, 8K, or 16K memory devices on the module, and use of the memory in either a high-speed mode or a universal memory mode. Typical data-transfer rates are up to 4 MHz (to support the Rockwell Design Center (RDC) System) in the high speed mode and 1- to 2-MHz in the universal memory mode. Rates are dependent both on memory devices used and system configuration. Memory devices that can be used with the module are RAM's, ROM's, EPROM's, and EEPROM's.

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ORDERING INFORMATION

Part No.	Description
RM65-3264NE	Universal Memory Module

FUNCTIONAL DESCRIPTION

Data Bus Transceivers buffer and invert data signals BD0/ through BD7/. Data signals from the RM 65 Bus pass through the bidirectional transceivers into the module during a write operation and out from the module through the transceivers to the RM 65 Bus during a read operation. Data in is inverted for use in the module, and data out (from the module) is inverted for use on the RM 65 Bus. Transfers occur when any of the chip-select signals and the $\phi 2$ clock pulse are in the active states concurrently. Direction of data flow either into or out of the module is controlled by the R/W signal state.

Address and Control Buffer logic consists of inverters that buffer address signals BA0/ through BA13/ and the read/write signal BR/W/. These signals are converted to positive signals BA0 through BA13 and BR/W for use within the module.

Bank Address Select logic is controlled by the state of the BADDR/ signal, which functions as a seventeenth address bit. The state of the BADDR/ signal indicates which of the two 65K memory banks is addressed. In the high speed memory mode, the module can be configured to operate in either one or both 65K memory banks. In the universal memory mode, each half of the memory is configurable to either one or both 65K memory banks.

Module Active logic is enabled when any chip-select signal is enabled. Thus, when any memory device in either Memory A or Memory B is enabled by a chip-select signal, the BACT/, or Module Active, signal is in the active state.

Address signals BA13/, BA14/, and BA15/, in conjunction with B0, are decoded by a 3:8 decoder to enable one of eight possible outputs. Each output signal in a low state indicates an 8K address boundary signal. Thus, the 8K address boundaries are \$0000, \$2000, \$4000, . . . \$E000. Each of these signals is used as a memory chip-select signal during operation of the memory in the high-speed mode and as a 2K, 4K, 8K, and 16K decoder enabling signal in the universal memory mode.

By connecting a pin on the Address Header to a specific output (chip select) pin from the 8K Decoder, that 8K address boundary signal is connected to one specific memory device (in one of the eight memory device sockets) only in high speed mode.

The module can be used either as a high speed memory or as a universal memory. The removable 16-pin 8-position shunt is placed either in the High Speed Option Shunt socket for high speed memory operation, or in the Universal Memory Option Shunt socket for universal memory operation. In the high speed mode, Memory A Decoder and Memory B Decoder are not used, and the address (chip-select) signal from the Address Header is applied directly to the applicable Memory A or Memory B devices. As a result, decoding time is saved.

Memory A consists of 2K, 4K, 8K, or 16K memory devices installed in the four sockets assigned as Memory A. Memory B also consists of memory devices located in four sockets designated as Memory B. Thus, the capacity of Memory A or Memory B is dependent on the capacity of the memory devices installed in each socket. Each of the two groups of four sockets can be configured with jumpers to accept one of the four types (2K, 4K, 8K, or 16K) of memory devices. Each memory device in the memory sockets in Memory A or Memory B must have the same capacity.

Device Select A consists of jumpers E3, E4, and E7 through E10 determine the particular type memory device (2K, 4K, 8K, or 16K) installed in the Memory A sockets. Similarly, Device Select B jumpers E5, E6, and E11 through E14 determine memory device types in Memory B.

Memory A Decoder is a programmable array logic (PAL) device internally configured to decode a combination of input signals and generate one output (chip-select) signal. Memory Decoders A and B are used only when the module is being operated in the universal memory mode. Both decoders operate in the same manner, but only one is used at a time. Thus, when Memory A is addressed, Memory Decoder A is used, and Memory Decoder B when Memory B is addressed.

DEVICES SUPPORTED

In the universal memory mode, the following is a partial list of devices supported:

16K of the following 2K devices:

R2316	ROM-Rockwell
2716	EPROM-Intel
2516	EPROM-TI
2016	RAM-Toshiba
5516	RAM-Toshiba
6116	RAM-Hitachi
R5213/2816	EEPROM-Rockwell
X2816	EEPROM-XICOR

32K of the following 4K devices:

R2332	ROM-Rockwell
2732A	ROM-Intel
2532 (350ns)	ROM-TI

64K of the following 8K devices:

R2364A, R2364B	ROM-Rockwell
68A764	EPROM-Motorola
68766	EPROM-Motorola
2764	EPROM-Intel
5564	RAM-Toshiba
6264	RAM-Hitachi
8464	RAM-Fujitsu

128K of the following 16K devices:

R23128	ROM-Rockwell
27128	EPROM-Intel

In the high speed mode, the following is a partial list of devices supported:

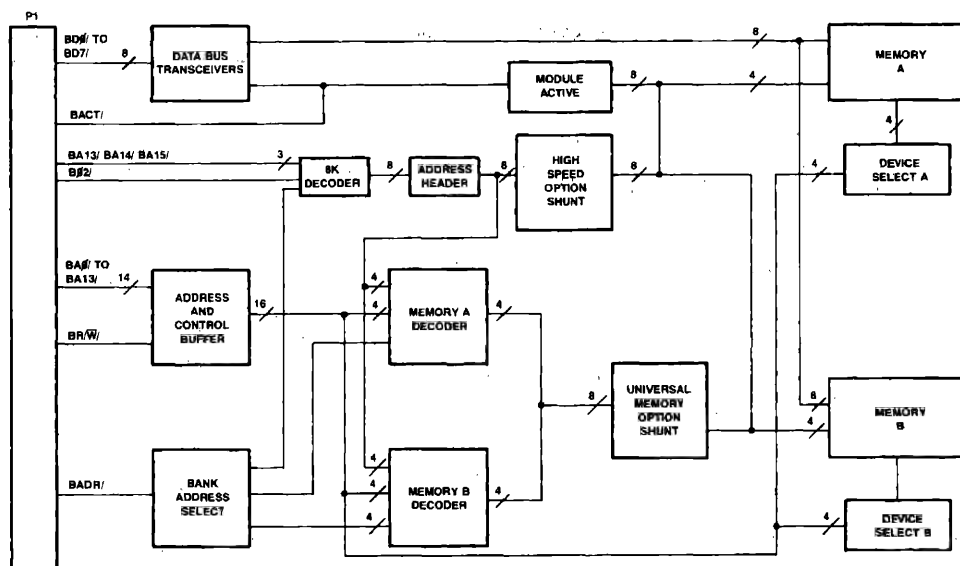
64K of the following 8K devices:

R2364A, R2364B	ROM-Rockwell
68A764	EPROM-Motorola
68766	EPROM-Motorola
2764	EPROM-Intel
5564	RAM-Toshiba
6264	RAM-Hitachi
8464	RAM-Fujitsu

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	B ϕ 1	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	*Buffered DMA Request 1
15a	BRDY	*Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	-12V/-V	*-12 Vdc/-V
17a	+12V/+V	*+12 Vdc/+V	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	B ϕ 0	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR/W/	Buffered Read/Write "Not"	21c	BDRQ2/	*Buffered DMA Request 2
22a		*System Spare	22c	BR/W/	*Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	*Buffered Interrupt Request	24c	BNMI/	*Buffered Non-Maskable Interrupt
25a	B ϕ 2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	B ϕ 2	Buffered Phase 2 Clock	26c	BRES/	*Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note: *Not used on this module



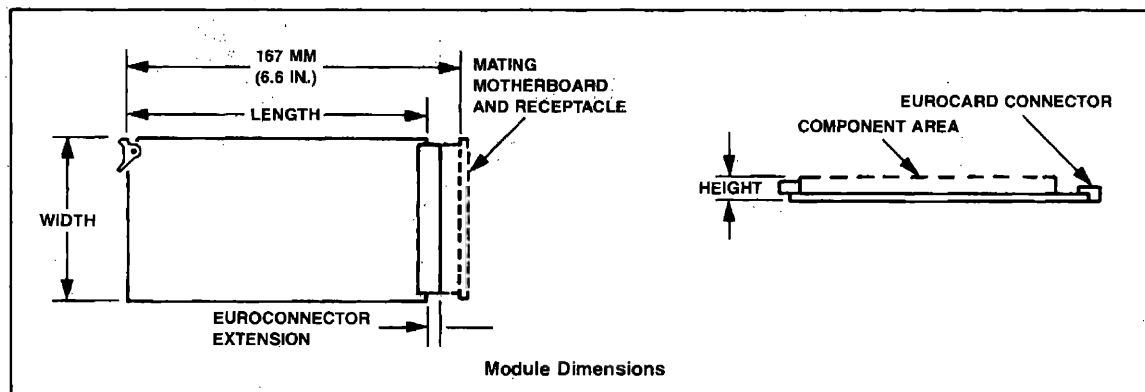
Universal Memory Module Block Diagram

SPECIFICATIONS

Parameter	Value
Dimensions^(1,2,3)	
Width	100 mm (3.94 in.)
Length	160 mm (6.3 in.)
Height	14 mm (0.56 in.)
Weight	156 g (5.5 oz.)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to 85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	5.0V (420 ma. typical, 640 ma. maximum with no memory devices installed)
Connector RM 65 Bus Connector P1	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)—mates with Burndy P196B32R00A00L-9 or equivalent.

Notes:

1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. Length does not include the added extension due to the module ejector.
3. Dimensions conform to DIN 41612.





RM65-5101E RM 65 FLOPPY DISK CONTROLLER (FDC) MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-5101E Floppy Disk Controller Module is one of the hardware options available for the RM 65 Microcomputer Module family.

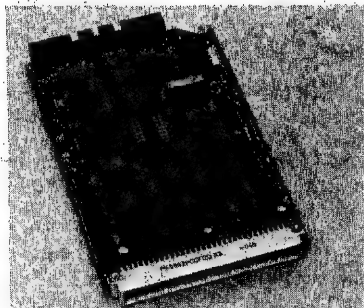
RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 modules use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The RM 65 Floppy Disk Controller (FDC) Module controls up to four standard (8") or mini- (5¼") floppy disk drives, single or double sided, soft sector with either single density (FM) or double density (MFM) format. Software control of media density allows single or double density disks to be used in any connected drives.

Two DIP headers configure the FDC to interface with either standard or mini-floppy disk drives. An on-board jumper selects single or double sided drives and a switch disables on-board ROM. The FDC directly interfaces to most popular drives with only switch and/or header changes. Bank Select and Bank Select Enable switches allow the FDC module to be dedicated to one of two 65K memory banks or assigned common to both banks. The FDC module I/O can be assigned to any page (256 bytes) using a standard PROM if the ROM is deselected.



RM65-5101E Floppy Disk Controller (FDC) Module

FEATURES

- Compact size—about 4" × 6¼" (100 mm × 160 mm)
- Pin and socket bus connection
- RM 65 Bus compatible
- Buffered address, data and control lines
- Supports single or double sided, standard or mini-floppy disk drives
- Controls up to four disk drives
- Interfaces directly to Shugart SA-850 or SA-450 disk drives, with user options for other popular floppy disk drives
- Supports single-density IBM 3740 (FM) or double-density IBM System 34 (MFM) formats
- DMA data transfer capability
- Supports interrupt-driven or polled operation
- Bipolar PROM Base Address decoding
- Switches or jumpers for
 - Bank Selection to one or two banks
 - Double or Single sided operation
 - Select or deselect ROM
 - Module disable
- On-board header configures I/O for 8" or 5¼" drive interface
- Fully assembled, tested and warranted

ORDERING INFORMATION

Part No.	Description
RM65-5101E	Floppy Disk Controller (FDC) Module with on-board ROM*
RM65-5101NE	Floppy Disk Controller (FDC) Module without on-board ROM
A65-090	AIM 65 DOS 1.0 ROM**
A65/40-7090	AIM 65/40 DOS 1.0 ROM**
Order No.	Description
802	FDC Module User's Manual (included with RM65-5101E, RM65-5101NE, A65-090 and A65/40-7090)

*ROM contains FDC module primitive subroutines only.
 **ROM contains FDC module primitive subroutines and operator selectable file management functions integrated with host computer I/O functions.

9

FUNCTIONAL DESCRIPTION

The Data Transceivers invert and transfer 8-bits of parallel data between the FDC module and the RM 65 bus, based on control signals from the Base Address Decoder and the Control Buffers. The read/write control line determines the direction, while the bus active enables the Data Transceivers.

The Address Buffers invert and transfer 12 of the 16 parallel address lines from the RM 65 bus to the Base Address Decoder, the Program ROM and the Floppy Disk Controller (FDC) device.

The Control Buffers invert and transfer phase 2 clock, reset, and read/write control signals from the RM 65 bus onto the module.

The Bank Select Control circuit detects when the module's assigned memory bank is addressed by comparing the bank address signal from the RM 65 bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch assigns the module to be active in common memory (both Bank 0 and Bank 1) or only in the Bank set by the Bank Select switch (either Bank 0 or Bank 1).

The Interrupt and DMA Control circuit enables operation in either an interrupt driven mode or under DMA control. Both Interrupt generation and DMA requests can be disabled under program control. The DMA request is jumper selectable for either of two DMA request lines connected to the RM 65 bus.

The Base Address Decoder, with the Base Address Select PROM, the Bank Select Control circuit, the ROM Disable switch, and the phase 2 and read/write signals control device selection on the module. The Base Address Select PROM compares the eight most significant address lines to the programmed addresses to generate device select signals to the Program ROM and the I/O devices. The ROM Disable switch assigns the module to be active either in a 256 byte page (disabled) or in a 4K byte block (enabled). A separate Module Disable switch allows the entire module to be disabled.

When the ROM is disabled, only the I/O devices are active, in the 256 byte page that matches all eight Base Address Select bits. For the I/O devices, the three least significant address lines, along with the phase 2 clock and read/write control signals, drive register select lines to the FDC device, and device select lines to the Drive Status Buffer and Drive Control Register.

When the ROM is enabled, the module is active in the 4K byte block that matches the four most significant Base Address select bits. The program ROM is selected except when the address matches the four least significant Base Address Select bits, in which case the I/O device select lines are selected.

The Controller Clock derives a reference frequency for the FDC device from a crystal controlled oscillator. The frequency is 1 MHz or 2 MHz, depending on the Drive Configuration Header position.

The FDC device, in conjunction with the Data Separator and Precompensation Circuitry, interfaces the RM 65 bus to the Floppy Disk medium. The circuitry supports 5¼" or 8", single or double sided disk drives, with choice of single or double den-

sity, soft sector formats. The FDC features powerful commands, including single or multiple record read/write with selectable record lengths. Write precompensation circuitry ensures reliable data recovery in double density formats. The Precompensation jumper selects precompensation on all tracks, only on tracks 44 and greater, or no precompensation at all.

The Drive Configuration header selects the I/O connector and FDC circuitry for either 5¼" mini-floppy or 8" standard floppy disk formats. The 50-pin I/O receptacle connects the FDC module to a mass terminated cable connected to the installed disk drives. A 34-pin cable and mating connector can be used to connect the 5¼" mini-floppy drives while a 50-pin cable and mating connector is needed to connect to the 8" floppy drives.

The Drive Status Buffer allows detection of the Drive Configuration header and Single/Double Sided Drive jumper positions, as well as selected density and side information.

The Drive Control Register provides control of the side and drive selection, motor on, head load, double density, and interrupt disable. The Active Side 0 Level jumper allows the use of various drives without modification.

The Ready State Generator provides wait states as required by the FDC device.

The Program ROM contains primitive subroutines to support operations with up to four disk drives (single or double side, single or double density), including:

Format a Disk	Read or Write Multiple Sectors
Read or Write a Sector	Read or Write a Track
Seek or Verify Seek of a Track	Turn Motors On or Off
Restore the Head	Select or De-select any Drive

A user-provided program may call these subroutines to build an application dependent file-handling system.

OPTIONAL DISK OPERATING SYSTEM (DOS) FIRMWARE

Two optional ROMs are available that integrate the FDC primitive subroutines with operator selectable file management functions for operation on the AIM 65 and AIM 65/40 microcomputers. Either of these ROMs may be installed into the PROM/ROM socket on the FDC module to provide a firmware based Disk Operating System (DOS).

This version 1.0 ROM-based system offers the same convenience as the other AIM 65 and AIM 65/40 firmware in that it is immediately available for use through the Debug Monitor/Text Editor upon power turn-on. Mass storage operation may, therefore, proceed without waiting for loading of the DOS into RAM.

Text and program source code may be written to, and read from, disk with the Editor LIST (L) and READ (R) commands, respectively. Similarly, binary data and program object code may be written to, and loaded from, disk using the Monitor DUMP (D) and LOAD (L) commands, respectively. AIM 65 and AIM 65/40

Assembler and PL/65 files, both source and object code, are therefore supported. AIM 65 and AIM 65/40 BASIC programs may also be saved on, and loaded from disk.

The primary DOS commands are:

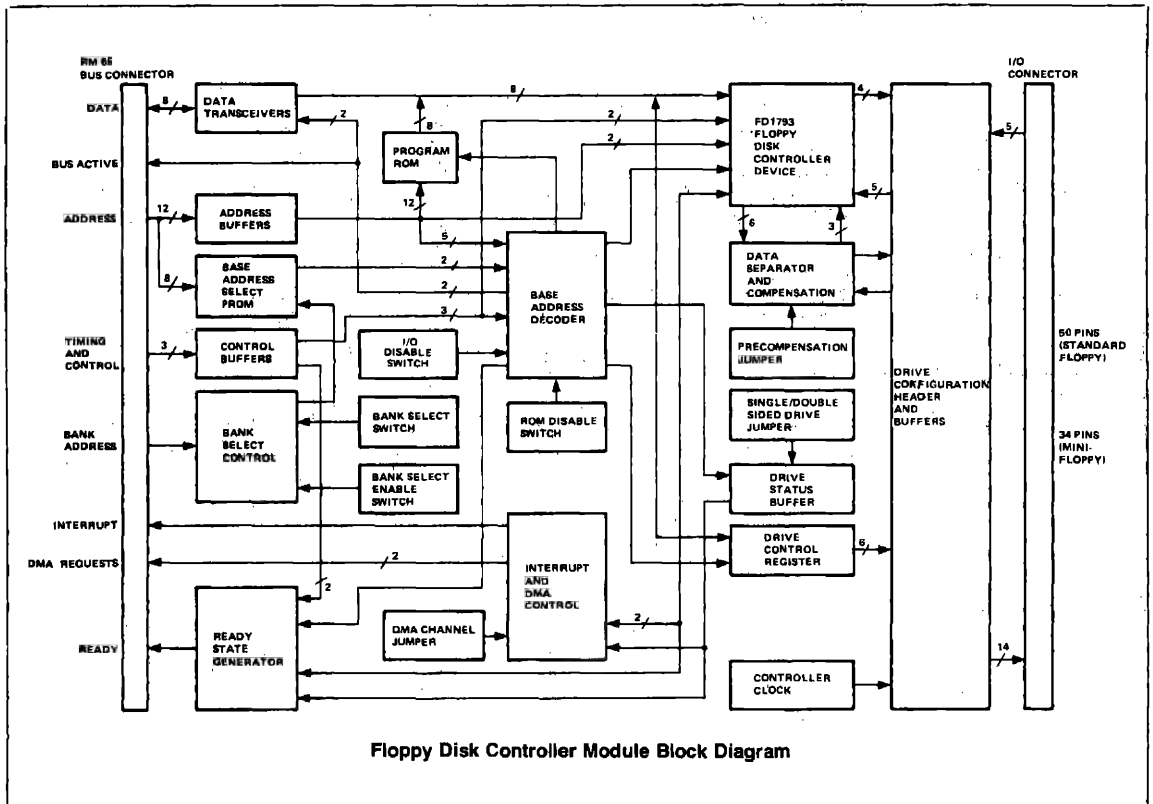
Format a Disk	Delete a File Name
List the Directory	Recover a File Name
List a File	Backup a Disk

Files are created automatically upon writing a file to disk. A file name (up to 10 characters in length) and the disk drive number (from 1 to 8) are operator entered in response to system prompts. (Double-sided drives are treated as two separate sides.)

The disk format function initializes a disk depending upon size, density and drive number. 5¼" and 8" disks are initialized to 35 and 77 tracks, respectively, however these values are user-alterable.

The contents of a file may be listed to another peripheral, including a file on another disk drive to allow copying of a file. All the active files on a disk may be copied to another disk using the backup function.

A file may be deleted (if active) to prevent it from being accessed or recovered (if deleted) to allow it to be accessed.



RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADF/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	Bφ1	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	Buffered DMA Request 1
15a	BRDY	Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	-12V/-V	*-12 Vdc/-V
17a	+12V/+V	+12 Vdc	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	Bφ0	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR/W/	Buffered Read/Write "Not"	21c	BDRQ2/	Buffered DMA Request 2
22a		*System Spare	22c	BR/W/	*Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request	24c	BNMI/	*Buffered Non-Maskable Interrupt
25a	Bφ2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	Bφ2	*Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

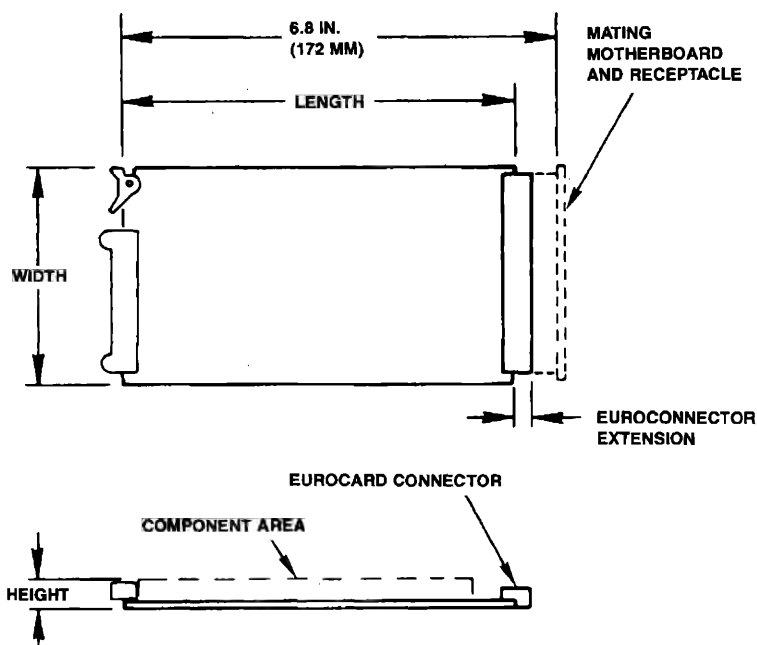
Note:
*Not used on this module.

I/O Connector Pin Assignments

FDC Module I/O Connector Pin	Standard Floppy Disk Drive Interface Cable Connector		Mini-Floppy Disk Drive Interface Cable Connector (2)	
	Pin	Signal Name	Pin	Signal Name
2	2	Track > 43 (Remex & MFE or equivalents)		
4	4	N.C.		
6	6	N.C.		
8	8	Track > 43 (Caldisk or equivalents)		
10	10	N.C.		
12	12	N.C.		
14	14	2nd Side Select		
16	16	N.C.		
18	18	Head Load	2	N.C.
20	20	Index	4	N.C.
22	22	Drive Ready	6	Drive Select #4
24	24	N.C.	8	Index
26	26	Drive Select #1	10	Drive Select #1
28	28	Drive Select #2	12	Drive Select #2
30	30	Drive Select #3	14	Drive Select #3
32	32	Drive Select #4	16	Motor On
34	34	Direction In	18	Direction In
36	36	Step Pulse	20	Step Pulse
38	38	Write Data	22	Write Data
40	40	Write Gate	24	Write Gate
42	42	Track Zero	26	Track Zero
44	44	Write Protected	28	Write Protected
46	46	Read Data	30	Read Data
48	48	N.C.	32	2nd Side Select
50	50	N.C.	34	N.C.

Notes:

1. All odd numbered pins are GND.
2. Pin 1 of the 34-pin mini-floppy disk drive interface cable connector should be keyed to pin 17 of the FDC module I/O connector.



Floppy Disk Controller Module Dimensions

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3)	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	5.2 oz. (145 g)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C
Relative Humidity	0% to 85% (Without condensation)
Power Requirements	
	+5 Vdc $\pm 5\%$ @ 600 mA—Typical 900 mA—Maximum
	+12 Vdc $\pm 5\%$ @ 60 mA—Typical 100 mA—Maximum
Interfaces	
RM 65 Bus Interface	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)
I/O Connector	50-pin mass terminated connector (0.100 in. centers) Mates with I&B/Ansley Part No. 609-5001M or equivalent
Notes: 1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.). 2. Length does not include the added extension due to the module ejector. 3. Dimensions conform to DIN 41612.	



RM65-5102E RM 65 CRT CONTROLLER (CRTC) MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-5102E CRT Controller Module is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 modules use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The CRT Controller (CRTC) Module interfaces the RM 65 to a CRT monitor or television receiver. The CRTC module outputs HSYNC, VSYNC, and raw video signals for direct connection to a CRT Monitor, and composite video for connection to a CRT monitor or to a TV receiver through an RF modulator. A socketed on-board ROM generates 5 × 7 characters with two descenders in a 7 × 10 dot matrix field to provide upper and lower case alphanumerics and special symbols. The 2K bytes of on-board display RAM are memory-mapped.

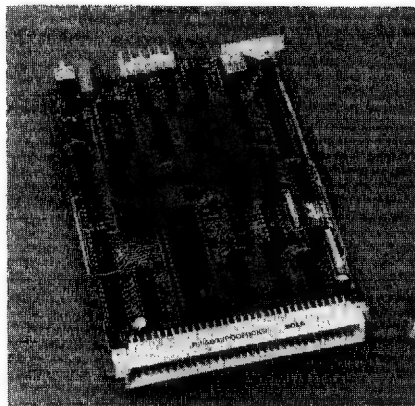
A 2K-byte program ROM provides firmware to configure the display format for 80 columns by 25 rows or 40 columns by 16 rows, scan rate of 50 or 60 Hz, and a CRT display driver for AIM 65. There are also cursor control, screen editing, and utility routines.

ORDERING INFORMATION

Part No.	Description
RM65-5102E	CRT Controller (CRTC) Module
Order No.	Description
814	CRT Controller (CRTC) Module User's Manual (included with RM65-5102E)

FEATURES

- Compact size—about 4" × 6¼" (100 mm × 160 mm)
- RM 65 bus compatible
- 4K Byte character generator ROM with:
 - Upper and lower case alphabetics
 - Special characters
 - Numbers including subscripts and superscripts
 - Math symbols
 - Semi-graphics
- On-board ROM firmware supports:
 - Scrolling
 - Screen editing
 - Full cursor movement control
 - Full screen standard or inverse video
 - Predefined formats for
 - 80 column by 25 row (50/60 Hz)
 - 72 column by 22 row (50/60 Hz)
 - 40 column by 25 row (60 Hz)
 - 40 column by 16 row (60 Hz)
 - Selectable format from 1 to 80 columns by 1 to 25 rows
 - NTSC (60 Hz, 525 lines per frame) and European (50 Hz, 625 lines per frame) raster format
 - CRT display driver for AIM 65
- Single 5 volt operation
- Fully assembled, tested and warranted



RM65-5102E CRT Controller (CRTC) Module

FUNCTIONAL DESCRIPTION

The Data Transceivers invert and transfer 8 bits of parallel data between the CRTC Module and the RM 65 bus, based on control signals from the Base Address Decoder and the Control Buffers. The read/write control line determines the direction, while the bus active enables the Data Transceivers.

The Address Buffers invert and transfer the 16-bit parallel address lines from the RM 65 bus to the Base Address Decoders, the R2316 ROM, the CRT Controller (CRTC) device, and to the Refresh RAM device.

The Control Buffers invert and transfer the phase 2 clock and read/write control signals from the RM 65 bus onto the module.

The Bank Select Control circuit detects when the module's assigned memory bank is addressed, by comparing the bank address signal from the RM 65 bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch allows the board to reside in common memory (both Bank 0 and Bank 1) or only in the Bank set by the Bank Select switch (either Bank 0 or Bank 1).

The Base Address Decoder, with the Base Address Select switches, the Bank Select Control circuit, the ROM Disable Switch and the read/write and phase 2 clock signals, generates device selects for the on-board ROM, RAM, and I/O (CRTC device and Display Enable Status Buffer). The Base Address Select switches allow the module to be selected to any 4K block. Within the selected 4K block, the RAM is assigned to the lower 8 pages (2K bytes), and the I/O to the first 256 byte page of the upper 2K bytes. When the ROM is disabled, only the RAM and I/O can be selected and the module is assigned 9 pages (2304 bytes) in memory. When the ROM is enabled, the module is assigned the full 4K bytes, with 7 pages for ROM, in addition to the RAM and I/O.

The Controller Clock uses a crystal-controlled oscillator to derive a 6 MHz or 12 MHz reference for the shift register dot clock depending on the Dot Clock Select jumper position. With the 6 MHz clock, up to 40 characters per line can be displayed on any monitor or standard television using an RF modulator. Up to 80 characters per line can be achieved with the 12 MHz clock and a high bandwidth monitor. The dot clock is divided by seven to provide a Character Clock for the CRTC device and a load character signal for the shift register.

The Refresh RAM provides 2K bytes of display memory, for screen densities of up to 25 lines with as many as 80 characters each. The RAM is directly mapped into the RM 65 memory map,

so the display can be updated by a block memory move or under DMA control. The Refresh RAM Multiplexer and RAM Transceiver allow the RM 65 bus and the CRTC device to both access the Refresh RAM, with the RM 65 bus having priority when any conflict occurs.

The Display Enable Status Buffer allows the RM 65 bus to monitor the active display times, so that display memory transfers can be made with no visible distortion.

The Character Generator ROM holds the fonts for the character set. These fonts are stored as 256 characters, each with 10 seven-bit rows. The four CRTC device row address lines and the eight Character Latch bits, which hold the character being refreshed, create an address for the character generator ROM. The output data of the ROM, which is seven parallel bits, represents the display pattern. The Shift Register takes this data and forms the serial video data. The Video Summer combines and buffers the serial video data with CRTC device timing signals to form a composite video output and a separate video, horizontal sync, and vertical sync.

The Program ROM contains the firmware for an intelligent CRT driver, in addition to utilities to aid in custom CRT display application software. There are six predefined screen formats, including 25 lines of 80 characters (50 or 60 Hz), 22 lines of 72 characters (50 or 60 Hz), 25 lines of 40 characters (50 Hz), and 16 lines of 40 characters (60 Hz). For other formats, any dimensions from 1 to 25 lines of from 1 to 80 characters can be defined (50 or 60 Hz). Full screen inverse video and 256 display characters allow flexible display capabilities.

The intelligent display driver controls all screen updating and cursor movement for the selected screen format. The cursor can be on, off, or blinking with movements including up, down, left, right, home, and carriage return, as well as to any row and column position. There are many commands to facilitate screen editing, such as:

- Insert character or line
- Delete character or line
- Clear to end of line
- Clear to end of screen
- Clear line or screen
- Set or Clear special character mode

The firmware utilities are useful for special applications. There is also a display driver which replaces the AIM 65 on-board display with a CRT monitor and an AIM 65 Assembler listing reformat which takes advantage of the longer display lines.

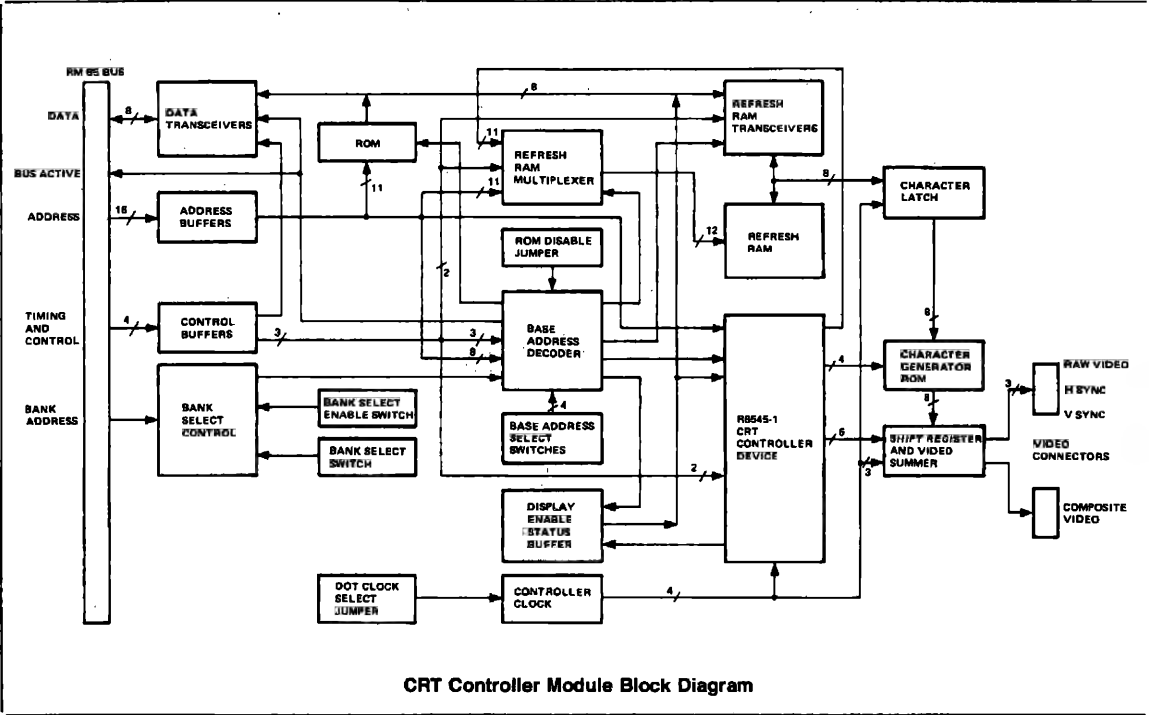
RM 65 CRTC Control Commands

Hex Code	Character	Description	Hex Code	Character	Description
00	CTRL @	*	10	CTRL P	Pass Through Next Character
01	CTRL A	Clear Line	11	CTRL Q	*
02	CTRL B	Clear to End of Line	12	CTRL R	*
03	CTRL C	Clear Screen	13	CTRL S	Toggle Insert Character Mode
04	CTRL D	Clear to End of Screen	14	CTRL T	Delete One Character
05	CTRL E	Clear Screen	15	CTRL U	Insert One Line
06	CTRL F	Clear to End of Screen	16	CTRL V	Delete One Line
07	CTRL G	*	17	CTRL W	Display Cursor
08	CTRL H	Backspace (←)	18	CTRL X	Blank Cursor
09	CTRL I	Horizontal Tab (→)	19	CTRL Y	Relink AIM 65 Display
0A	CTRL J	Line Feed (↓)	1A	CTRL Z	*
0B	CTRL K	Vertical Tab (↓)	1B	CTRL [Escape Character (ESC) (1)
0C	CTRL L	Form Feed (Clear Screen)	1C	CTRL \	Blinking Cursor
0D	CTRL M	Carriage Return (Home on Line)	1D	CTRL]	Enter Normal Characters
0E	CTRL N	Home on Screen	1E	CTRL ^	Perform Self Test
0F	CTRL O	Home on Screen	1F	CTRL _	Reverse Video

*These characters have no effect.

(1) There are two escape sequences as follows:

Hex Code	Character Sequence	Function
1B 3D YY XX	ESC = y x	Move the cursor to the row y and column x position, with row y between top (\$00) and bottom (\$19), and column x between leftmost (\$00) and rightmost (\$4F).
1B 47	ESC G	Enter Graphics Character Mode

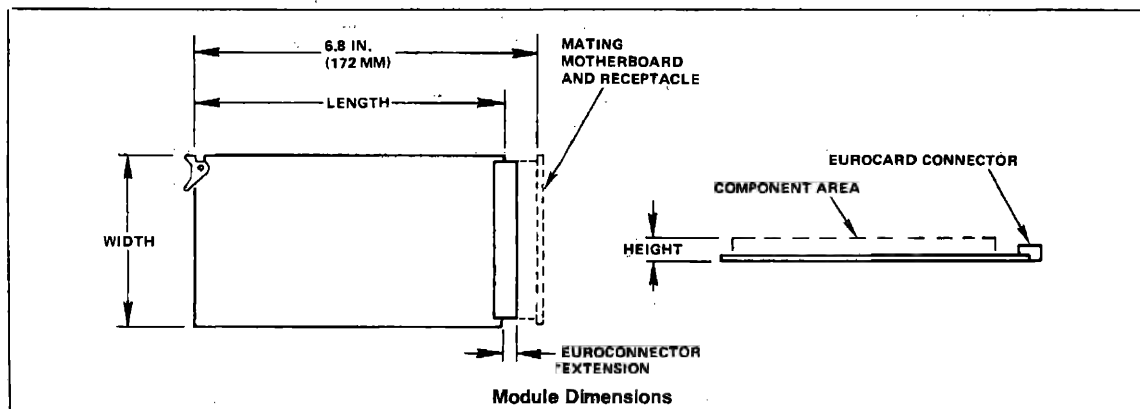


CRT Controller Module Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	Bφ1	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	*Buffered DMA Request 1
15a	BRDY	*Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	-12V/-V	*-12 Vdc/-V
17a	+12V/+V	*+12 Vdc/+V	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	Bφ0	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR/W/	*Buffered Read/Write "Not"	21c	BDRQ2/	*Buffered DMA Request 2
22a		*System Spare	22c	BR/W/	Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	*Buffered Interrupt Request	24c	BNM/	*Buffered Non-Maskable Interrupt
25a	Bφ2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	Bφ2	Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note:
*Not used on this module.



Character Set

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	00000000	00000001	00000010	00000011	00000100	00000101	00000110	00000111	00001000	00001001	00001010	00001011	00001100	00001101	00001110	00001111
1	00010000	00010001	00010010	00010011	00010100	00010101	00010110	00010111	00011000	00011001	00011010	00011011	00011100	00011101	00011110	00011111
2	00100000	00100001	00100010	00100011	00100100	00100101	00100110	00100111	00101000	00101001	00101010	00101011	00101100	00101101	00101110	00101111
3	00110000	00110001	00110010	00110011	00110100	00110101	00110110	00110111	00111000	00111001	00111010	00111011	00111100	00111101	00111110	00111111
4	01000000	01000001	01000010	01000011	01000100	01000101	01000110	01000111	01001000	01001001	01001010	01001011	01001100	01001101	01001110	01001111
5	01010000	01010001	01010010	01010011	01010100	01010101	01010110	01010111	01011000	01011001	01011010	01011011	01011100	01011101	01011110	01011111
6	01100000	01100001	01100010	01100011	01100100	01100101	01100110	01100111	01101000	01101001	01101010	01101011	01101100	01101101	01101110	01101111
7	01110000	01110001	01110010	01110011	01110100	01110101	01110110	01110111	01111000	01111001	01111010	01111011	01111100	01111101	01111110	01111111
8	10000000	10000001	10000010	10000011	10000100	10000101	10000110	10000111	10001000	10001001	10001010	10001011	10001100	10001101	10001110	10001111
9	10010000	10010001	10010010	10010011	10010100	10010101	10010110	10010111	10011000	10011001	10011010	10011011	10011100	10011101	10011110	10011111
A	10100000	10100001	10100010	10100011	10100100	10100101	10100110	10100111	10101000	10101001	10101010	10101011	10101100	10101101	10101110	10101111
B	10110000	10110001	10110010	10110011	10110100	10110101	10110110	10110111	10111000	10111001	10111010	10111011	10111100	10111101	10111110	10111111
C	11000000	11000001	11000010	11000011	11000100	11000101	11000110	11000111	11001000	11001001	11001010	11001011	11001100	11001101	11001110	11001111
D	11010000	11010001	11010010	11010011	11010100	11010101	11010110	11010111	11011000	11011001	11011010	11011011	11011100	11011101	11011110	11011111
E	11100000	11100001	11100010	11100011	11100100	11100101	11100110	11100111	11101000	11101001	11101010	11101011	11101100	11101101	11101110	11101111
F	11110000	11110001	11110010	11110011	11110100	11110101	11110110	11110111	11111000	11111001	11111010	11111011	11111100	11111101	11111110	11111111

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3) Width Length Height	3.9 in. (100 mm) 6.3 in. (160 mm) 0.56 in. (14 mm)
Environment Operating Temperature Storage Temperature Relative Humidity	0°C to 70°C -40°C to +85°C 0% to 85% (without condensation)
Power Requirements	+5 Vdc $\pm 5\%$, 0.94 A (4.7 W)—Typical 1.30 A (6.8 W)—Maximum
Interface RM 65 Bus Interface I/O Connector Composite Video Raw Video and Sync	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed) Mini-coax connector (50 ohm SMC type) Mates to Sealectro Part No. 050-024-0000-220 or equivalent 6-pin connector Mates to AMP No. 87159-6 or equivalent

Notes:

- Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
- Length does not include the added extension due to the module ejector.
- Dimensions conform to DIN 41612.



RM65-5104E **RM 65 DIRECT MEMORY ACCESS** **CONTROLLER MODULE**

RM 65 MICROCOMPUTER MODULES

The RM65-5104E Direct Memory Access Controller (DMAC) Module is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Modules products are designed for OEM and end user microcomputer applications when state-of-the-art performance, compact size, modular design, and low cost are required. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC, and Forth. Both BASIC and Forth are available in ROM and can be incorporated into the user's system.

RM 65 modules use a motherboard interconnect concept in which any card can be inserted into any slot. The 64-line RM 65 Bus permits memory addressing up to 128K bytes, provides high immunity to electrical noise, and contains growth provisions for user functions. A selection of card cages allows packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desk-top microcomputer applications.

PRODUCT OVERVIEW

The RM65-5104E DMAC Module performs high speed data transfers between memory and/or I/O devices connected to the RM 65 Bus. The data transfer rate when controlled by the DMAC Module hardware is typically four times faster than the data transfer rate achieved by CPU software. Thus by using the DMAC Module, substantial time is saved when transferring large blocks of data.

After a DMA transfer is initiated by the CPU module, the DMAC Module takes control of the RM 65 Bus and independently completes the data transfers. Operation of the DMAC Module can be controlled by an AIM 65, an AIM 65/40 SBC Module, or any other CPU module connected to the RM 65 Bus. During the DMA data transfers, the RM 65 SBC, AIM 65, or AIM 65/40 can continue operations on its internal buses.

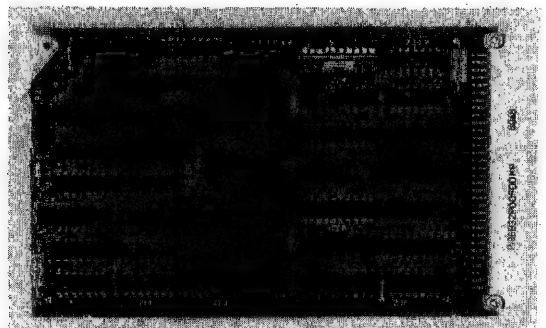
The DMAC Module is especially effective in the rapid transfer of data between either 5¼-inch or 8-inch floppy disks controlled by either the FDC Module (RM65-5101E) or the RM 65 IEEE-488 Module (RM65-7102E) and other memory or I/O modules connected to the RM 65 Bus.

FEATURES

- Rockwell RM 65 Bus compatible
- Compact size—100 mm × 160 mm (approximately 4 in. × 6.25 in.)
- Executes memory-to-memory, I/O-to-I/O, memory-to-I/O, and I/O-to-memory transfers
- DMA data transfers can be either within the same bank or between banks
- Memory address counters can either be incremented or decremented
- Interleaved, cycle steal, and burst modes
- Processor-hold and processor-run operations
- Two DMA request channels
- DMA interrupt selectable either to the Non-Maskable Interrupt or the Interrupt Request (BIRQ) line
- 500K bytes per second maximum transfer rate
- DMA termination signal to abort any DMA transfer operation in progress
- Supports RM 65 FDC 8-inch double-density operation
- Programmable Byte Counter for up to 65K-byte transfers
- Bank switches to assign I/O addresses to either one or two 65K memory banks
- I/O Base Address switch selectable to a page boundary
- Operates from a single +5V power source
- Fully assembled and tested with a one-year warranty

ORDERING INFORMATION

Part No.	Description
RM65-5104E	Direct Memory Access Controller (DMAC) Module



**RM65-5104E Direct Memory Access
Controller (DMAC) Module**

FUNCTIONAL DESCRIPTION

Addresses on the RM 65 Bus are compared with the address set by the module Base Address switches. If the Bank Select Enable switch is set, the bank-address signal (BADR/) is compared with the signal from the Bank Select switch. When the BADR/ and address signal states on the bus match the signal states generated by the Base Address and Bank Select switches, the Microcode Generator, Chip Select, and Data Buffer circuits are enabled.

When the module circuits are enabled, the four least significant address signals and the read/write signal (R/W-) generate chip-select and microcode signals. The chip-select signals enable devices within the DMAC Module either to accept or to output data. The microcode signals control which registers are active in the DMA Source Address, Destination Address, and Byte Count Generators.

After the generators are enabled and selected, data can be transferred between the module and the RM 65 Bus. Before the start of a DMA operation, these generators must be initialized. The Source Address Generator and the Destination Address Generator, respectively, must be loaded to specify the starting address of the source and the destination address during DMA data transfers. Control registers must be loaded to specify if the address is to be incremented or decremented after each byte. The Byte Count Generator must be loaded to specify the number of bytes of data to be transferred. A control byte in the Byte Count Generator indicates whether the contents of the register are to be incremented or decremented. Typically, the Byte Count Generator is set up to count down because the DMA transfer stops when the byte count becomes zero.

Contents of the Command Register specify the parameters the DMAC Module is to use and start the DMA cycle. After the Command Register has been loaded, the DMAC Module waits for two signals before beginning a DMA cycle. If the DMAC Module is to transfer data to or from an I/O device, a DMA request signal must be received from the I/O device. For I/O-to-I/O transfers, a DMA request must be received from each I/O device. For memory-to-memory transfers, the DMA request is generated by the DMAC Module. The second signal required for DMA transfers is the sync signal. When the sync signal goes high, the DMAC Module forces the ready signal low (if the processor-stop mode is enabled), floats (effectively disconnects) the RM 65 Bus from the microprocessor, and switches module operation to the Read state.

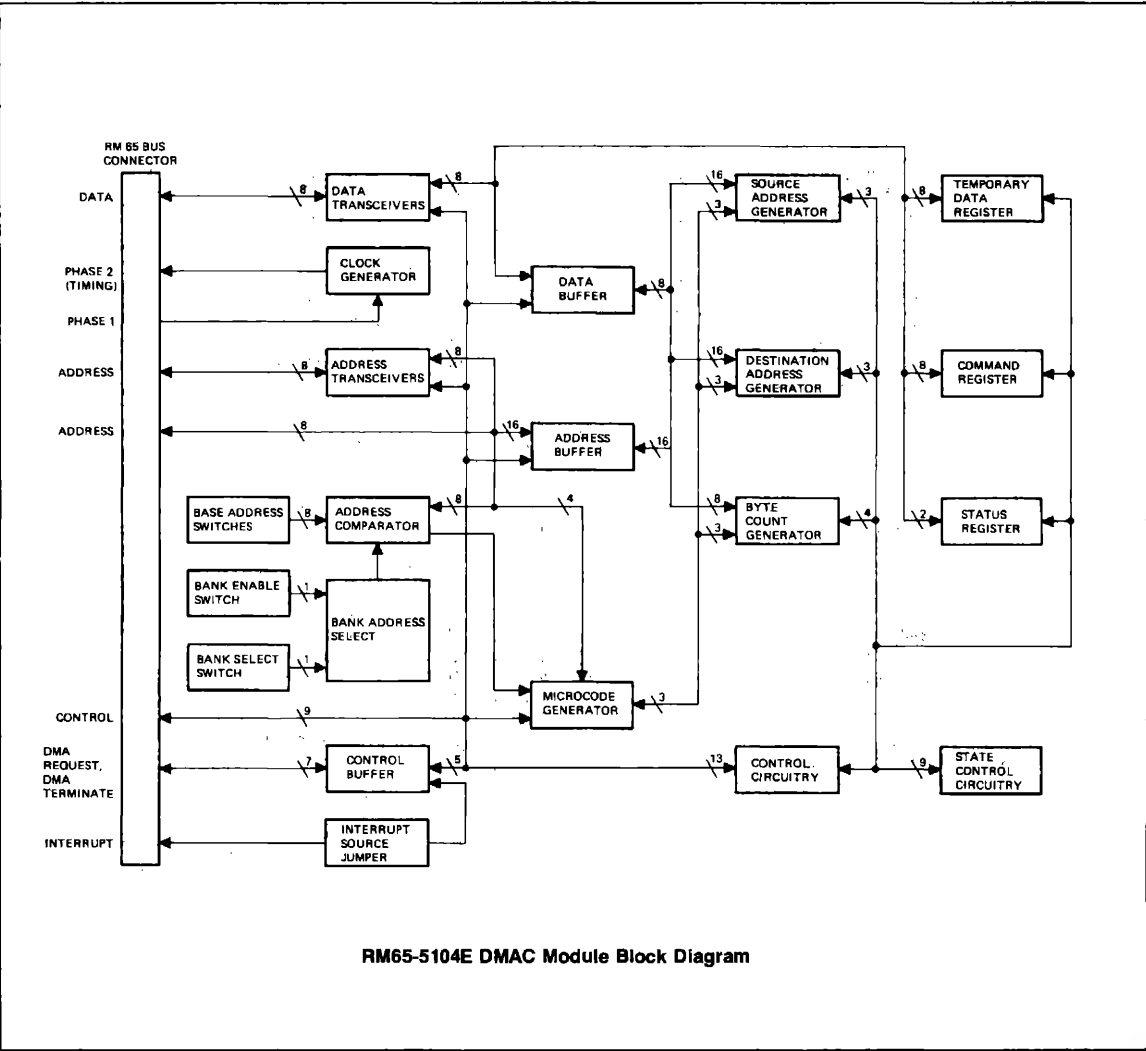
During DMA cycles, the DMAC Module is controlled by the State Control Circuitry. When the DMAC Module is idle, module operation starts or concludes in the Initialize And Conclude state. In the Read state, the source address from the Source Address Generator is placed on the RM 65 address lines. Data on the RM 65 data lines is then transferred from the source device and saved in a temporary storage register. During the Write state, the destination address from the Destination Address Generator is placed on the RM 65 address lines. Data in the Temporary Data Register is then placed on the RM 65 data lines and transferred to the destination device.

After the Write state, the byte count and mode of operation affect the state which the DMAC Module next enters. If the byte count is zero, DMAC Module operation switches to the Initialize And Conclude state and control of both the RM 65 Bus and the system returns to the processor. If the byte count is not zero, then the mode of operation affects the next DMA state. When the byte count is not zero and the data transfer is between two memory devices, operation of the DMAC Module switches to the Read state.

When the data transfer involves I/O devices, DMAC Module operation switches to a Read state if the DMA request signal (or signals during I/O-to-I/O transfers) is present. If the DMA request signal is not present and the module is in the burst mode, the mode of operation switches to a Hold state and remains in the state until the DMA request signal is present. Module operation then switches to a Read state. If the DMAC Module is operating in an interleaved mode, the operation is switched to the Initialize And Conclude state and control returns to the processor. The module takes control again as soon as sync and DMA request signals are present.

At the end of a DMA cycle, after the byte count has been reduced to zero and DMAC Module control has switched to the Initialize And Conclude state, system control returns to the microprocessor. The ready signal is disabled. The DMAC Module Command Register is cleared and the transfer-complete flag is written into the Status Register. If the interrupt mask bit is not set, either an interrupt request or a nonmaskable interrupt signal is generated.

DMAC Module operating modes are controlled by bits in the DMAC Module Command Register. Modes available are Halt, Interrupt Mask, Burst, and Interleaved.



RM65-5104E DMAC Module Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Pin	Signal Mnemonic	Signal Name	I/O	Pin	Signal Mnemonic	Signal Name	I/O
1a	GND	Ground		1c	+5V	+5 Vdc	
2a	BADR/	Buffered Bank Address	I/O	2c	BA15/	Buffered Address Bit 15	I/O
3a	GND	Ground		3c	BA14/	Buffered Address Bit 14	I/O
4a	BA13/	Buffered Address Bit 13	I/O	4c	BA12/	Buffered Address Bit 12	I/O
5a	BA11/	Buffered Address Bit 11	I/O	5c	GND	Ground	
6a	BA10/	Buffered Address Bit 10	I/O	6c	BA9/	Buffered Address Bit 9	I/O
7a	BA8/	Buffered Address Bit 8	I/O	7c	BA7/	Buffered Address Bit 7	I/O
8a	GND	Ground		8c	BA6/	Buffered Address Bit 6	I/O
9a	BA5/	Buffered Address Bit 5	I/O	9c	BA4/	Buffered Address Bit 4	I/O
10a	BA3/	Buffered Address Bit 3	I/O	10c	GND	Ground	
11a	BA2/	Buffered Address Bit 2	I/O	11c	BA1/	Buffered Address Bit 1	I/O
12a	BA0/	Buffered Address Bit 0	I/O	12c	B01	Buffered Phase 1 Clock	I
13a	GND	Ground		13c	BSYNC	Buffered Sync	I/O
14a	BSO	*Buffered Set Overflow		14c	BDRQ1/	Buffered DMA Request 1	I
15a	BRDY	Buffered Ready	O	15c	GND	Ground	
16a		*User Spare 1		16c	-12V/-V	* -12 Vdc/-V	
17a	+12V/+V	* +12 Vdc/+V		17c		*User Spare 2	
18a	GND	Ground		18c	BFLT/	Buffered Bus Float	O
19a	BDMT/	Buffered DMA Terminate	I	19c	B00	*Buffered External Phase 0 Clock	
20a		*User Spare 3		20c	GND	Ground	
21a	BR/W/	Buffered Read/Write "Not"	I/O	21c	BDRQ2/	Buffered DMA Request 2	I
22a		*System Spare		22c	BR/W/	Buffered Read/Write	I/O
23a	GND	Ground		23c	BACT/	Buffered Bus Active	O
24a	BIRQ/	Buffered Interrupt Request	O	24c	BNMI/	Buffered Non-Maskable Interrupt	O
25a	B02/	Buffered Phase 2 "Not" Clock	O	25c	GND	Ground	
26a	B02	Buffered Phase 2 Clock	I/O	26c	BRES/	Buffered Reset	I
27a	BD7/	Buffered Data Bit 7	I/O	27c	BD6/	Buffered Data Bit 6	I/O
28a	GND	Ground		28c	BD5/	Buffered Data Bit 5	I/O
29a	BD4/	Buffered Data Bit 4	I/O	29c	BD3/	Buffered Data Bit 3	I/O
30a	BD2/	Buffered Data Bit 2	I/O	30c	GND	Ground	
31a	BD1/	Buffered Data Bit 1	I/O	31c	BD0/	Buffered Data Bit 0	I/O
32a	+5V	+5 Vdc		32c	GND	Ground	

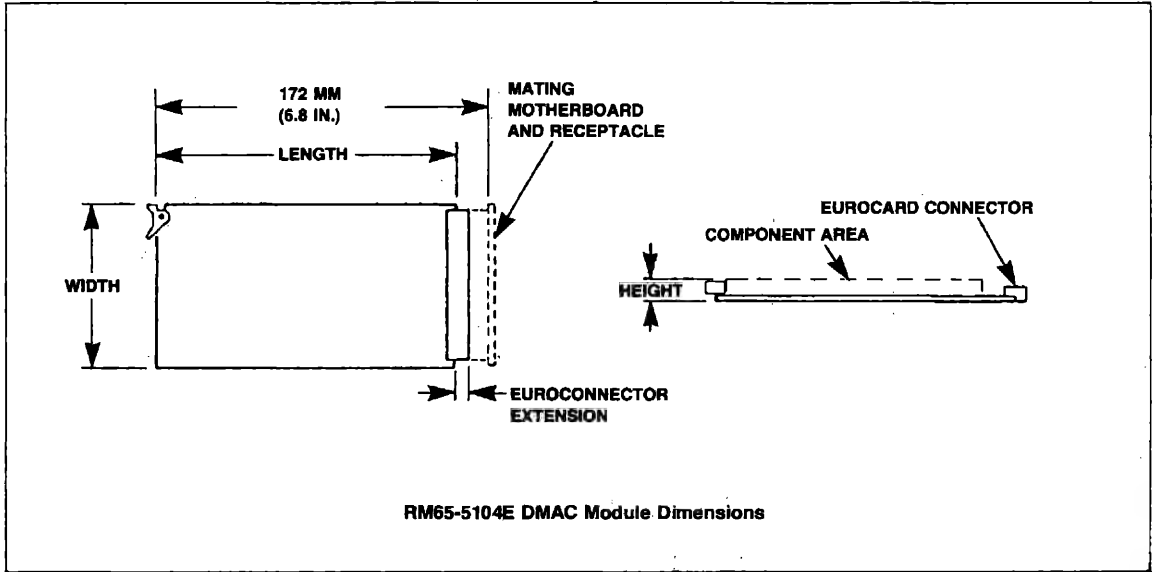
Note:
 *Not used on this module.

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3)	
Width	100 mm (3.9 in.)
Length	164 mm (6.4 in.)
Height	14 mm (0.56 in.)
Weight	137 g (4.8 oz.)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C
Relative Humidity	0% to 85%, without condensation
Power Requirements	
	+5 Vdc ±5%, at 1.2A (6.0W)—Typical 1.9A (9.5W)—Maximum
RM 65 Bus Interface	64-pin plug (0.100 in. centers) per DIN 41612 (a and b with c not installed)

Notes:

1. Height includes the maximum values for component height above the board surface (0.4 in.), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. Length does not include extensions beyond the edge of the module due to connectors or the module ejector.
3. Connector conforms to DIN 41612.





RM65-5222E

RM 65 GENERAL PURPOSE INPUT/OUTPUT (GPIO) & TIMER MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-5222E GPIO & Timer Module is one of the hardware options available for the RM 65 Microcomputer Module family.

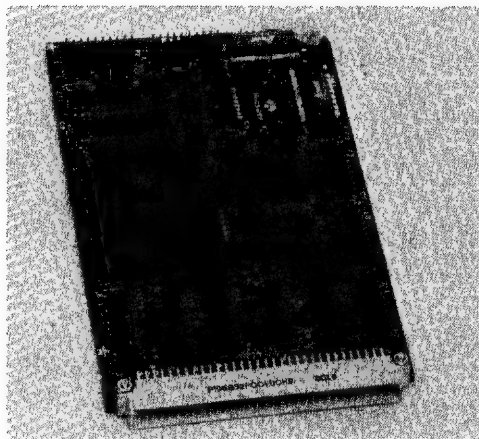
RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 modules use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desk-top microcomputer applications.

PRODUCT OVERVIEW

The RM65-5222E General Purpose Input/Output (GPIO) & Timer Module provides a parallel I/O interface to the RM 65 Bus. Two R6522 Versatile Interface Adapter (VIA) devices provide four 8-bit bidirectional data ports and four 2-bit control ports; 40 I/O lines in all. Two multi-mode 16-bit timer/counters extend the versatility of the module. All I/O lines are TTL buffered.

The GPIO & Timer Module I/O can be assigned either to one of two 65K byte memory banks or common to both banks. Eight switches allow I/O addresses to be set to any page (256 bytes). Eight switches (two per I/O port) manually set the I/O transceiver data direction or allow software control using the associated port control lines. Twelve jumpers specify the direction of the control lines.



RM65-5222E General Purpose Input/Output (GPIO) & Timer Module

ORDERING INFORMATION

Part No.	Description
RM65-5222E	General Purpose Input/Output (GPIO) and Timer Module
Order No.	Description
801	General Purpose Input/Output (GPIO) and Timer Module User's Manual (included with RM65-5222E)

FEATURES

- Compact size—about 4" × 6¼" (100 mm × 160 mm)
- Pin and socket bus connector
- RM 65 Bus compatible
- Fully buffered address, data and control bus interface lines
- Fully buffered data and control I/O lines
- Four 8-bit parallel bidirectional data ports
- Four 2-bit control ports
- Four programmable 16-bit counter/timers
- Two 8-bit shift registers for synchronous serial communications
- Manually or software-controlled data line direction
- Jumper-selectable control line direction
- Bank select switches assign I/O addresses to one or two 65K banks
- I/O base address switch selectable to a page boundary
- Four I/O connectors
- +5V operation
- Fully assembled, tested and warranted

FUNCTIONAL DESCRIPTION

The heart of the GPIO & Timer module is two R6522 Versatile Interface Adapter (VIA) devices. Each VIA provides two 8-bit bidirectional input/output ports, four I/O control lines, two fully programmable 16-bit timer/counters and an 8-bit shift register for serial interface. There is also control of interrupt generation from independent I/O conditions.

The two 8-bit input/output peripheral ports are fully bidirectional. Data direction registers allow each peripheral pin to independently act as either an input or an output. The four control lines can also be used for I/O or can provide handshaking for the associated data ports. Each control input can be programmed to interrupt the microprocessor on detection of a rising or falling edge.

The two 16-bit counter/timers are capable of many complex timing and counting functions. One timer provides four modes of operation: free running, with pulsed or toggled output, one-shot interval timer with a low-level output on a peripheral port line, or one-shot interval timer with a toggle output on a peripheral port line. The three modes of the second 16-bit timer provide a one-shot interval timer, a count of external pulses, or a clock for serial shift register. The shift register can shift in, or shift out, data at the system clock rate, the timer clock rate, or an external clock rate. Both timers and the shift register can be programmed to interrupt the microprocessor upon time-out or shift completion.

The Data Transceivers invert and buffer 8-bits of parallel data between the RM 65 Bus and the two R6522 VIA devices. The Data Transceivers are enabled when a valid address is present at the Base Address Decoders. During a read operation, data is transferred from the addressed R6522 to the RM 65 Bus. During a write operation, data is transferred from the RM 65 Bus to the addressed R6522.

The Address Buffers invert the five least significant address bits used to select the R6522 devices and registers.

The Bank Control circuit detects when the GPIO & Timer Module's assigned memory bank is addressed by comparing the bank address signal from the RM 65 Bus to the Bank Select Enable and Bank Select switches. The Bank Select Enable switch allows the module to be assigned common to either both banks, or to Bank 0 (lower 65K) or Bank 1 (upper 65K) depending on the Bank Select switch.

The Control Buffers drive read/write, phase 2 clock, and reset signals from the RM 65 Bus to the GPIO & Timer Module. The interrupt request and bus active signals are driven from the GPIO & Timer Module.

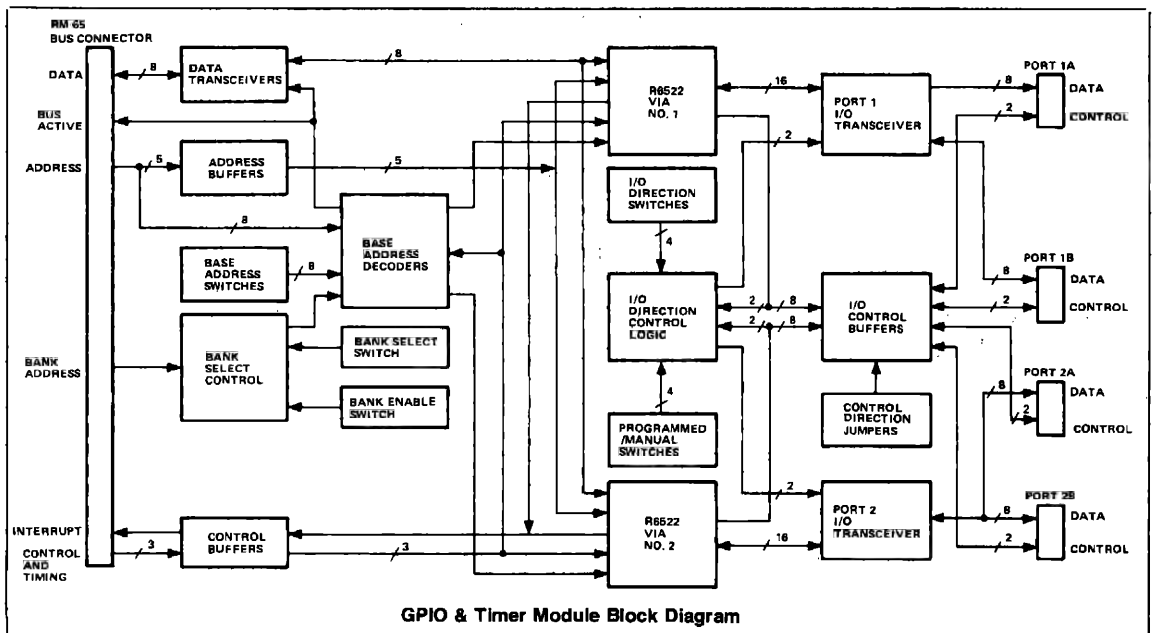
The Base Address Decoders use the eight most significant address lines to assign the 32 I/O addresses to a page (256 bytes) boundary. When an address is within range of the Base Address switches and the Bank Control is enabled, a chip select is generated to one of the R6522 devices.

Twelve Control Direction Jumpers allow the three bidirectional control lines (CA1, CB1, and CB2) on each R6522 to be configured for either input or output mode.

Four I/O Direction Switches provide direction control to each of the Port I/O transceivers. Four Programmed/Manual Select switches allow the direction control to be established from the Direction Control switches in the Manual mode or from a R6522 control line in the Programmed mode.

The I/O Transceivers buffer each of four 8-bit I/O ports. The direction is determined by the Direction Control logic. There are also eight buffers provided for the control lines (2 per I/O port), six of which can be configured for input or output as determined by the Handshake Direction Buffers.

All I/O data and control signals are brought out to four connectors that will each accept a 20-pin mass terminated ribbon cable (cable and mass terminated connectors are not supplied with the GPIO & Timer Module). Each connector is dedicated to one port with 8 data, 2 control and 10 ground lines.



RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	*Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	*Buffered Address Bit 6
9a	BA5/	*Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	B01	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	*Buffered DMA Request 1
15a	BRDY	*Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	-12V/-V	*-12 Vdc/-V
17a	+12V/+V	*+12 Vdc/+V	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	B00	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR/W/	Buffered Read/Write "Not"	21c	BDRQ2/	*Buffered DMA Request 2
22a		*System Spare	22c	BR/W	*Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request	24c	BNMI/	*Buffered Non-Maskable Interrupt
25a	B02/	*Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	B02	Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note:
*Not used on this module.

I/O Connector Pin Assignments

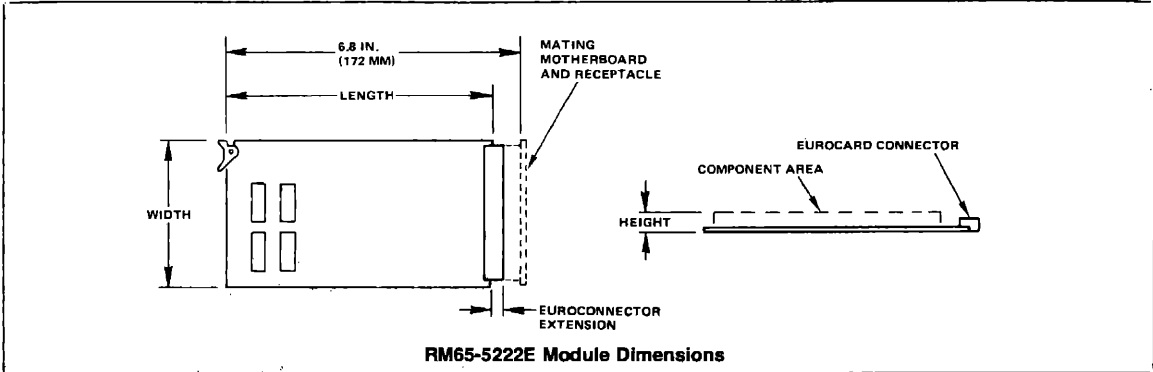
Pin	Signal
1	Port 1A Data 0
3	Port 1A Data 1
5	Port 1A Data 2
7	Port 1A Data 3
9	Port 1A Data 4
11	Port 1A Data 5
13	Port 1A Data 6
15	Port 1A Data 7
17	Port 1A Control CA1
19	Port 1A Control CA2

Notes:
1. Similar for ports 1B, 2A and 2B
2. Even Pins 2-20 are ground

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3) <div>Width</div> <div>Length</div> <div>Height</div>	<div>3.9 in. (100 mm)</div> <div>6.3 in. (160 mm)</div> <div>0.56 in. (14 mm)</div>
Weight	5.0 oz. (140 g)
Environment <div>Operating Temperature</div> <div>Storage Temperature</div> <div>Relative Humidity</div>	<div>0°C to 70°C</div> <div>−40°C to +85°C</div> <div>0% to 85% (without condensation)</div>
Power Requirements	<div>+5 Vdc ±5% 0.52 A (2.6 W)—Maximum</div> <div>+5 Vdc ±5% 0.94 A (4.70 W)—Maximum</div>
Interface <div>RM 65 Bus Interface</div> <div>I/O Interface</div> <div>I/O Connectors (4)</div>	<div>64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)</div> <div>20-pin vertical mass termination plug (0.3 in. pins on 0.100 in. centers)</div>

- Notes:
- 1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
 - 2. Length does not include extensions beyond the edge of the module due to connectors or the module ejector.
 - 3. Dimensions conform to DIN 41612.





RM65-5223E RM 65 MULTI-FUNCTION PERIPHERAL INTERFACE MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-5223E Multi-Function Interface (MPI) Module is one of the hardware options available for the RM 65 Microcomputer Module family.

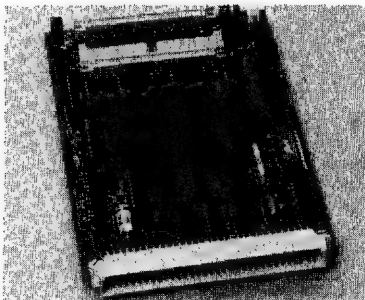
RM 65 Microcomputer Modules products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 modules use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desk-top microcomputer applications.

PRODUCT OVERVIEW

The RM65-5223E RM 65 Multi-function Interface (MPI) Module provides a parallel I/O interface to the RM 65 Bus. Two R6522 Versatile Interface Adapter (VIA) devices provide four 8-bit bidirectional data ports and four 2-bit control ports; 40 I/O lines in all. Two multi-mode 16-bit timer/counters extend the versatility of the module. All I/O lines are TTL buffered and available on two 40 pin I/O connectors compatible with the AIM 65/40 SBC and RM 65 SBC Parallel Application connectors. Data buffer direction is under direct software control. Twelve jumpers specify the direction of the control lines, while an additional 6 jumpers control the optional features.

The MPI Module I/O can be assigned either to one of two 65K byte memory banks or common to both banks. Eight switches allow I/O addresses to be set to any page (256 bytes).



**RM65-5223E Multi-function Peripheral
Interface (MPI) Module**

FEATURES

- Compact size—about 4" × 6¼" (100 mm × 160 mm)
- Pin and socket bus connection
- RM 65 Bus compatible
- Two R6522 Versatile Interface Adapter (VIA) devices
- Four fully buffered 8-bit parallel data ports
- Four fully buffered 2-bit control ports
- Four programmable 16-bit counter/timers
- Two serial input/output ports
- Multiple interrupt conditions
- Full buffering on all I/O data and control lines
- Software-controlled data line direction
- Jumper-selectable control line direction
- Data port buffering can be removed
- All I/O lines are available on two 40-pin I/O connectors
- I/O connectors are compatible with both the AIM 65/40 and RM 65 SBC module parallel I/O connectors and AIM 65/40 intelligent peripherals
- One connector is fully compatible with the AIM 65/40 standard or extended keyboard
- Bank switches assign I/O addresses to one or two 65K banks
- I/O base address switch selectable to a page boundary
- +5V operation
- Fully assembled, tested and warranted

ORDERING INFORMATION

Part No.	Description
RM65-5223E	Multi-function Peripheral Interface (MPI) Module
Order No.	Description
817	Multi-function Peripheral Interface Module (MPI) Module User's Manual (included with RM65-5223E)

FUNCTIONAL DESCRIPTION

The heart of the MPI module is two R6522 Versatile Interface Adapter (VIA) devices. Each VIA provides two 8-bit bidirectional input/output ports, four I/O control lines, two fully programmable 16-bit timer/counters and an 8-bit shift register for serial interface. There is also control of interrupt generation from independent I/O conditions.

The two 8-bit input/output peripheral ports are fully bidirectional. Data direction registers allow each peripheral pin to independently act as either an input or an output. The four control lines can also be used for I/O or can provide handshaking for the associated data ports. Each control input can be programmed to interrupt the microprocessor on detection of a rising or falling edge.

The two 16-bit counter/timers are capable of many complex timing and counting functions. One timer provides four modes of operation: free running, with pulsed or toggled output, one-shot interval timer with a low-level output on a peripheral port line, or one-shot interval timer with a toggle output on a peripheral port line. The three modes of the second 16-bit timer provide a one-shot interval timer, a count of external pulses, or a clock for serial shift register. The shift register can shift in, or shift out data at the system clock rate, the timer clock rate, or an external clock rate. Both timers and the shift register can be programmed to interrupt the microprocessor upon time-out or shift completion.

Four Port Transceivers buffer the VIA data lines for input or output modes. The I/O Data Direction Control logic allows the direction of each 8-bit port to be independently set for input or output mode under software controls. In the buffered output mode, the Port Transceivers are capable of sinking 16 mA on any data line. For applications where buffering is not desired, any of the Port Transceivers can be replaced with DIP shunts for direct connection to the VIA peripheral data pins.

The I/O Control Signal Buffers fully buffer all eight VIA Control lines. On each VIA, one control line (CA1) has only an input mode which is buffered as such. Twelve I/O Control Direction Jumpers allow the three bidirectional control lines (CA2, CB1, and CB2) on each R6522 to be configured for either input or output mode.

A number of options available on VIA No. 1 make it particularly well-suited for keyboard applications. The A port of VIA No. 1 is supplemented with Line Low Detection circuitry which generates an interrupt through control line CA1 when any line goes

low; a reset switch on control line CB2 is passed off the board from the RESET connector to be used by reset conditioning circuitry on an RM 65 SBC module, AIM 65 microcomputer or AIM 65/40 SBC module; an attention switch on control line CB1 is debounced by the Attention Interrupt Conditioning circuitry to generate a non-maskable interrupt when enabled by the Attention Interrupt jumper.

Two 40-pin Parallel I/O connectors support all the R6522 VIA signals as well as the Attention and Reset switch options. These connectors can be configured to match the RM 65 or AIM 65/40 SBC module Parallel Application connectors, while also being compatible with AIM 65/40 peripherals—keyboard, display or printer. The I/O Power Source jumpers allow +5V to be supplied to the interfacing equipment through the Parallel I/O Connector.

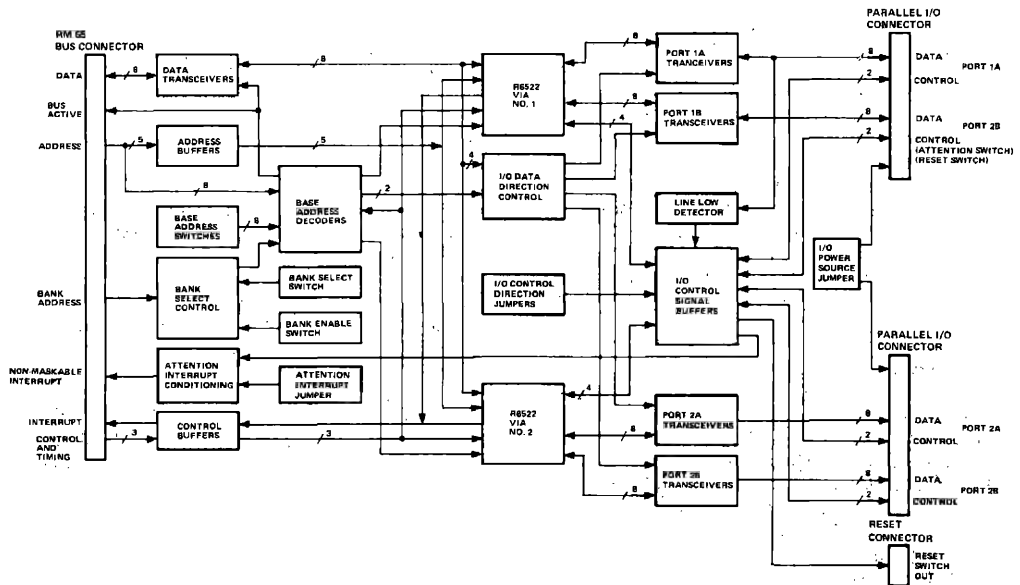
The Data Transceivers invert and buffer 8-bits of parallel data between the RM 65 Bus and the two R6522 VIA devices or the I/O Direction Control logic. The Data Transceivers are enabled when a valid address is present at the Base Address Decoders. During a read operation, data is transferred from the addressed I/O to the RM 65 Bus. During a write operation, data is transferred from the RM 65 Bus to the addressed I/O.

The Address Buffers invert the six least significant address bits used to select the R6522 devices and registers and also the I/O Direction Control Logic.

The Control Buffers drive read/write, phase 2 clock, and reset signals from the RM 65 Bus to the MPI module. The interrupt request and bus active signals are driven from the MPI module.

The Bank Select Control circuit detects when the MPI module's assigned memory bank is addressed by comparing the bank address signal from the RM 65 Bus to the Bank Select Enable and Bank Select switches. The Bank Select Enable switch allows the module to be assigned either common to both banks, or to Bank 0 (lower 65K) or Bank 1 (upper 65K) depending on the Bank Select switch.

The Base Address Decoders use the eight most significant address lines to assign the MPI module to a page (256 bytes) boundary. When an address is within range of the Base Address switches and the Bank Control is enabled, a chip select is generated to one of the R6522 devices or the I/O Direction Control logic is selected.



MPI Module Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADF/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	*Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	*Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	B01	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	*Buffered DMA Request 1
15a	BRDY	*Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	-12V/-V	*-12 Vdc/-V
17a	+12V/+V	*+12 Vdc/+V	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	B00	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR/W/	Buffered Read/Write "Not"	21c	BDRQ2/	*Buffered DMA Request 2
22a		*System Spare	22c	BR/W	*Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request	24c	BNM/	Buffered Non-Maskable Interrupt
25a	B02/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	B02	*Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note:
*Not used on this module.

Connector J1 and J2 (Parallel I/O Connector) Pin Assignments

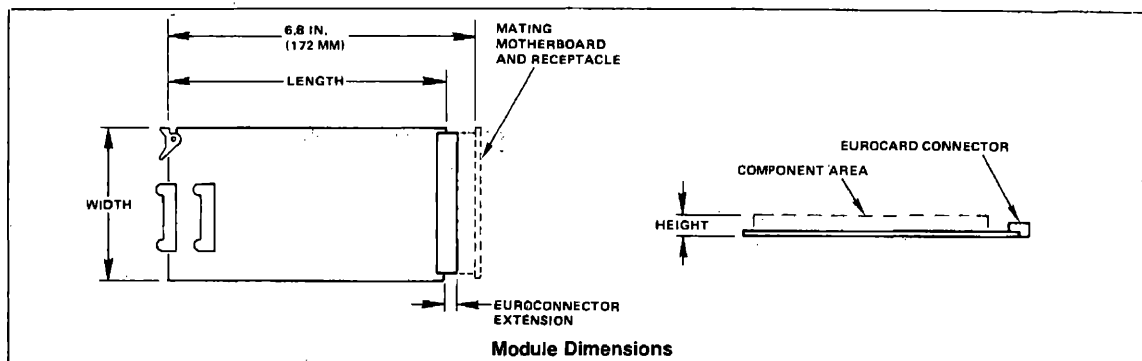
Pin	Signal	I/O	Type	Pin	Signal	Type
1	CB2/RES	I/O	NMOS	2	GND/+5V*	Power
3	CB1/ATTN	I/O	NMOS	4	GND	Power
5	PB7	I/O	NMOS	6	GND	Power
7	PB6	I/O	NMOS	8	GND	Power
9	PB5	I/O	NMOS	10	GND	Power
11	PB4	I/O	NMOS	12	GND	Power
13	PB3	I/O	NMOS	14	GND	Power
15	PB2	I/O	NMOS	16	GND	Power
17	PB1	I/O	NMOS	18	GND	Power
19	PB0	I/O	NMOS	20	GND	Power
21	PA7	I/O	NMOS	22	GND	Power
23	PA6	I/O	NMOS	24	GND	Power
25	PA5	I/O	NMOS	26	GND	Power
27	PA4	I/O	NMOS	28	GND	Power
29	PA3	I/O	NMOS	30	GND	Power
31	PA2	I/O	NMOS	32	GND	Power
33	PA1	I/O	NMOS	34	GND	Power
35	PA0	I/O	NMOS	36	GND	Power
37	CA2	I/O	NMOS	38	GND	Power
39	CA1	I	NMOS	40	GND/+5V*	Power

Notes:

1. Pins 2 and 40 can be optionally jumpered to +5V (maximum current through each pin should not exceed 200 mA).
2. Pin 1 of J1 can be optionally jumpered to RESET connector or to CB2.
3. Pin 3 of J1 can be optionally jumpered to the Attention Interrupt Conditioning circuit or to CB1.

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3)	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	5.1 oz. (145 g)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	
	+5 Vdc $\pm 5\%$ 0.65 A (3.25 W)—Typical
	+5 Vdc $\pm 5\%$ 1.03 A (5.15 W)—Maximum
Interfaces	
RM 65 Bus Interface	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)
I/O Interface	
Parallel I/O Connectors (2)	40-pin 3M #3495-1002, or equivalent, receptacle. Mates with 3M #3418-0000T, or equivalent, ribbon cable connector
Reset Connector	2 vertical pins (0.3 in. high) on 0.200 in. center
Notes: 1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.). 2. Length does not include extensions beyond the edge of the module due to connectors or the module ejector. 3. Dimensions conform to DIN 41612.	





RM65-5302E AND RM 65-5303E RM 65 ANALOG INPUT AND ANALOG INPUT/OUTPUT MODULES

RM 65 MICROCOMPUTER MODULES

The RM65-5302E Analog Input Module and the RM65-5303E Analog Input/Output Module are hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 modules use a motherboard interconnect concept in which any card can be inserted in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, provides high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages allows packaging flexibility. RM 65 products can also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The RM65-5303E Analog Input/Output module provides either 16 single-ended or 8 differential analog input channels with 12-bit analog-to-digital conversion and two independent analog output channels with 12-bit digital-to-analog conversion. This single module can satisfy a wide range of applications requiring both monitoring and control of interfacing analog devices. For applications requiring only the monitoring of sensors, the RM65-5302E Analog Input module provides the same input capability as the RM65-5303E module but does not have analog output provision.

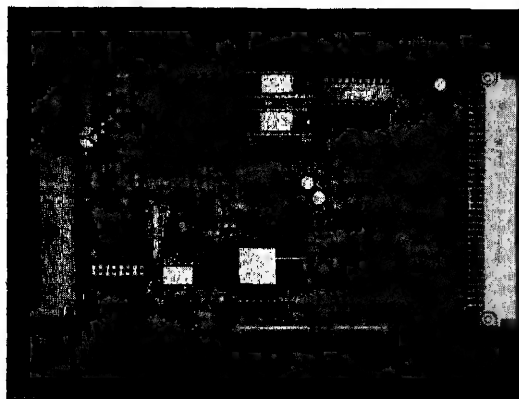
The analog input section is easily jumper configured to accept inputs in one of five voltage ranges in either single-ended or differential input connection (depending upon the position of a plug-in header). Automatic input conversion start upon reading of input data simplifies software processing. Each of the two independent analog output channels initiates output conversion automatically upon the receipt of output data thus similarly reducing software steps. Each output channel can also be separately configured to operate in one of five output ranges with internal reference or in one of six output gain ranges with external reference.

ORDERING INFORMATION

Part No.	Description
RM65-5302E	Analog Input Module
RM65-5303E	Analog Input/Output Module
Order No.	Description
818	Analog Input/Output Module User's Manual (included with RM65-5302E and RM65-5303E)

FEATURES

- Compact size—about 100 mm × 160 mm (4" × 6¼")
- RM 65 Bus compatible
- 16 Single-ended or 8 differential analog input channels
 - 12-bit analog-to-digital converter (ADC)
 - Software control of input channel
 - Input over-voltage protected to $\pm 15V$
 - Input impedance of 100 megohms minimum
 - Five analog input voltage ranges
 - 70 db of common-mode rejection with differential inputs
 - Sample and hold isolation of analog input during conversion time
 - Software selectable data length conversion (8 or 12 bits)
 - Automatic conversion start upon reading the most significant byte
 - Maskable interrupt generation upon conversion completion
- Two independent analog output channels each with:
 - 12-bit digital-to-analog converter (DAC)
 - Five analog output voltage ranges with internal reference
 - Six analog output gain ranges with external reference
 - Settling time of 6 microseconds
 - Double-buffered DAC data registers
 - Automatic conversion start upon writing the least significant byte
- Trim potentiometers for zero-offset and full-scale reference adjustments
- All analog I/O signals are available on a 40-pin connector compatible with mass-terminated twisted-pair cables
- Fully assembled and tested with a one-year warranty



RM65-5303E Analog Input/Output Module

FUNCTIONAL DESCRIPTION

RM 65 BUS INTERFACE

The Base Address Comparator compares the address lines to Base Address switches S1-1 through S1-8 to determine if the address is within the 256-byte (1 page) block of memory selected by the switches. When the address lines match the switch positions, the module is enabled.

Bank Select logic exclusively NORs the Bank Address line with the Bank Select switch position (S1-9) then routes the output through the Bank Select Enable switch (S1-10) to select the bank (0, 1 or both) that the module responds to when addressed. This bank enable signal is then routed to the Command Decoder.

Control Line Buffers invert and drive the read/write, reset, phase 2 and address line 0 onto the module for use by other on-board circuitry. The Interrupt Request from the ADC conversion logic and the Bus Active from the Address Decoder logic are driven onto the RM 65 Bus.

Data Transceivers invert and transfer eight parallel data lines between the module and the RM 65 data bus. The transceivers are enabled by the Address Decoder logic when the module is addressed in the selected page and bank. The direction of data transfer is controlled by R/W. When the transceivers are enabled during a write operation, data is transferred from the RM 65 data bus for use by the ADC MUX Channel Select, the ADC Control Register, or the two DACs. When the transceivers are enabled during a read operation, data is transferred to the RM 65 data bus from the ADC, the ADC MUX Channel Monitor, or the ADC Status Register.

COMMAND DECODER

Command Decoder logic is enabled when the address is within the page selected by the base address switches, and the bank address matches the selected bank. When enabled, bus address lines BA1/ and BA2/ as well as R/W from the Control Line Buffers are decoded and combined with other logic into the following major control lines, which enable the Data Transceivers, drive Bus Active, and control the other major module functions.

ANALOG INPUT

Analog input signals are routed from the J1 I/O Connector to the multiplexer (MUX) which consists of two 8-to-1 MUX devices. For single-ended inputs, the 16 individual signals are routed to one of the two MUX devices; eight channels (CH0-CH7) to MUX 2 and eight channels (CH8-CH15) to MUX 1. The signal return is connected to ground through the corresponding channel return at Connector J1. For differential inputs, eight channels are connected to both MUX devices; eight (CH0+ through CH7+) to MUX 2 and the accompanying eight (CH0- through CH7-) to MUX 1.

The ADC MUX Channel Select logic latches the upper four RM 65 data bus lines. When a Write ADC MUX Channel command is decoded by the Command Decoder, the encoded channel number (0 to 7) is output to the MUX devices. Latched data lines are routed to each MUX device to select one of eight channels. The high and low latched D7 and $\overline{D7}$ lines are routed through

the Analog Input Header to enable either MUX 1 or MUX 2. For single-ended inputs, MUX 2 is enabled when channel 0-7 is selected while MUX 1 is enabled when Channel 8-15 is selected. For differential inputs, both MUX devices are enabled when channel 0-7 is selected. The ADC MUX Channel Monitor copies the latched MUX channel select lines onto data bus lines when a Read ADC MUX Channel Monitor command is decoded by the Command Decoder.

The selected MUX output is routed through the Analog Input Header to the INST AMP. The plug-in shunt type header contains alternating open and closed circuits and is provided with the module to allow easy selection of either single-ended or differential inputs by merely reversing the orientation of the header in the socket. When single-ended inputs are selected, the high signal from the selected MUX device is routed to the INST AMP "+" input while GND is routed to the INST AMP "-" input. When a differential input is selected, the signal from MUX 2 is connected to the INST AMP "+" input while the signal from MUX 1 is routed to the INST AMP "-" input. One pin of the Analog Input Header socket is routed to ADC Status Register to indicate the installed position of the header to the processor.

The INST AMP provides a precision gain to the differential voltage between its "+" and "-" input terminals. The ADC Amplifier Gain jumper allows a gain of either 1 or 2 to be selected. Two potentiometers allow the zero offset and gain to be adjusted.

The S/H amplifier and associated hold capacitor samples the output from the INST AMP and holds its output steady while the interfacing ADC device converts the analog signal to the digital equivalent.

A/D CONVERSION AND ADC READ LOGIC

The ADC and associated A/D conversion/read logic controls the converting of the analog input signal to digital format and the transferring of the digital data onto the data bus.

CONVERT A/D CYCLE

The convert A/D cycle controls the sampling and holding of the analog input signal and its conversion to digital format. The convert cycle is initiated in response to a Read ADC MSB command.

The ADC device uses a 12-bit successive approximation technique to convert the analog input voltage to a 12- or 8-bit digital format then stores the digital data in an internal data storage register (for subsequent output to data lines D0-D7 in response to read ADC commands). The Input Type jumper selects either unipolar or bipolar operation. The ADC Range jumper routes the input signal from the S/H to either the 10V or 20V input pin on the ADC.

When the conversion is complete, the ADC Data Ready bit (ADCRDY) is set in the ADC Status Register. This indicates that the conversion is complete and that ADC data may be read from the ADC. ADCRDY also generates the Interrupt Request if the Interrupt Enable (IRQEN) is set in the ADC Control Register.

READ ADC CYCLE

The converted analog input signal is output to the RM 65 data bus through Data Transceivers in response to one of two read

ADC commands decoded by the Command Decoder. One command, Read ADC LSB, transfers the least significant byte consisting of the four least significant bits and four zeros onto the RM 65 data bus. One other command, Read ADC MSB, transfers the most significant byte consisting of the eight most significant bits onto the RM 65 data bus. The least significant byte is always read first since reading the most significant byte restarts the conversion cycle.

ADC STATUS AND CONTROL REGISTER

The ADC Status Register, when enabled by the decoded Read ADC Status Register command, drives the status of four signals onto the data bus.

Signal Name	Description
HDRPOS	Analog Input Header Position
IRQENS	Interrupt Request Enable Status
ADCRDY	ADC Data Ready
IRQ-	Interrupt Request Flag Status

HDRPOS reflects the installed position of the Analog Input Header. IRQENS copies the Interrupt Request Enable Command output from the ADC Control Register. ADCRDY indicates the ADC conversion status from the ADC. The IRQ- Interrupt Request Flag indicates if an interrupt request has been issued to the RM 65 Bus.

The ADC Control Register, when enabled by the decoded Write ADC Control Register command, latches the lower four bits of the data bus lines to drive two ADC control signals.

Signal Name	Description
IRQENC	Interrupt Request Enable Command
12/8	Conversion Length

IRQEN is the status of the interrupt enable command to the ADC Status Register. 12/8 is the A/D conversion length command to the ADC device.

ANALOG OUTPUT

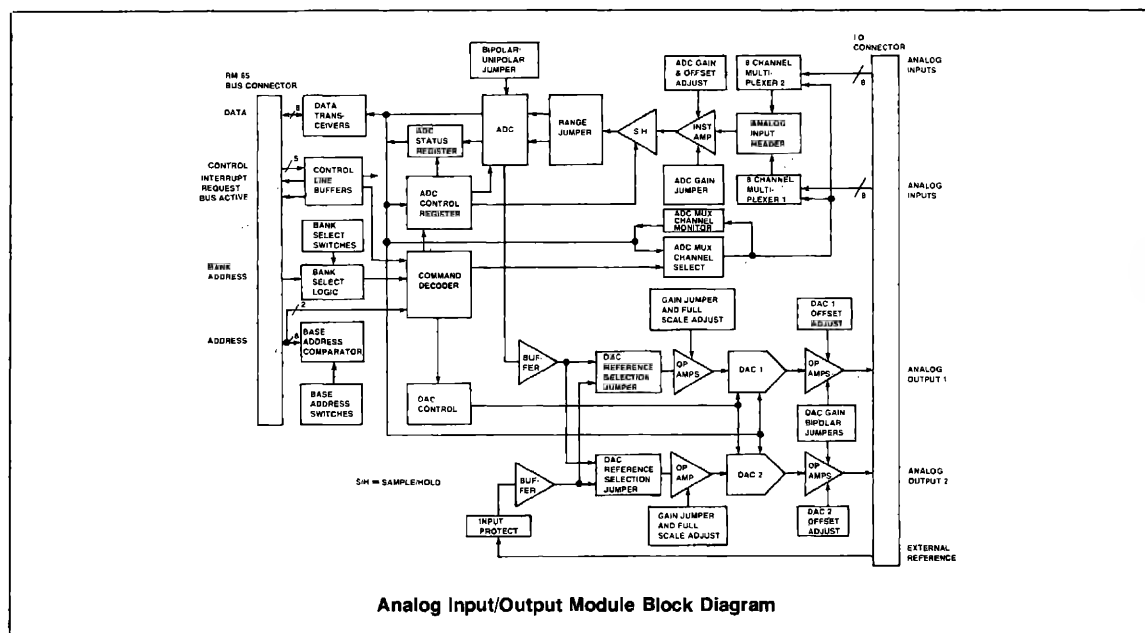
Analog output signals originate as digital data (two bytes) on the RM 65 Bus. These data bytes are input through the Data Transceivers into DAC 1 and DAC 2 in response to commands decoded by the Command Decoder and other logic to distinguish the individual data bytes. These commands enable the respective DACs and initiate the data conversion upon writing of the least significant data byte. Two addresses associated with each DAC transfer the 12-bit digital data in separate 8-bit bytes.

The reference voltage to each DAC may be either an internal precision reference originating from the ADC or an external input voltage of $\pm 11V$. Separate buffers amplify the internal reference voltage and the external reference voltage. Either the internal or external reference voltage source is selected by a Reference Source jumper on each channel.

The selected reference voltage is amplified using a gain selected by the DAC Reference Amplifier Gain jumper position. The DAC gain adjust potentiometer trims the amplifier gain.

Each DAC provides an output current directly proportional to the product of the reference voltage and the digital input word. A second output current is similarly proportional to the complement of the digital input value.

An OP AMP converts the output current to a unipolar voltage and a second OP AMP converts the voltage to bipolar levels if jumper selected. One jumper selects the output gain while another jumper determines the output polarity. A potentiometer trims the output gain.



Analog Input/Output Module Block Diagram

I/O Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal
1	ADC CH0 (CH0+)	I	2	ADC CH0 GND
3	ADC CH1 (CH1+)	I	4	ADC CH1 GND
5	ADC CH2 (CH2+)	I	6	ADC CH2 GND
7	ADC CH3 (CH3+)	I	8	ADC CH3 GND
9	ADC CH4 (CH4+)	I	10	ADC CH4 GND
11	ADC CH5 (CH5+)	I	12	ADC CH5 GND
13	ADC CH6 (CH6+)	I	14	ADC CH6 GND
15	ADC CH7 (CH7+)	I	16	ADC CH7 GND
17	ADC CH8 (CH0-)	I	18	ADC CH8 GND
19	ADC CH9 (CH1-)	I	20	ADC CH9 GND
21	ADC CH10 (CH2-)	I	22	ADC CH10 GND
23	ADC CH11 (CH3-)	I	24	ADC CH11 GND
25	ADC CH12 (CH4-)	I	26	ADC CH12 GND
27	ADC CH13 (CH5-)	I	28	ADC CH13 GND
29	ADC CH14 (CH6-)	I	30	ADC CH14 GND
31	ADC CH15 (CH7-)	I	32	ADC CH15 GND
33	DAC 2 OUT	O	34	DAC 2 GND
35	DAC 1 OUT	O	36	DAC 1 GND
37	External Reference	I	38	External Reference GND
39	GND	—	40	GND

Notes:

1. Signal name in parentheses applies to differential input connection.
2. Pins 39 and 40 are connected internally to DAC 2 GND.

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	*Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	*Buffered Address Bit 6
9a	BA5/	*Buffered Address Bit 5	9c	BA4/	*Buffered Address Bit 4
10a	BA3/	*Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	*Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	Bφ1	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	*Buffered DMA Request 1
15a	BRDY	Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	-12V/-V	-15 Vdc
17a	+12V/+V	+15 Vdc	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	Bφ0	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR/W	Buffered Read/Write "Not"	21c	BDRQ2/	*Buffered DMA Request 2
22a		*System Spare	22c	BR/W	*Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request	24c	BNMI/	*Buffered Non-Maskable Interrupt
25a	Bφ2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	Bφ2	Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note:

*Not used on this module.

Analog Input/Output Module Conversion Characteristics

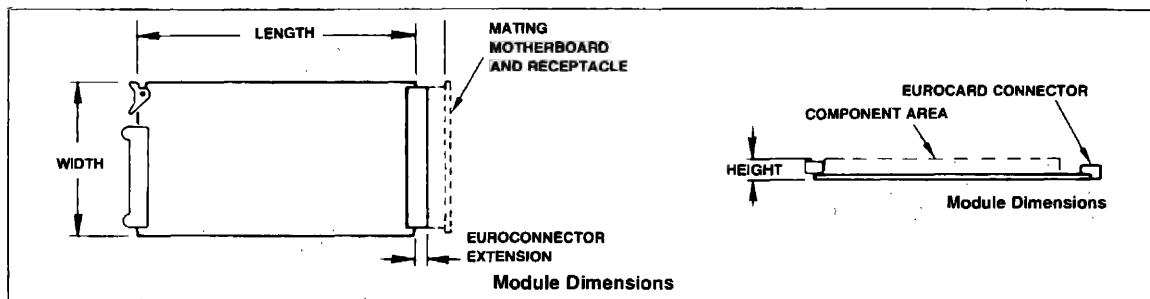
Characteristic	Value
Analog Inputs	
Number of Inputs (Header Selectable)	
Single-Ended	16
Differential	8
Input Voltage Ranges (Jumper Selectable)	
Unipolar	0 to +5V, 0 to +10V
Bipolar	$\pm 2.5V$, $\pm 5V$, $\pm 10V$
Input (Bias) Current	± 50 nA (max.) (25°C)
Input Impedance	
ON Channel	3×10^9 ohm, 50 pf
OFF Channel	1×10^{10} ohm, 20 pf
Input Overvoltage	$\pm V \pm 15V$ (max.) ($\pm V$ supply ON or OFF)
Input Overvoltage Current	15 ma ($\pm V \pm 15V$)
Common Mode Rejection (Differential) (DC-60 Hz with 1K ohm source unbalance)	74 db (min.)
Resolution	12 bits (1 part in 4096)
Accuracy	
Gain error	0.3% FSR (max., adjustable to zero)
Unipolar offset	± 110 mV (max., adjustable to zero)
Bipolar offset	± 150 mV max., adjustable to zero)
Linearity error	0.1% FSR (max.)
Temperature Coefficients	
Gain	± 50 PPM FSR /°C
Offset	± 60 PPM FSR /°C
Differential Linearity (no missing codes over temperature range)	10 Bits
Signal Dynamics	
Conversion Time (from read of most significant byte)	
12-Bit	35 μ s—typical 45 μ s—maximum
8-Bit	25 μ s—typical 35 μ s—maximum
Small-signal Bandwidth, 1% flatness	50 kHz
Full Peak Response	15 kHz
Analog Outputs	
Number of Outputs	2
With Internal Reference Voltage	
Output Voltage Ranges (Jumper Selectable)	
Unipolar	0 to +5V, 0 to +10V
Bipolar	$\pm 2.5V$, $\pm 5V$, $\pm 10V$
With External Reference Voltage (V_{REF})	
Input Impedance	4.7K ohms $\pm 5\%$
Reference Voltage Range	$\pm 11V$
Output Voltage Gain Range (Jumper Selectable)	
Unipolar	0 to $+5 V_{REF}$, 0 to V_{REF} , 0 to $2 V_{REF}$
Bipolar	$\pm .25 V_{REF}$, $\pm .5V_{REF}$, $\pm V_{REF}$
Output Drive Current ($\pm 10V$)	+5 mA (min)
Resolution	12 Bits (1 part in 4096)
Accuracy	
Gain Error	0.3% FSR (max., adjustable to zero)
Unipolar Offset	30 mV (max., adjustable to zero)
Bipolar Offset	60 mV (max., adjustable to zero)
Linearity Error	0.05% FSR (max.)
Temperature Coefficients	
Gain	± 60 PPM FSR /°C
Offset	± 15 PPM FSR /°C
Differential Linearity (no missing codes over temperature range)	10 Bits
Signal Dynamics	
Settling time to 0.05% FSR	10 μ s
Output Slew Rate	10 V/ μ s

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3)	
Width	100 mm (3.94 in.)
Length	160 mm (6.3 in.)
Height	14 mm (0.56 in.)
Weight	156 g (5.5 oz.)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	
Analog Input/Output (RM65-5303E)	+5 Vdc \pm 5% at 425 mA—typical, 675 mA—max. +15 Vdc \pm 5% at 30 mA—typical, 60 mA—max. -15 Vdc \pm 5% at 40 mA—typical, 80 mA—max.
Analog Input (RM65-5302E)	+5 Vdc \pm 5% at 425 mA—typical, 675 mA—max. +15 Vdc \pm 5% at 12 mA—typical, 25 mA—max. -15 Vdc \pm 5% at 25 mA—typical, 50 mA—max.
Connectors	
RM 65 Bus Connector P1	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)—mates with Burndy P196B32R00A00L-9 or equivalent.
I/O Connector J1	40-pin mass termination (0.100 in. centers)—mates with Burndy FRS40BS4P connector or equivalent.

Notes:

1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. Length does not include the added extension due to the module ejector.
3. Dimensions conform to DIN 41612.





RM65-5451E

RM 65 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA) MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-5451E ACIA Module is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 modules use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desk-top microcomputer applications.

PRODUCT OVERVIEW

The RM65-5451E Asynchronous Communications Interface Adapter (ACIA) Module interfaces two independent, asynchronous serial I/O channels to the RM 65 Bus. Each channel may operate as a data terminal or a data set, as selected by jumpers on the module. Both RS-232C and 20 ma TTY current loop interfaces are provided on Channel No. 1. An RS-232C interface is provided on Channel No. 2.

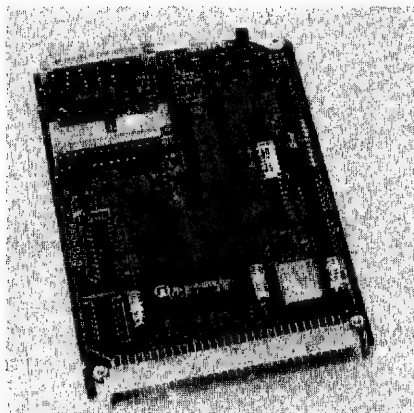
Each I/O channel performs serial-to-parallel and parallel-to-serial data conversions using an R6551 Asynchronous Communication Interface Adapter (ACIA). Both receiver and transmitter may operate with a programmable word length of 5, 6, 7, or 8 bits. Further, each channel can transmit and receive at 15 different program-selectable rates, between 50 and 19,200 baud. The receive rate is the same as the transmit rate.

FEATURES

- Compact size—Approximately 4" × 6¼" (100 mm × 160 mm)
- Buffered address, data and control lines
- Two independent channels
- On-board 1.8432 MHz crystal frequency reference
- Programmable baud rate selection of 15 different rates (50, 75, 109.92, 134.58, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, or 19,200 bits per second)
- Programmable control of:
 - Word length (5, 6, 7 or 8 bits)
 - Number of stop bits (1, 1½, 2)
 - Parity (odd, even or none)
- Address select switch allows the starting address of the serial channel I/O to be assigned to a page boundary.
- On-board DC/DC Converter allows +5V only operation for RS-232 interface.

ORDERING INFORMATION

Part No.	Description
RM65-5451E	Asynchronous Communications Interface Adapter (ACIA) Module
Order No.	Description
804	Asynchronous Communications Interface Adapter (ACIA) Module User's Module



RM65-5451E Asynchronous Communications
Interface Adapter (ACIA) Module

FUNCTIONAL DESCRIPTION

The Data Transceivers invert and transfer 8-bits of parallel data between the R6551 ACIA devices and the RM 65 Bus depending on the state of the transceiver enable and read/write signals. During a write operation, the data received from the bus are written into the addressed ACIA device. During a read operation, the data read from the addressed ACIA device are driven onto the bus. When the ACIA module is not addressed, the transceivers are disabled.

The Address Buffers invert and transfer the three least significant address lines to the ACIA devices. Two lines generate the register address while one line selects one of the two ACIA devices.

The Control Buffers invert and drive the bank address, clock and read/write signals from the bus onto the module and drive the bus active and interrupt request lines onto the bus.

The ACIA module may be assigned to common banks (both Bank 0 and Bank 1) or to a dedicated bank (either Bank 0 or Bank 1), depending on the Bank Select and Bank Select Enable switch positions. The Bank Select Control circuit detects when the ACIA module is bank-addressed, by comparing the bank address control signal from the RM 65 Bus with the Bank Select switch position. If a match occurs and the Bank Select Enable switch is on, base address decoding is enabled.

The Base Address Buffer/Comparator buffers the eight most significant address lines from the bus and compares them to the Base Address Select switches. When a match occurs, the ACIA module is enabled.

Two R6551 ACIA devices convert data from serial-to-parallel format for input to the RM 65 Bus and from parallel-to-serial format for output from the bus. Each ACIA device contains a programmable control register to allow baud rate, word length and the number of stop bits to be programmed. A command register allows ACIA interrupt and parity modes to be specified under program control. A status register may be interrogated to determine the status of the data transfer and the cause for an interrupt request.

The RS-232 Interface circuit contains line receivers and line drivers, to convert signals from internal TTL levels to external RS-232C levels. Jumpers are provided to specify Data Set or Data Terminal operation. Jumpers are also provided to simulate RS-232 control signals that are not available from the interfacing equipment.

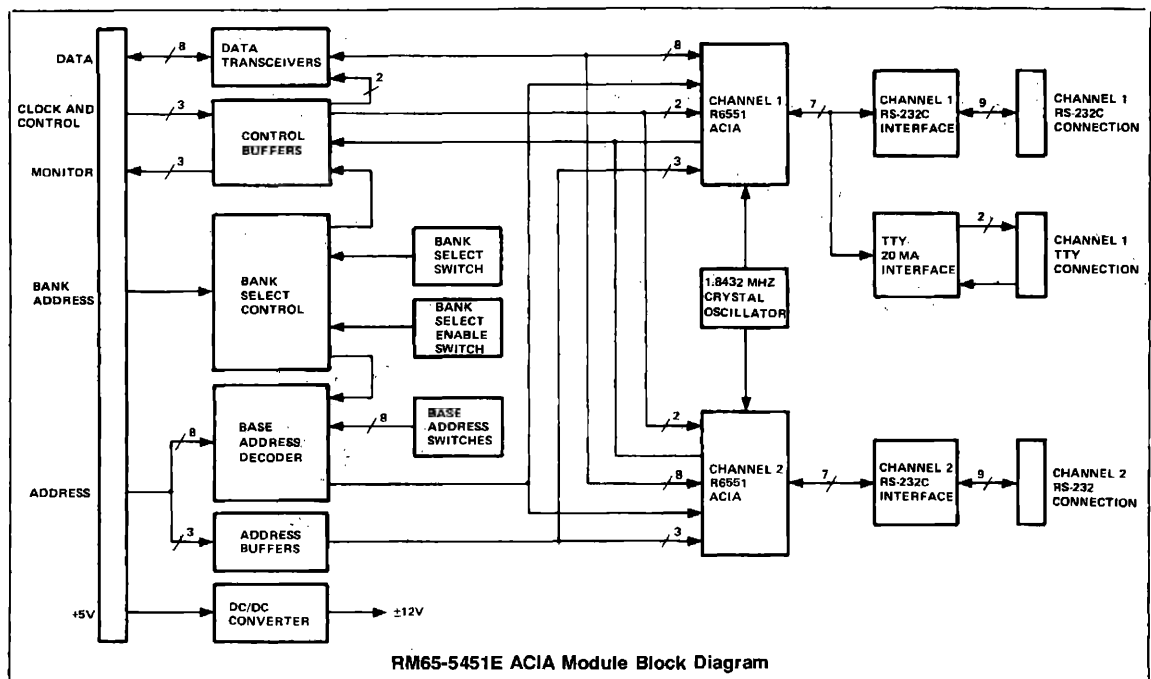
Opto-couplers in the TTY Interface circuit provide 20 ma current loop sourcing and sinking between the ACIA module and an external TTY.

A 1.8432 Mhz crystal generates the data transmission frequency reference, which the ACIA devices convert to the desired baud rate under program control.

The DC/DC Converter generates ± 12 Vdc from +5 Vdc for RS-232 operation.

Power Source For TTY Operation

For TTY operation, the ± 12 Vdc must be obtained from the RM 65 Bus, by removing the DC/DC voltage converter and installing two jumpers.



RM 65 Bus Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Pin	Signal Mnemonic	Signal Name	Input/Output	Pin	Signal Mnemonic	Signal Name	Input/Output
1a	GND	Ground		1c	+5V	+5 Vdc	
2a	BADP/	Buffered Bank Address	I	2c	BA15/	Buffered Address Bit 15	I
3a	GND	Ground		3c	BA14/	Buffered Address Bit 14	I
4a	BA13/	Buffered Address Bit 13	I	4c	BA12/	Buffered Address Bit 12	I
5a	BA11/	Buffered Address Bit 11	I	5c	GND	Ground	
6a	BA10/	Buffered Address Bit 10	I	6c	BA9/	Buffered Address Bit 9	I
7a	BA8/	Buffered Address Bit 8	I	7c	BA7/	*Buffered Address Bit 7	
8a	GND	Ground		8c	BA6/	*Buffered Address Bit 6	
9a	BA5/	*Buffered Address Bit 5		9c	BA4/	*Buffered Address Bit 4	
10a	BA3/	*Buffered Address Bit 3		10c	GND	Ground	
11a	BA2/	Buffered Address Bit 2	I	11c	BA1/	Buffered Address Bit 1	I
12a	BA0/	Buffered Address Bit 0	I	12c	B ϕ 1	*Buffered Phase 1 Clock	
13a	GND	Ground		13c	BSYNC	*Buffered Sync	
14a	BSO	*Buffered Set Overflow		14c	BDRQ1/	Buffered DMA Request 1	
15a	BRDY	*Buffered Ready		15c	GND	Ground	
16a		*User Spare 1		16c	-12V/-V	-12 Vdc/-V	
17a	+12V/+V	+12 Vdc/+V		17c		*User Spare 2	
18a	GND	Ground Line		18c	BFLT/	*Buffered Bus Float	
19a	BDMT/	*Buffered DMA Terminate		19c	B ϕ 0	*Buffered External Phase 0 Clock	
20a		*User Spare 3		20c	GND	Ground	
21a	BR/W/	Buffered Read/Write "Not"	I	21c	BDRQ2/	*Buffered DMA Request 2	
22a		*System Spare		22c	BR/W/	*Buffered Read/Write	
23a	GND	Ground		23c	BACT/	Buffered Bus Active	O
24a	BIRQ/	Buffered Interrupt Request	O	24c	BNMI/	*Buffered Non-Maskable Interrupt	
25a	B ϕ 2/	Buffered Phase 2 "Not" Clock	I	25c	GND	Ground	
26a	B ϕ 2	*Buffered Phase 2 Clock		26c	BRES/	Buffered Reset	I
27a	BD7/	Buffered Data Bit 7	I/O	27c	BD6/	Buffered Data Bit 6	I/O
28a	GND	Ground		28c	BD5/	Buffered Data Bit 5	I/O
29a	BD4/	Buffered Data Bit 4	I/O	29c	BD3/	Buffered Data Bit 3	I/O
30a	BD2/	Buffered Data Bit 2	I/O	30c	GND	Ground	
31a	BD1/	Buffered Data Bit 1	I/O	31c	BD0/	Buffered Data Bit 0	I/O
32a	+5V	+5 Vdc		32c	GND	Ground	

Note:

*Not used on this module.

I/O Connector J1—TTY Interface

Pin	Signal Mnemonic	Signal Name	Input/Output
1	RTS	Request-To-Send	O
2	TD	Transmit Data	O
3	RD	Receive Data	I
4	-12V	-12 Vdc	

I/O Connector J2 and J3—RS-232 Interface

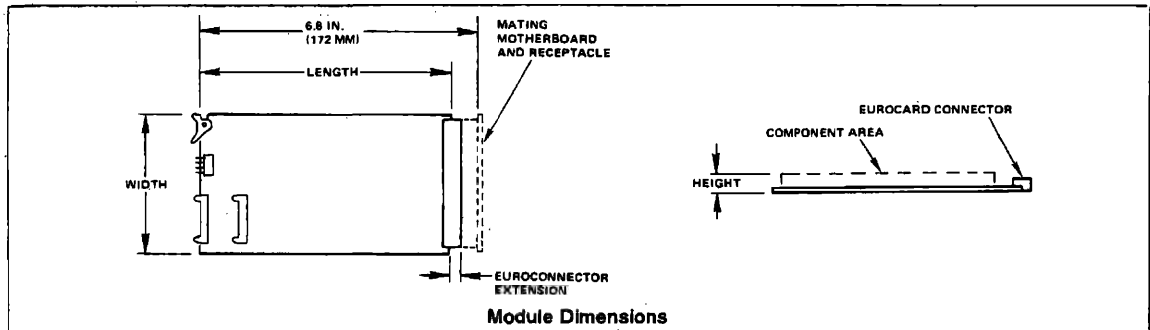
Pin	Signal Mnemonic	Signal Name	Input/Output	
			Data Set	Data Terminal
1	GND	Ground		
2	TD	Transmit Data	I	O
3	RD	Receive Data	O	I
4	RTS	Request-To-Send	I	O
5	CTS	Clear-To-Send	O	I
6	DSR	Data-Set-Ready	O	I
7	GND	Ground		
8	DCD	Data-Carrier-Detected	O	I
9-19		Not Used		
20	DTR	Data-Terminal-Ready	I	O
21-26		Not Used		

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3) Width Length Height	3.9 in. (100 mm) 6.3 in. (160 mm) 0.56 in. (14 mm)
Weight	5.2 oz. (145 g)
Environment Operating Temperature Storage Temperature Relative Humidity	0°C to 70°C -40°C to +85°C 0% to 85%, without condensation
Power Requirements RS-232 Interface Operation, with DC/DC Converter TTY Operation, without DC/DC Converter	+5 Vdc \pm 5% @ 0.4A (2.0W)—Typical 0.7A (3.5W)—Maximum +5 Vdc \pm 5% @ 0.5A (2.5W)—Maximum +12 Vdc \pm 10% @ 0.12A (1.4W)—Maximum -12 Vdc \pm 10% @ 0.12A (1.4W)—Maximum
Interfaces RM 65 Bus I/O Interface RS-232 TTY	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed) 26-pin mass termination connector (0.100 in. centers) 4-pin plug (0.156 in. centers)

Notes:

- Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
- Length does not include extensions beyond the edge of the module due to connectors or the module ejector.
- Dimensions conform to DIN 41612.





RM65-7004E AND RM65-7004NE RM 65 4-SLOT PIGGYBACK MODULE STACK AND MOTHERBOARD

RM 65 MICROCOMPUTER MODULES

The RM65-7004E 4-Slot Piggyback Module Stack (PMS) and RM65-7004NE Motherboard is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Modules products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 module products use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A set of card cages allows a broad variety of packaging options. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and desktop microcomputer applications.

PRODUCT OVERVIEW

The 4-Slot Piggyback Module Stack (PMS) consists of a 4-slot RM 65 Bus compatible motherboard in a card cage. Memory, I/O or special functions may be added to the AIM 65 Microcomputer by use of the PMS. When connected to the AIM 65 Master Module through the Buffer/Adapter Module, the PMS may be mounted over, under, or behind the AIM 65 Master Module in a variety of orientations to meet unique application requirements. The form factor of the PMS allows low profile placement in a table top or terminal style enclosure.

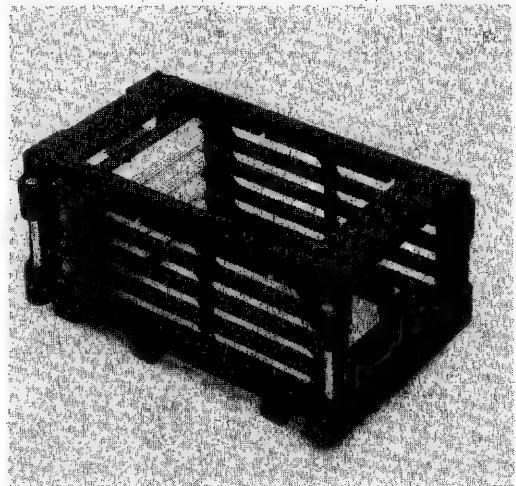
The 4-Slot Motherboard is a printed circuit board (PCB) less four connectors, mini-terminal strip, four mounting blocks used to fasten the PCB to the card cage. Connectors, mini-terminal strip and custom mounting blocks can easily be added to meet unique installation requirements.

FEATURES

- 4-slot card cage with integral module guides
- Rugged, but lightweight construction
- Accepts axial module cooling fan
- Screw-down terminals for connecting external power (+5V, +12V/+V, -12V/-V, GND)
- Predrilled holes for various mounting configurations
- Assembled, tested and warranted

ORDERING INFORMATION

Part No.	Description
RM65-7004E	4-Slot Piggyback Module Stack
RM65-7004NE	4-Slot Motherboard



RM65-7004E 4-Slot Piggyback Module Stack (PMS)

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RM65-7004E • RM65-7004NE 4-Slot Piggyback Module Stack and Motherboard

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	Bφ1	Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	Buffered Sync
14a	BSO	Buffered Set Overflow	14c	BDRQ1/	Buffered DMA Request 1
15a	BRDY	Buffered Ready	15c	GND	Ground
16a		User Spare 1	16c	-12V/ -V	-12 Vdc/ -V
17a	+12V/+V	+12 Vdc/+V	17c		User Spare 2
18a	GND	Ground Line	18c	BFLT/	Buffered Bus Float
19a	BDMT/	Buffered DMA Terminate	19c	Bφ0	Buffered External Phase 0 Clock
20a		User Spare 3	20c	GND	Ground
21a	BR/W/	Buffered Read/Write "Not"	21c	BDRQ2/	Buffered DMA Request 2
22a		System Spare	22c	BR/W/	Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request	24c	BNMI/	Buffered Non-Maskable Interrupt
25a	Bφ2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	Bφ2	Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

RM65-7004E • RM65-7004NE 4-Slot Piggyback Module Stack and Motherboard

MOTHERBOARD CONNECTION AND MODULE INSTALLATION

Connect power to TB1. The power lines should be long enough to allow the PMS to be oriented and positioned as required.

WARNING

The external power supplies must be turned off before connecting to TB1.

- Connect +5V from an external power supply to the terminal marked "+5". "+5" is connected to all +5V pins on all module receptacles.
- Connect GND from the power supply to either terminal marked "G". Both of these terminals are connected to all GND pins on all module receptacles.
- Connect +12V/+V from an external power supply to the terminal marked "+V". "+V" is connected to Pin 17a on each module receptacle.
- Connect GND from the +12V/+V power supply to either "G" terminal.
- Connect -12V/-V from an external power supply to the terminal marked "-V". "-V" is connected to Pin 16c on each module receptacle.
- Connect GND from the -12V/-V power supply to either "G" terminal.

Install the PMS in the desired position. Mounting holes are provided to allow attachment at the top or bottom of the PMS.

CAUTION

Ensure that neither the left nor right side of the PMS is blocked such that the flow of forced cooling air is impeded.

NOTE

If the PMS is positioned on the AIM 65 Master Module, ensure that the PMS feet rest in areas free of components.

Attach an axial cooling fan to the left side of the PMS. Connect the cooling fan power leads to the required power supply.

The following 3½ inch cooling fans or equivalent are recommended:

Manufacturer—ETRI Inc

- Model 760-99XW-182-11115*
115 Vac, 50/60 Hz, 6 watts
2500 RPM, 30 CFM
10 oz.
- Model 760-99XW-181-11220*
220 Vac, 50/60 Hz, 6 watts
2500 RPM, 30 CFM
10 oz.

*Requires plug-in power cord, 30" long—Model 760-9601-6.

Manufacturer—ROTRON Inc

- Model WA2F79**
115 Vac, 50/60 Hz, 13 watts
3000 RPM, 33 CFM
9 oz.
- Model WA2F77**
220 Vac, 50/60 Hz, 13 watts
3000 RPM, 33 CFM
9 oz.

**Includes two 6" power leads.

NOTE

ETRI Finger guard Model 760-9901-43 may be used with any of these fans.

Install a module in the PMS as follows:

CAUTION

Power must be turned off to the PMS motherboard before installing a module.

- Position the module, component side up, in front of the desired card slot.

Card slot No. 1 (top-most slot) has 0.85 inch of component clearance whereas the other three slots are on 0.6 inch centers. If a module is higher than 0.4 inches above the surface of the module, install it in card slot No. 1.

- Insert the module into the card guide and slide the module straight in until it touches the mating motherboard receptacle.

NOTE

The card slot guides may be snug on the inserted module.

- Ensure that the module connector is positioned properly against the mating receptacle.
- Press in firmly on the exposed edge of the module until it is firmly seated.

Remove a module from the PMS as follows:

CAUTION

Remove power from the PMS motherboard before removing a module.

- Lift up on the module ejector tab, if installed; otherwise grasp the exposed edge of the module and pull, to release the module from the mating receptacle.
- Pull the module straight back until it is free from the card slot guides.

RM65-7004E • RM65-7004NE 4-Slot Piggyback Module Stack and Motherboard

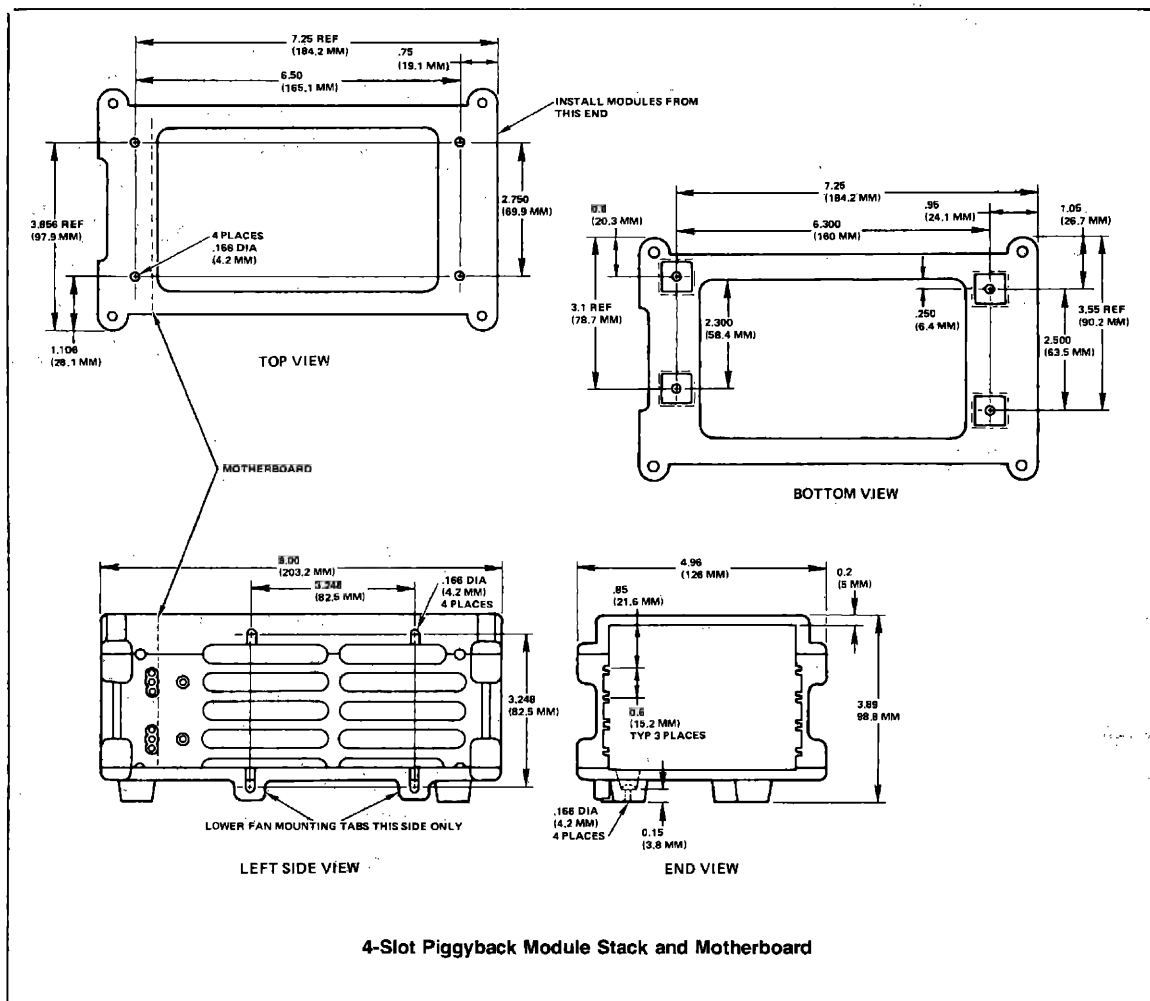
4-CONNECTOR MOTHERBOARD ASSEMBLY

The RM65-7004NE 4-slot motherboard can be assembled as follows:

- Install up to four module connectors (receptacles) from the front of the PCB. Be sure to observe correct connector orientation. The following connectors or their equivalent, may be used:

Part No.	Manufacturer
P196B32R00K00K9	Burndy Corporation Norwalk, CT 06856
96S-6033-0531-3	Winchester Electronics Oakville, CT 06779
00-8257-096-649-124	Elco Corporation Huntington, PA 16652

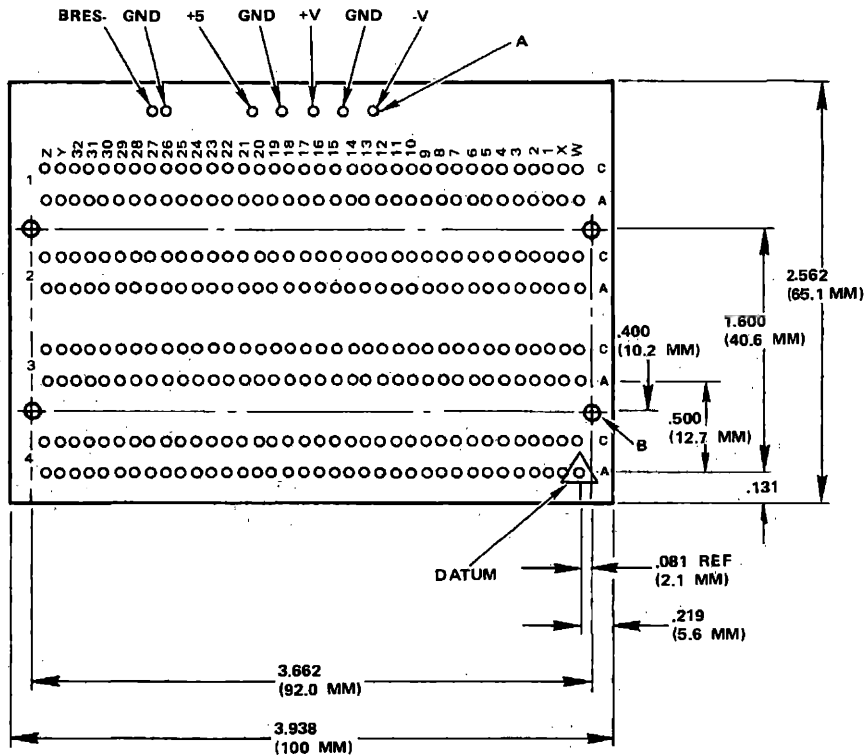
- Solder the receptacle pin connections to the back of the PCB.
- Install the mini-terminal strip to the power supply connection holes from the back of the PCB.
- Solder the mini-terminal strip leads to the front of the PCB.



RM65-7004E • RM65-7004NE 4-Slot Piggyback Module Stack and Motherboard

SPECIFICATIONS

Parameter	Value
RM65-7004E 4-Slot PMS Dimensions	
Width	4.96 in. (126 mm)
Length	8.00 in. (203 mm)
Height	3.89 in. (99 mm)
Weight	13 oz. (370 g)
Module Separation	
Slot 1: Centerline to Inside Top Cover	0.85 in. (22 mm)
Other Slots: Centerline to Centerline	0.6 in. (15 mm)
RM65-7004NE Motherboard Dimensions	
Width	3.938 in. (100 mm)
Length	2.562 in. (65.1 mm)
Height	0.062 in. (1.6 mm)
Hole Size	
Uncoded	0.037 in. (0.940 mm) dia.
A	0.044 in. (1.12 mm) dia.
B	0.128 in. (3.25 mm) dia.



RM65-7004NE 4-Slot Motherboard (Rear View)



RM65-7008E AND RM65-7008NE RM 65 8-SLOT CARD CAGE AND MOTHERBOARD

RM 65 MICROCOMPUTER MODULES

The RM65-7008E 8-Slot Card Cage and RM65-7008NE 8-Slot Motherboard is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 modules use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A set of card cages allows a broad variety of packaging options. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and desktop microcomputer applications.

PRODUCT OVERVIEW

The RM65-7008E 8-slot Card Cage consists of an 8-slot RM 65 Bus compatible motherboard in a card cage. Memory, I/O or special functions may be added to the AIM 65 Microcomputer by use of the 8-slot card cage. When connected to the AIM 65 Master Module through the Buffer/Adapter Module, the card cage may be mounted over, under, or behind the AIM 65 Master Module in a variety of orientations to meet unique application requirements. The form factor of the 8-slot card cage allows low profile placement in a table top or terminal style enclosure.

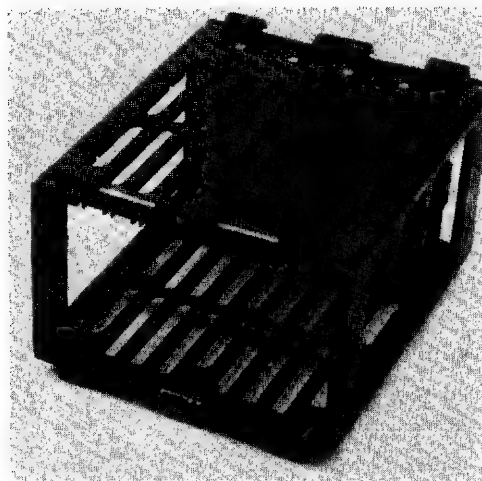
The RM65-7008NE 8-Slot Motherboard is a printed circuit board (PCB) less eight connectors, three filter capacitors, two mini-terminal strips and eight mounting blocks used to fasten the PCB to the card cage. Connectors, mini-terminal strips, filter capacitors and custom mounting blocks as needed can easily be added to meet unique installation requirements.

FEATURES

- 8-slot card cage with integral module guides
- Rugged, but lightweight construction
- Accepts axial module cooling fan
- Screw-down terminals for connecting external power (+5V, +12V/+V, -12V/-V, GND)
- Predrilled holes for various mounting configurations
- Assembled, tested and warranted
- Removable jumpers on motherboard support $\pm 12V$ as well as $\pm V$.

ORDERING INFORMATION

Part No.	Description
RM65-7008E	8-Slot Card Cage
RM65-7008NE	8-Slot Motherboard



RM65-7008E 8-Slot Card Cage

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	B ϕ 1	Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	Buffered Sync
14a	BSO	Buffered Set Overflow	14c	BDRQ1/	Buffered DMA Request 1
15a	BRDY	Buffered Ready	15c	GND	Ground
16a		User Spare 1	16c	-12V/-V	-12 Vdc/-V
17a	+12V/+V	+12 Vdc/+V	17c		User Spare 2
18a	GND	Ground Line	18c	BFLT/	Buffered Bus Float
19a	BDMT/	Buffered DMA Terminate	19c	B ϕ 0	Buffered External Phase 0 Clock
20a		User Spare 3	20c	GND	Ground
21a	BR/ \overline{W} /	Buffered Read/Write "Not"	21c	BDRQ2/	Buffered DMA Request 2
22a		System Spare	22c	BR/ \overline{W}	Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request	24c	BNMI/	Buffered Non-Maskable Interrupt
25a	B ϕ 2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	B ϕ 2	Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

MOTHERBOARD CONNECTION AND MODULE INSTALLATION

Connect power to TB1 and/or TB2. The power lines should be long enough to allow the card cage to be oriented and positioned as required.

WARNING

The external power supplies must be turned off before connecting to TB1 or TB2.

- Connect +5V from an external power supply to either terminal marked "+5". "+5" is connected to all +5V pins on all module receptacles.
- Connect GND from the power supply to either terminal marked "G". Both of these terminals are connected to all GND pins on all module receptacles.
- Connect +12V/+V from an external power supply to the terminal marked "+V". "+V" is connected to Pin 17a on each module receptacle.

NOTES

If both +12V and +V (e.g., +15V) are required, remove the soldered jumper corresponding to pin 17a between receptacle 6 and 7 on the soldered side of the motherboard. Connect +12V to TB1 if six or less modules require +12V, or to TB2 if more than six modules require +12V. Connect +V to the other terminal strip.

If the jumper has been removed and only one voltage is required (i.e., +12V or +V), connect the power lead to both TB1 and TB2.

- Connect GND from the +12V/+V power supply to either "G" terminal.
- Connect -12V/-V from an external power supply to the terminal marked "-V". "-V" is connected to Pin 16c on each module receptacle.

NOTES

If both -12V and -V (e.g., -15V) are required, remove the soldered jumper corresponding to pin 16c between

receptacle 6 and 7 on the soldered side of the motherboard. Connect -12V to TB1 if six or less modules require -12V or to TB2 if more than six modules require -12V. Connect -V to the other terminal strip.

If the jumper has been removed and only one voltage is required (i.e., -12V or -V) connect the power lead to both TB1 and TB2.

- f. Connect GND from the -12V/-V power supply to either "G" terminal.

Install the card cage in the desired position. Mounting holes are provided to allow attachment at the top or bottom of the card cage.

CAUTION

Adequate cooling must be provided to keep the temperature of the installed modules within specified operating limits.

Install a module in the card cage as follows:

CAUTION

Power must be turned off to the card cage motherboard before installing a module.

- a. Position the module, component side facing TB1 end, in front of the desired card slot.

Card slot No. 1 (slot closest to TB1) has 0.85 inch of component clearance whereas the other fifteen slots are 0.6 inch centers. If a module is higher than 0.4 inch above the surface of the module, install it in card slot No. 1.

CAUTION

If $\pm 12V$ and $\pm V$ have been connected to different terminal strips (TB1 or TB2), ensure that any modules requiring $\pm 12V$ or $\pm V$ are installed in the slots corresponding to the proper voltage.

- b. Insert the module into the card guide and slide the module straight in until it touches the mating motherboard receptacle.

NOTE

The card slot guides may be snug on the inserted module.

- c. Ensure that the module connector is positioned properly against the mating receptacle.

CAUTION

A key is installed in each edge connector receptacle between pin 5 and pin 6. Forcing an edge connector module without a corresponding slot in the plug may damage the receptacle and/or the module.

- d. Press in firmly on the exposed edge of the module until it is firmly seated.

Remove a module from the card cage as follows:

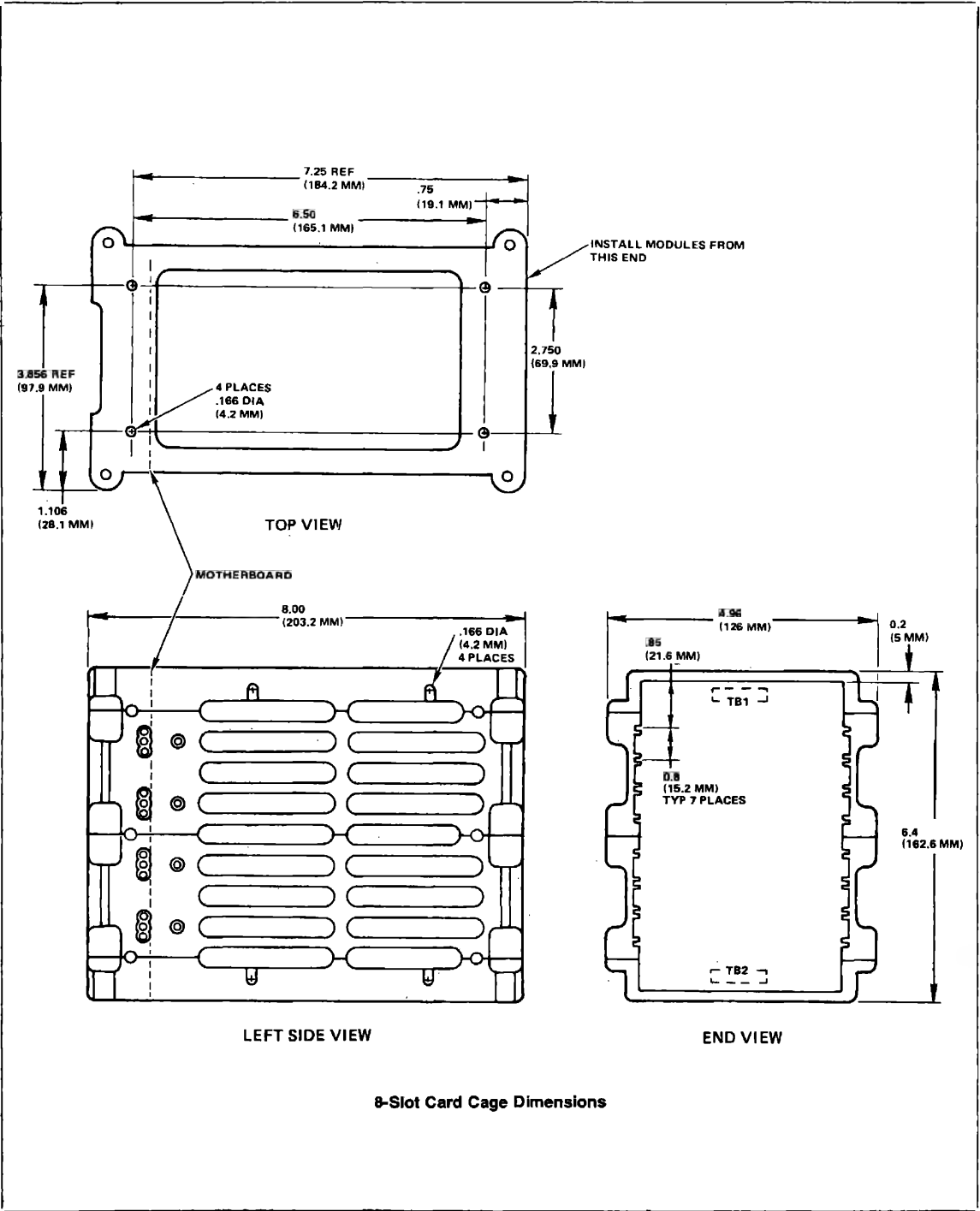
CAUTION

Remove power from the card cage motherboard before removing a module.

- a. Lift up on the module ejector tab, if installed; otherwise grasp the exposed edge of the module and pull, to release the module from the mating receptacle.
- b. Pull the module straight back until it is free from the card slot guides.

SPECIFICATIONS

Parameter	Value
8-Slot Card Cage Dimensions	
Width	4.96 in. (126 mm)
Length	8.00 in. (203 mm)
Height	6.40 in. (162.6 mm)
Module Separation	
Slot 1: Centerline to Inside Top Cover	0.85 in. (22 mm)
Other Slots: Centerline to Centerline	0.6 in. (15 mm)
Weight	1 lb. 6 oz. (624 g)
8-Slot Motherboard Dimensions	
Width	3.938 in. (100 mm)
Length	5.725 in. (145 mm)
Height	0.062 in. (1.6 mm)
Hole Size	
Uncoded	0.037 in. (0.940 mm) dia.
A	0.044 in. (1.12 mm) dia.
B	0.128 in. (3.25 mm) dia.



8-SLOT MOTHERBOARD ASSEMBLY

The RM65-7008NE 8-slot motherboard can be assembled using the printed circuit board as follows:

- a. Install up to eight module connectors (receptacles) from the front of the PCB. Be sure to observe correct connector orientation. The following connectors or their equivalent, may be used:

Part No.	Manufacturer
P196B32R00K00K9	Burndy Corporation Norwalk, CT 06856
96S-6033-0531-3	Winchester Electronics Oakville, CT 06779
00-8257-096-649-124	Elco Corporation Huntington, PA 16652

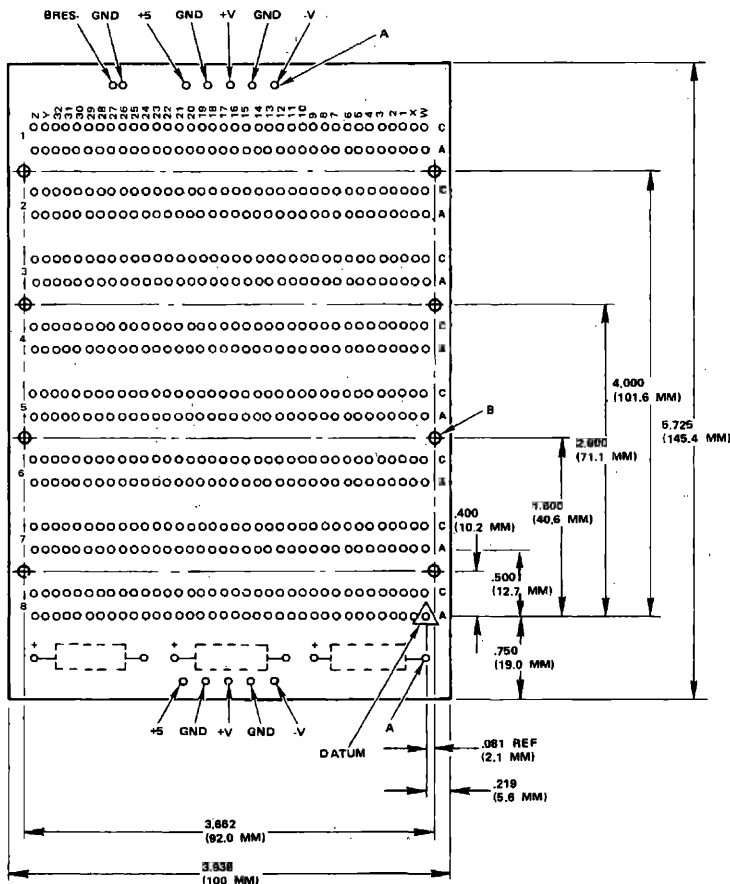
- b. Solder the receptacle pin connections to the back of the PCB.

- c. Install three 100 ufd, 25 Vdc capacitors from +5V to GND, +V to GND, and -V to GND, from the front of the PCB. Be sure to observe correct polarity.

- d. Solder the capacitor leads to the back of the PCB.

- e. Install one or two miniterminal strips to the power supply connection holes from the back of the PCB.

- f. Solder the miniterminal strip leads to the front of the PCB.





RM65-7016E AND RM65-7016NE RM 65 16-SLOT CARD CAGE AND MOTHERBOARD

RM 65 MICROCOMPUTER MODULES

The RM65-7016E 16-Slot Card Cage and RM65-7016NE Motherboard are one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Modules products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 modules use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A set of card cages allows a broad variety of packaging options. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and desktop microcomputer applications.

PRODUCT OVERVIEW

The RM65-7016E 16-slot card cage consists of a 16-slot RM 65 Bus compatible motherboard in a card cage. Memory, I/O or special functions may be added to the AIM 65 Microcomputer by use of the 16-slot card cage. When connected to the AIM 65 Master Module through the Adapter/Buffer, the card cage may be mounted over, under, or behind the AIM 65 Master Module in a variety of orientations to meet unique application requirements. The form factor of the 16-slot card cage allows low profile placement in a table top or terminal style enclosure.

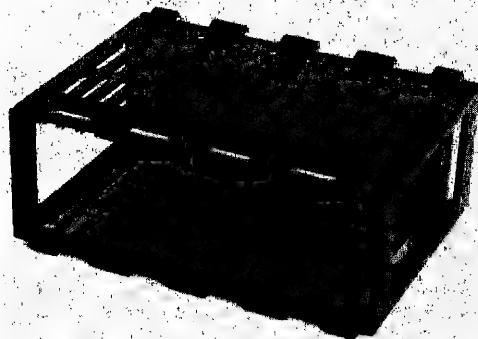
The RM65-7016NE 16-Slot Motherboard is a printed circuit board (PCB) less 16 connectors, two mini-terminal strips, three filter capacitors and 16 mounting blocks used to fasten the PCB to the RM65-7016E card cage. Connectors, mini-terminal strips, filter capacitors, and custom mounting blocks as needed can easily be added to meet unique installation requirements.

FEATURES

- 16-slot card cage with integral module guides
- Rugged, yet lightweight construction
- Screw-down terminals for connecting external power (+5V, +12V/+V, -12V/-V, GND)
- Predrilled holes for various mounting configurations
- Assembled, tested and warranted
- Removable jumpers on motherboard support $\pm 12V$ as well as $\pm V$.

ORDERING INFORMATION

Part No.	Description
RM65-7016E	16-Slot Card Cage
RM65-7016NE	16-Slot Motherboard



RM65-7016E 16-Slot Card Cage

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	B ϕ 1	Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	Buffered Sync
14a	BSO	Buffered Set Overflow	14c	BDRQ1/	Buffered DMA Request 1
15a	BRDY	Buffered Ready	15c	GND	Ground
16a		User Spare 1	16c	-12V/-V	-12 Vdc/-V
17a	+12V/+V	+12 Vdc/+V	17c		User Spare 2
18a	GND	Ground Line	18c	BFLT/	Buffered Bus Float
19a	BDMT/	Buffered DMA Terminate	19c	B ϕ 0	Buffered External Phase 0 Clock
20a		User Spare 3	20c	GND	Ground
21a	BR/W/	Buffered Read/Write "Not"	21c	BDRQ2/	Buffered DMA Request 2
22a		System Spare	22c	BR/W/	Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request	24c	BNMI/	Buffered Non-Maskable Interrupt
25a	B ϕ 2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	B ϕ 2	Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

MOTHERBOARD CONNECTION AND MODULE INSTALLATION

Connect power to TB1 and/or TB2. The power lines should be long enough to allow the card cage to be oriented and positioned as required.

WARNING

The external power supplies must be turned off before connecting to TB1 or TB2.

- Connect +5V from an external power supply to either terminal marked "+5". "+5" is connected to all +5V pins on all module receptacles.
- Connect GND from the power supply to either terminal marked "G". Both of these terminals are connected to all GND pins on all module receptacles.
- Connect +12V/+V from an external power supply to the terminal marked "+V". "+V" is connected to Pin 17a on each module receptacle.

NOTES

- If both +12V and +V (e.g., +15V) are required, remove the soldered jumper corresponding to pin 17a between receptacle 3 and 4 on the soldered side of the motherboard. Connect +12V to TB1 if three or less modules require +12V, or to TB2 if more than three modules require +12V. Connect +V to the other terminal strip.
- If the jumper has been removed and only one voltage is required (i.e., +12V or +V), connect the power lead to both TB1 and TB2.
- Connect GND from the +12V/+V power supply to either "G" terminal.
- Connect -12V/-V from an external power supply to the terminal marked "-V". "-V" is connected to Pin 16c on each module receptacle.

NOTES

- If both -12V and -V (e.g., -15V) are required, remove the soldered jumper corresponding to pin 16c between

receptacle 3 and 4 on the soldered side of the motherboard. Connect $-12V$ to TB1 if three or less modules require $-12V$ or to TB2 if more than three modules require $-12V$. Connect $-V$ to the other terminal strip.

2. If the jumper has been removed and only one voltage is required (i.e., $-12V$ or $-V$) connect the power lead to both TB1 and TB2.

- f. Connect GND from the $-12V$ – V power supply to either "G" terminal.

Install the card cage in the desired position. Mounting holes are provided to allow attachment at the top or bottom of the card cage.

CAUTION

Ensure that neither the left nor right side of the card cage is blocked such that the flow of forced cooling air is impeded.

Install a module in the card cage as follows:

CAUTION

Ensure that power is turned off to the card cage motherboard before installing a module.

- a. Position the module, component side facing TB1 end, in front of the desired card slot.

Card slot No. 1 (slot closest to TB1) has 0.85 inch of component clearance whereas the other seven slots are 0.6 inch centers. If a module is higher than 0.4 inch above the surface of the module, install it in card slot No. 1.

CAUTION

If $\pm 12V$ and $\pm V$ have been connected to different terminal strips (TB1 or TB2), ensure that any modules requiring $\pm 12V$ or $\pm V$ are installed in the slots corresponding to the proper voltage.

- b. Insert the module into the card guide and slide the module straight in until it touches the mating motherboard receptacle.

NOTE

The card slot guides may be snug on the inserted module.

- c. Ensure that the module connector is positioned properly against the mating receptacle.

CAUTION

A key is installed in each edge connector receptacle between pin 5 and pin 6. Forcing an edge connector module without a corresponding slot in the plug may damage the receptacle and/or the module.

- d. Press in firmly on the exposed edge of the module until it is firmly seated.

Remove a module from the card cage as follows:

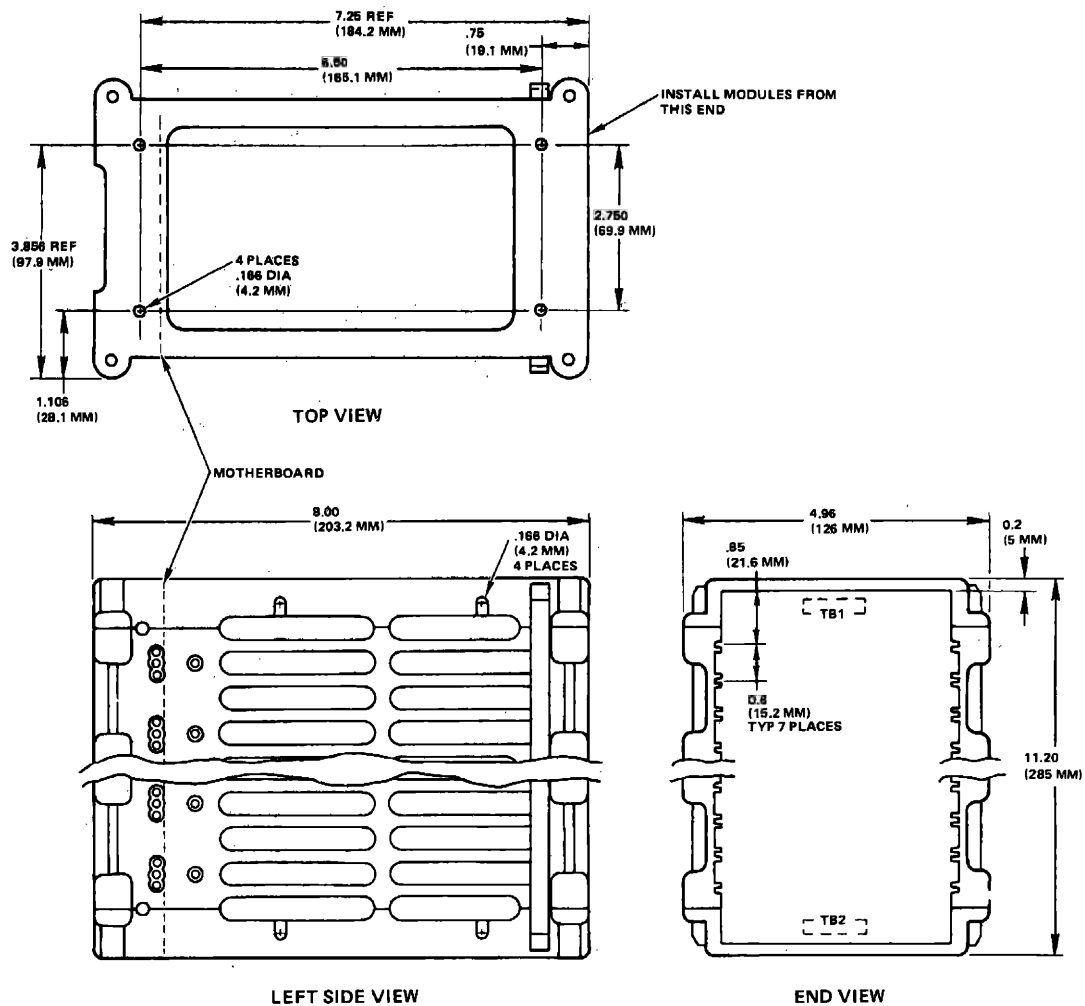
CAUTION

Remove power from the card cage motherboard before removing a module.

- a. Lift up on the module ejector tab, if installed; otherwise grasp the exposed edge of the module and pull, to release the module from the mating receptacle.
- b. Pull the module straight back until it is free from the card slot guides.

SPECIFICATIONS

Characteristic	Value
RM65-7016E Card Cage Dimensions	
Width	4.96 in. (126 mm)
Length	8.00 in. (203 mm)
Height	11.20 in. (285 mm)
Weight	2 lb. 10 oz. (1.20 kg)
Module Separation:	
Slot 1: Centerline to Inside Top Cover	0.85 in. (22 mm)
Other Slots: Centerline to Centerline	0.6 in. (15 mm)
RM65-7016NE Motherboard Dimensions	
Width	3.938 in. (100 mm)
Length	10.525 in. (267 mm)
Height	0.062 in. (1.6 mm)
Hole Size	
Uncoded	0.037 in. (0.940 mm) dia.
A	0.044 in. (1.12 mm) dia.
B	0.128 in. (3.25 mm) dia.



16-Slot Card Cage and Motherboard

16-CONNECTOR MOTHERBOARD ASSEMBLY

The RM65-7016NE 16-slot motherboard can be assembled as follows:

Install up to 16 module connectors (receptacles) from the front of the PCB. Be sure to observe correct connector orientation.

a. The following connectors or their equivalent, may be used:

Part No.	Manufacturer
P196B32R00K00K9	Bumdy Corporation Norwalk, CT 06856
96S-6033-0531-3	Winchester Electronics Oakville, CT 06779
00-8257-096-649-124	Elco Corporation Huntington, PA 16652

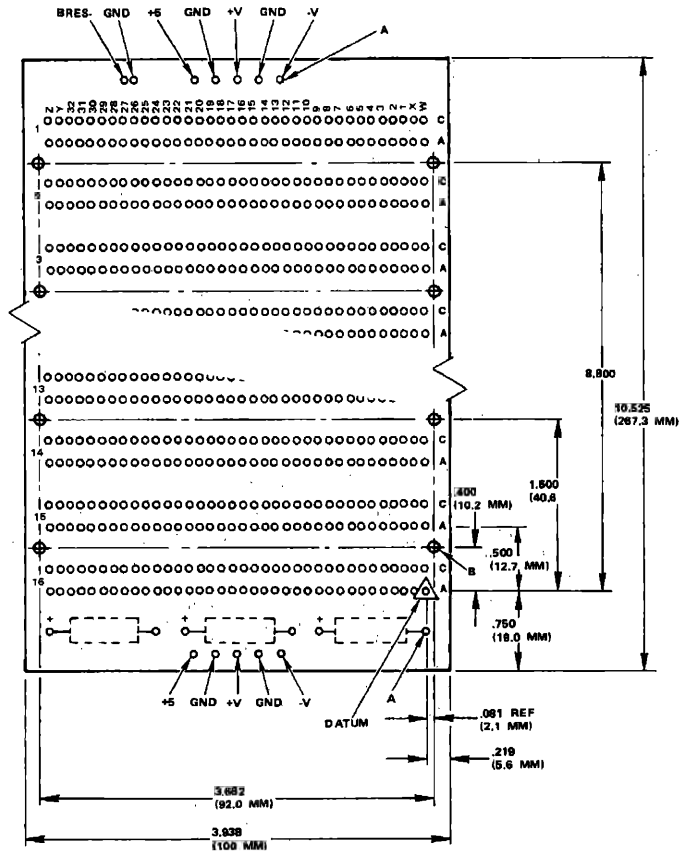
b. Solder the receptacle pin connections to the back of the PCB.

c. Install three 100 ufd, 25 VDC capacitors from +5V to GND, +V to GND, and -V to GND, from the front of the PCB. Be sure to observe correct polarity.

d. Solder the capacitor leads to the back of the PCB.

e. Install one or two mini-terminal strips to the power supply connection holes from the back of the PCB.

f. Solder the mini-terminal strip leads to the front of the PCB.



16-Slot Motherboard (Rear View)



RM65-7101E

RM 65 SINGLE CARD ADAPTER FOR AIM 65

RM 65 MICROCOMPUTER MODULES

The RM65-7101E Single Card Adapter for the AIM 65 Microcomputer is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 module products use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

FEATURES

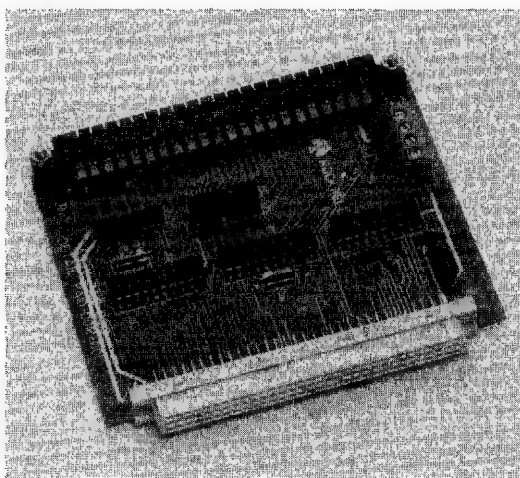
- Drives one RM 65 Bus-compatible module
- Provision for power and ground routing
- Extends address, data and control lines
- Pin and socket bus connector
- Fully assembled, tested and warranted

PRODUCT OVERVIEW

The RM65-7101E Single-Card Adapter allows one RM 65 Bus compatible module to be connected to the AIM 65 Master Module, through the AIM 65 Expansion connector. The Adapter routes the AIM 65 address, data and control lines from the AIM 65 Expansion connector pin assignments to the RM 65 Bus pin assignments. Drive circuitry is included on the address and data lines.

ORDERING INFORMATION

Part No.	Description
RM65-7101E	Single Card Adapter for AIM 65



RM65-7101E Single Card Adapter for AIM 65

FUNCTIONAL DESCRIPTION

The Single Card Adapter interfaces AIM 65 Expansion Connector signals to an attached RM 65 Bus receptacle. Data and address lines are buffered, whereas control lines are directly wired. All signals are routed from the AIM 65 Expansion Connector positions to corresponding RM 65 Bus receptacle pin positions. Ground is connected to the interspersed RM 65 Bus GND pins.

The Data Transceivers invert and drive 8-bits of parallel data between the AIM 65 Expansion Connector and the RM 65 Bus interface. During a write operation, data received from the AIM 65 Expansion Connector are driven into the interfacing RM 65 module. During a read operation, data read from the RM 65 module are transmitted into the AIM 65. When the RM 65 module is not addressed, the transceivers are disabled.

The Address Buffers invert and buffer 16 parallel address bits from the AIM 65 to the connected RM 65 module. The bank address line is held high to address Bank 0 (lower 65K) in the interfacing RM 65 module.

Eleven control and timing signals are directly connected between the AIM 65 Expansion Connector and the RM 65 module. The read/write, phase 2 clock, phase 1 clock, sync and reset AIM 65 output lines are routed directly to the RM 65 receptacle. The ready, interrupt request, set overflow and non-maskable interrupt lines from the RM 65 receptacle are connected straight through to the AIM 65 Expansion Connector interface.

A terminal block allows external +5V, +12V/+V, and -12V/-V power supplies to be connected as required. An on-board jumper allows the +5V for the RM 65 module to originate from the AIM 65 Expansion Connector or from the external +5V power supply.

POWER CONNECTION

+5 VOLT POWER CONNECTION

The +5 volt (+5V) required for the Single Card Adapter can be provided from the AIM 65 microcomputer through the AIM 65 Expansion Connector or directly from an external power supply through a connection to the on-board terminal board (TB1). Jumper A/B routes the +5V power from the selected source.

CAUTION

Turn off the external power supply before connecting power leads to the Single Card Adapter.

AIM 65 +5V POWER SOURCE CONNECTION

- Install Jumper A/B in the A position.
- Disconnect the +5V lead of the external power supply from the +5V connection on TB1.

WARNING

If the mating RM 65 module draws over 0.5A, the external connection to +5V must be used or the AIM 65 Master Module may be damaged.

EXTERNAL +5V POWER SOURCE CONNECTION

- Install Jumper A/B in the B position.
- Connect the +5V lead from the external power supply to the +5V connection on TB1.
- Connect the ground lead from the external +5V power supply to either of the two GND connections on TB1.

±12V/±V POWER CONNECTION

Connection points are provided on TB1 for ±12 Vdc, or other voltages, as required by the mating RM 65 module.

- Connect the +12V/+V lead from the external power supply to the TB1 connection marked +15V or +V. This terminal is connected to connector J1 pin 17a.
- Connect the -12V/-V lead from the external power supply to the TB1 connection marked -15V or -V. This terminal is connected to connector J1 pin 16c.

INSTALLATION

Before installing the module, inspect for damage and grease, dirt, liquid or other foreign material that will affect performance.

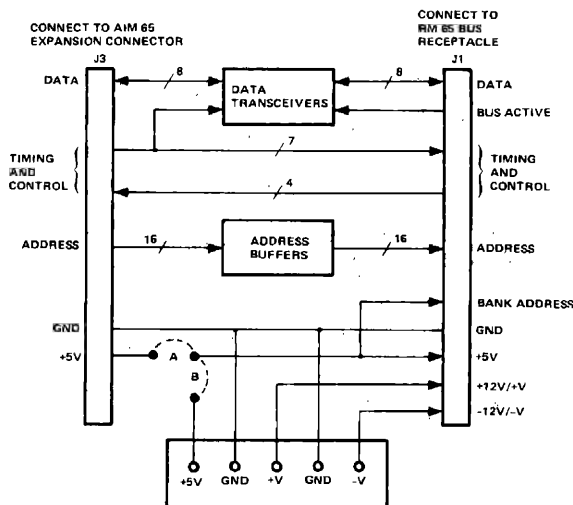
CAUTION

Prior to module installation, turn off power to the AIM 65 and, if applicable, the optional external +5V and/or ±12V/±V power supply input to the Adapter.

- Align pin 1 of J3 on the SCA with pin 1 of the Expansion Connector on the AIM 65 Master Module (component side up).
- Carefully insert the Adapter into the Expansion Connector.
- Press in firmly until all pins are securely seated.
- Install the RM 65 module into the J1 connector on the Adapter using installation procedures described in the documentation for the particular module. Ensure that Bank Select switches on the add-on module are positioned to Bank Select 0 or Bank Select Disable, as appropriate.
- Turn on power to the AIM 65 and, if applicable, turn on external +5 Vdc and/or ±12V/±V to the SCA module.

REMOVAL

- Turn off power to the AIM 65 and if applicable, to the external ±12V/±V power supplies.
- Pull the Adapter straight back while moving it slightly from side to side to disconnect it from the AIM 65 Expansion Connector.



Single Card Adapter Block Diagram

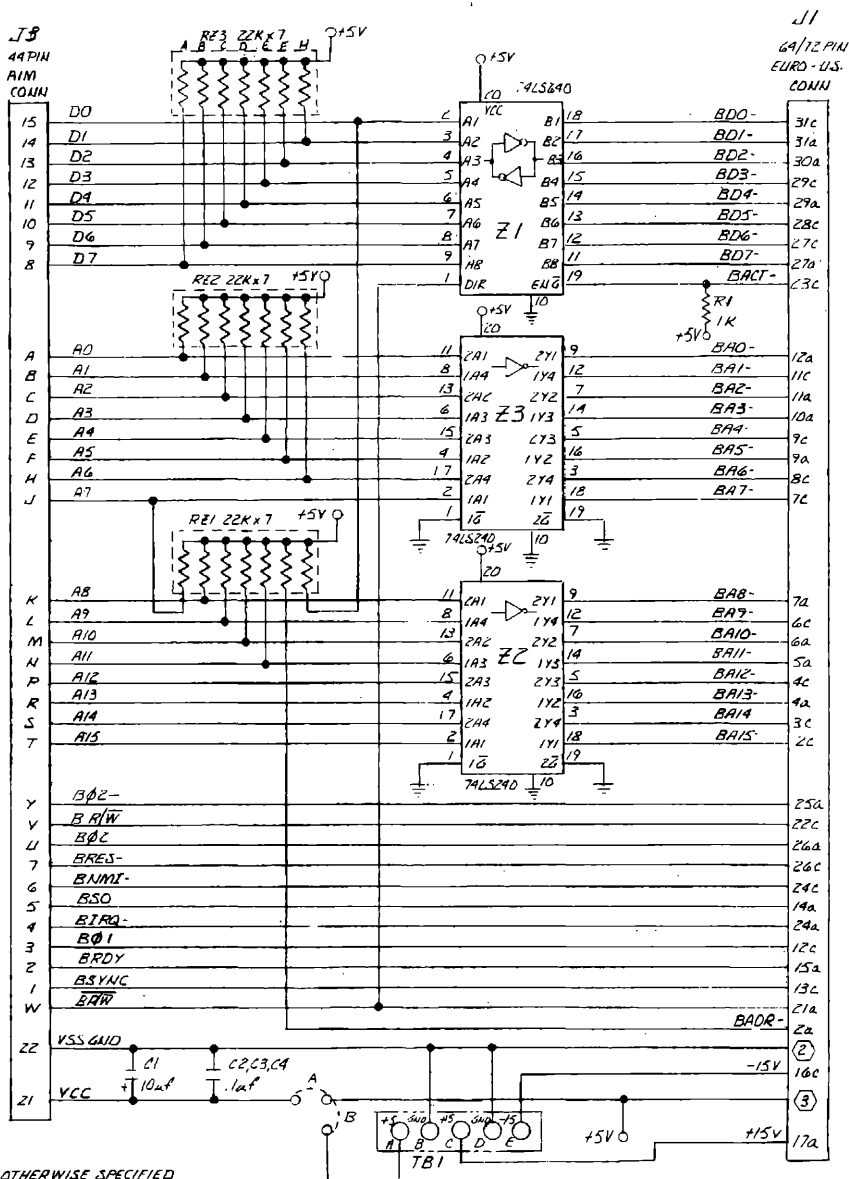
RM 65 Bus Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Pin	Signal Mnemonic	Signal Name	I/O	Pin	Signal Mnemonic	Signal Name	I/O
1a	GND	Ground		1c	+5V	+5 Vdc	
2a	BADR/	Buffered Bank Address	O	2c	BA15/	Buffered Address Bit 15	O
3a	GND	Ground		3c	BA14/	Buffered Address Bit 14	O
4a	BA13/	Buffered Address Bit 13	O	4c	BA12/	Buffered Address Bit 12	O
5a	BA11/	Buffered Address Bit 11	O	5c	GND	Ground	
6a	BA10/	Buffered Address Bit 10	O	6c	BA9/	Buffered Address Bit 9	O
7a	BA8/	Buffered Address Bit 8	O	7c	BA7/	Buffered Address Bit 7	O
8a	GND	Ground		8c	BA6/	Buffered Address Bit 6	O
9a	BA5/	Buffered Address Bit 5	O	9c	BA4/	Buffered Address Bit 4	O
10a	BA3/	Buffered Address Bit 3	O	10c	GND	Ground	
11a	BA2/	Buffered Address Bit 2	O	11c	BA1/	Buffered Address Bit 1	O
12a	BA0/	Buffered Address Bit 0	O	12c	Bφ1	Buffered Phase 1 Clock	O
13a	GND	Ground		13c	BSYNC	Buffered Sync	O
14a	BSO	Buffered Set Overflow	I	14c	BDRQ1/	*Buffered DMA Request 1	
15a	BRDY	Buffered Ready	I	15c	GND	Ground	
16a		*User Spare 1		16c	-12V/-V	-12 Vdc/-V	
17a	+12V/+V	+12 Vdc/+V		17c		*User Spare 2	
18a	GND	Ground Line		18c	BFLT/	*Buffered Bus Float	I
19a	BDMT/	*Buffered DMA Terminate		19c	Bφ0	*Buffered External Phase 0 Clock	
20a		*User Spare 3		20c	GND	Ground	
21a	BR/W	Buffered Read/Write "Not"	O	21c	BDRQ2/	*Buffered DMA Request 2	
22a		*System Spare		22c	BR/W	Buffered Read/Write	O
23a	GND	Ground		23c	BACT/	Buffered Bus Active	I
24a	BIRQ/	Buffered Interrupt Request	I	24c	BNMI/	Buffered Non-Maskable Interrupt	I
25a	Bφ2/	Buffered Phase 2 "Not" Clock	O	25c	GND	Ground	
26a	Bφ2	Buffered Phase 2 Clock	O	26c	BRES/	Buffered Reset	O
27a	BD7/	Buffered Data Bit 7	I/O	27c	BD6/	Buffered Data Bit 6	I/O
28a	GND	Ground		28c	BD5/	Buffered Data Bit 5	I/O
29a	BD4/	Buffered Data Bit 4	I/O	29c	BD3/	Buffered Data Bit 3	I/O
30a	BD2/	Buffered Data Bit 2	I/O	30c	GND	Ground	
31a	BD1/	Buffered Data Bit 1	I/O	31c	BD0/	Buffered Data Bit 0	I/O
32a	+5V	+5 Vdc		32c	GND	Ground	

Note:

*Not used on this module.

SINGLE CARD ADAPTER SCHEMATIC



NOTE: UNLESS OTHERWISE SPECIFIED

1. REF ASSY DWG PA10-DD10

2. PINS 1a, 3a, 5c, 8a, 10c, 13a, 15c, 18a, 20c, 23a, 25c, 28a, 30c, 32c SHALL BE CONNECTED TO GROUND.

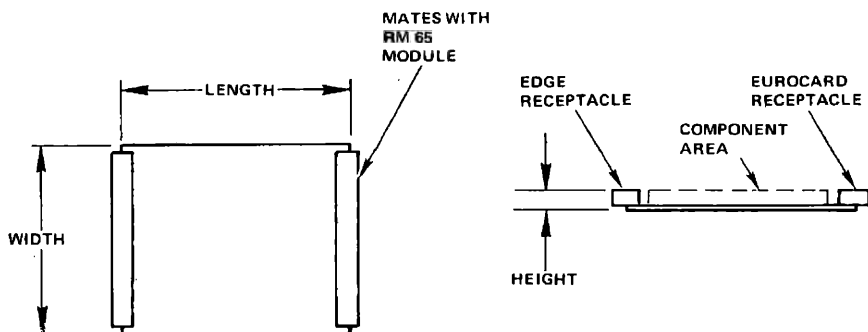
3. PINS 1c, 32a ON EURO CONNECTOR AND PINS XA, XI, YA, Yc, 1c, 32a ON U.S. CONNECTOR SHALL BE TIED TO +5V.

AIM 65 Expansion Connector Pin Assignments

Top (Component Side)				Bottom (Solder Side)			
Pin	Signal Mnemonic	Signal Name	Input/Output	Pin	Signal Mnemonic	Signal Name	Input/Output
1	SYNC	Sync	I	A	A0	Address Bit 0	I
2	RDY	Ready	O	B	A1	Address Bit 1	I
3	$\phi 1$	Phase 1 Clock	I	C	A2	Address Bit 2	I
4	\overline{IRQ}	Interrupt Request	O	D	A3	Address Bit 3	I
5	S.O.	Set Overflow	O	E	A4	Address Bit 4	I
6	NMI	Non-Maskable Interrupt	O	F	A5	Address Bit 5	I
7	RES	Reset	I	H	A6	Address Bit 6	I
8	D7	Data Bit 7	I/O	J	A7	Address Bit 7	I
9	D6	Data Bit 6	I/O	K	A8	Address Bit 8	I
10	D5	Data Bit 5	I/O	L	A9	Address Bit 9	I
11	D4	Data Bit 4	I/O	M	A10	Address Bit 10	I
12	D3	Data Bit 3	I/O	N	A11	Address Bit 11	I
13	D2	Data Bit 2	I/O	P	A12	Address Bit 12	I
14	D1	Data Bit 1	I/O	R	A13	Address Bit 13	I
15	D0	Data Bit 0	I/O	S	A14	Address Bit 14	I
16	-12V	*-12 Vdc		T	A15	Address Bit 15	I
17	+12V	*+12 Vdc		U	SYS $\phi 2$	System Phase 2 Clock	I
18	CS8	*Chip Select 8		V	SYS R/W	System Read/Write	I
19	CS9	*Chip Select 9		W	R/W	Read/Write "Not"	I
20	CSA	Chip Select A		X	*TEST	Test	I
21	+5V	+5 Vdc	I	Y	$\phi 2$	Phase 2 Clock "Not"	I
22	GND	Ground		Z	*RAM R/W	RAM Read/Write	I

Note:

*Not used on this module.



Module Dimensions

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3) Width Length Height	4.4 in. (111 mm) 3.7 in. (93 mm) 0.56 in. (14 mm)
Weight	3.0 oz. (90 g)
Environment Operating Temperature Storage Temperature Relative Humidity	0°C to 70°C -40°C to +85°C 0% to 85% (without condensation)
Power	+5V \pm 5% 110 mA (0.55W)—Typical 200 mA (1.00W)—Maximum
Interface AIM 65 Expansion Connector RM 65 Bus	22/44—edge receptacle (0.156 in. centers) 64-pin receptacle (0.100 centers) per DIN 41612 (Row b is not installed)
Notes: 1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.). 2. Length does not include extensions beyond the edge of the module due to connectors. 3. Dimensions conform to DIN 41612.	



RM65-7102E

RM 65 IEEE-488 BUS INTERFACE MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-7102E IEEE-48 Bus Interface Module is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 modules use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

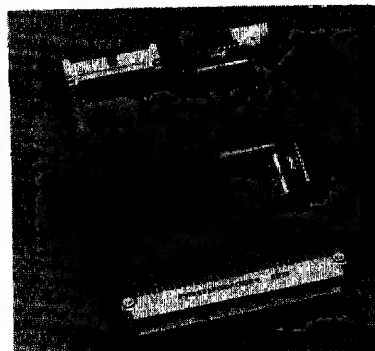
The RM 65 IEEE-488 Bus Interface Module connects an AIM 65, AIM 65/40 or RM 65 SBC based system to the IEEE-488 General Purpose Interface Bus (GPIB). Complete controller, talker and listener functions, as defined in the IEEE-488, 1978 Standard, are implemented. The module also supports extended addressing and multiple bus controllers. On-board ROM firmware implements all 12 functions specified by the interface standard. Features not defined in the standard, but also supported, include manual talk or listen disable, dual primary addressing, and an external trigger line. Switches select the Device Talk/Listen Address, Enable Dual Primary Addressing Mode, Disable Talk, Disable Listen, and System Controller mode. The bus interface transceivers meet the electrical specifications of the IEEE-488 interface standard. An 8-inch ribbon cable mates the IEEE-488 module to the IEEE-488 bus with a standard 24-pin connector.

ORDERING INFORMATION

Part No.	Description
RM65-7102E	IEEE-488 Bus Interface Module
Order No.	Description
815	IEEE-488 Bus Interface Module User's Manual (included with RM65-7102E)

FEATURES

- Compact size—about 4" × 6½" (100 mm × 160 mm)
- Pin and socket bus connection
- RM 65 Bus compatible
- Buffered address, data and control lines
- Listen, talk, and controller functions
- IEEE-488, 1978 standard fully implemented
- Uses TI 9914 GPIB Adapter device
- On-board ROM contains bus protocol and utility firmware
- Switches for
 - Device Talk/Listen Address
 - Disable Talk
 - Disable Listen
 - Enable Dual Primary Addressing mode
 - System Controller
 - Base Address to page boundary for I/O
 - Bank Selection to one or both 65K banks
- Jumper for ROM enable/disable
- LEDs show current address register contents
- Supports DMA data transfers
- +5V operation
- Fully assembled, tested and warranted



RM65-7102E IEEE-488 Bus Interface Module

FUNCTIONAL DESCRIPTION

The Data Transceivers invert and transfer 8-bits of parallel data between the IEEE-488 Bus Interface Module and the RM 65 bus, based on data direction signals from the Base Address Decoder.

The Address Buffers invert and transfer the 16-bit parallel address lines from the RM 65 bus to the Base Address Decoders, to the R2332 ROM and to the GPIB Adapter.

The Control Buffers invert and transfer phase 2 clock, reset, and read/write control signals from the RM 65 bus onto the module. The interrupt request is buffered and driven onto the RM 65 bus.

The Bank Select Control circuit detects when the module's assigned memory bank is addressed by comparing the bank address signal from the RM 65 bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch allows the board to reside in common memory (both Bank 0 and Bank 1) or only in the Bank set by the Bank Select switch (either Bank 0 or Bank 1).

The DMA Control circuit allows DMA requests from the TI 9914 GPIB Adapter device to be driven on the RM 65 bus or disabled under program control. This line is jumper selectable for either of two DMA request lines on the RM 65 bus.

The Base Address Decoder compares the eight most significant address lines to the eight Base Address switches. The ROM Disable Jumper allows the module to be active in a 4K block when enabled or active in a page (256 locations) when disabled. When an address for the selected bank matches the four most significant switches and the ROM is enabled, the Data Transceivers are enabled and the bus active signal is generated. When this address also matches the four least significant switches the GPIB Adapter and I/O are selected. When there is no match on the four least significant switches, the ROM is selected. When the GPIB Adapter and I/O are selected, the four least significant address lines, phase 2 clocks, and read/write control lines are used to derive register selects for the GPIB Adapter, device selects for the GPIB Status Latch, GPIB Sense Buffers, System Controller Select, and DMA Control Circuits. The read/write control lines also determine the direction for the Data Transceivers.

The TMS 9914 GPIB Adapter device provides hardware control of the IEEE-488 bus interface, using firmware subroutines provided in ROM. All bus interface lines are buffered by the GPIB Data and Control Transceivers, to conform to the electrical specifications of the IEEE-488 Standard. These lines are brought out through a cable to a standard IEEE-488 connector. An additional connector provides an external trigger output not defined by the IEEE-488 Standard.

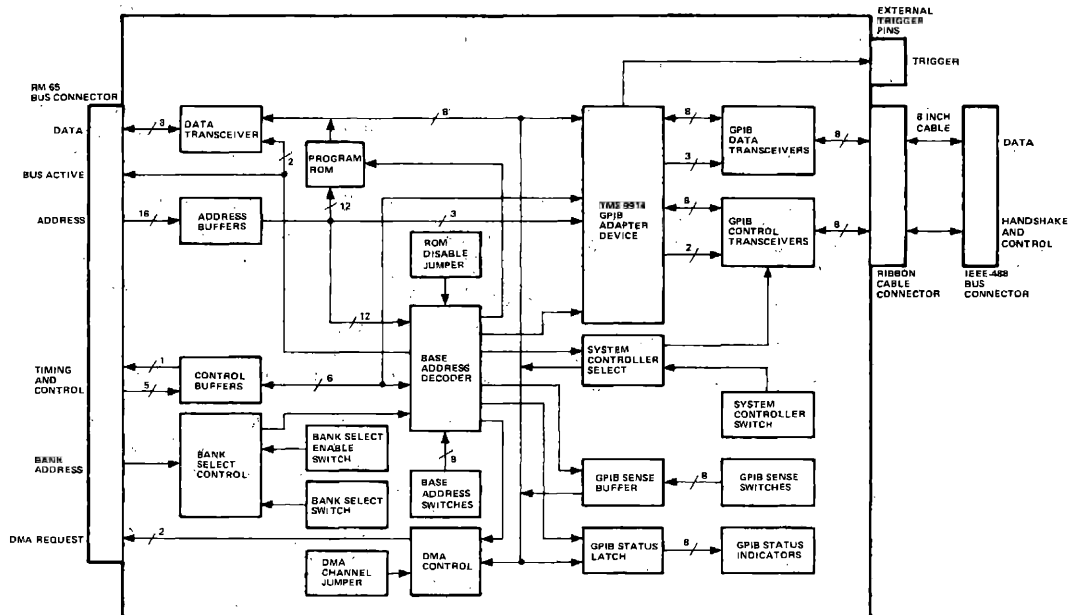
The System Controller Select circuit allows manual selection of System Controller capabilities in multiple controller configurations.

The GPIB Sense Buffer allows the GPIB Sense Switches to be read for Device Talk/Listen Address, Talk or Listen Disable, and Dual Primary Address Mode selection. The GPIB Status Latch latches the positions of the GPIB Sense Switches and displays them on the GPIB Status Indicators. This allows a visual verification of the Device Talk/Listen Address and Operating modes.

ON-BOARD PROGRAM ROM FIRMWARE

The Program ROM firmware completely supports all 12 Bus functions described in the IEEE-488, 1978 Standard, as well as features of the TMS 9914 GPIB Adapter device not defined in the Standard. These utility functions make both the Bus protocol and the GPIB Adapter device transparent to the programmer. The firmware, organized as subroutines, is linked to the user program through a jump table. Many of these routines are interrupt-driven, to minimize the processor time in servicing the module. User-alterable vectors and parameters are located in RAM, to allow custom applications. Output data or commands for the Bus are handled as tables, easing the set-up and transfer of information. Extensive error checking by the utility subroutines allow resident or user-provided error handling routines to ensure proper operation of the module, the IEEE-488 Bus and status of data transfer. Two self-test routines verify proper module operation.

The firmware is compatible with the input/output functions in the AIM 65 Debug Monitor and the AIM 65/40 I/O ROM.



IEEE-488 Bus Interface Module Block Diagram

IEEE-488 Bus Interface Connector Pin Assignments

Pin	Signal Mnemonic	Signal Name	Input/Output	Pin	Signal Mnemonic	Signal Name	Input/Output
1	DI01	Data Input/Output 1	I/O	13	DI05	Data Input/Output 5	I/O
2	DI02	Data Input/Output 2	I/O	14	DI06	Data Input/Output 6	I/O
3	DI03	Data Input/Output 3	I/O	15	DI07	Data Input/Output 7	I/O
4	DI04	Data Input/Output 4	I/O	16	DI08	Data Input/Output 8	I/O
5	EOI	End or Identify	I/O	17	REN	Remote Enable	I/O
6	DAV	Data Available	I/O	18	GND	Ground	N/A
7	NRFD	Not Ready for Data	I/O	19	GND	Ground	N/A
8	NDAC	Not Data Accepted	I/O	20	GND	Ground	N/A
9	IFC	Interface Clear	I/O	21	GND	Ground	N/A
10	SRQ	Service Request	I/O	22	GND	Ground	N/A
11	ATN	Attention	I/O	23	GND	Ground	N/A
12	SHIELD	Ground	N/A	24	GND	Logic Ground	N/A

External Trigger Pin Assignments

Pin	Signal Mnemonic	Signal Name	Input/Output
1	TRIG	Trigger Out	O
2	GND	Ground	

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	B ϕ 1	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	Buffered DMA Request 1
15a	BRDY	*Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	-12V/-V	*-12 Vdc/-V
17a	+12V/+V	*+12 Vdc/+V	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	B ϕ 0	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR \overline{W} /	Buffered Read/Write "Not"	21c	BDRQ2/	Buffered DMA Request 2
22a		*System Spare	22c	BR \overline{W}	Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request	24c	BNMI/	*Buffered Non-Maskable Interrupt
25a	B ϕ 2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	B ϕ 2	Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note:

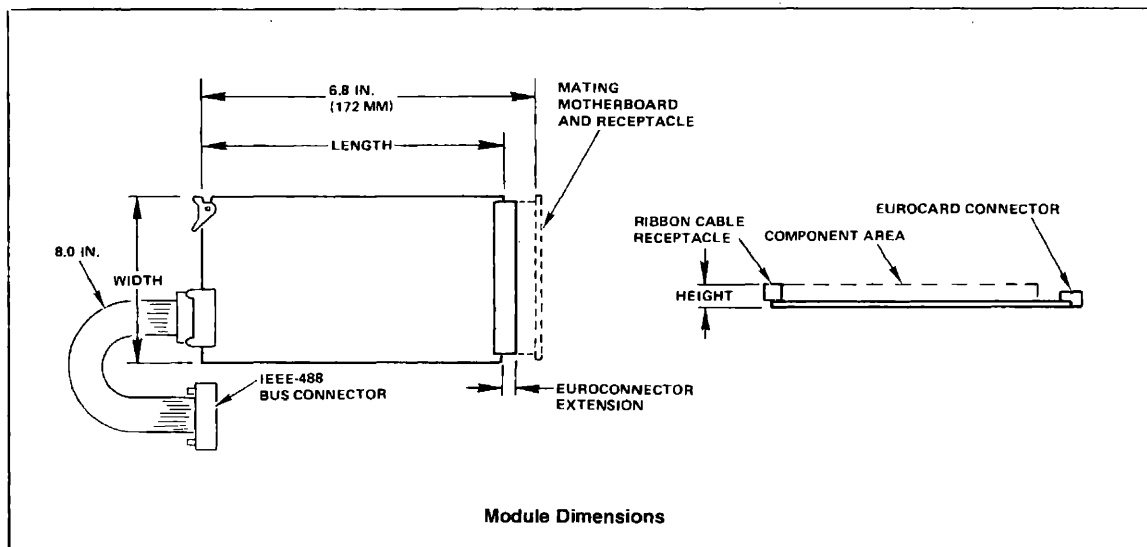
*Not used on this module.

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3)	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	5.0 oz. (140 g)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	+5 Vdc $\pm 5\%$ @ 0.65A (3.25W)—Typical 1.0A (5.25W)—Maximum
Interface	
RM 65 Bus Interface	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)
Module	
I/O Interface	
Cable Receptacle	26-pin mass terminated (0.100 in. centers)
Trigger Connector	Two vertical wire wrap pins (0.3 in. high on 0.200 in. centers)
IEEE-488 Bus Interface Cable	
IEEE-488 Bus Connector	24-pin mass terminated (2.16 mm centers) with metric thread lock screws (Amphenol 57 or equivalent)
Module Connector	26-pin mass terminated (0.100 in. centers)
Cable Length	8 inches
Type	Flat ribbon
Number of Conductors	24
Wire Size	#28 AWG

Notes:

1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. Length does not include the added extension due to the module ejector.
3. Dimensions conform to DIN 41612.





RM65-7104E

RM 65 ADAPTER/BUFFER FOR AIM 65

RM 65 MICROCOMPUTER MODULES

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 Module products use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

ORDERING INFORMATION

Part No.	Description
RM65-7104E	Adapter Buffer for AIM 65

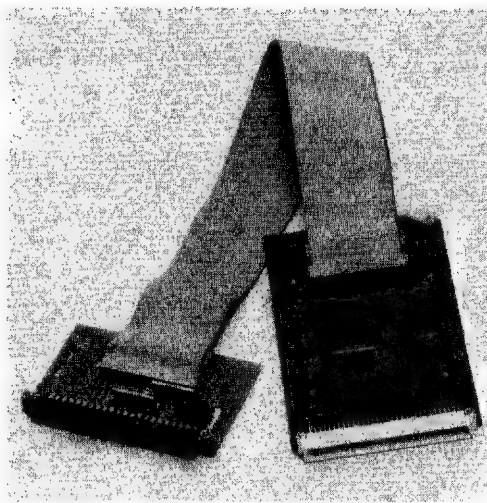
FEATURES

- RM 65 Bus Compatible
- Buffered address data and control lines
- Drives up to 15 modules
- Fully assembled, tested and warranted

PRODUCT OVERVIEW

The RM65-7104E Adapter/Buffer extends the AIM 65 Expansion Bus from the AIM 65 Expansion Connector to an RM 65 Bus motherboard that is situated up to 16 inches away. Included circuitry permits the Adapter/Buffer to drive up to 15 RM 65 Bus-compatible modules. (The similar Cable Driver Adapter/Buffer, Part Number RM65-7116, provides the same drive capability for applications in which the motherboard is up to six feet from the Expansion Connector.)

The Adapter/Buffer consists of an adapter module, a buffer module and two 16-inch interconnect cables. Both cables are flexible, so the motherboard may be installed in a wide variety of locations and orientations relative to the AIM 65.



RM65-7104E Adapter/Buffer for AIM 65

FUNCTIONAL DESCRIPTION

The Adapter/Buffer consists of two modules and two interconnect cables. The Adapter module connects to the AIM 65 Expansion connector and the Buffer module connects to an RM 65 Bus motherboard receptacle.

The Adapter module transfers data, address and control lines from AIM 65 Expansion Connector to the interconnect cables. The eight data and 16 address lines are routed directly, without buffering. The read/write, clock, sync and reset AIM 65 output control lines are also routed directly through the Adapter. The ready, set overflow, interrupt request and non-maskable interrupt AIM 65 input lines are buffered on the module.

Two 16-inch 40 conductor flat ribbon cables connect the Adapter module to the Buffer module. The cables are mass terminated at each end, and are permanently attached to the interfacing module.

The Buffer module buffers and routes all interface signals between the interconnect cables and the RM 65 Bus connector.

The Data Transceivers invert and drive 8-bits of parallel data. During a write operation, data received from the cables are driven onto the RM 65 Bus. During a read operation, data received from the RM 65 Bus are driven onto the cables. The bus active signal enables the Transceivers. When the bus float signal is active, the Transceivers are disabled.

The Address Buffers invert and transfer 16 parallel address lines from the interconnect cable to the RM 65 Bus. When the bus float signal is active, the Buffers are disabled.

Jumper E1 selects the source for the bank address line (BADR)—either the buffer module or an external module. When the buffer module is the source (position A), the bank address line is held high to address Bank 0 (Lower 65K) on the Bus; this line is disabled when the bus float line is active. For an external source (position B), the bank address line is not used by the buffer module, and must be controlled by another module on the Bus.

The seven read/write, clock, sync and reset lines from the cables to the bus are buffered by the Control Drivers. All of these lines, except reset and phase 1, are disabled when the bus float line is active. The ready, set overflow, interrupt request and non-maskable lines from the bus to the interconnect cables are also buffered by the Control Drivers.

Jumper E2 selects the source for the DMA Terminate line (BDMT)—either the buffer module or an external module. When the buffer module is the source (position A), the DMA terminate line is held high (inactive). For an external source (position B), the DMA terminate line is not used by the buffer module, and must be controlled by another module on the bus.

INSTALLATION/REMOVAL

Installing the Adapter/Buffer

Before installing the module, inspect for damage and grease, dirt, liquid or other foreign material that will affect performance.

- Before installing the Adapter/Buffer, turn off power to the AIM 65 and the interfacing RM 65 Bus motherboard.
- Configure Jumpers E1 and E2, per the Functional Description.
- Align the Adapter module connector J3 pin 1 with the AIM 65 Expansion Connector J3 pin 1.
- Plug the Adapter module onto the Expansion Connector. Press in firmly on the end of module until all pins are securely seated.
- Install connector P1 of the Buffer module into the desired slot on the mating RM 65 Bus motherboard.

CAUTION

RM 65 Bus connectors are keyed to prevent improper module connection. If the module does not insert into the receptacle with moderate pressure applied, check the orientation and connector alignment of the module. Forcing the module improperly into the receptacle may damage the receptacle and/or the module.

- Apply power to the AIM 65 and to the mating RM 65 Bus motherboard.

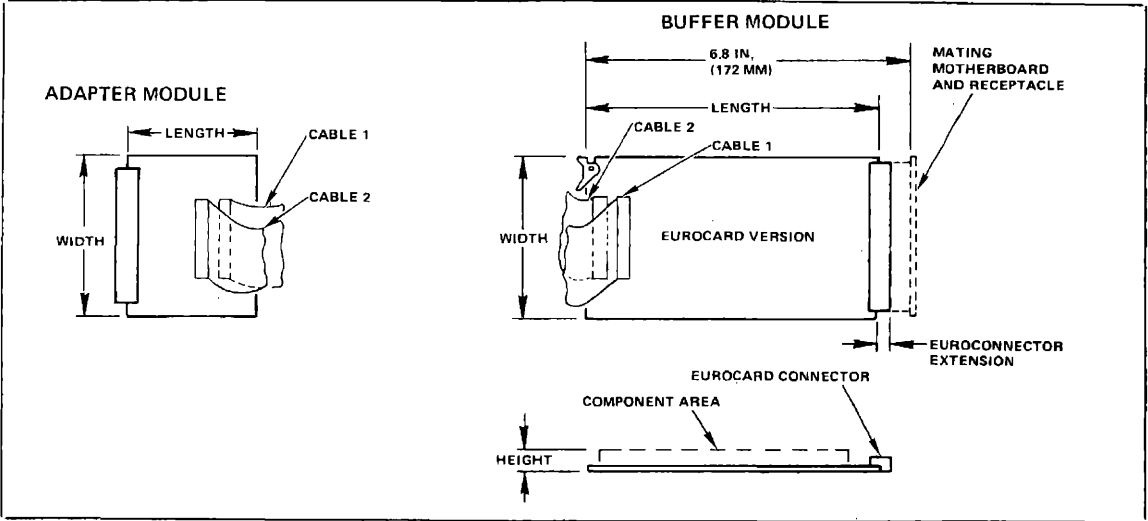
Removing the Adapter/Buffer

- Turn off power to the AIM 65 and to the RM 65 Bus motherboard.
- Lift up on the Buffer module ejector tab to release the module from the mating RM 65 Bus receptacle. Pull the module straight back until it is free from the card slot guides.
- Pull back on the Adapter module while moving it slightly from side to side until it is free from the AIM 65 Expansion Connector.

Buffer Module to RM 65 Bus Connector Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Signal Mnemonic	Signal Name	Input/ Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/ Output
GND	Ground		1a	1c	+5V	+5 Vdc	
BADR/	Buffered Bank Address	O	2a	2c	BA15/	Buffered Address Bit 15	O
GND	Ground		3a	3c	BA14/	Buffered Address Bit 14	O
BA13/	Buffered Address Bit 13	O	4a	4c	BA12/	Buffered Address Bit 12	O
BA11/	Buffered Address Bit 11	O	5a	5c	GND	Ground	
BA10/	Buffered Address Bit 10	O	6a	6c	BA9/	Buffered Address Bit 9	O
BA8/	Buffered Address Bit 8	O	7a	7c	BA7/	Buffered Address Bit 7	O
GND	Ground		8a	8c	BA6/	Buffered Address Bit 6	O
BA5/	Buffered Address Bit 5	O	9a	9c	BA4/	Buffered Address Bit 4	O
BA3/	Buffered Address Bit 3	O	10a	10c	GND	Ground	
BA2/	Buffered Address Bit 2	O	11a	11c	BA1/	Buffered Address Bit 1	O
BA0/	Buffered Address Bit 0	O	12a	12c	Bφ1	Buffered Phase 1 Clock	O
GND	Ground		13a	13c	BSYNC	Buffered Sync	O
BSO	Buffered Set Overflow	I	14a	14c	BDRQ1/	*Buffered DMA Request 1	
BRDY	Buffered Ready	I	15a	15c	GND	Ground	
	*User Spare 1		16a	16c	-12V/ -V	*-12 Vdc/ -V	
+12V/+V	*+12 Vdc/+V		17a	17c		*User Spare 2	
GND	Ground Line		18a	18c	BFLT/	Buffered Bus Float	I
BDMT/	Buffered DMA Terminate		19a	19c	Bφ0	*Buffered External Phase 0 Clock	
	*User Spare 3		20a	20c	GND	Ground	
BR/W/	Buffered Read/Write "Not"	O	21a	21c	BDRQ2/	*Buffered DMA Request 2	
	*System Spare		22a	22c	BR/W	Buffered Read/Write	O
GND	Ground		23a	23c	BACT/	Buffered Bus Active	I
BIRQ/	Buffered Interrupt Request	I	24a	24c	BNMI/	Buffered Non-Maskable Interrupt	I
Bφ2/	Buffered Phase 2 "Not" Clock	O	25a	25c	GND	Ground	
Bφ2	Buffered Phase 2 Clock	O	26a	26c	BRES/	Buffered Reset	O
BD7/	Buffered Data Bit 7	I/O	27a	27c	BD6/	Buffered Data Bit 6	I/O
GND	Ground		28a	28c	BD5/	Buffered Data Bit 5	I/O
BD4/	Buffered Data Bit 4	I/O	29a	29c	BD3/	Buffered Data Bit 3	I/O
BD2/	Buffered Data Bit 2	I/O	30a	30c	GND	Ground	
BD1/	Buffered Data Bit 1	I/O	31a	31c	BD0/	Buffered Data Bit 0	I/O
+5V	+5 Vdc		32a	32c	GND	Ground	

Note
*Not used on this module.

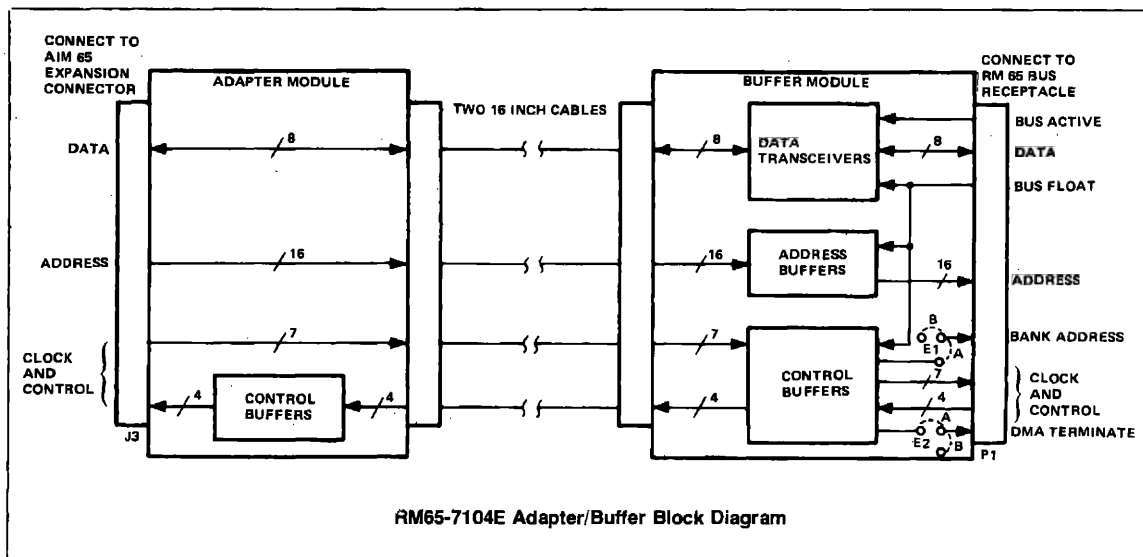


Adapter Module to AIM 65 Expansion Connector Pin Assignments

Top (Component Side)				Bottom (Solder Side)			
Signal Mnemonic	Signal Name	Input/Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/Output
SYNC	SYNC	I	1	A	A0	Address Bit 0	I
RDY	Ready	O	2	B	A1	Address Bit 1	I
$\phi 1$	Phase 1 Clock	I	3	C	A2	Address Bit 2	I
IRQ	Interrupt Request	O	4	D	A3	Address Bit 3	I
S.O.	Set Overflow	O	5	E	A4	Address Bit 4	I
NMI	Non-Maskable Interrupt	O	6	F	A5	Address Bit 5	I
RES	Reset	O	7	H	A6	Address Bit 6	I
D7	Data Bit 7	I/O	8	J	A7	Address Bit 7	I
D6	Data Bit 6	I/O	9	K	A8	Address Bit 8	I
D5	Data Bit 5	I/O	10	L	A9	Address Bit 9	I
D4	Data Bit 4	I/O	11	M	A10	Address Bit 10	I
D3	Data Bit 3	I/O	12	N	A11	Address Bit 11	I
D2	Data Bit 2	I/O	13	P	A12	Address Bit 12	I
D1	Data Bit 1	I/O	14	R	A13	Address Bit 13	I
D0	Data Bit 0	I/O	15	S	A14	Address Bit 14	I
-12V	*-12 Vdc		16	T	A15	Address Bit 15	I
+12V	*+12 Vdc		17	U	SYS $\phi 2$	System Phase 2 Clock	I
CS8	*Chip Select 8		18	V	SYS R/W	System Read/Write	I
CS9	*Chip Select 9		19	W	R/W	Read/Write "Not"	I
CSA	*Chip Select A		20	X	TEST	*Test	I
+5V	+5 Vdc		21	Y	$\phi 2$	Phase 2 Clock "Not"	I
GND	Ground		22	Z	RAM R/W	*RAM Read/Write	I

Note

* = Not used on this module.



RM65-7104E Adapter/Buffer Block Diagram

SPECIFICATIONS

Parameter	Value
Dimension (See Notes)	
Adapter Module	
Width	4.4 in. (111 mm)
Length	2.6 in. (67 mm)
Height	0.56 in. (14 mm)
Buffer Module	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	7.2 oz. (205 g)
Power	
Adapter Module	+5V \pm 5% 30 mA (0.15W)—Typical 50 mA (0.25W)—Maximum
Buffer Module	+5V \pm 5% 190 mA (0.95W)—Typical 330 mA (1.7W)—Maximum
Environmental	
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to 85°C
Relative Humidity	0% to 85% (without condensation)
Propagation Time	20 ns—Maximum
Interface Connectors	
AIM 65 Expansion Connector	22/44—edge receptacle (0.156 in. centers)
RM 65 Bus	64-pin plug (0.100 in. centers) per DIN 41612 (Row b is not installed)
Interface Cables	
Number of Cables	Two
Cable Length	16 inches
Type	Flat ribbon
Number of conductors per cable	40
Wire Size	#28 AWG

Notes:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.)
2. The length does not include extensions beyond the edge of the module due to the connectors or the module ejector.
3. The Adapter Module dimensions conform to DIN 41612.



RM65-7116E RM 65 CABLE DRIVER ADAPTER/BUFFER FOR AIM 65

RM 65 MICROCOMPUTER MODULES

The RM65-7116E Cable Driver Adapter/Buffer is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 module products use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

ORDERING INFORMATION

Part No.	Description
RM65-7116E	Cable Driver Adapter Buffer for AIM 65

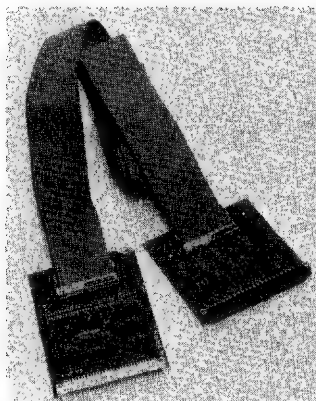
FEATURES

- RM 65 Bus compatible
- Buffered address data and control lines
- Drives up to 15 modules
- Long cable for distances of up to 6 feet
- Fully assembled, tested and warranted

PRODUCT OVERVIEW

The RM65-7116E Cable Driver Adapter/Buffer extends the AIM 65 Expansion Bus from the AIM 65 Expansion Connector to an RM 65 Bus motherboard that is situated up to six feet away. Included circuitry permits the Cable Driver Adapter/Buffer to drive up to 15 RM 65 Bus-compatible modules. (The similar Adapter/Buffer, Part Number RM65-7104, provides the same drive capability for applications in which the motherboard need not be more than 16 inches from the Expansion Connector.)

The Cable Driver Adapter/Buffer consists of a cable driver adapter module, a buffer module and two 6-foot interconnect cables. Both cables are flexible, so the motherboard may be installed in a wide variety of locations and orientations relative to the AIM 65.



RM65-7116E Cable Driver Adapter/Buffer for AIM 65

FUNCTIONAL DESCRIPTION

The Cable Driver Adapter/Buffer consists of two modules and two interconnect cables. The Adapter Module connects to the AIM 65 Expansion connector and the Buffer module connects to an RM 65 Bus motherboard receptacle.

The Cable Driver Adapter module buffers data, address and control lines between the AIM 65 Expansion Connector and the interconnect cables.

The Data Transceivers drive 8-bits of parallel data. During a write operation, data received from the AIM 65 are driven onto the cables. During a read operation, data received from the cables are driven into the AIM 65. The bus active signal enables the Data Transceivers.

The Address Buffers drive 16-bits of parallel data from the AIM 65 onto the cables.

The Control Buffers transfer the timing and control signals between the AIM 65 and the cables. The seven read/write, clock, sync, and reset lines are driven from the AIM 65 onto the cables. The four ready, set overflow, interrupt request and non-maskable interrupt lines are driven from the cables onto the AIM 65.

Two 6-foot 40 conductor flat ribbon cables connect the Cable Driver Adapter module to the Buffer module. The cables are mass terminated at each end, and are permanently attached to the interfacing module.

The Buffer module buffers and routes all interface signals between the interconnect cables and the RM 65 Bus connector.

The Data Transceivers invert and drive 8-bits of parallel data. During a write operation, data received from the cables are driven onto the RM 65 Bus. During a read operation, data received from the RM 65 Bus are driven onto the cables. The bus active signal enables the Transceivers. When the bus float signal is active, the Transceivers are disabled.

The Address Buffers invert and transfer 16 parallel address lines from the interconnect cable to the RM 65 Bus. When the bus float signal is active, the Buffers are disabled.

Jumper E1 selects the source for the bank address line (BADR)—either the buffer module or an external module. When the buffer module is the source (position A), the bank address line is held high to address Bank 0 (lower 65K) on the Bus; this line is disabled when the bus float line is active. For an external source (position B), the bank address line is not used by the buffer module, and must be controlled by another module on the Bus.

The seven read/write, clock, sync and reset lines from the cables to the bus are buffered by the Control Buffers. All of these lines, except reset and phase 1, are disabled when the

bus float line is active. The ready, set overflow, interrupt request and non-maskable lines from the bus to the interconnect cables are also buffered by the Control Buffers.

Jumper E2 selects the source for the DMA Terminate line (BDMT)—either the buffer module or an external module. When the buffer module is the source (position A), the DMA terminate line is held high (inactive). For an external source (position B), the DMA terminate line is not used by the buffer module, and must be controlled by another module on the bus.

INSTALLATION/REMOVAL

CABLE DRIVER ADAPTER/BUFFER INSTALLATION

CAUTION

RM 65 Bus connectors are keyed to prevent improper module connection. If the module does not insert into the receptacle with moderate pressure applied, check the orientation and connector alignment of the module. Forcing the module improperly into the receptacle may damage the receptacle and/or the module.

- Before installing the Cable Driver Adapter/Buffer, turn off power to the AIM 65 and the interfacing RM 65 Bus motherboard.
- Configure Jumpers E1 and E2, per the Functional Description.
- Align Cable Driver Adapter module connector J3 pin 1 with the AIM 65 Expansion Connector J3 pin 1.
- Plug the Cable Driver Adapter module onto the Expansion Connector. Press in firmly on the end of module until all pins are securely seated.
- Install connector P1 of the Buffer module into the desired slot on the mating RM 65 Bus motherboard.
- Apply power to the AIM 65 and to the mating RM 65 Bus motherboard.

CABLE DRIVER/ADAPTER/BUFFER REMOVAL

- Turn off power to the AIM 65 and to the RM 65 Bus motherboard.
- Lift up on the Buffer module ejector tab to release the module from the mating RM 65 Bus receptacle. Pull the module straight back until it is free from the card slot guides.
- Pull back on the Cable Driver module while moving it slightly from side to side until it is free from the AIM 65 Expansion Connector.

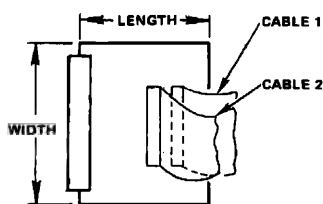
Buffer Module to RM 65 Bus Connector Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Pin	Signal Mnemonic	Signal Name	Input/Output	Pin	Signal Mnemonic	Signal Name	Input/Output
1a	GND	Ground		1c	+5V	+5 Vdc	
2a	BADR/	Buffered Bank Address	O	2c	BA15/	Buffered Address Bit 15	O
3a	GND	Ground		3c	BA14/	Buffered Address Bit 14	O
4a	BA13/	Buffered Address Bit 13	O	4c	BA12/	Buffered Address Bit 12	O
5a	BA11/	Buffered Address Bit 11	O	5c	GND	Ground	
6a	BA10/	Buffered Address Bit 10	O	6c	BA9/	Buffered Address Bit 9	O
7a	BA8/	Buffered Address Bit 8	O	7c	BA7/	Buffered Address Bit 7	O
8a	GND	Ground		8c	BA6/	Buffered Address Bit 6	O
9a	BA5/	Buffered Address Bit 5	O	9c	BA4/	Buffered Address Bit 4	O
10a	BA3/	Buffered Address Bit 3	O	10c	GND	Ground	
11a	BA2/	Buffered Address Bit 2	O	11c	BA1/	Buffered Address Bit 1	O
12a	BA0/	Buffered Address Bit 0	O	12c	Bφ1	Buffered Phase 1 Clock	O
13a	GND	Ground		13c	BSYNC	Buffered Sync	O
14a	BSO	Buffered Set Overflow	I	14c	BDRQ1/	*Buffered DMA Request 1	
15a	BRDY	Buffered Ready	I	15c	GND	Ground	
16a		*User Spare 1		16c	-12V/-V	*-12 Vdc/-V	
17a	+12V/+V	*+12 Vdc/+V		17c		*User Spare 2	
18a	GND	Ground Line		18c	BFLT/	Buffered Bus Float	I
19a	BDMT/	Buffered DMA Terminate		19c	Bφ0	*Buffered External Phase 0 Clock	
20a		*User Spare 3		20c	GND	Ground	
21a	BR/W/	Buffered Read/Write "Not"	O	21c	BDRQ2/	*Buffered DMA Request 2	
22a		*System Spare		22c	BR/W	Buffered Read/Write	O
23a	GND	Ground		23c	BACT/	Buffered Bus Active	I
24a	BIRQ/	Buffered Interrupt Request	I	24c	BNMI/	Buffered Non-Maskable Interrupt	I
25a	Bφ2/	Buffered Phase 2 "Not" Clock	O	25c	GND	Ground	
26a	Bφ2	Buffered Phase 2 Clock	O	26c	BRES/	Buffered Reset	O
27a	BD7/	Buffered Data Bit 7	I/O	27c	BD6/	Buffered Data Bit 6	I/O
28a	GND	Ground		28c	BD5/	Buffered Data Bit 5	I/O
29a	BD4/	Buffered Data Bit 4	I/O	29c	BD3/	Buffered Data Bit 3	I/O
30a	BD2/	Buffered Data Bit 2	I/O	30c	GND	Ground	
31a	BD1/	Buffered Data Bit 1	I/O	31c	BD0/	Buffered Data Bit 0	I/O
32a	+5V	+5 Vdc		32c	GND	Ground	

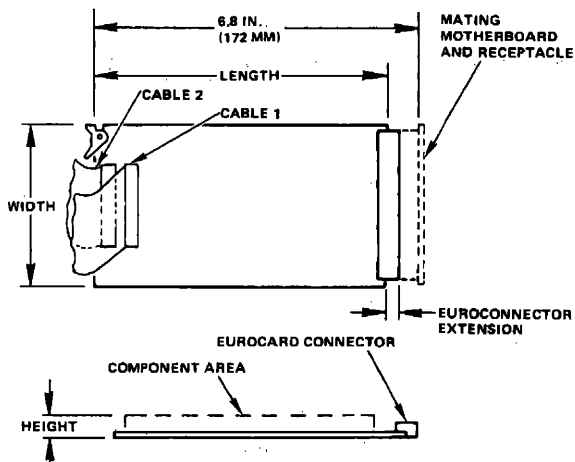
Note:

*Not used on this module.

CABLE DRIVER ADAPTER MODULE



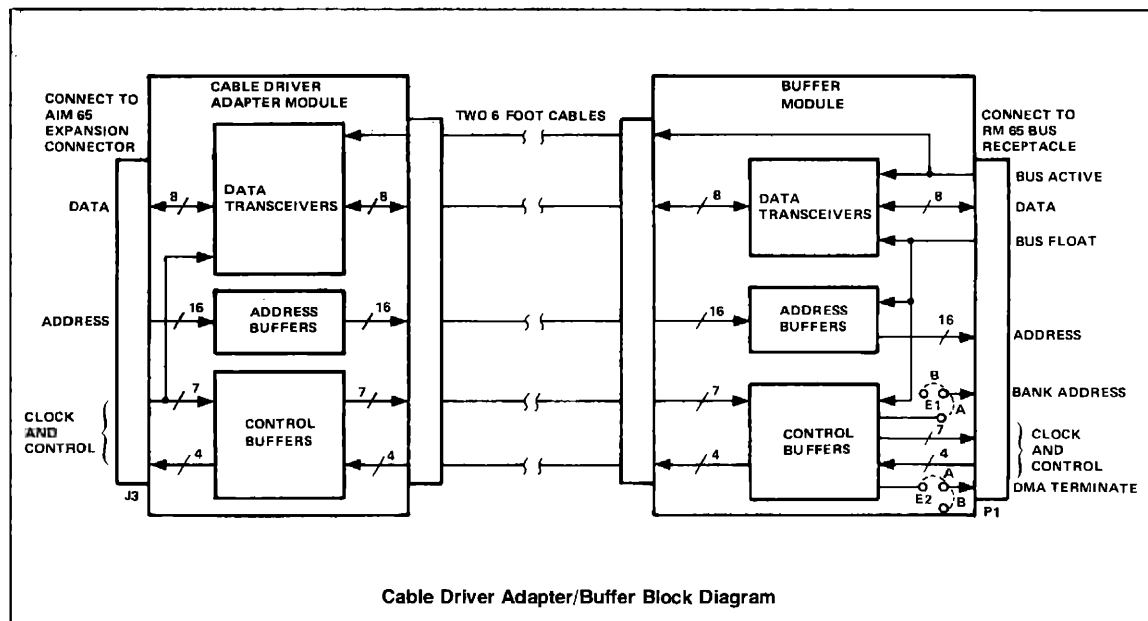
BUFFER MODULE DIMENSIONS



Cable Driver Adapter Module to AIM 65 Expansion Connector Pin Assignments

Top (Component Side)				Bottom (Solder Side)			
Pin	Signal Mnemonic	Signal Name	Input/Output	Pin	Signal Mnemonic	Signal Name	Input/Output
1	SYNC	SYNC	I	A	A0	Address Bit 0	I
2	RDY	Ready	O	B	A1	Address Bit 1	I
3	O1	Phase 1 Clock	I	C	A2	Address Bit 2	I
4	IRQ	Interrupt Request	O	D	A3	Address Bit 3	I
5	S.O.	Set Overflow	O	E	A4	Address Bit 4	I
6	NMI	Non-Maskable Interrupt	O	F	A5	Address Bit 5	I
7	RES	Reset	O	H	A6	Address Bit 6	I
8	D7	Data Bit 7	I/O	J	A7	Address Bit 7	I
9	D6	Data Bit 6	I/O	K	A8	Address Bit 8	I
10	D5	Data Bit 5	I/O	L	A9	Address Bit 9	I
11	D4	Data Bit 4	I/O	M	A10	Address Bit 10	I
12	D3	Data Bit 3	I/O	N	A11	Address Bit 11	I
13	D2	Data Bit 2	I/O	P	A12	Address Bit 12	I
14	D1	Data Bit 1	I/O	R	A13	Address Bit 13	I
15	D0	Data Bit 0	I/O	S	A14	Address Bit 14	I
16	-12V	*-12 Vdc		T	A15	Address Bit 15	I
17	+12V	*+12 Vdc		U	SYS 02	System Phase 2 Clock	I
18	CS8	*Chip Select 8		V	SYS R/W	System Read/Write	I
19	CS9	*Chip Select 9		W	R/W	Read/Write "Not"	I
20	CSA	*Chip Select A		X	TEST	*Test	I
21	+5V	+5 Vdc		Y	02	Phase 2 Clock "Not"	I
22	GND	Ground		Z	RAM R/W	*RAM Read/Write	I

Note:
* = Not used on this module.



Cable Driver Adapter/Buffer Block Diagram

[illegible]

- ① PINS 1C, 32A ON EURO CONNECTION AND PINS 1A, 1C, 14C, 1C, 32A ON U.S. CONNECTION SHALL BE TIED TO 15V
- ② PINS 1A, 3A, 5C, 8C, 10C, 14A, 15C, 18A, 20C, 23A, 25C, 28A, 30C, 32A, SHALL BE TIED TO GND.
- ③ ALL EVEN NUMBER PINS (2 THRU 40) SHALL BE TIED TO GND.

4. ALL CAPACITORS ARE .10UF \pm 20%, 50V.

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3)	
Cable Driver Adapter Module	
Width	4.4 in. (111 mm)
Length	5 in. (127 mm)
Height	0.56 in. (14 mm)
Buffer Module	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	1.0 lb (450 g)
Power	
Cable Driver Adapter Module	+5V \pm 5% 30 mA (0.15W)—Typical 275 mA (0.25W)—Maximum
Buffer Module	+5V \pm 5% 190 mA (0.95W)—Typical 330 mA (1.7W)—Maximum
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C
Relative Humidity	0% to 85% (without condensation)
Propagation Time	50 ns—Maximum
Interfaces	
Interface Connectors	
AIM 65 Expansion Connector	22/44—edge receptacle (0.156 in. centers)
RM 65 Bus	64-pin plug (0.100 in. centers) per DIN 41612 (Row b is not installed)
Interface Cables	
Number of Cables	Two
Cable Length	6 feet
Type	Flat ribbon
Number of conductors per cable	40
Wire Size	#28 AWG

Notes:

1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. Length does not include extensions beyond the edge of the module due to connectors or the module ejector.
3. Dimensions conform to DIN 41612.



RM65-7141E

RM 65 ADAPTER CABLE AND BUFFER MODULE FOR AIM 65/40

RM 65 MICROCOMPUTER MODULES

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 Module products use a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

ORDERING INFORMATION

Part No.	Description
RM65-7141E	Adapter Cable and Buffer Module for AIM 65/40

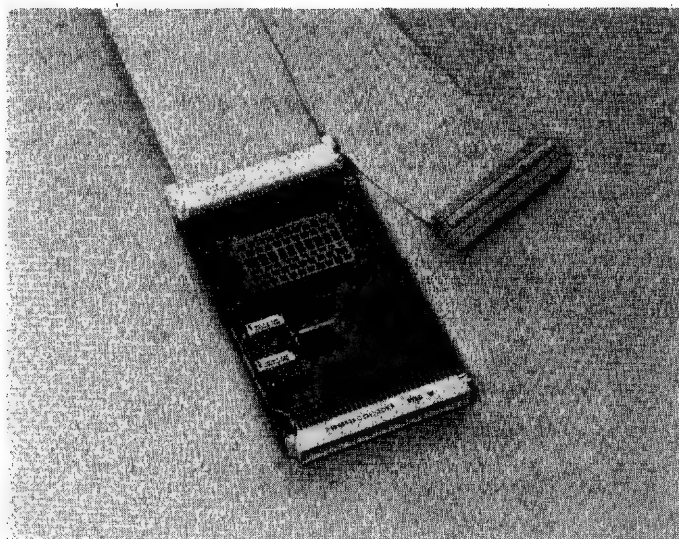
PRODUCT OVERVIEW

The RM65-7141E Adapter Cable and Buffer Module extends the AIM 65/40 Expansion Bus from the AIM 65/40 Expansion Connector to RM 65 Bus motherboard that is situated up to two meters (78 inches) away. On-board circuitry permits the buffer module to drive up to 15 RM 65 Bus-compatible modules.

The Adapter Cable and Buffer Module consists of a buffer module and a 2-meter interconnect cable. The cable is flexible, so the motherboard may be installed in a wide variety of locations and orientations relative to the AIM 65/40 SBC module.

FEATURES

- RM 65 Bus compatible
- Buffered address, data and control lines
- Drives up to 15 modules
- Long cable for distances up to 2 meters
- Edge connector and Eurocard versions
- Fully assembled, tested and warranted



RM65-7141E Adapter Cable and Buffer Module for AIM 65/40

FUNCTIONAL DESCRIPTION

The RM65-7141E Adapter Cable and Buffer Module consists of one module and one interconnect cable. The cable connects to the AIM 65/40 SBC module Expansion connector and the module connects to an RM 65 Bus motherboard receptacle.

The two meter 64-conductor flat ribbon cable connects the AIM 65/40 SBC module to the buffer module. The cable is mass terminated at each end. One end of the cable connects to the SBC module Expansion connector (Euro connector) and the other end connects to the buffer module.

The module buffers and routes all interface signals between the interconnect cable and the RM 65 Bus connector.

The Data Transceivers (Z6) invert and drive 8-bits of parallel data. During a write operation, data received from the cable are driven onto the RM 65 Bus. During a read operation, data received from the RM 65 Bus are driven onto the cable. The bus active signal (BACT/) enables the Transceivers. When the bus float signal (BFLT/) is active, the Transceivers are disabled.

The Address Buffers (Z1 and Z3) invert and transfer 16 parallel address lines from the interconnect cables to the RM 65 Bus. When the bus float signal (BFLT/) is active, the Buffers are disabled.

Jumper E1 selects the source for the bank address line (BADR/)—either the AIM 65/40 SBC module or another controlling module on the RM 65 Bus. When the AIM 65/40 SBC module is the source (position A), the bank address line (BADR/) is sourced by the AIM 65/40 SBC module; this line is disabled when the bus float line (BFLT/) is active. For an external source (position B), the bank address line is not used by the buffer module, and must be controlled by another module on the RM 65 Bus.

The read/write (BR/W and BR/W/), clock (B02, B02/ and B01), BSYNC and reset (BRES/) lines from the cable to the bus are buffered by the Control Buffers (Z5). All of these lines, except BRES/ and B01 are disabled when the bus float line (BFLT/) is active. The ready (BRDY), set overflow (BSO), interrupt request (BIRQ/) and non-maskable interrupt (BNMI/) lines from the bus to the interconnect cable are also buffered by the Control Buffers.

Jumper E2 selects the source for the DMA Terminate line (BDMT/)—either the buffer module or an external module. When

the AIM 65/40 SBC module is the source (position A), the DMA terminate line (BDMT/) from the AIM 65/40 SBC module is put on the RM 65 Bus. For an external source (position B), the DMA terminate line is not used by the buffer module, and must be controlled by another module on the bus.

INSTALLATION/REMOVAL

Installing the Adapter Cable and Buffer Module

Before installing the module, inspect for damage and grease, dirt, liquid or other foreign materials that will affect performance.

- Before installing the AIM 65/40 Adapter Cable and Buffer Module, turn off power to the AIM 65/40 SBC module and the interfacing RM 65 Bus motherboard.
- Configure Jumpers E1 and E2, per the Functional Description.
- Connect the cable Euro receptacle connector onto the AIM 65/40 SBC module Expansion connector (Euro connector).
- Connect the other cable connector onto buffer module connector P2.
- Install connector P1 of the buffer module into the desired slot on the mating RM 65 Bus motherboard.

CAUTION

RM 65 Bus connectors are keyed to prevent improper module connection. If the module does not insert into the receptacle with moderate pressure applied, check the orientation and connector alignment of the module. Forcing the module improperly into the receptacle may damage the receptacle and/or the module.

- Apply power to the AIM 65/40 SBC module and to the mating RM 65 Bus motherboard. (Power to the RM 65 motherboard is not supplied by the Adapter Cable and Buffer Module.)

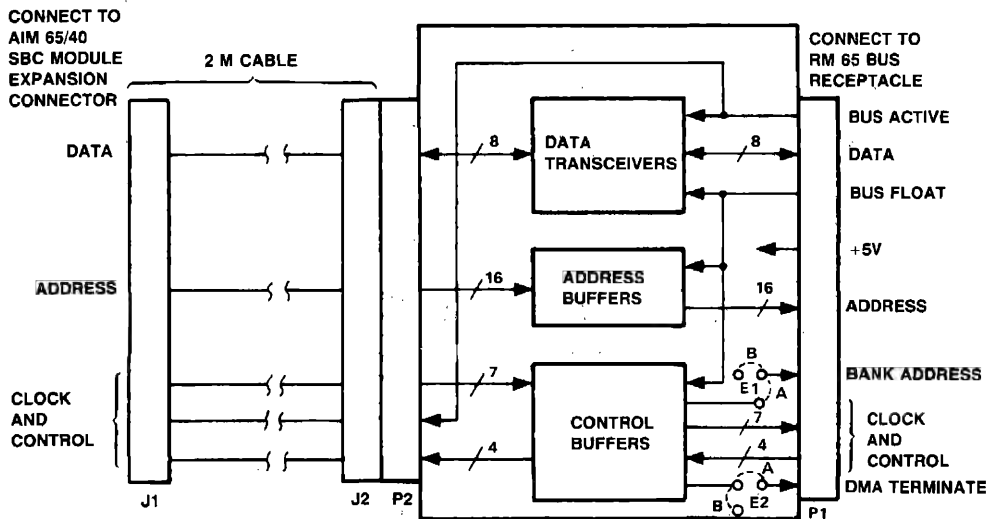
Removing the Adapter Cable and Buffer Module

- Turn off power to the AIM 65/40 SBC module and to the RM 65 Bus motherboard.
- Pull the buffer module straight back until it is free from the RM 65 Bus receptacle and card cage slot guides.
- Disconnect the cable connector from the AIM 65/40 SBC module Expansion connector.

RM 65 Bus Pin Assignments

Bottom (Solder Side)					Top (Component Side)				
Pin	Signal Mnemonic	Signal Name	I/O	Type	Pin	Signal Mnemonic	Signal Name	I/O	Type
1a	GND	Ground		Power	1c	+5V	+5 Vdc		Power
2a	BADR/	Buffered Bank Address	O	3S TTL	2c	BA15/	Buffered Address Bit 15	O	3S TTL
3a	GND	Ground		Power	3c	BA14/	Buffered Address Bit 14	O	3S TTL
4a	BA13/	Buffered Address Bit 13	O	3S TTL	4c	BA12/	Buffered Address Bit 12	O	3S TTL
5a	BA11/	Buffered Address Bit 11	O	3S TTL	5c	GND	Ground		3S TTL
6a	BA10/	Buffered Address Bit 10	O	3S TTL	6c	BA9/	Buffered Address Bit 9	O	3S TTL
7a	BA8/	Buffered Address Bit 8	O	3S TTL	7c	BA7/	Buffered Address Bit 7	O	3S TTL
8a	GND	Ground		Power	8c	BA6/	Buffered Address Bit 6	O	3S TTL
9a	BA5/	Buffered Address Bit 5	O	3S TTL	9c	BA4/	Buffered Address Bit 4	O	3S TTL
10a	BA3/	Buffered Address Bit 3	O	3S TTL	10c	GND	Ground		Power
11a	BA2/	Buffered Address Bit 2	O	3S TTL	11c	BA1/	Buffered Address Bit 1	O	3S TTL
12a	BA0/	Buffered Address Bit 0	O	3S TTL	12c	B01	Buffered Phase 1 Clock	O	TP TTL
13a	GND	Ground		Power	13c	BSYNC	Buffered Sync		3S TTL
14a	BSO	Buffered Set Overflow	I	OC TTL	14c	BDRQ1/	*Buffered DMA Request 1		
15a	BRDY	Buffered Ready	I	OC TTL	15c	GND	Ground		Power
16a		*User Spare 1			16c	-12V/-V	*-12 Vdc/-V		
17a	+12V/+V	*+12 Vdc/+V			17c		*User Spare 2		
18a	GND	Ground Line		Power	18c	BFLT/	Buffered Bus Float	I	OC TTL
19a	BDMT/	Buffered DMA Terminate	O		19c	B00	*Buffered External Phase 0 Clock		
20a		*User Spare 3			20c	GND	Ground		Power
21a	BR/W/	Buffered Read/Write "Not"	O	3S TTL	21c	BDRQ2/	*Buffered DMA Request 2		
22a		*System Spare			22c	BR/W	Buffered Read/Write	O	3S TTL
23a	GND	Ground		Power	23c	BACT/	Buffered Bus Active	I	OC TTL
24a	BIRQ/	Buffered Interrupt Request	I	OC TTL	24c	BNMI/	Buffered Non-Maskable Interrupt	I	OC TTL
25a	B02/	Buffered Phase 2 "Not" Clock	O	3S TTL	25c	GND	Ground		Power
26a	B02	Buffered Phase 2 Clock	O	3S TTL	26c	BRES/	Buffered Reset	O	OC TTL
27a	BD7/	Buffered Data Bit 7	I/O	3S TTL	27c	BD6/	Buffered Data Bit 6	I/O	3S TTL
28a	GND	Ground		Power	28c	BD5/	Buffered Data Bit 5	I/O	3S TTL
29a	BD4/	Buffered Data Bit 4	I/O	3S TTL	29c	BD3/	Buffered Data Bit 3	I/O	3S TTL
30a	BD2/	Buffered Data Bit 2	I/O	3S TTL	30c	GND	Ground		Power
31a	BD1/	Buffered Data Bit 1	I/O	3S TTL	31c	BD0/	Buffered Data Bit 0	I/O	3S TTL
32a	+5V	+5 Vdc		Power	32c	GND	Ground		Power

Notes:
 *Not used on this module. Signal name reflects RM 65 Bus reserved function.



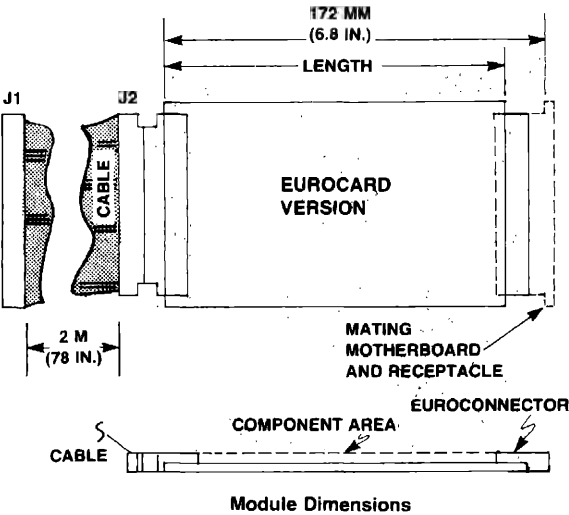
RM65-7141E Adapter Cable and Buffer Module Block Diagram



SPECIFICATIONS

Characteristic	Value
Dimension (See Notes) Width Length Height (see Note 1)	100 mm (3.9 in.) 160 mm (6.3 in.) 14 mm (0.56 in.)
Weight	1.0 lb. (140 g)
Power (Supplied from RM 65 Bus)	+5V \pm 5% 170 mA (0.85 W)—Typical 270 mA (1.35 W)—Maximum
Environment Operating Temperature Storage Temperature Relative Humidity	0°C to 70°C -40°C to 85°C 0% to 85% (without condensation)
Propagation Time (maximum)	35 ns Address Bus 70 ns Data Bus (ref BACT/)
Interface Connectors AIM 65/40 Expansion Connector RM 65 Bus	64-pin DIN connector (0.100 in. centers) per DIN 41612 (mates with Burndy RPI96B32POA02K9 or equivalent) 64-pin plug (0.100 in. centers) per DIN 41612 (Row b is not installed)
Interface Cables Number of Cables Cable Length Type Number of conductors per cable Wire Size Connectors (Part Number)	One 2 m (78 in.) Flat ribbon 64 #28 AWG J1 Winchester 965-6053-0531-12 or equivalent J2 Winchester 645-6053-422-12 T & B Ansley 609-641-2 Cannon 006D64R3BAL or equivalent

Notes:
1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.). Allow an additional 19 mm (0.75 in.) for the connector on the bottom of the module and cable bend.
2. The length does not include extensions beyond the edge of the module due to connectors or the module ejector.
3. The dimensions conform to DIN 41612.





RM65-7201E

RM 65 DESIGN PROTOTYPING MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-7201E Design Prototyping Module is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 module products use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40. Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

ORDERING INFORMATION

Part No.	Description
RM65-7201E	Design Prototyping Module

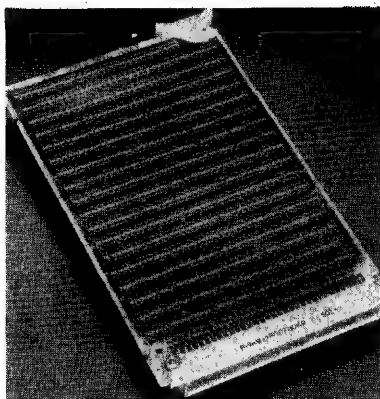
FEATURES

- Compact size—approximately 4" × 6¼" (100 mm × 160 mm)
- Provision for mounting mass-terminated cable connectors
- All wire-wrap holes pre-drilled on 0.100 in. centers
- Provision for installing decoupling capacitors
- Spacing for 0.300, 0.400 and 0.600 in. wide components
- +5V and ground extended throughout the module
- Isolated power strips allow connection to other supply voltages

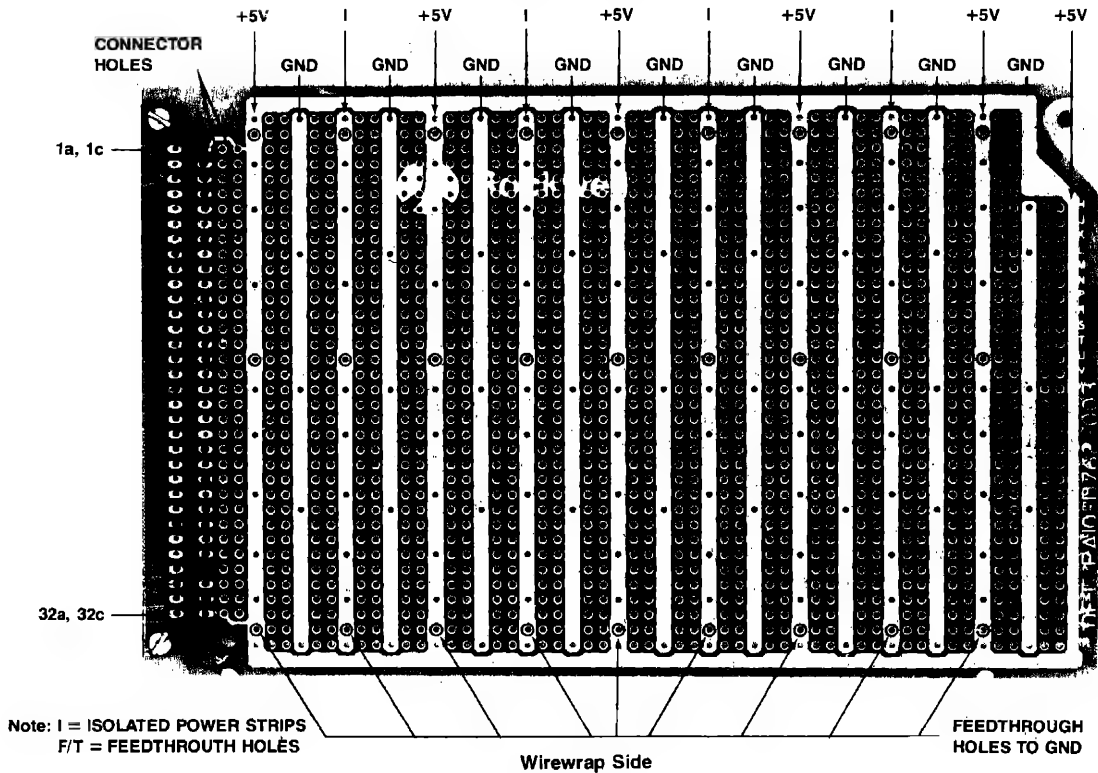
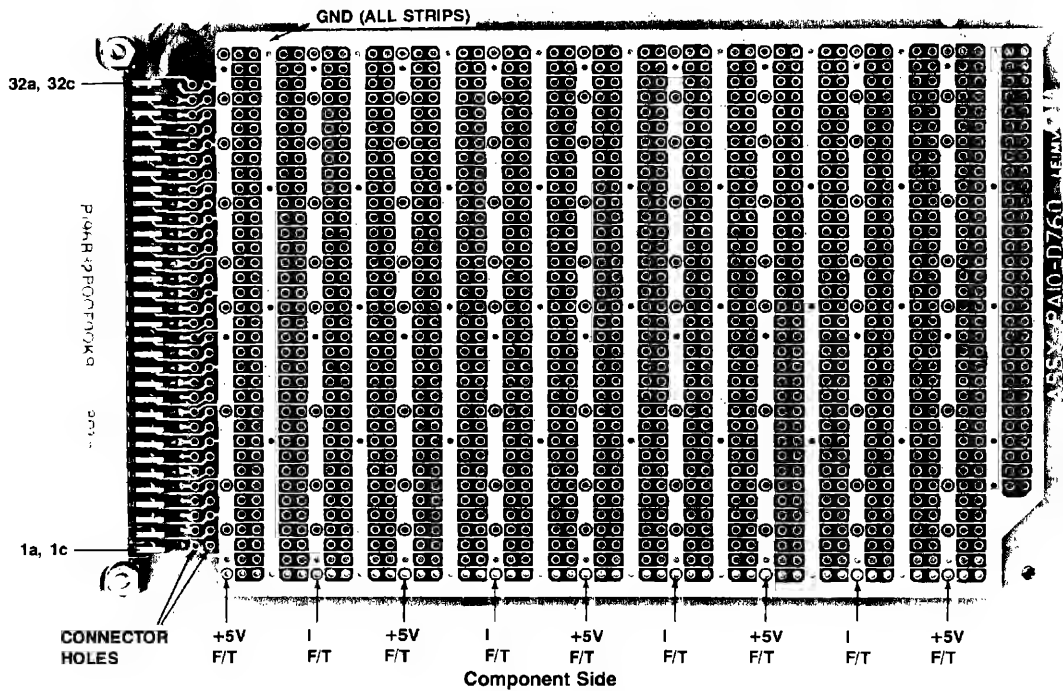
PRODUCT OVERVIEW

The RM65-7201E Design Prototyping Module allows you to develop custom application circuits for installation in any RM 65 motherboard.

Power and return lines are prerouted throughout the module. Plated-through holes, spaced beside the power lines, permit wire-wrap sockets to be installed. The hole pattern allows manual or automatic wire-wrapping. The holes at the I/O end of the module accept a variety of wire-wrap flat ribbon cable connectors. Additional predrilled holes permit mounting of decoupling capacitors.



RM65-7201E Design Prototyping Module



RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADP/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	B ϕ 1	Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	Buffered Sync
14a	BSO	Buffered Set Overflow	14c	BDRQ1/	Buffered DMA Request 1
15a	BRDY	Buffered Ready	15c	GND	Ground
16a		User Spare 1	16c	-12V/-V	-12 Vdc/-V
17a	+12V/+V	+12 Vdc/+V	17c		User Spare 2
18a	GND	Ground Line	18c	BFLT/	Buffered Bus Float
19a	BDMT/	Buffered DMA Terminate	19c	B ϕ 0	Buffered External Phase 0 Clock
20a		User Spare 3	20c	GND	Ground
21a	BR \overline{W} /	Buffered Read/Write "Not"	21c	BDRQ2/	Buffered DMA Request 2
22a		System Spare	22c	BR \overline{W}	Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request	24c	BNMI/	Buffered Non-Maskable Interrupt
25a	B ϕ 2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	B ϕ 2	Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

INSTALLATION

Before installing the module, inspect for damage and grease, dirt, liquid or other foreign materials that will affect performance.

- a. Solder jumpers between the isolated power strips and the power (+5V, +12/+V, or -12V/-V) traces as required.

CAUTION

Before proceeding, ensure that the power strips are not shorted to GND.

- b. Solder power filter capacitors as required between the power strips and GND.
c. Install and wire components on the Design Prototype Module:

1. Insert wire-wrap sockets into the desired holes. Solder two pins (on opposite ends of the socket) to the associated feedthrough to hold the socket in place.
2. Insert the solder stakes for mounting of discrete components, power connection and test points into the desired holes and solder to the associated feedthroughs.
3. Insert and solder individual or strip stakes into connector holes for all RM 65 bus signals used on the module.

4. Wire wrap wires between the protruding pins and other pins or power/GND traces as required.

- d. Double check the hookup to ensure proper connection.

CAUTION

Ensure that no power lines are shorted to GND before installation into the RM 65 bus. Shorting power to ground may damage your circuitry, module, power supply and/or interfacing modules unless proper current limiting protection is provided.

- e. Install components into sockets as required.
f. Remove power from the RM 65 bus.

CAUTION

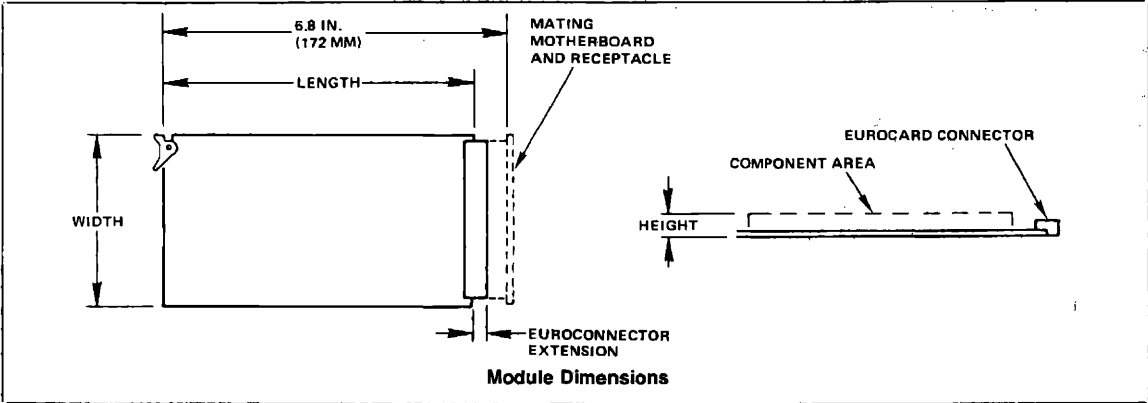
Never install or remove modules with power on—it may cause damage to your module and/or host system.

- g. Insert the module in the RM 65 Bus motherboard or single card adapter receptacle.
h. Apply power to the RM 65 bus.

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3)	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	2.5 oz. (65 g)
RM 65 Bus Interface	64-pin plug (0.100 in. centers) per DIN 41612 (Row b is not installed)
Component Mounting Area:	
Number of Component Hole Columns:	36
Number of Component Hole Rows:	36
Number of +5V power strips:	6
Number of isolated power strips:	4
Number of ground strips:	9
Vertical hole spacing:	0.100 in.
Horizontal hole spacing:	0.100 in.

- Notes:
- 1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
 - 2. Length does not include the added extensions due to the module ejector.
 - 3. Dimensions conform to DIN 41612.





RM65-7211E RM 65 EXTENDER MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-7211E Extender Module is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 module products use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

ORDERING INFORMATION

Part No.	Description
RM65-7211E	Extender Module

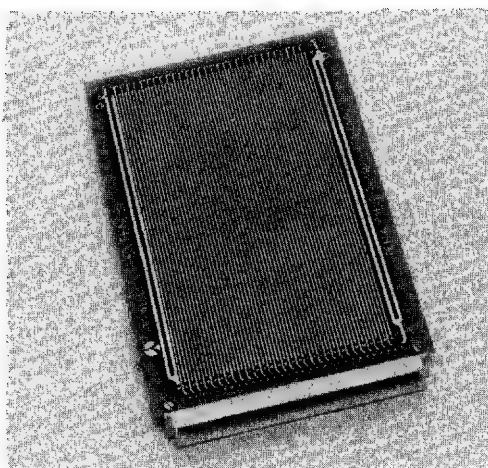
FEATURES

- Extends all RM 65 Bus Lines
- Terminals for GND and +5V
- Assembled, tested and warranted

PRODUCT OVERVIEW

The RM 65 Extender Module physically extends a module that is electrically connected to an RM 65 motherboard. This simplifies signal tracing and troubleshooting by providing access to the module outside of its card cage or enclosure.

The RM 65 Extender Module consists of a series of bus lines connecting the RM 65 connector plug on one end, to an RM 65 compatible connector receptacle on the other end. The lines are connected pin-for-pin between the plug and receptacle.



RM65-7211E Extender Module

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	B ϕ 1	Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	Buffered Sync
14a	BSO	Buffered Set Overflow	14c	BDRQ1/	Buffered DMA Request 1
15a	BRDY	Buffered Ready	15c	GND	Ground
16a		User Spare 1	16c	-12V/-V	-12 Vdc/-V
17a	+12V/+V	+12 Vdc/+V	17c		User Spare 2
18a	GND	Ground Line	18c	BFLT/	Buffered Bus Float
19a	BDMT/	Buffered DMA Terminate	19c	B ϕ 0	Buffered External Phase 0 Clock
20a		User Spare 3	20c	GND	Ground
21a	BR \overline{W} /	Buffered Read/Write "Not"	21c	BDRQ2/	Buffered DMA Request 2
22a		System Spare	22c	BR \overline{W}	Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request	24c	BNMI/	Buffered Non-Maskable Interrupt
25a	B ϕ 2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	B ϕ 2	Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

INSTALLATION

Before installing the module, inspect for damage and grease, dirt, liquid or other foreign materials that will affect performance.

- Turn power off to the RM 65 bus.

CAUTION

Never install or remove modules with power on—it may cause damage to the host system or the modules being connected or disconnected.

- Remove module to be extended from the RM 65 card cage (if present).

- Insert the Extender Module in a vacant card slot in the card cage and connect it to the motherboard.

- Connect the module to be extended to J1 of the Extender Module.

CAUTION

Be sure the extended module is properly supported to prevent damage to the module and/or the Extender Module.

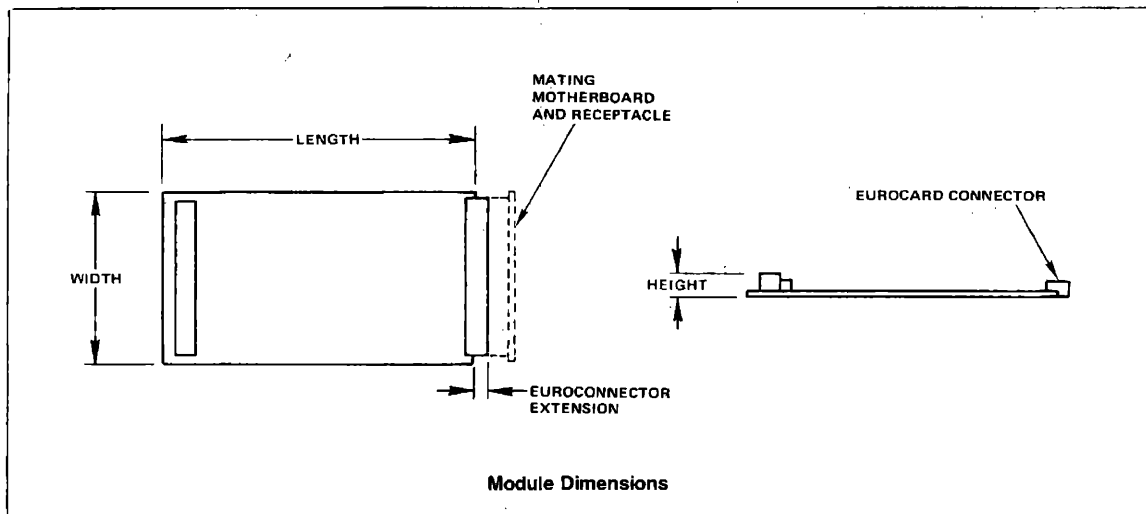
- Apply power to the RM 65 bus.

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3)	
Width	3.9 in. (100 mm)
Length	7.4 in. (187 mm)
Height	0.56 in. (14 mm)
Weight	3.2 oz. (90 g)
Interface Connectors	
RM 65 Bus	64-pin plug (0.100 in. centers) per DIN 41612 (Row b is not used)
RM 65 Module	64-pin plug (0.100 in. centers) per DIN 41612 (Row b is not used)

Notes:

1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. Length does not include the added extension due to the module ejector.
3. Dimensions conform to DIN 41612.



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INTEGRAL MODEMS

Highest Quality, Performance at Competitive Cost

Rockwell International's high-speed integral modem subsystems offer better performance and greater reliability than any others. They're also more cost effective and are optimized to match more applications than others. That's why Rockwell produces more high-speed integral modem subsystems than any other company.

The chances are, if you're using a high-speed box modem, a Rockwell subsystem is in it. Practically every facsimile machine uses our modems. Rockwell is, by far, the leading supplier to Japanese facsimile machine manufacturers. With 99.6% of our subsystems accepted by incoming inspection, we have documented an MTBF of 200,000 hours, or about 23 years between service calls.

As for performance, our modems don't lose a bit in a million, even over long distance lines of the commercial telephone network. Much of this is because of our signal processing capabilities, equalization and diagnostics.

Built-in diagnostics, such as eye pattern and mean squared error, allow thorough modem testing. Several stages of equalization permit accurate transmission over even unconditioned lines. In fact, adaptive equalization, which compensates for phase shifts and frequency delays, was originated in modem technology under a basic patent owned by Rockwell.

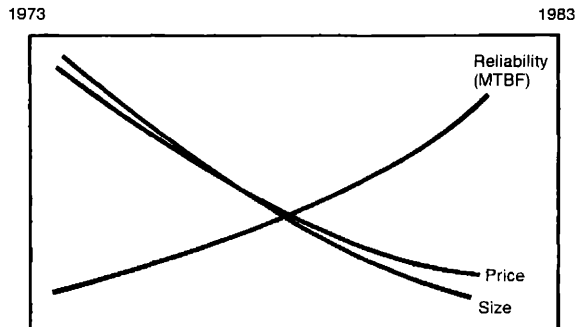
Much of modem technology came from Rockwell International. Our first modems date back to vacuum tube versions in 1955. We made the first LSI integral modems in 1969. Today, we cover all speeds from 1200 to 9600 bps, with a 14,400 bps model to be announced.

Our newest third-generation LSI family members are designed to be addressed as microcomputer peripherals, thus simplifying design and reducing costs of the host equipment. They're on interchangeable cards, small Eurocard sized, so you can switch communication speeds without expensive design changes.

And, they're optimized for specific applications—for box modems and statistical multiplexers, for facsimile equipment, for use in multi-point system terminals, etc.

They're also low in price and readily available. Being the largest manufacturer lets us pass our advantages on to our customers. We offer the best cost/performance modem subsystems, with the highest reliability. There's no one else close.

Rockwell Integral Modem Subsystems Lead The Industry



MTBF (Thousand Hours)

ACCEPTANCE (%)

CARD SIZE (Sq. In.)

	50	100	200
ACCEPTANCE (%)	95	99.5	99.7
CARD SIZE (Sq. In.)	112	54	10



R96FAX **9600 BPS FACSIMILE MODEM**

PRELIMINARY

INTRODUCTION

The Rockwell R96FAX is a synchronous serial 9600 bps modem designed for operation over either dedicated unconditioned lines or over the general switched telephone network.

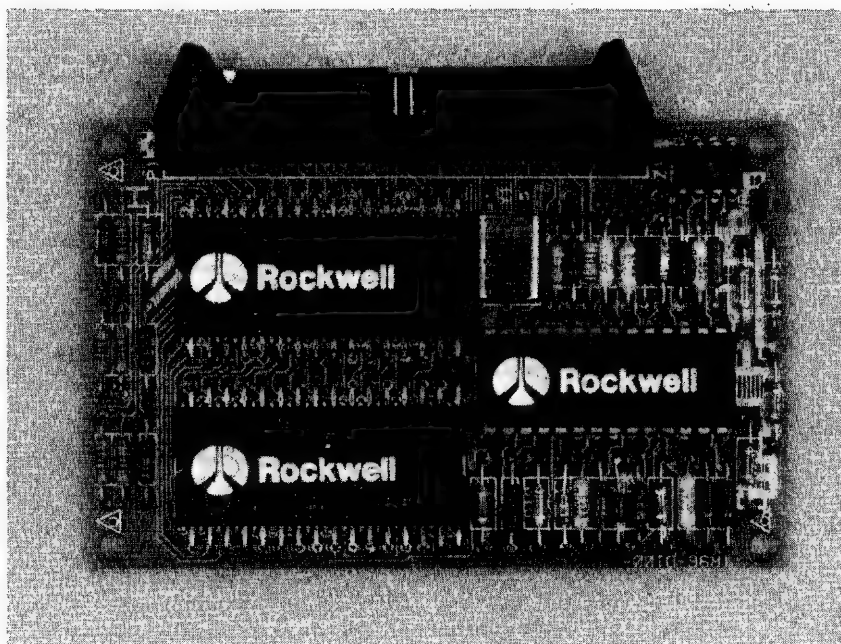
The modem satisfies telecommunications requirements specified in CCITT Recommendations V.29 and V.27 ter, and of Recommendations T.30, T.4 and T.3.

The R96FAX is specifically optimized for use in Group III Facsimile machines with the added capability of Group II compatibility. The small size and low power consumption of the modem offer the user flexibility in creating a 9600 bps modem design customized for specific packaging and functional requirements.

The modem is capable of operating at 9600, 7200, 4800, 2400, and 300 bps.

FEATURES

- Ultimate User Compatibility:
 - CCITT V.29, V.27 ter, T.30, V.21 Channel 2, T.4, T.3
- Group III and Group II Facsimile
- Half-Duplex (2-Wire)
- Programmable Tone Generation and Detection
- Dynamic Range -43 dBm to 0 dBm
- Diagnostic Capability
- Equalization:
 - Automatic Adaptive
 - Compromise Cable (Selectable)
 - Compromise Link Amplitude (Selectable)
- DTE Interface:
 - Microprocessor Bus
 - CCITT V.24 (RS-232-C Compatible)
- Small Size — 100 mm × 65 mm (3.94 × 2.56 inches)
- Low Power Consumption (2 Watts, Typical)
- Transmit Output Level (+5.5 dBm ±0.5 dB)
- TTL and CMOS Compatible



R96FAX Modem

TECHNICAL SPECIFICATIONS

The following are the technical specifications for the R96FAX modem.

TRANSMITTER TONAL SIGNALING AND CARRIER FREQUENCIES

The transmitter tonal signaling and carrier frequencies are given in the following tables:

T. 30 Tonal Signaling Frequencies

Frequency Type	Specification (Hz \pm 0.5 Hz)
Calling Tone (CNG)	1100
Answer Tone (CED)	2100
Group II Identification (C12)	1850
Group II Command (GC2)	2100
Group II Confirmation (CFR2, MCF2)	1650
Line Conditioning Signal (LCS)	1100
End of Message (EOM)	1100
Procedure Interrupt (PIS)	462

Carrier Frequencies

Frequency Type	Specification (Hz \pm 0.5 Hz)
T.3 Carrier (Group II)	2100
V.27 ter Carrier	1800
V.29 Carrier	1700

tone generation

Under control of the host processor, the R96FAX can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

tone detection

In the 300 bps FSK receive configuration, the presence of tones at preset frequencies is indicated by bits in the interface memory of the R96FAX. The frequencies and responses may be altered by the user via microprocessor control.

SIGNALING AND DATA RATES

The signaling and data rates for the R96FAX are defined in the table below:

Signaling/Data Rates

Parameter	Specification (\pm 0.01%)
Signaling Rate: Data Rate:	2400 Baud 9600 bps, 7200 bps, 4800 bps
Signaling Rate: Data Rate:	1600 Baud 4800 bps
Signaling Rate: Data Rate:	1200 Baud 2400 bps

DATA ENCODING

At 2400 baud, the data stream is encoded per CCITT V.29. At 9600 bps, the data stream is divided in groups of four-bits (quads) forming a 16-point structure. At 7200 bps, the data stream

is divided into three bits (tribits) forming an 8-point structure. At 4800 bps, the data stream is divided into two bits (dibits) forming a 4-point structure.

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 ter.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 ter.

EQUALIZERS

The R96FAX provides equalization functions which can be used to improve performance when operating over poor lines.

Cable Equalizers — Selectable compromise cable equalizers are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Amplitude Equalizer — The selectable compromise amplitude equalizer may be inserted into the transmit and/or receive paths under control of the transmit amplitude equalizer enable and the receive amplitude equalizer enable bits in the interface memory. The amplitude select bit controls which of two amplitude equalizers is selected.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit for V.27 and V.29 configurations. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If neither the link amplitude nor cable equalizer is enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. 1200 Baud. Square root of 90 percent
2. 1600 Baud. Square root of 50 percent
3. 2400 Baud. Square root of 20 percent

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R96FAX incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 ter or V.29 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R96FAX can adapt to received frequency error of up to ± 10 Hz with less than a 0.2 dB degradation in BER performance. Group II carrier recovery capture range is 2100 ± 30 Hz.

RECEIVE LEVEL

The receiver circuit of the R96FAX satisfies all specified performance requirements for received line signal levels from 0dBm to -43dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

In the receive state, the R96FAX provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a $\pm 0.01\%$ frequency error in the associated transmit timing source.

TRANSMIT LEVEL

The transmitter output level is fixed at $+5.5 \text{ dBm} \pm 0.5 \text{ dB}$. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide $-0.5 \text{ dBm} \pm 0.5 \text{ dB}$ to the load.

TRANSMIT TIMING

In the transmit state, the R96FAX provides a Data Clock (DCLK) output with the following characteristics:

1. **Frequency.** Selected data rate of 9600, 7200, 4800, 2400, or 300 Hz ($\pm 0.01\%$). In Group II, DCLK tracks an external 10368 Hz clock.
2. **Duty Cycle.** $50 \pm 1\%$

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

TURN-ON SEQUENCE

A total of ten selectable turn-on sequences can be generated by the R96FAX, as defined in the following table:

Turn-On Sequences

NO.	V.29	V.27 ter	RTS-CTS Time (ms)	Comments
1	9600 bps		253	
2	7200 bps		253	
3	4800 bps		253	
4		4800 bps ²	708	
5		2400 bps ²	943	
6	9600 bps		458	Preceded By Echo Suppressor Disable Tone
7	7200 bps		458	
8	4800 bps		458	
9		4800 bps ²	913	
10		2400 bps ²	1148	

NOTES

1. Turn-on sequences six through ten can be generated for lines with protection against talker echo.
2. V.27 ter long training sequence only.

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled 1's followed by a 20 ms period of no transmitted energy.

CLAMPING

The following clamps are provided with the R96FAX:

1. **Received Data (RXD).** RXD is clamped to a constant mark (1) whenever RLSD is off.

2. **Received Line Signal Detector (RLSD).** RLSD is clamped off (squelched) during the time when RTS is on.
3. **Extended Squelch.** Optionally, RLSD remains clamped off for 130 ms after the on-to-off transition of RTS.

RESPONSE TIMES OF CLEAR-TO-SEND (CTS)

The time between the off-to-on transition of RTS and the off-to-on transition of CTS is dictated by the length of the training sequence. Response time is 253 ms for V.29, 708 ms for V.27 ter at 4800 bps, and 943 ms for V.27 ter at 2400 bps.

The time between the on-to-off transition of RTS and the on-to-off transition of CTS in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR (RLSD)

For either V.27 ter or V.29, RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 15 ± 10 ms. The RLSD on-to-off response time for V.27 is 10 ± 5 ms and for V.29 is 30 ± 9 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Two threshold options are provided:

1. Greater than -43 dBm (RLSD on)
Less than -48 dBm (RLSD off)
2. Greater than -47 dBm (RLSD on)
Less than -52 dBm (RLSD off)

NOTE

Performance may be at a reduced level when the received signal is less than -43 dBm .

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated carrier signal applied to the receiver's audio input (RXA).

MODES OF OPERATION

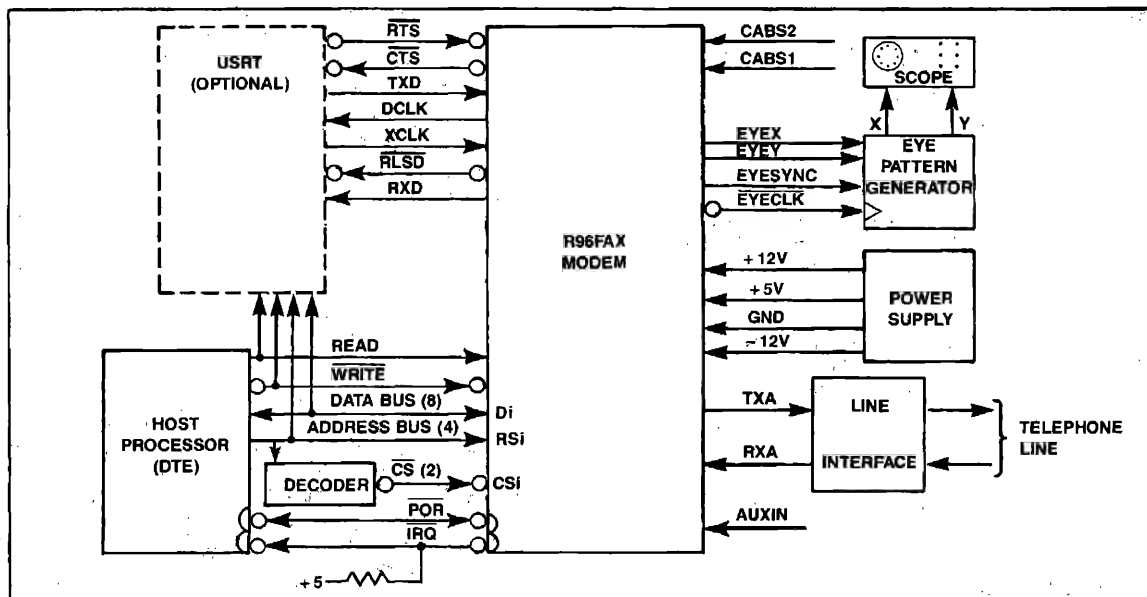
The R96FAX is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the R96FAX Interface Diagram) illustrates this capability.

PARALLEL MODE

The R96FAX has the capability of transferring channel data eight bits at a time via the microprocessor bus.



R96FAX Functional Interconnect Diagram

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the R96FAX is configured by the host processor via the microprocessor bus.

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 40-pin ribbon connector. Software circuits are assigned to specific bits in a 32-byte interface memory.

HARDWARE SUPERVISORY CIRCUITS

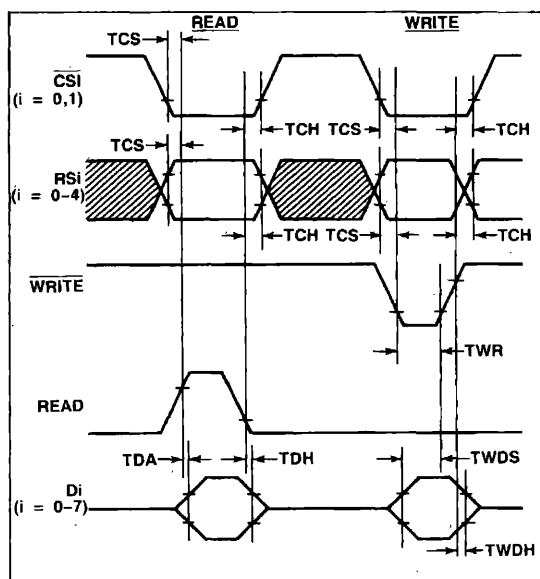
Signal names and descriptions of the hardware supervisory circuits, including the microprocessor interface, are listed in the R96FAX Hardware Supervisory Circuits table. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R96FAX Hardware Supervisory Circuits

Name	I/O	Pin No.	Description
A. OVERHEAD:			
GND	I	14,39	Ground
+5 volts	I	3,4	+5 volt supply
+12 volts	I	26	+12 volt supply
-12 volts	I	37	-12 volt supply
POR	I/O	36	Power-on-reset

R96FAX Hardware Supervisory Circuits (Cont.)

Name	I/O	Pin No.	Description
B. MICROPROCESSOR INTERFACE:			
D7	I/O	7	Data Bus (8 Bits)
D6	I/O	5	
D5	I/O	9	
D4	I/O	31	
D3	I/O	15	
D2	I/O	28	
D1	I/O	23	
D0	I/O	29	
RS3	I	30	Register Select (4 Bits)
RS2	I	8	
RS1	I	27	
RS0	I	10	
CS0	I	6	Chip Select for Bank 0
CS1	I	18	Chip Select for Bank 1
READ	I	1	Read Enable
WRITE	I	2	Write Enable
IRQ	O	32	Interrupt Request
C. V.24 INTERFACE:			
DCLK	O	13	Data Clock
XCLK	I	22	External Clock for Group II
RTS	I	19	Request-to-Send
CTS	O	17	Clear-to-Send
TXD	I	20	Transmitter Data
RXD	O	21	Receiver Data
RLSD	O	16	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABS1	I	33	Cable Select 1
CABS2	I	34	Cable Select 2
E. ANALOG SIGNALS:			
TXA	O	38	Transmitter Analog Output
RXA	I	40	Receiver Analog Input
AUXIN	I	35	Auxiliary Analog Input



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
CSi, RSi setup time prior to Read or Write	TCS	30	—	NS
Data Access time after Read	TDA	—	140	NS
Data hold time after Read	TDH	10	50	NS
CSi, RSi hold time after Read or Write	TCH	10	—	NS
Write data setup time	TWDS	75	—	NS
Write data hold time	TWDH	10	—	NS
Write strobe pulse width	TWR	75	—	NS

Cable Equalizer Selection

CABS 2	CABS 1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

INTERFACE MEMORY

The R96FAX has two banks of 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. These registers are referred to as interface memory. See R96FAX Interface Memory table. Registers in bank 0 update at the modem sample rate (9600 bps). Registers in bank 1 update at the selected baud rate.

When information in these registers is being discussed, the format Y:Z:Q is used. The bank is specified by Y(0 or 1), the register by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a 1.

R96FAX Interface Memory

Bank	(HEX) Reg No.	Description
0	F	Diagnostic Control
0	E	Handshake Status
0	D	Do Not Use
0	C	Do Not Use
0	B	Do Not Use
0	A	Do Not Use
0	9	Do Not Use
0	8	Do Not Use
0	7	Do Not Use
0	6	Do Not Use
0	5	Option
0	4	Configuration
0	3	Diagnostic Data Real MSB's; FREQM
0	2	Diagnostic Data Real LSB's; FREQL
0	1	Diagnostic Imaginary MSB's
0	0	Diagnostic Imaginary LSB's; Data Transfer Register
1	F	Diagnostic Control
1	E	Handshake Status
1	D	RAM Write Control
1	C	GII AGC Slew Rate Select
1	B	Tone Detect Indicator
1	A	Do Not Use
1	9	Do Not Use
1	8	Do Not Use
1	7	Receiver Status
1	6	Do Not Use
1	5	Receiver Status
1	4	Receiver Status
1	3	Diagnostic Data Real MSB's
1	2	Diagnostic Data Real LSB's
1	1	Diagnostic Imaginary MSB's
1	0	Diagnostic Imaginary LSB's

SOFTWARE SUPERVISORY CIRCUITS

The operation of the R96FAX is affected by a number of software control inputs. These inputs are written into registers within the modem via a microprocessor bus under external control. Modem operation is monitored by various software flags that are read from modem registers using the same microprocessor bus. The functions of all modem I/O registers are listed in the R96FAX Interface Memory table and are defined as follows:

CONFIGURATION REGISTER

The host processor configures the R96FAX by writing a control byte into the configuration register (0:4) in its interface memory space as shown in the following table:

Configuration Register (0:4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TNXMT	G2	FSK	V29	V27	DR3	DR2	DR1

Definition of Configuration Terms:

TXMXT.	Tone Transmit
G2.	Group II Facsimile
FSK.	300 bps FSK/Tone Detection
V29.	V.29 Configuration
V27.	V.27 Configuration
DR3.	Selects 9600 bps/V.29
DR2.	Selects 7200 bps/V.29, Selects 4800 bps/V.27
DR1.	Selects 4800 bps/V.29, Selects 2400 bps/V.27

Control words for the five configurations are given in hexadecimal format in the following table:

Configuration Control Words

No.	Configuration	Configuration Word (HEX)
1	V.29 9600	14
	V.29 7200	12
	V.29 4800	11
2	V.27 4800	0A
	V.27 2400	09
3	FSK	20
4	Group II	40
5	Tone Transmit	80

Definition of Configurations:

1. **V.29.** When any of the V.29 configurations has been selected, the modem operates as specified in CCITT Recommendation V.29.
2. **V.27.** When any of the V.27 configurations has been selected, the modem operates as specified in CCITT Recommendation V.27 ter.
3. **FSK.** The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 channel 2 modulation system.
4. **Group II.** The modem operates as a CCITT T.3 compatible AM modem. This permits transmission to and reception from Group II facsimile apparatus. A carrier frequency of 2100 Hz is used. A white signal is transmitted as maximum carrier. A black signal is transmitted as no carrier. The phase of the carrier representing white is reversed after each transition through black.

When in the receive state, the R96FAX recovers the carrier of the remote transmitting modem to perform a coherent demodulation of the incoming signal. This allows a baseband of 3400 Hz to be recovered. The recovered baseband signal is made available on the microprocessor bus as diagnostic data.

The baseband signal is converted to black or white by comparing the received signal level with a preset threshold number. This number may be changed by the user.

Receiver data is presented to the RXD output at a rate of 10368 samples per second. The user should strobe the data on the rising edge of the data clock (DCLK). A logical 1 level (high voltage) represents white. A logical 0 level (low voltage) represents black.

5. **Tone Transmit.** In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by the user. Two registers in the host interface memory space contain the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents $0.146484 \text{ Hz} \pm 0.01\%$. The frequency generated is: $f = 0.146484 (256 \text{ FREQM} + \text{FREQL}) \text{ Hz} \pm 0.01\%$.

Hexadecimal frequency numbers (FREQM, FREQL) for commonly generated tones are shown in the following chart:

Commonly Generated Tones

Frequency	FREQM	FREQL
462 Hz	0C	52
1100 Hz	1D	55
1650 Hz	2C	00
1850 Hz	31	55
2100 Hz	38	00

OPTION REGISTER

The host processor conveys option information to the R96FAX by writing a control byte into the Option Register (0:5) in its memory space as shown in the table below:

Option Register (0:5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTS	TDIS			EDIS	SQEXT	T2	LRTH

Definition of Option Terms:

RTS.	Request-to-Send
TDIS.	Training Disable
EDIS.	Echo Protector Disable
SQEXT.	Squelch Extend
T2.	T/2 Equalizer
LRTH.	Lower Receive Threshold

Definition of Options:

1. **Request-to-Send.** The R96FAX operates in the receive state until RTS (0:5:7) is turned on. At that time the modem switches to the transmit state and remains there until RTS is turned off, and the turn-off sequence has been completed.
2. **Training Disable.** When the TDIS bit (0:5:6) is on in the receive state, this bit prevents the modem from entering the training phase. When turned on prior to RTS going on, this bit prevents the generation of a training sequence at the start of transmission.

3. *Echo Protector Disable.* If the EDIS bit (0:5:3) is on, an unmodulated carrier is transmitted for 185 to 200 ms followed by 20 to 25 ms of no transmitted energy at the beginning of the training sequence. This option is available in both the V.27 and V.29 configurations although it is not specified in the CCITT V.29 Recommendation.
4. *Squelch Extend.* When on, the SQEXT bit (0:5:2) inhibits reception of signals for 130 ms after RTS is turned off.
5. *T/2 Equalizer.* If the T/2 equalizer bit (0:5:1) is off, an adaptive equalizer with one tap per baud is used. If the T/2 bit is on, an adaptive equalizer with two taps per baud is used.
6. *Lower Receive Threshold.* When on, the LRTH bit (0:5:0) lowers the receiver turn-on threshold from -43 dBm to -47 dBm.

DISCRETE CONTROL BITS

The discrete control bits are defined in the following table:

Discrete Control Bits

Name	I.D. No.	Description
PDM	0:F:7	When on, PDM places the R96FAX in the parallel mode and inhibits bank 0 diagnostics.
SETUP	0:E:3	When on, SETUP causes the R96FAX to reconfigure to the control word in the configuration register and to assume the options specified for equalizer (0:5:1) and threshold (0:5:0). Resets automatically. Note: Bit 0:4:0 through 0:4:4 should only change state while RTS is off to prevent errors in transmission.
IEO	0:E:2	When on, Interrupt Enable (Zero), causes the IRQ output to be low when the DA0 bit (0:E:0) is on.
RAMW	1:D:0	RAMW, when on, causes the 16-bit word in locations 1:0 and 1:1 to be written into RAM at the location specified in the diagnostic control register (1:F).
J3L	1:D:4	Japanese 3 link, when on, selects this standard for link amplitude equalizer; when off selects U.S. survey long.
RLE	1:D:5	Receiver link equalizer, when on, enables the link amplitude equalizer in the receiver.
TLE	1:D:6	Transmitter link equalizer, when on, enables the link amplitude equalizer in the transmitter.
G2FGC	1:C:0	G2FGC, when on, selects a fast AGC rate in Group II.
IE1	1:E:2	When on, Interrupt Enable (One) causes the IRQ output to be low when the DA1 bit (1:E:0) is on.

STATUS BITS

The status bits are defined in the following table:

Status Bits

Name	I.D. No.	Description
DA0	0:E:0	Data Available (Zero) goes on when the R96FAX writes data into registered 0:0. It is reset when the host processor reads or writes register 0:0. DA0 is used in the parallel mode and also for diagnostic data retrieval.
IA0	0:E:7	Interrupt Active (Zero) is on when bank 0 is causing IRQP to be active.
FED	1:5:6	Fast Energy Detect, when off, indicates energy on the receiver input. Not used for Group II.
P2DET	1:4:2	When off, P2DET indicates a P2 sequence has been detected. Sets to 1 at start of PN sequence.
PNDET	1:7:6	When off, PNDET indicates a PN sequence has been detected. Sets to 1 at end of PN sequence.
CDET	1:7:0	When off, CDET indicates that energy is being detected and a training sequence is not present. Goes off at start of data state.
DA1	1:E:0	Data Available (One) goes on when the R96FAX writes data into register 1:0. It is reset when the host processor reads or writes register 1:0.
IA1	1:E:7	Interrupt Active (One) is on when bank 1 is causing IRQ to be active.
F3	1:B:7	When on, these bits indicate reception of their respective tonal frequencies if the R96FAX is configured in FSK. Default frequencies are: F3 = 462 Hz, F2 = 1100 Hz, and F1 = 2100 Hz.
F2	1:B:6	
F1	1:B:5	

DIAGNOSTIC CAPABILITIES

The R96FAX provides the user with access to much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

HARDWARE DIAGNOSTIC CIRCUITS

Signal names and descriptions of the hardware diagnostic circuits are given in the table below:

Hardware Diagnostic Circuits

Name	I/O	Pin No.	Description
EYEX	0	24	Eye Pattern Data — X Axis
EYEX	0	25	Eye Pattern Data — Y Axis
EYECLK	0	11	Eye Pattern Clock
EYESYNC	0	12	Eye Pattern Synchronizing Signal

Eye Pattern Generation — The four hardware diagnostic circuits allow the user to generate and display an eye pattern. Circuits EYEX and EYEW serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the rising edge of the EYCLK output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

SOFTWARE DIAGNOSTIC CIRCUITS

Two diagnostic control registers are provided in the interface memory to allow user access to various RAM locations within the modem. The access code stored in bank 0 (0:F) selects the source of data for the real and imaginary diagnostic data registers in bank 0 (0:0 through 0:3). Similarly the access code stored in bank 1 (1:F) selects the source of data for registers 1:0 through 1:3. Bank 1 also provides the user with the ability to store the contents of registers 1:0 and 1:1 in the RAM location specified in register 1:F. Writing is performed by turning on control bit RAMW (1:13:0). Reading is performed by handshaking with the appropriate Data Available status bit. The eight most significant bits of real and imaginary data from bank 1 are also presented serially on EYEX and EYEW respectively.

RAM ACCESS CODES (READ)

The RAM Access Codes defined in the table below allow the host processor to read diagnostic information within the R96FAX.

RAM Access Codes (Read)

Bank	Function	Access	Data Type
0	Received Signal Samples	40	Real
	Demodulator Output	42	Complex
	Low Pass Filter Output	54	Complex
	One Baud Energy	04	Imaginary
	AGC Gain Word — MSB's	01	Real
	AGC Gain Word — LSB's	01	Imaginary
1	Equalizer Input	40	Complex
	Equalizer Tap Coefficients	01-20	Complex
	Unrotated Equalizer Output	22	Complex
	Rotated Equalizer Output	22	Complex
	(Received Point-Eye Pattern)		
	Decision Points (Ideal)	62	Complex
	Error Vector	63	Complex
	Rotation Angle	00	Imaginary
	Frequency Correction — MSB's	28	Real
	Frequency Correction — LSB's	28	Imaginary
	Group II Base Band Signal	4B	Real
	Group II Threshold	2A	Imaginary
	EQM	2B	Real

RAM ACCESS CODES (WRITE)

The RAM access codes defined in the following table allow the host processor to write parameter information into the R96FAX.

RAM Access Codes (Write)

Bank	Function	Access	Data Type
1	GII Black/White Threshold	2A	Imaginary
	F1 A10	2B	Imaginary
	F1 B11	2C	Imaginary
	F1 B12	2D	Imaginary
	F1 A00	2E	Imaginary
	F1 B01	2F	Imaginary
	F1 B02	30	Imaginary
	F2 A10	31	Imaginary
	F2 B11	32	Imaginary
	F2 B12	33	Imaginary
	F2 A00	34	Imaginary
	F2 B01	35	Imaginary
	F2 B02	36	Imaginary
	F3 A10	37	Imaginary
	F3 B11	38	Imaginary
	F3 B12	39	Imaginary
	F3 A00	3A	Imaginary
	F3 B01	3B	Imaginary
	F3 B02	3C	Imaginary
	F1 A20	B7	Real
	F1 B21	B8	Real
	F2 A20	B9	Real
	F2 B21	BA	Real
	F3 A20	BB	Real
	F3 B21	BC	Real

POWER-ON INITIALIZATION

When power is applied to the R96FAX, a period of 100 to 300 ms is required for initialization. The power-on-reset signal (POR) remains low during the initialization period. After the low to high transition of POR, the modem is ready to be configured.

At POR time the modem defaults to the following configuration: V.29/9600 bps, T/2 equalizer, serial mode, training enabled, echo protector disable tone, no extended squelch, higher receive threshold, interrupts disabled, no link equalizer, RAM access codes 00.

POR can also be used to initialize the users's host processor. It may be connected to a user supplied power-on-reset signal in a wire-or configuration.

PERFORMANCE

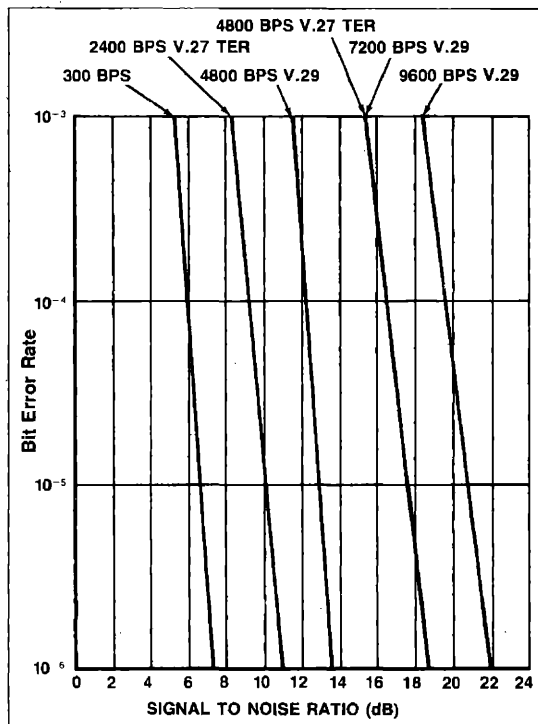
Whether functioning as a V.27 ter or V.29 type modem, the R96FAX provides the user with unexcelled high performance.

Bit Error Rates — The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of -40 dBm as illustrated.

Phase Jitter — At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 60° peak-to-peak phase jitter at 30 Hz.



Typical Bit Error Rate Performance

INTERFACE CIRCUIT CHARACTERISTICS

DIGITAL INTERFACE CIRCUITS

Digital Input Characteristics

Input Logic State	Allowed Input Voltage Levels
Low	0.0V to +0.8V at -0.01 mA
High	+2.0V to +5.0V at $+0.1$ mA

Notes

1. The digital inputs are directly TTL/CMOS compatible. The capacitive loading on each input is 25 pF (maximum).
2. Positive current is defined as current into the node.

Digital Output Characteristics

Input Logic State	Allowed Input Voltage Levels
Low	0.0V to +0.4V at $+1.6$ mA
High	+2.4V to +5.0V at -40 μ A

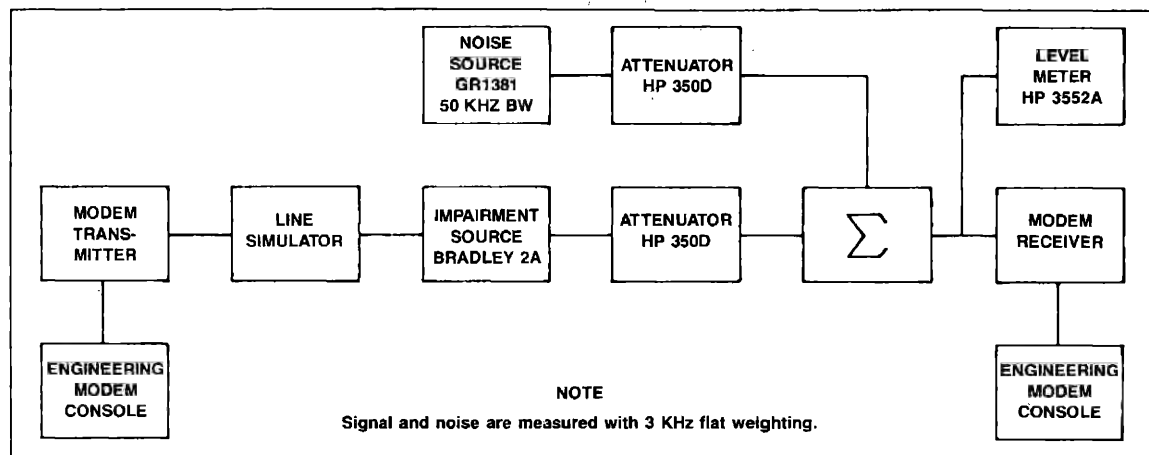
Notes

1. The digital outputs are directly CMOS and TTL compatible.
2. Positive current is defined as current into the node.

ANALOG INTERFACE CIRCUITS

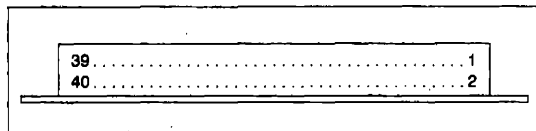
Transmitter Output — The transmitter output is a low impedance operational amplifier output. To match to 600 Ω , an external series resistor is required.

Receiver Input — The receiver input impedance is 63.4K ohm $\pm 5\%$.

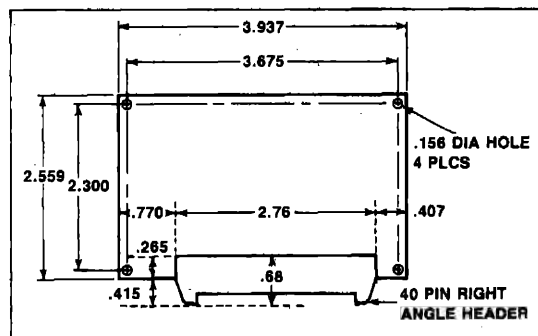


BER Performance Test Set-up

Auxiliary Analog Input — The auxiliary analog input (AUXIN) allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input signals above 4800 Hz will cause aliasing errors. The input impedance is 1K ohm and the gain to transmitter output is 0dB.



Header Pin Assignment



Printed Circuit Board Dimensions

R96FAX SPECIFICATIONS

Power

Voltage	Tolerance	Current (Typical)	Current (Max)
+5 Vdc	± 5%	300 mA	< 500
+12 Vdc	± 5%	5 mA	< 10
-12 Vdc	± 5%	30 mA	< 50

Note: All voltages must have ripple ≤ 0.1 volts peak-to-peak.

Environmental

Parameter	Specification
Temperature	0°C to +60°C (32 to 140°F)
Operating	
Storage	-40°C to +90°C (-40 to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Mechanical

Parameter	Specification
Board Structure	Single PC board with single right angle header with 40 pins
Dimensions	3VH50/IJND5 or equivalent mating connector. Width—2.56 in. (65 mm) Length—3.94 in. (100 mm) Height—0.40 in. (1.02 cm)
Weight	Less than 0.16 lbs. (0.07 kg)



R96DP 9600 BPS DATA PUMP MODEM

PRELIMINARY

INTRODUCTION

The Rockwell R96DP is a synchronous serial 9600 bps modem designed for full-duplex operation over either four-wire dedicated unconditioned lines or half-duplex operation over the general switched telephone network.

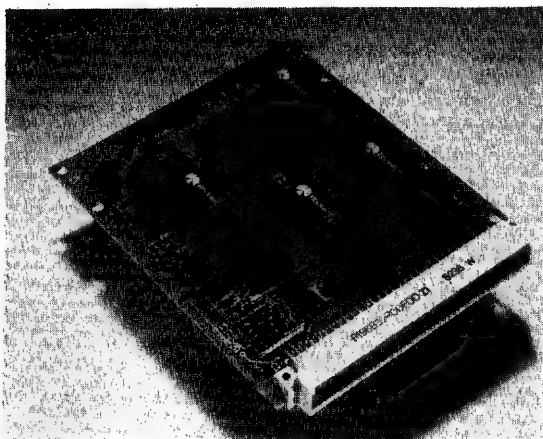
The modem satisfies telecommunications requirements specified in CCITT Recommendations V.29 and V.27 bis/ter.

The small size and low power consumption of the modem offer the user flexibility in creating a 9600 bps modem design customized for specific packaging and functional requirements.

The modem is capable of operating at 9600, 7200, 4800, and 2400 bps.

FEATURES

- User Compatibility:
 - CCITT V.29, and V.27 bis/ter
- Full-Duplex (4-Wire)
- Half-Duplex
- Programmable Tone Generation
- Dynamic Range -43 dBm to 0 dBm
- Diagnostic Capability
- Equalization:
 - Automatic Adaptive
 - Compromise Cable (Selectable)
 - Compromise Link (Selectable)
- DTE Interface:
 - Microprocessor Bus
 - CCITT V.24 (RS-232-C Compatible)
- Loopbacks (V.54 Loop 2, 3 and 4)
 - Local Analog
 - Remote Analog (Locally Activated)
 - Remote Digital (Locally Activated)
- Small Size — 100 mm x 120mm (4.0 x 4.8 inches)
- Low Power Consumption (3 watts, typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R96DP Modem

TECHNICAL SPECIFICATIONS

The following are the technical specifications for the R96DP modem.

TRANSMITTER CARRIER FREQUENCIES

The transmitter carrier frequencies are given in the following table:

Transmitter Carrier Frequencies

Frequency Type	Specification (Hz ± 0.5 Hz)
V.27 bis/ter Carrier	1800
V.29 Carrier	1700

tone GENERATION

Under control of the host processor, the R96DP can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

SIGNALING AND DATA RATES

The signaling and data rates for the R96DP are defined in the table below:

Signaling/Data Rates

Parameter	Specification ($\pm 0.01\%$)
Signaling Rate: Data Rate:	2400 Baud 9600 bps, 7200 bps, 4800 bps
Signaling Rate: Data Rate:	1600 Baud 4800 bps
Signaling Rate: Data Rate:	1200 Baud 2400 bps

DATA ENCODING

At 2400 baud, the data stream is encoded per CCITT V.29. At 9600 bps, the data stream is divided in groups of four-bits (quad-bits) forming a 16-point structure. At 7200 bps, the data stream is divided into three bits (tribits) forming an 8-point structure. At 4800 bps, the data stream is divided into two bits (dibits) forming a 4-point structure.

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 bis/ter.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 bis/ter.

EQUALIZERS

The R96DP provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. 1200 Baud. Square root of 90 percent
2. 1600 Baud. Square root of 50 percent
3. 2400 Baud. Square root of 20 percent

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R96DP incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 bis/ter or V.29 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R96DP can adapt to received frequency error of up to ± 10 Hz with less than 0.2 dB degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from 0 dBm to -43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

The R96DP provides a data derived Receive Data Clock (RDCLK) output in the form of a squarewave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a $\pm 0.01\%$ frequency error in the associated transmit timing source.

TRANSMIT LEVEL

The transmitter output level is accurate to ± 1.0 dB and is programmable from -1.0 dBm to -15.0 dBm in 2 dB steps.

TRANSMIT TIMING

The R96DP provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. Frequency. Selected data rate of 9600, 7200, 4800, or 2400 Hz ($\pm 0.01\%$).
2. Duty Cycle. 50% $\pm 1\%$

Input data presented on TXD is sampled by the R96DP at the low to high transition of TDCLK. Data on TXD must be stable for at least one microsecond prior to the rising edge of TDCLK and remain stable for at least one microsecond after the rising edge of TDCLK.

EXTERNAL TRANSMIT CLOCK

The transmitter data clock (TDCLK) can be phase locked to a signal on input XTCLK. This input signal must equal the desired data rate to $\pm 0.01\%$ with a duty cycle of $50\% \pm 20\%$.

TURN-ON SEQUENCE

A total of 14 selectable turn-on sequences can be generated as defined in the following table:

Turn-On Sequences

No.	V.29	V.27 bis/ter	CTS Response Time (milliseconds)	Comments
1	9600 bps		253	
2	7200 bps		253	
3	4800 bps		253	
4		4800 bps long	708	
5		2400 bps long	943	
6		4800 bps short	50	
7		2400 bps short	67	
8	9600 bps		458	Preceded by Echo Suppressor Disable Tone for lines using echo suppressors*
9	7200 bps		458	
10	4800 bps		458	
11		4800 bps long	913	
12		2400 bps long	1148	
13		4800 bps short	255	
14		2400 bps short	272	

*For short echo protect tone, subtract 155 ms from values of CTS response time.

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled 1's followed by a 20 ms period of no transmitted energy.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) whenever the Received Line Signal Detector (RLSD) is off.

RESPONSE TIMES OF CLEAR-TO-SEND (CTS)

The time between the off-to-on transition of Request-To-Send (RTS) and the off-to-on transition of CTS is dictated by the length of the training sequence and the echo suppressor disable tone, if used. These times are listed in the Turn-On Sequences table. If training is not enabled RTS/CTS delay is less than 1 ms.

The time between the on-to-off transition of RTS and the on-to-off transition of CTS in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR (RLSD)

For either V.27 bis/ter or V.29, RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 15 ± 10 ms. The RLSD on-to-off response time for V.27 is 10 ± 5 ms and for V.29 is 30 ± 9 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Four threshold options are provided:

- Greater than -43 dBm (RLSD on)
Less than -48 dBm (RLSD off)
- Greater than -33 dBm (RLSD on)
Less than -38 dBm (RLSD off)
- Greater than -26 dBm (RLSD on)
Less than -31 dBm (RLSD off)
- Greater than -16 dBm (RLSD on)
Less than -21 dBm (RLSD off)

NOTE

Performance may be at a reduced level when the received signal is less than -43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated carrier signal applied to the receiver's audio input (RXA).

MODES OF OPERATION

The R96DP is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

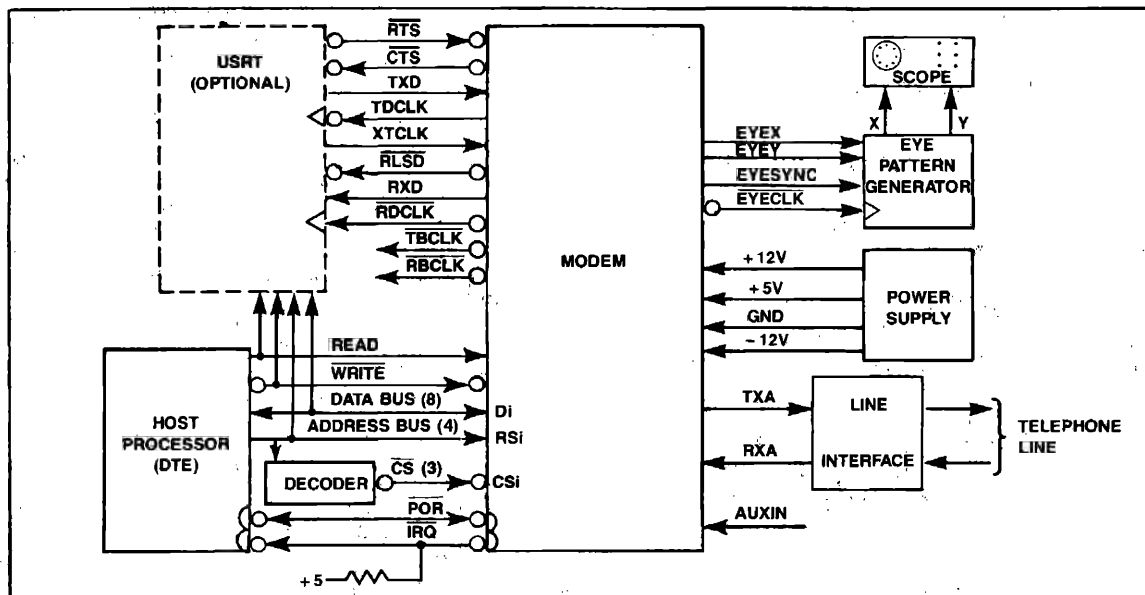
The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R96DP has the capability of transferring channel data up to eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the R96DP is configured by the host processor via the microprocessor bus.



R96DP Functional Interconnect Diagram

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 48-byte interface memory.

HARDWARE SUPERVISORY CIRCUITS

Signal names and descriptions of the hardware supervisory circuits, including the microprocessor interface, are listed in the R96DP Hardware Supervisory Circuits table. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R96DP Hardware Supervisory Circuits

Name	I/O	Pin No.	Description
A. OVERHEAD:			
AGND	I	31C, 32C	Analog Ground
DGND	I	3C, 8C, 5A, 10A	Digital Ground
+5 volts	I	19C, 23C, 26C, 30C	+5 volt supply
+12 volts	I	15A	+12 volt supply
-12 volts	I	12A	-12 volt supply
POR	I/O	13C	Power-on-reset

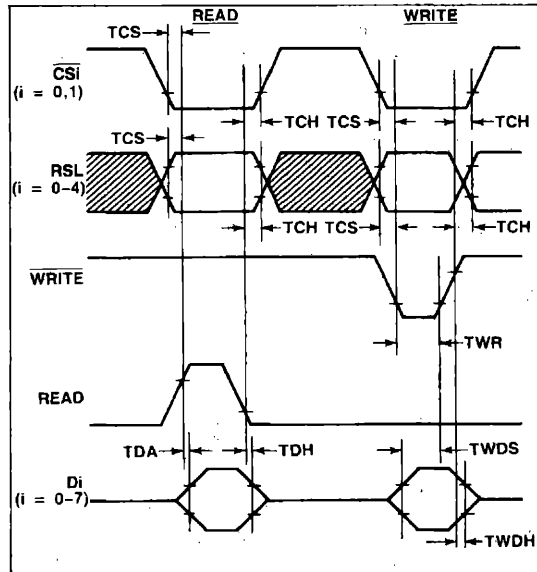
R96DP Hardware Supervisory Circuits (Cont.)

Name	I/O	Pin No.	Description
B. MICROPROCESSOR INTERFACE:			
D7	I/O	1C	Data Bus (8 Bits)
D6	I/O	1A	
D5	I/O	2C	
D4	I/O	2A	
D3	I/O	3A	
D2	I/O	4C	
D1	I/O	4A	
D0	I/O	5C	
RS3	I	6C	Register Select (4 Bits)
RS2	I	6A	
RS1	I	7C	
RS0	I	7A	
CS0	I	10C	Chip Select for Bank 0
CS1	I	9C	Chip Select for Bank 1
CS2	I	9A	Chip Select for Bank 2
READ	I	12C	Read Enable
WRITE	I	11A	Write Enable
IRQ	O	11C	Interrupt Request
C. V.24 INTERFACE:			
RDCLK	O	21A	Receive Data Clock
TDCLK	O	23A	Transmit Data Clock
XTCLK	I	22A	External Transmit Clock
RTS	I	25A	Request-to-Send
CTS	O	25C	Clear-to-Send
TXD	I	24C	Transmitter Data
RXD	O	22C	Receiver Data
RLSD	O	24A	Received Line Signal Detector

R96DP Hardware Supervisory Circuits (Cont.)

Name	I/O	Pin No.	Description
D. ANCILLARY CIRCUITS:			
RBCLK	O	26A	Receiver Baud Clock
TBCLK	O	27C	Transmitter Baud Clock
E. ANALOG SIGNALS:			
TXA	O	31A	Transmitter Analog Output
RXA	I	32A	Receiver Analog Input
AUXIN	I	30A	Auxiliary Analog Input

registers are collectively referred to as interface memory. See R96DP Interface Memory table. Access to the three banks of registers (bank 0, bank 1 and bank 2) is enabled by the Chip Select signals $\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$ respectively. Four Register Select signals (RS0, RS1, RS2, and RS3) are provided to address an individual register within an enabled bank. Registers in bank 1 operate at the sample rate of 9600 samples per second. Registers in banks 0 and 2 operate at the selected baud rate.



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
CSi, RSi setup time prior to Read or Write	TCS	30	—	nsec
Data access time after Read	TDA	—	140	nsec
Data hold time after Read	TDH	10	50	nsec
CSi, RSi hold time after Read or Write	TCH	10	—	nsec
Write data setup time	TWDS	75	—	nsec
Write data hold time	TWDH	10	—	nsec
Write strobe pulse width	TWR	75	—	nsec

INTERFACE MEMORY

The R96DP has three banks of 16 input/output (I/O) registers to which an external (host) microprocessor has access. Although these I/O registers are within the modem, they may be addressed as part of the host processor's memory space. These I/O

R96DP Interface Memory

Bank	(HEX) Reg No.	Description
0	F	Do Not Use
	E	Transmitter Handshake
	D	Do Not Use
	C	Do Not Use
	B	Do Not Use
	A	Do Not Use
	9	Do Not Use
	8	Do Not Use
	7	Transmitter Option
	6	Transmitter Configuration
	5	Equalizer
	4	Loop/Level
	3	FREQM
	2	FREQL
	1	Do Not Use
	0	Transmitter Data
1	F	Do Not Use
	E	Receiver Sample Handshake
	D	Do Not Use
	C	Do Not Use
	B	Receiver Baud Status
	A	Do Not Use
	9	Receiver Sample Status 2
	8	Receiver Sample Status 1
	7	Receiver Option
	6	Receiver Configuration
	5	Diagnostic Control XS
	4	Diagnostic Control YS
	3	Diagnostic Data XSM
	2	Diagnostic Data XSL
	1	Diagnostic Data YSM
	0	Diagnostic Data YSL; Receiver Data
2	F	Do Not Use
	E	Receiver Baud Handshake
	D	Do Not Use
	C	Do Not Use
	B	Do Not Use
	A	Do Not Use
	9	Do Not Use
	8	Do Not Use
	7	Do Not Use
	6	Do Not Use
	5	Diagnostic Control XB
	4	Diagnostic Control YB
	3	Diagnostic Data XBM
	2	Diagnostic Data XBL
	1	Diagnostic Data YBM
	0	Diagnostic Data YBL

When information in these I/O registers is being discussed, the format Y:Z:Q is used. The bank is specified by Y(0-2), the register by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a 1.

SOFTWARE SUPERVISORY CIRCUITS

The operation of the R96DP is affected by a number of software control inputs. These inputs are written into registers within the modem via a microprocessor bus under external control. Bits designated by an X are "Don't Care" inputs that can be set to either 1 or 0. Modem operation is monitored by various software flags that are read from modem registers using the same microprocessor bus. Bits designated by an X are "undefined" outputs that may be either 1 or 0. The functions of all modem I/O registers are listed in the R96DP Interface Memory table and are defined as follows:

TRANSMITTER CONFIGURATION REGISTER

The host processor configures the R96DP transmitter by writing a control byte into the transmitter configuration register (0:6) in its interface memory space as shown in the following table:

Transmitter Configuration Register (0:6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TNXMT	0	TLTS	TV29	X	TDR3	TDR2	TDR1

Definition of Transmitter Configuration Terms:

TNXMT:	Tone Transmit
TLTS:	Transmitter Long Training Sequence
TV29:	Transmitter V.29 Configuration
TDR3:	Transmitter Data Rate 3 (Selects 9600 bps/V.29)
TDR2:	Transmitter Data Rate 2 (Selects 7200 bps/V.29, and Selects 4800 bps/V.27)
TDR1:	Transmitter Data Rate 1 (Selects 4800 bps/V.29, and Selects 2400 bps/V.27)

Control bytes for the three configurations are given in hexadecimal format in the following table:

Configuration Control Bytes

No.	Configuration	Configuration Bytes (HEX)
1	V.29 9600	14
	V.29 7200	12
	V.29 4800	11
2	V.27 4800 Long	22
	V.27 2400 Long	21
	V.27 4800 Short	02
	V.27 2400 Short	01
3	Tone Transmit	80

Definition of Transmitter Configurations:

1. **V.29.** When any of the V.29 configurations have been selected, the modem operates as specified in CCITT recommendation V.29.
2. **V.27.** When any of the V.27 configurations have been selected, the modem operates as specified in CCITT recommendation V.27.
3. **Tone Transmit.** In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by the user. Two registers in the host interface memory space contain the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents $0.146484 \text{ Hz} \pm 0.01\%$.

TRANSMITTER OPTION

The host processor conveys option information to the transmitter by writing a control byte into the Option Register (0:7) in its interface memory space as shown in the table below:

Transmitter Option Register (0:7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTS	TTDIS	SDIS	MHLD	EDIS	TPDM	XCEN	SEDT

Definition of Transmitter Option Terms:

RTS:	Request-to-Send
TTDIS:	Transmitter Training Disable
SDIS:	Scrambler Disable
MHLD:	Mark Hold
EDIS:	Echo Protector Disable
TPDM:	Transmitter Parallel Data Mode
XCEN:	External Clock Enable
SEDT:	Short Echo Protection Disable Tone

Definition of Transmitter Options:

1. **Request-to-Send.** The R96DP begins a transmit sequence when the RTS bit (0:7:7) is turned on and continues transmitting until RTS is turned off and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input.
2. **Transmitter Training Disable.** When the TTDIS bit (0:7:6) is on, the transmitter does not generate a training sequence at the start of transmission.
3. **Scrambler Disable.** When the SDIS bit (0:7:5) is on, the transmitter scrambler circuit is removed from the data path.
4. **Mark Hold.** When the MHLD bit (0:7:4) is on, the transmitter input data stream is forced to all marks (1's).
5. **Echo Protector Disable.** When the EDIS bit (0:7:3) is on, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission. Note that this option is available in both V.27 and V.29 configurations although it is not specified in the CCITT V.29 recommendation.

6. **Transmitter Parallel Data Mode.** When the TPDM bit (0:7:2) is on, the transmitter accepts data for transmission from the data input register rather than the serial hardware data input.
7. **External Clock Enable.** When the XCEN bit (0:7:1) is on, the transmitter timing is established by the external clock supplied at the hardware input XTCLK (pin 22A).
8. **Short Echo Protector Disable Tone.** When the SEDT bit (0:7:0) is on, the echo protector disable tone is 30 ms long rather than 185 ms.

EQUALIZER

The host processor conveys equalizer selection information to the modem by writing a control byte into the equalizer register (0:5) in the interface memory space as shown in the following:

Equalizer Register (0:5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	CABS2	CABS1	LAEN	LDEN	A3L	D3L

Definition of Equalizer Terms:

CABS1,2: Cable Equalizer (Selects bits 1 or 2)
LAEN: Link Amplitude Equalizer Enable
LDEN: Link Delay Equalizer Enable
A3L: Amplitude 3-Link Select
D3L: Delay 3-Link Select

Definition of Equalizer Parameters:

1. **Cable Equalizer.** The cable equalizer select bits simultaneously control amplitude and delay compromise equalizers in both the transmit and receive paths. The following table gives the possible bit combinations.

Cable (0.4 mm diameter) Equalizer Selection

CABS2	CABS1	Cable Length
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

2. **Link Equalizer.** The link equalizer enable and select bits control separate amplitude and delay compromise equalizers in the receive path. The following tables give the possible bit combinations.

Link Amplitude Equalizer Selection

LAEN	A3L	Curve Matched
0	X	No Equalizer
1	0	U.S. Survey Long
1	1	Japanese 3-Link

Link Delay Equalizer Selection

LDEN	D3L	Curve Matched
0	X	No Equalizer
1	0	U.S. Survey Long
1	1	Japanese 3-Link

LOOP/LEVEL

The host processor conveys loopback selection and transmitter output level to the modem by writing a control byte into the loop/level register (0:4) in the interface memory space as shown in the following table:

Loop/Level Register (0:4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L3ACT	L4ACT	L4HG	TL3	TL2	TL1	L2ACT	X

Definition of Loop/Level Terms:

L3ACT: Local Analog Loopback (CCITT loop 3) Activate
L4ACT: Remote Analog Loopback (CCITT loop 4) Activate
L4HG: Loop 4 High Gain
TL3-TL1: Transmitter Level (Selects bits 3, 2, and 1)
L2ACT: Remote Digital Loopback (CCITT loop 2) Activate

Definition of Loop/Level Control:

1. **Local Analog Loopback Activate.** When the L3ACT bit (0:4:7) is on, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT recommendation V.54 loop 3.
2. **Remote Analog Loopback Activate.** When the L4ACT bit (0:4:6) is on, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier.
3. **Loop 4 High Gain.** When the L4HG bit (0:4:5) is on, the loop 4 variable gain amplifier is set for +16 dB. When L4HG is off, the gain is 0 dB.
4. **Remote Digital Loopback Activate.** When the L2ACT bit (0:4:1) is on, the receiver digital output is connected to the transmitter digital input in accordance with CCITT recommendation V.54 loop 2.
5. **Transmitter Level Select 3, 2 and 1.** Transmitter analog output level is determined by bits TL3, TL2, and TL1 as shown in the following table:

Transmitter Level Selection

TL3	TL2	TL1	Transmitter Analog Output
0	0	0	- 0.5 dBm \pm 0.5 dB*
0	0	1	- 2.5 dBm \pm 0.5 dB
0	1	0	- 4.5 dBm \pm 0.5 dB
0	1	1	- 6.5 dBm \pm 0.5 dB
1	0	0	- 8.5 dBm \pm 0.5 dB
1	0	1	- 10.5 dBm \pm 0.5 dB
1	1	0	- 12.5 dBm \pm 0.5 dB
1	1	1	- 14.5 dBm \pm 0.5 dB

*Each step is a 2 dB change \pm 0.2 dB

TRANSMITTER DATA

The host processor conveys output data to the transmitter in parallel mode by writing a data byte to the transmitter Data Register (0:0) in the interface memory space. The data must be divided on integral baud boundaries as shown in the following table:

Transmitter Data Register (0:0)

Configuration	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
V.29 9600 bps	Baud 1				Baud 0			
V.29 7200 bps	X		Baud 1			Baud 0		
V.29 4800 bps	Baud 3		Baud 2		Baud 1		Baud 0	
V.27 4800 bps	X		Baud 1			Baud 0		
V.27 2400 bps	Baud 3		Baud 2		Baud 1		Baud 0	
NOTE: Data Transmitted Bit 0 First.								

FREQM/FREQL

The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQM/FREQL registers (0:3 and 0:2) in the interface memory space as shown in the following tables:

FREQM Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸

FREQL Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰

The frequency number (N) determines the frequency (F) as follows: $F = 0.146484N \text{ Hz} \pm 0.01\%$

Hexadecimal frequency numbers (FREQM, FREQL) for commonly generated tones are given in the following table:

Commonly Generated Tones

Frequency	FREQM	FREQL
462 Hz	0C	52
1100 Hz	1D	55
1650 Hz	2C	00
1850 Hz	31	55
2100 Hz	38	00

TRANSMITTER HANDSHAKE

The host processor performs a handshake sequence with the transmitter by controlling and testing bits in the transmitter handshake register (0:E) in the interface memory space as shown in the following table:

Transmitter Handshake Register (0:E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIA	X	X	X	TSB	TIE	X	TBA

Definition of Transmitter Handshake Terms:

TIA: Transmitter Interrupt Active
 TSB: Transmitter Setup Bit
 TIE: Transmitter Interrupt Enable
 TBA: Transmitter Buffer Available

Definition of Transmitter Handshake Sequences:

1. **Transmitter Buffer Available.** The TBA bit goes off when the host processor writes data to transmitter data register (0:0). When the transmitter empties register 0:0 the TBA bit is on.
2. **Transmitter Interrupt Enable.** When the host processor writes a 1 in the TIE bit, the IRQ line of the hardware interface is driven low when TBA is on.
3. **Transmitter Interrupt Active.** Status bit TIA is on whenever the transmitter is driving IRQ low.
4. **Transmitter Setup Bit.** When the host processor changes the transmitter configuration register, the host must write a 1 in the TSB bit. Bit TSB goes to 0 when the change becomes effective.

RECEIVER CONFIGURATION

The host processor configures the receiver by writing a control byte into the receiver configuration register (1:6) in the interface memory space as shown in the following table:

Receiver Configuration Register (1:6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	RLTS	RV29	X	RDR3	RDR2	RDR1

Definition of Receiver Configuration Terms:

RLTS: Receiver Long Training Sequence
 RV29: Receiver V.29 Configuration
 RDR3: Receiver Data Rate 3 (Selects 9600 bps/V.29)
 RDR2: Receiver Data Rate 2 (Selects 7200 bps/V.29 and Selects 4800 bps/V.27)
 RDR1: Receiver Data Rate 1 (Selects 4800 bps/V.29 and Selects 2400 bps/V.27)

Control words for the two receiver configurations are given in hexadecimal format in the following table:

Receiver Configuration Control

No.	Configuration	Configuration Word (HEX)
1	V.29 9600	14
	V.29 7200	12
	V.29 4800	11
2	V.27 4800 Long	22
	V.27 2400 Long	21
	V.27 4800 Short	02
	V.27 2400 Short	01

Definition of Receiver Configurations:

1. **V.29.** When any of the V.29 configurations has been selected, the transmitter operates as specified in CCITT recommendation V.29.
2. **V.27.** When any of the V.27 configurations has been selected, the transmitter operates as specified in CCITT recommendation V.27.

RECEIVER OPTION

The host processor conveys option information to the transmitter by writing a control byte into the option register (1:7) in its interface memory space as shown in the following table:

Receiver Option Register (1:7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTH2	RTH1	DDIS	RPDM	SWRT	BWRT	T2	RTDIS

Definition of Receiver Option Terms:

- RTH2, 1:** Receiver Energy Detector Threshold (Bits 2 and 1)
DDIS: Descrambler Disable
RPDM: Receiver Parallel Data Mode
SWRT: Sample Write
BWRT: Baud Write
T2: T/2 Equalizer Select
RTDIS: Receiver Training Disable

Definition of Receiver Options:

1. **Receiver Energy Detector Threshold (Bits 2 and 1).** The receiver energy detector threshold is set by bits RTH2 and RTH1 according to the following table:

Receiver Energy Detect Thresholds

RTH2	RTH1	RLSD On	RLSD Off
0	0	> -43 dBm	< -48 dBm
0	1	> -33 dBm	< -38 dBm
1	0	> -26 dBm	< -31 dBm
1	1	> -16 dBm	< -21 dBm

2. **Descrambler Disable.** When the DDIS bit (1:7:5) is on, the receiver descrambler circuit is removed from the data path.
3. **Receiver Parallel Data Mode.** When the RPDM bit (1:7:4) is on, the receiver supplies data to the receiver data register (1:0) in parallel with the hardware serial data output.
4. **Sample Write.** When the SWRT bit (1:7:3) is on, the 16-bit word in registers 1:1 and 1:0 is written in the RAM location specified by the contents of register 1:4.
5. **Baud Write.** When the BWRT bit (1:7:2) is on, the 16-bit word in locations 2:1 and 2:0 is written in the RAM location specified by the contents of register 2:4.

6. **T/2 Equalizer Select.** When the T2 bit (1:7:1) is on, an adaptive equalizer with two taps per baud is used. When T2 is off the equalizer has one tap per baud.
7. **Receiver Training Disable.** When the RTDIS bit (1:7:0) is on, the receiver is prevented from recognizing a training sequence.

RECEIVER SAMPLE HANDSHAKE

The host processor performs a handshake sequence with the receiver sample rate device by controlling and testing bits in the receiver sample handshake register (1:E) in the interface memory space as shown in the following table:

Receiver Sample Handshake Register (1:E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSIA	X	X	X	RSSB	RSIE	X	RSDA

Definition of Receiver Sample Handshake Terms:

- RSIA:** Receiver Sample Interrupt Active
RSSB: Receiver Sample Setup Bit
RSIE: Receiver Sample Interrupt Enable
RSDA: Receiver Sample Data Available

Definition of Receiver Sample Handshake Sequence:

1. **Receiver Sample Data Available.** The RSDA bit goes on when the receiver writes data into the receiver data register (1:0). The bit goes off when the host processor reads data from register 1:0.
2. **Receiver Sample Interrupt Enable.** When the host processor writes a 1 in the RSIE bit, the IRQ line of the hardware interface is driven low when RSDA is on.
3. **Receiver Sample Interrupt Active.** Status bit RSIA is on whenever the Receiver Sample rate device is driving IRQ low.
4. **Receiver Setup Bit.** When the host processor changes the receiver configuration or bits 6 or 7 in the option register, the host must write a 1 in the RSB bit. Bit RSB goes to 0 when the changes become effective.

RECEIVER BAUD HANDSHAKE

The host processor performs a handshake sequence with the receiver baud rate device by controlling and testing bits in the receiver baud handshake register (2:E) in the interface memory space as shown in the following table:

Receiver Baud Handshake Register (2:E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBIA	X	X	X	X	RBIE	X	RBD A

Definition of Receiver Baud Handshake Terms:

RBIA: Receiver Baud Interrupt Active
 RBIE: Receiver Baud Interrupt Enable
 RBDA: Receiver Baud Data Available

Definition of Receiver Baud Handshake Sequence:

1. *Receiver Baud Data Available.* The RBDA bit goes on when the receiver writes data into register (2:0). The bit goes off when the host processor reads data from register 2:0.
2. *Receiver Baud Interrupt Enable.* When the host processor writes a 1 in the RBIE bit, the IRQ line of the hardware interface is driven low when RBDA is on.
3. *Receiver Baud Interrupt Active.* Status bit RBIA is on whenever the receiver baud rate device is driving $\overline{\text{IRQ}}$ low.

RECEIVER SAMPLE STATUS

The host processor has access to various status bits that reflect operation of the receiver sample rate device. These bits can be tested by the host by reading the receiver sample status word (1:8 and 1:9) in the interface memory space as shown in the following tables:

Receiver Sample Status Register 1 (1:8)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	P2DET	X	X

Receiver Sample Status Register 2 (1:9)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	FED	X	X	X	X	X	X

Definition of Receiver Sample Status Terms:

P2DET: Period Two Detector
 FED: Fast Energy Detector

Definition of Receiver Sample Status Conditions:

1. *Period Two Detector.* When the P2DET bit (1:8:2) is off, it indicates that a P2 sequence has been detected. This bit sets to a 1 at the start of the receive data state.
2. *Fast Energy Detector.* When the FED bit (1:9:6) is off, it indicates that energy above the receiver threshold is present in the passband.

RECEIVER BAUD STATUS

The host processor has access to status bits that reflect operation of the receiver baud rate device. These bits can be tested by the host by reading the receiver baud status word (1:B) in the interface memory space as shown in the following table:

Receiver Baud Status Register (1:B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	PNDET	X	X	X	X	X	CDET

Definition of Receiver Baud Status Terms:

PNDET: Period N Detector
 CDET: Carrier Detector

Definition of Receiver Baud Status Conditions:

1. *Period N Detector.* When the PNDET bit (1:B:6) is off, it indicates a PN sequence has been detected. This bit sets to a 1 at the end of the PN sequence.
2. *Carrier Detector.* When the CDET bit (1:B:0) is off, it indicates that passband energy is being detected and that a training sequence is not in process. It goes off at start of data state and goes to a 1 at end of received signal.

RECEIVER DATA

The host processor accepts input data from the receiver in parallel mode by reading a byte from the receiver data register (2:0) in the interface memory space. The data is divided on integral baud boundaries identical to the transmitter data register with bit 0 received first. Note that the receiver data register is used for diagnostic data in the serial mode.

DIAGNOSTIC CAPABILITIES

The R96DP provides the user with access to much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

HARDWARE DIAGNOSTIC CIRCUITS

Signal names and descriptions of the hardware diagnostic circuits are given in the following table:

Hardware Diagnostic Circuits

Name	I/O	Pin No.	Description
EYEX	0	15C	Eye Pattern Data — X Axis
EYEX	0	14A	Eye Pattern Data — Y Axis
EYECLK	0	14C	Eye Pattern Clock
EYESYNC	0	13A	Eye Pattern Synchronizing Signal

Eye Pattern Generation — The four hardware diagnostic circuits allow the user to generate and display an eye pattern. Circuits EYEX and EYEW serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the rising edge of the EYECLK output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

SOFTWARE DIAGNOSTIC CIRCUITS

Each receiver device (sample rate and baud rate) contains six registers in the interface memory space dedicated to reading and writing modem RAM locations from the host processor bus. Four of these registers are organized into 2-byte data words and the remaining two registers form 1-byte control registers that hold RAM access codes. Data is read from RAM into the data registers. Data is written into RAM from the data registers. The RAM location involved in the data transfer is specified by the RAM access code stored in the associated diagnostic control register. The diagnostic registers are related as shown in the following table:

Software Diagnostic Registers

Device	Control Register	Write Bit	Data Word (MSB)	Data Word (LSB)
Sample	XS (1:5)	None	XSM (1:3)	XSL (1:2)
Sample	YS (1:4)	SWRT (1:7:3)	YSM (1:1)	YSL (1:0)*
Baud	XB (2:5)	None	XBM (2:3)	XBL (2:2)
Baud	YB (2:4)	BWRT (1:7:2)	YBM (2:1)	YBL (2:0)

*In parallel mode, register 1:0 is used for receive data and not diagnostic data.

Data transfer is regulated by the appropriate data available bit. Reading always takes place at the designated rate, and data left in the data registers is overwritten each cycle. When the associated write bit is set, a write cycle is performed each time the associated data available bit is off.

The eight bits of registers 2:3 and 2:1 are continuously presented serially on hardware interface lines EYEX and EYEW respectively.

RAM ACCESS CODES

The following table lists access codes for frequently used RAM data:

RAM Access Codes

Bank	Function	Real Access	Imag. Access
1	Received Signal Samples	C0	—
	Demodulator Output	C2	42
	Low Pass Filter Output	D4	54
	One Baud Energy	—	04
	AGC Gain Word — MSB's	81	—
	AGC Gain Word — LSB's	—	01
2	Equalizer Input	C0	40
	Equalizer Tap Coefficients	81-A0	01-20
	Unrotated Equalizer Output	E1	61
	Rotated Equalizer Output (Received Points)	A2	22
	Decision Points (Ideal Data Points)	E2	62
	Error	E3	63
	Rotation Angle	—	00
	Frequency Correction (MSB's)	AA	—
	Frequency Correction (LSB's)	—	2A
	EQM	2B	—

POWER-ON INITIALIZATION

When power is applied to the R96DP, a period of 100 to 300 ms is required for initialization. The power-on-reset signal (POR) remains low during the initialization period. After the low to high transition of POR, the modem is ready to operate. At POR time the modem defaults to the following configuration: V.29, 9600 bps, T/2, long echo protect disable tone, serial data mode, internal clock, cable select 1.8 Km, amplitude and delay equalizers enabled and Japanese 3 link curves selected, transmitter output level set to $-0.5 \text{ dBm} \pm 0.5 \text{ dB}$, interrupts disabled, and receiver threshold set to -43 dBm .

POR can also be used to initialize the users's host processor. It may be connected to a user supplied power-on-reset signal in a wire-or configuration.

PERFORMANCE

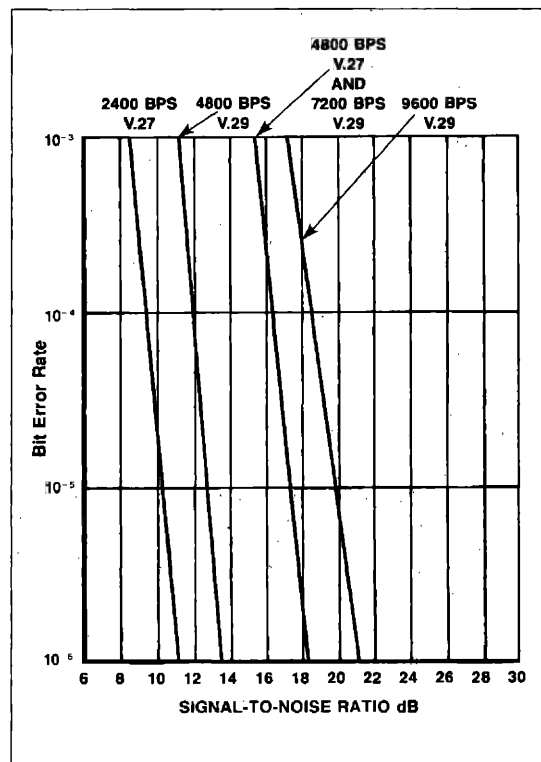
Whether functioning as a V.27 bis/ter or V.29 type modem, the R96DP provides the user with unexcelled high performance.

Bit Error Rates — The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of -40 dBm as illustrated.

Phase Jitter — At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

10

At 4800 bps (V.27 bis/ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.



Typical Bit Error Rate Performance

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 60° peak-to-peak phase jitter at 30 Hz.

INTERFACE CIRCUIT CHARACTERISTICS

DIGITAL INTERFACE CIRCUITS

Digital Input Characteristics

Input Logic State	Allowed Input Voltage Levels
Low	0.0V to +0.8V at $-2.5 \mu\text{A}$
High	+2.0V to +5.0V at $+2.5 \mu\text{A}$

Notes

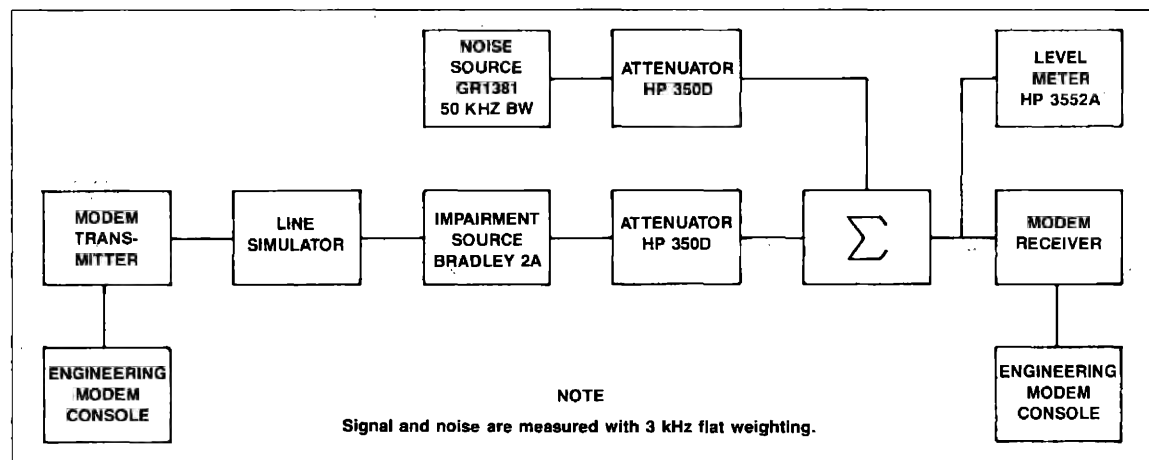
1. The digital inputs are directly TTL/CMOS compatible. The capacitive loading on each input is 25 pF (maximum).
2. Positive current is defined as current into the node.

Digital Output Characteristics

Output Logic State	Output Voltage Level
Low	+0.4V at +1.6 mA
High	+2.4V at $-100 \mu\text{A}$

Notes

1. The digital outputs are directly TTL/CMOS compatible. Capacitive drive capability is 25 pF.
2. Positive current is defined as current into the node.



NOTE

Signal and noise are measured with 3 kHz flat weighting.

BER Performance Test Set-up

ANALOG INTERFACE CIRCUITS

Transmitter Output Level — The transmitter output level is adjustable in 2 dB steps from -0.5 dBm to -14.5 dBm accurate to ± 0.5 dB. This level is measured at TXA into a 600 ohm impedance.

Receiver Input — The receiver input impedance is 63.4K ohm $\pm 5\%$.

Auxiliary Transmitter Input — The auxiliary transmitter input (AUXIN) allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, signals above 4800 Hz will cause aliasing errors. The input impedance is 1K ohm and the gain to transmitter output is 0dB.

R96DP SPECIFICATIONS

Power Requirements

Voltage	Tolerance	Current (Max)
+ 5 Vdc	$\pm 5\%$	<700 mA
+ 12 Vdc	$\pm 5\%$	<20 mA
- 12 Vdc	$\pm 5\%$	<80 mA

Note: All voltages must have ripple ≤ 0.1 volts peak-to-peak.

Environmental

Parameter	Specification
Temperature: Operating— Storage—	0°C to +60°C (32 to 140°F) -40°C to +90°C (-40 to 176°F) Stored in heat sealed antistatic bag and shipping container
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Mechanical Information

Parameter	Specification
Board Structure:	Single PC board with single right angle header with 64 pins, DIN 41612 or equivalent mating connector.
Dimensions:	Width—3.94 in. (100 mm) Length—4.70 in. (120 mm) Height—0.55 in. (1.40 cm)
Weight:	Less than .22 lbs. (.08 kg)



R96FT **9600 BPS FAST TRAIN MODEM**

PRELIMINARY

INTRODUCTION

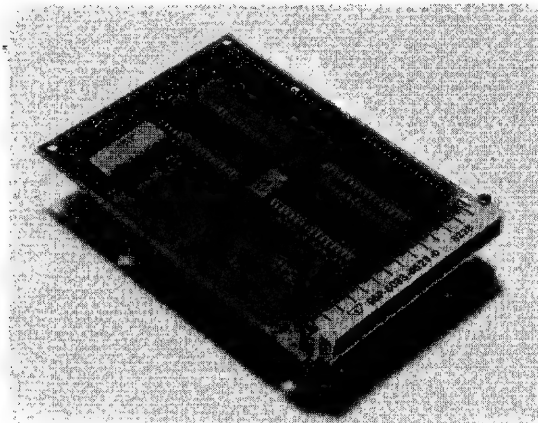
The R96 Fast Train (FT) is a synchronous, serial 9600/7200/4800/2400 bps modem suitable for operation over dedicated unconditioned lines. It satisfies the telecommunications requirements specified in CCITT Recommendations V.29 and V.27 bis/ter.

The R96FT is specifically optimized for use in a multipoint environment requiring a fast training sequence of less than 30 msec at 9600 bps and less than 20 msec at 4800 bps. The optional secondary channel, small size (100mm by 160mm), and low power consumption (4 watts typical) offer the user flexibility in creating a 9600 bps modem customized for specific packaging and functional requirements.

Data can be transferred to and from the modem either serially over the CCITT V.24 interface or in parallel over the microprocessor bus interface.

The R96FT is a member of Rockwell's family of plug compatible 9600/4800 bps modems.

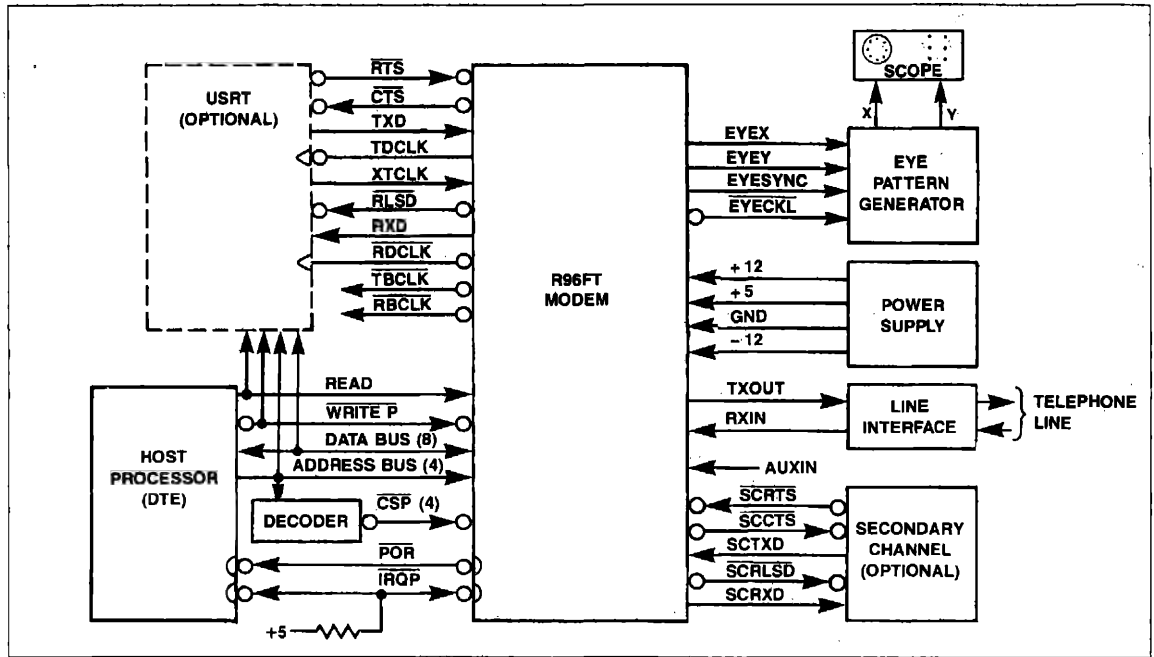
Product availability is winter, 1984.



R96FT Modem

FEATURES

- Configurations
 - CCITT V.29, V.27 bis/ter
- Fast Training Sequence <30 msec/9600 bps, <20 msec/4800 bps
- Ideal for Multipoint Applications
- Plug Compatible with Rockwell R96DP, R48DP Modems
- Secondary Channel (Optional) 110, 75 bps
- Dynamic Range: -43 dBm to 0 dBm
- Equalization
 - Automatic Adaptive
 - Compromise Cable (Selectable)
 - Compromise Link Amplitude (Selectable)
- DTE Interface: Two Alternate Ports
 - Microprocessor Bus
 - CCITT V.24 (RS-232-C Compatible)
- Diagnostics
 - Provides Telephone Line Quality Monitoring Statistics
- Programmable Transmit Output Level
- Loopbacks
 - Local Analog
 - Remote Analog (Locally Activated)
 - Remote Digital (Locally Activated)
- Small Size—100mm x 160mm (3.94" x 6.30")
- Power Consumption—5 Watts Typical
- TTL and CMOS Compatible



R96FT Functional Interconnect Diagram

SPECIFICATIONS

Power Requirements

+5 Vdc $\pm 5\%$ <900ma
 +12 Vdc $\pm 5\%$ <30ma
 -12 Vdc $\pm 5\%$ <130ma

Temperature: Operating 0 to 60°C

Storage -40 to 90°C

Relative Humidity: Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.



V96P/1 **HIGH SPEED 9600 BPS MODEM**

INTRODUCTION

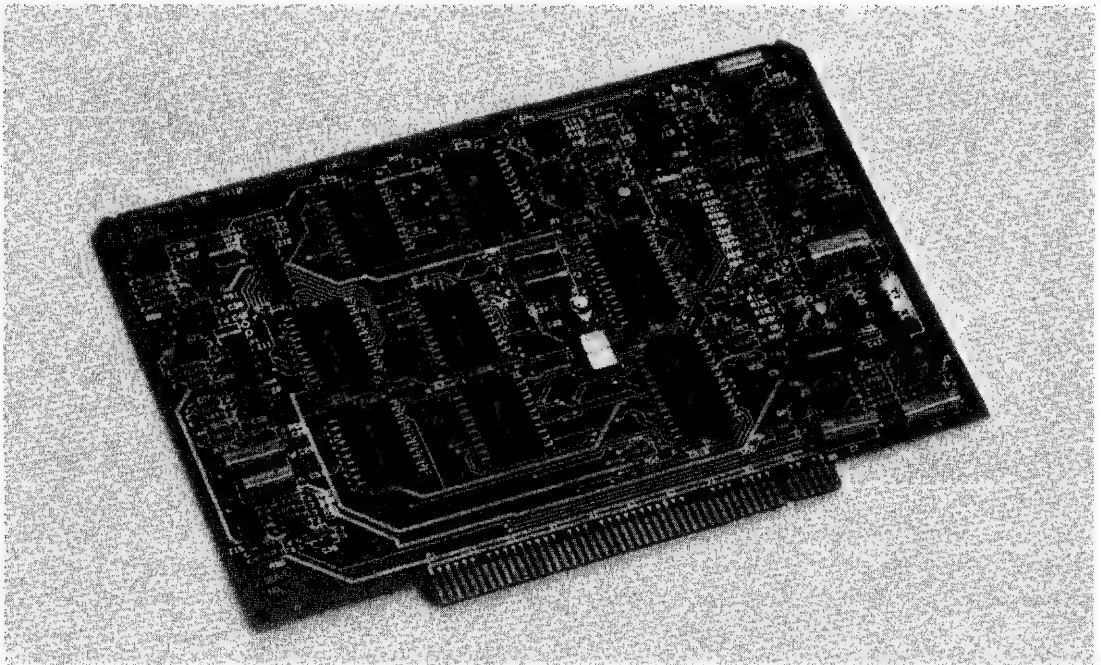
The Rockwell V96P/1 is a versatile, high performance, 9600 bps modem on a single printed circuit board. Being CCITT V.29 and V.27 compatible, the V96P/1 (with minimal interface circuitry) can operate on dedicated 2-wire or 4-wire half-duplex or 4-wire full-duplex lines. The V96P/1 can also operate in half-duplex on the general switched network.

Measuring approximately 9.2 inches (23.3 cm) by 6.3 inches (16.0 cm), the V96P/1 is the smallest full-feature 9600 bps modem that approaches data communication theoretical performance limits.

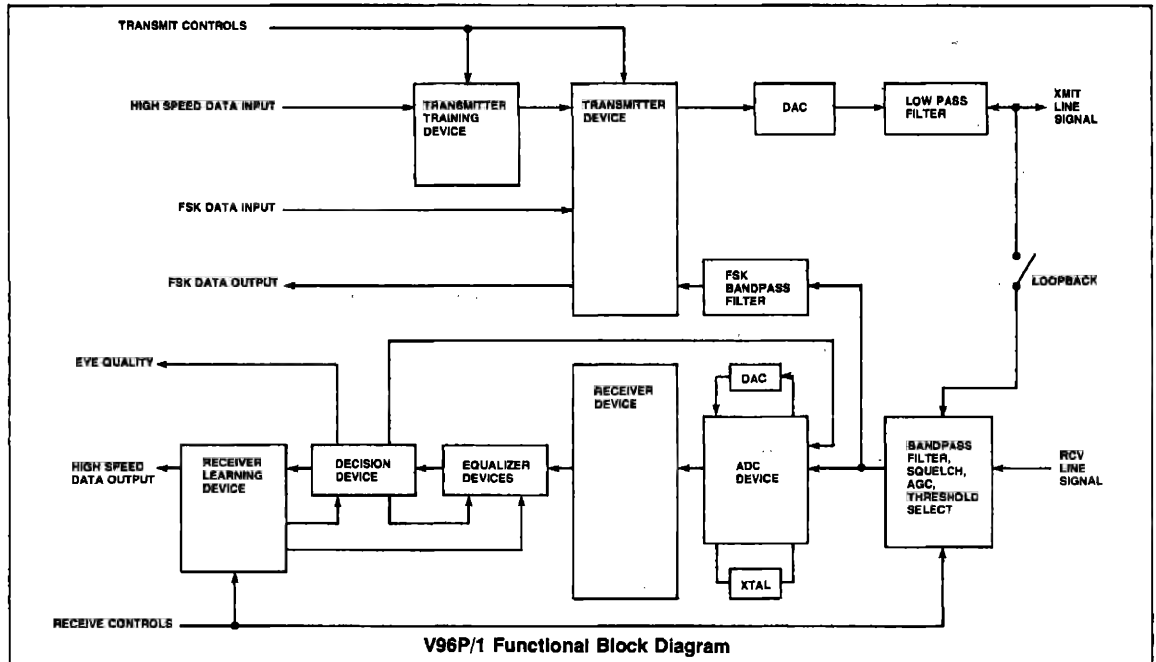
The V96P/1 meets the tolerances specified in the CCITT V.29, V.27 bis (alternate A), V.27 ter and FSK T.30 specifications. In addition, the V96P/1 can be configured to be functionally compatible with those enhanced specifications available in the Rockwell V96P, M96P, and V29P modem series.

FEATURES

- Single printed circuit card
- 9600/7200/4800/2400 bps modes
- Full-duplex or half-duplex
- Dedicated or general switched network lines operation
- Ultimate user flexibility:
 - CCITT V.29, V.27 ter, V.27 bis compatible
 - Also 300 bps binary signalling per CCITT T.30
- TTL compatibility
- Automatic adaptive equalizer
- Analog loopback test circuitry
- 0 to -45 dBm dynamic AGC
- LSI signal processing
- High reliability
- Low power consumption:
 - Typically 3.5 watts
- Automatic training sequence for receiver



FUNCTIONAL SPECIFICATIONS



V96P/1 Functional Block Diagram

Transmit Carrier and Signalling Frequencies

Carrier Frequency Codex	
Compatible QAM:	1706.667 Hz \pm 0.01%
Carrier Frequency V.29:	1700 Hz \pm 0.01%
Carrier Frequency V.27:	1800 Hz \pm 0.01%
Echo Suppression Frequencies:	2100 Hz \pm 0.01%
	2025 Hz \pm 0.01%
Signalling Frequencies of T.30:	1850 Hz \pm 0.01%
	1650 Hz \pm 0.01%
	1300 Hz \pm 0.01%
	1100 Hz \pm 0.01%

Received Signal Frequency Tolerance

The receiver can receive frequency errors of up to ± 10 Hz with less than a 0.2 dB degradation in Bit Error Rate performance.

Data Signalling and Modulation Rate

At 2400 baud:	
Signalling Rate—	2400 baud \pm 0.01%
Data Rate—	9600 bps \pm 0.01%
	7200 bps \pm 0.01%
	4800 bps \pm 0.01%
At 1600 baud:	
Signalling Rate—	1600 baud \pm 0.01%
Data Rate—	4800 bps \pm 0.01%
At 1200 baud:	
Signalling Rate—	1200 baud \pm 0.01%
Data Rate—	2400 bps \pm 0.01%

Transmitted Data Spectrum

At 2400 and 1600 baud the transmitted spectrum is shaped by approximately a square root of 50 percent raised cosine filter function. At 1200 baud the spectrum is shaped by approximately a square root of 90 percent raised cosine filter function.

The 2400 baud configurations require a line with typical 3002-C2 or M1020 characteristics over the frequency range from 450 Hz to 2950 Hz. The 1600 and 1200 baud rate configurations require a usable bandwidth from 950 Hz to 2650 Hz and 1150 Hz to 2450 Hz respectively.

Data Encoding

At 2400 baud the data stream is divided into groups of four bits (quadrants), three bits (tribits), or two bits (dibits). The data rate of 9600 bps, 7200 bps, or 4800 bps is selected by a 16-point, 8-point, or 4-point data structure, respectively. For 2400 baud operation, when V.29 configuration is selected, encoding of the quadrants, tribits, and dibits are per CCITT Recommendation V.29.

At 1600 baud the data stream is divided into groups of three bits (tribits). The data rate of 4800 bps may use either an 8-point QAM structure or 8-phase structure. Encoding of the tribits in the 8-phase structure are per CCITT Recommendation V.27 ter.

At 1200 baud the data stream is divided into groups of two bits (dibits). The data rate of 2400 bps uses a 4-phase data

structure. Encoding of the dibits may be per the fallback rate of CCITT Recommendation V.27 bis and ter (same as V.26A) or V26B depending on the selected configuration.

Turn-on, Turn-off Sequences

The V96P/1 turn-on sequences are compatible with CCITT Recommendations V.29, V.27 bis (alternate i), V.27 and Rockwell M96P modem specifications.

The turn-off sequences for all V.27 modes (except the 1600 baud rate manual V.27 mode) consists of 5 to 10 milliseconds of remaining data followed by continuous scrambled 1's followed by no transmission energy. The period of no transmission energy is provided by turning off the transmitter key signal for a recommended duration of 20 milliseconds.

The turn-off sequences for all non-V.27 modes consists of 4 to 7 milliseconds of remaining data followed by a period of no transmission energy.

Ready For Sending Response Times

The Ready For Sending response time to a Request To Send is determined by the configuration selected and its corresponding training time. In the following chart of configurations, the Training Times are shown in milliseconds. Note, however, that the 1600 baud manual CCITT configurations actually specify the synchronizing sequence timing per CCITT V.27 rather than the training time. Also note the following abbreviations.

ITC (1P-5P): Transmitter Configuration Inputs 1 through 5. These five bits establish the octal code shown where P1 and P2 are the most significant octal digit and P3 through P5 establish the least significant octal digit shown in the chart.

IRC (1P-5P): Receiver Configuration Inputs 1 through 5. These five bits establish the octal code shown where P1 and P2 are the most significant octal digit and P3 through P5 establish the least significant octal digit shown in the chart.

IRSS (1P-2P), ITSS (1P-2P): Receiver Signal Structure and Transmitter Signal Structure. Where P1 and P2 establish an octal code of 0, 1, 2, or 3. They define the signal structures as follows:

- 0 selects 16-point QAM
- 1 selects 8-point QAM
- 2 selects 4-point QAM
- 3 selects DPSK as:
 - 8-phase at 1600 baud
 - 4-phase at 1200 baud

Received Line Signal Detector (D109)

The time response of the Received Line Signal detector circuit (D109) is a function of the length of the received turn-on sequence. Circuit D109 turns on after synchronizing is completed and prior to user data appearing on the received output line. D109 turns on for approximately 2 milliseconds after the echo protect tone disappears in the V27EP configurations (Nos. 16, 18, 21, 23, 25, 29 and 32 in Table 1).

For non-CCITT configurations (Nos. 7, 8 and 9 in the table on page 4), D109 momentarily goes on at the beginning of the synchronizing sequence.

When no synchronizing signal is detected at the receiver, D109 turns on in 5 to 15 milliseconds for an applied signal greater than 3 dB above the turn-on threshold. If training is not enabled at the receiver, D109 turns on in 5 to 15 milliseconds.

Three threshold options are provided:

1) Greater than -43 dBm:	D109 ON
Less than -48 dBm:	D109 OFF
2) Greater than -26 dBm:	D109 ON
Less than -31 dBm:	D109 OFF
3) Greater than -16 dBm:	D109 ON
Less than -21 dBm:	D109 OFF

The three threshold options are controlled by the condition of the THRESH1 and THRESH2 control lines as indicated below.

dB Level	THRESH1	THRESH2
-43 dBm ON	Open Circuit	Open Circuit
-26 dBm ON	Open Circuit	0 to -0.5V
-16 dBm ON	0 to -0.5V	Open Circuit

When the received signal drops 5 dB below the D109 turn off threshold, D109 will turn off in 5 to 15 milliseconds. The condition of D109 between the selected turn-on and turn-off thresholds is not specified except that a hysteresis action of greater than 2 dB exists between the off-to-on and on-to-off transition levels.

Recommended circuits to control THRESH1 and THRESH2 input interface lines are shown in the diagrams on page 5 (A, B and C).

Bit Error Rates

The V96P/1 is thoroughly tested to guarantee Bit Error Rate (BER) performance under test conditions equivalent to CCITT Recommendation V.26. The test set-up used by Rockwell is shown in the BER Performance Test Set-up diagram.

The results of these BER performance tests are shown in the Typical Bit Error Rate Performance diagram.

V96P/1 Configurations

No.	Configuration	Transmitter ITC (1P-5P) (Octal Code)	Receiver IRC (1P-5P) (Octal Code)	Signal Structure IRSS (1P-2P) ITSS (1P-2P) (Octal Code)	Data Rate (bps)	Training Time (msec)	Carrier Frequency (Hz)
1.	2400 Baud DIAL	02	00	0,1,2		320	1706 2/3
2.	2400 Baud DIAL — T/2	02	01	0,1,2	9600	320	1706 2/3
3.	2400 Baud P-P	00	00	0,1,2	7200	280	1706 2/3
4.	2400 Baud P-P — T/2	00	01	0,1,2	4800	280	1706 2/3
5.	2400 Baud V29	01	02	0,1,2		233	1700
6.	2400 Baud V29 — T/2	01	03	0,1,2		233	1700
7.	1600 Baud DIAL, CCITT DIAL	22	22	1,3	4800	181	NOTE
8.	1600 Baud DIAL — T/2	22	36	1,3	4800	181	NOTE
9.	1600 Baud DIAL Slow	36	22	1,3	4800	221	NOTE
10.	1600 Baud P-P	20	20	1,3	4800	141	NOTE
11.	1600 Baud P-P — T/2	20	32	1,3	4800	141	NOTE
12.	1600 Baud Echo	34	34	1,3	4800	480	NOTE
13.	1600 Baud Manual CCITT	32	30	3	4800	20 (V.27 Sync Sequence)	1800
14.	1600 Baud Manual CCITT	30	30	3	4800	50 (V.27 Sync Sequence)	1800
15.	1600 Baud V27 DIAL/P-P	23	23	3	4800	708	1800
16.	1600 Baud V27 DIAL/P-P EP	27	23	3	4800	923	1800
17.	1600 Baud V27 DIAL/P-P — T/2	23	33	3	4800	708	1800
18.	1600 Baud V27 DIAL/P-P — T/2 EP	27	33	3	4800	923	1800
19.	1600 Baud V27 Multipoint — T/2	21	27	3	4800	50	1800
20.	1600 Baud V27 Resync (use with configuration 15)	21	25	3	4800	50	1800
21.	1600 Baud V27 Resync EP (use with configuration 16)	25	25	3	4800	265	1800
22.	1600 Baud V27 Resync — T/2 (use with configuration 17)	21	35	3	4800	50	1800
23.	1600 Baud V27 Resync — T/2 EP (use with configuration 18)	25	35	3	4800	265	1800
24.	1600 Baud V27 Echo	23	37	3	4800	708	1800
25.	1600 Baud V27 Echo EP	27	37	3	4800	923	1800
26.	1200 Baud DIAL	14	10	3	2400	170	1800
27.	1200 Baud P-P	10	10	3	2400	117	1800
28.	1200 Baud V27 DIAL/P-P	13	11	3	2400	943	1800
29.	1200 Baud V27 DIAL/P-P EP	17	11	3	2400	1158	1800
30.	1200 Baud V27 Multipoint	11	15	3	2400	66	1800
31.	1200 Baud V27 Resync (use with configuration 28)	11	13	3	2400	66	1800
32.	1200 Baud V27 Resync EP (use with configuration 29)	15	13	3	2400	281	1800

NOTE: Carrier frequency is 1706 2/3 Hz when IRSS (1P-2P) is a 1 (8-point).
Carrier frequency is 1800 Hz when IRSS (1P-2P) is a 3 (8-phase DPSK).

Data Scrambler Selection

The V96P/1 makes available to the user one CCITT V.29 compatible scrambler, five different period 127 scramblers (and descramblers), and a no-scramble option. These scramblers provide data transmitted by the V96P/1 with the degree of randomness necessary to ensure the continued convergence of all adaptive processes at the receiver. The seven possible scrambler configurations that are user software selectable are:

- Period 127 cryptographic
- Period 127 synchronizing
- CCITT period 127 self-synchronizing (compatible with CCITT Recommendation V.29)
- Period 8,388,607 self-synchronizing (compatible with CCITT Recommendation V.29)
- Period 127 self-synchronizing with 8-bit protection

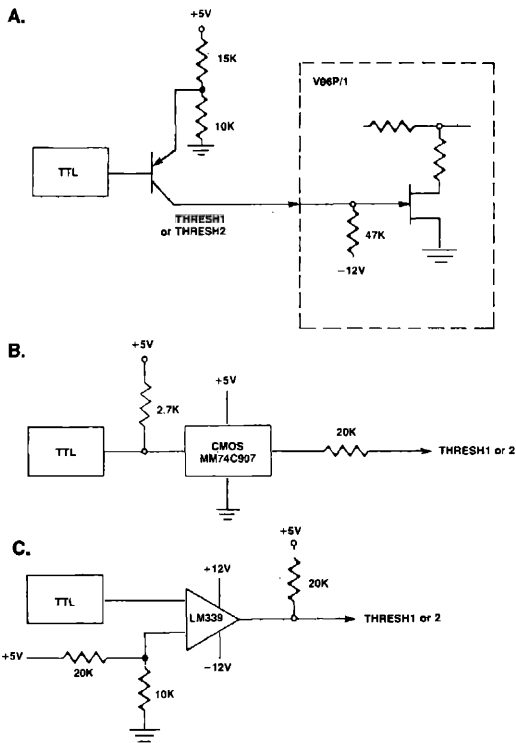
- CCITT period 127 self-synchronizing (compatible with CCITT Recommendations V.27 bis and ter)
- No scrambler

All scramblers can be used with all modem configurations listed in the above table except for the cryptographic scrambler which cannot be used in the CCITT V.29 configuration.

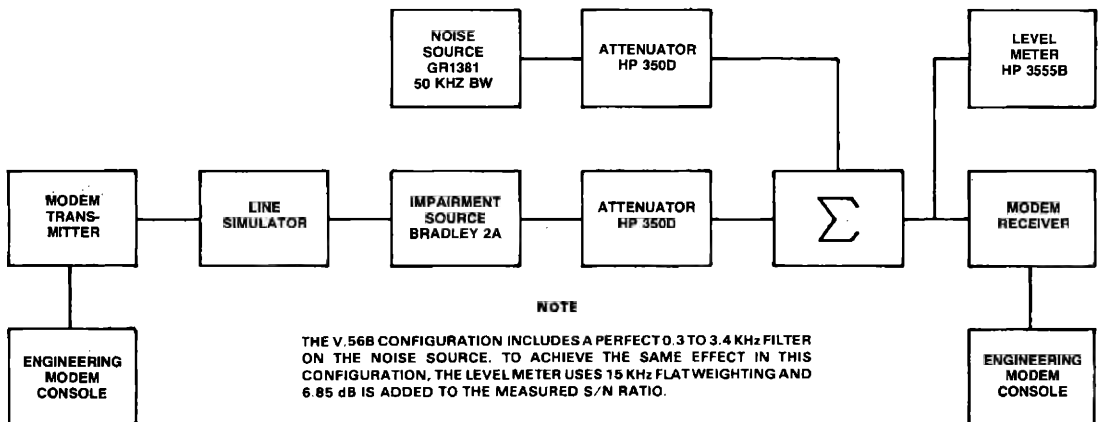
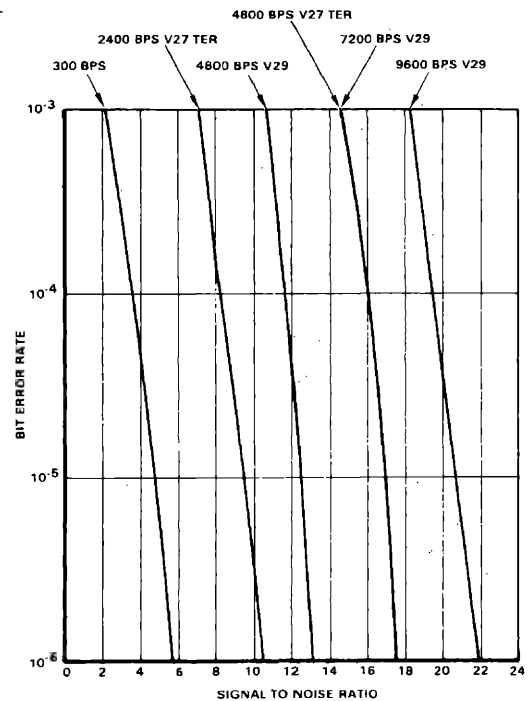
MODES OF OPERATION

The V96P/1 has two modes of operation; a training mode and a data mode. In order for the receiver to correctly decode the transmitted data, the V96P/1 must detect the presence of a line signal, adjust the AGC, detect the presence of a training sequence, recover the baud timing of the transmitter, phase and frequency lock to the carrier associated with the received signal, and adapt the equalizer to the amplitude and delay characteristics of the channel. This learning process is accomplished most efficiently when the transmitter initiates a training sequence whenever a new transmitter-receiver

10



Suggested Interface Circuits for Controlling THRESH1 and THRESH2 Input Lines



BER Performance Test Set-up

connection is made. It is possible to set up the receiver without a training sequence, but it is a manual mode requiring considerable user effort. In a training mode, an internal generated pattern is transmitted to the receiver to facilitate synchronization. During the training mode, the data input line to the receiver is ignored and the output line does not reflect the state of the data input.

In the data mode of operation, information on the data input is strobed by the transmitter signal element clock and transmitted to the receiver. The receiver demodulates and decodes the passband signal and outputs the recovered data on the output where it is then ready to be strobed by the receiver signal element clock.

Request To Send—Ready For Sending

To initiate transmitter operation in the data or training mode, the Request to Send input is brought high. If a training mode is not initiated, the Ready for Sending indicator goes high within one baud interval and data transmission commences.

The mode of the receiver is indicated by the data channel received line signal detector (D109). For data mode, D109 is high and the receiver training mode indicator is low.

If the receiver enters the training mode, the receiver training mode indicator goes high until the training mode is completed. When training is completed the receiver training mode indicator goes low and, if sufficient signal energy is present on the input line, D109 goes high, enabling the data mode.

Training Mode—Dial and Point-To-Point

For dial and point-to-point configurations, the V96P/1 receiver training is automatically initiated whenever a training sequence is detected in the received line signal. The training sequence consists of two phases: Phase 1 causes the training detector to turn on and also makes a coarse adjustment of the carrier frequency variable, which compensates for any frequency translation due to the channel; Phase 2 is used to converge the adaptive equalizer, which is part of the V96P/1 structure.

A short scrambler synchronization sequence follows Phase 2 and is used to generate the success indicator. In order for training to be successful, the incoming training sequence must have been generated by a similarly configured transmitter using a compatible training sequence.

At the receiver, detection of a training sequence requires that there be sufficient signal energy and that the receiver's carrier frequency variable be within 30 Hz of nominal.

Training Resync (V.27 bis/ter Turnaround)

In a 2-wire half-duplex data communication system, data can be transmitted in only one direction at any given instant. Therefore, the modems at the local and remote sites are required to interchange their roles as the receiver and the transmitter, respectively. This turnaround operation requires constant resynchronization to meet CCITT Recommendations for V.27 bis/ter.

The resync configurations are used for reacquiring synchronization in turnaround operation without having to go through the normal long training sequence. The resync training sequences are relatively short and are used for recovering carrier phase, symbol timing and achieving equalizer convergence without resetting carrier frequency and equalizer taps.

Training Mode—Multipoint

In the V96P/1 modem, two multipoint configurations are provided for 4-wire circuits conforming to M1020 which permit short training sequences. In these configurations, the first train signal must be high to process the short training sequences; otherwise the receiver will ignore the training sequence and enter directly into the data mode. The receiver will enter into the training mode if the first train signal is high and there is sufficient signal energy.

For 4-wire circuits which are worse than M1020 and for 2-wire circuits, a long training sequence should be used rather than the multipoint configuration. These training sequences require that the receiver be in the proper dial/point-to-point configuration.

Training Mode—Manual

The V96P/1 modem includes two manual configurations in which the remote modem need not transmit a special training sequence to the local receiver. In these configurations, the equalizer tap coefficients for the local receiver must be initialized from an external source. The tap coefficients may be initialized by controlling three input terms—ICR, ICI and ICLCP—in synchronization with the Baud Rate Clock.

In order to operate the modem in the manual configurations, both the transmitter and receiver must be set according to the code shown in Table 1 Modem Configuration. Manual configuration code octal 30 has a longer synchronizing sequence than configuration code octal 32, but both synchronizing sequences conform to the CCITT Recommendation V.27. However, neither sequence is of sufficient duration to aid in training the receiver.

Receiver Operation During Loss of Line Signal

When there is no line signal present, all receiver update relating to the equalizer, carrier frequency variable and baud timing are inhibited and the current values of the equalizer taps and the carrier frequency variable are retained.

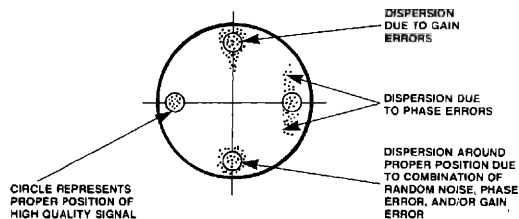
DATA QUALITY

The receiver generates an Eye Quality Monitor (EQM) signal that can be used to determine the equivalent Gaussian signal to noise ratio of the overall system within approximately \pm

2 db. Eye quality is determined by calculating the difference between the received signal point after equalization and the transmitted or expected signal point. The receiver output DEQ2P is a filtered version of this error signal. It is a serial word clocked by the system bit clock (345.6 kHz or 230.4 kHz, depending on baud rate). Output signal DQGTP is a gating signal which delineates the eight MSB's of DEQ2P. The use and interpretation of these binary signals are quite complex and are dependent on the application and the signal structure. The user can derive a meaningful interpretation of the EQM readings by monitoring them while testing the modem against his performance criteria.

Visual Display of Eye Pattern

A visual indication of the modem's performance can be obtained by displaying the received baseband signal structure after equalization. This is done by converting the eight MSB's of the real and imaginary equalized signal points available on DRERP and DIERP to analog voltages which are then used to drive the horizontal and vertical sweeps of an oscilloscope. The resultant display will be a symmetrical dot pattern of 16 points, 8 points, or 4 points which is a time representation of the received baseband signal. Any uncompensated distortion over the transmission path will cause each dot in the pattern to enlarge or otherwise show distortion. A typical visual eye pattern of a 4-point display is shown in the following diagram.



Typical Eye Pattern

Success Indicator

A second data quality indicator is provided for in all configurations except the 1200 baud non-V.27 modes. This signal provides a rough indication that the training has been successful and that data will be properly received. This "success" output (DSUCP) will go high during the last one to twenty milliseconds of receiver training, provided training has been successful. During the data mode (DRTMP low and D109 high), DSUCP will go high whenever 15 consecutive data marks or spaces are decoded at the receiver data output.

ADDITIONAL CAPABILITIES

The V96P/1 provides many additional capabilities germane to data communication system design and implementation. Capabilities such as local loopback, tone generation and detection, external clock facilities, and 300 bps FSK operation are briefly described in the following paragraphs.

Local Loopback Capability

A local loopback option is available for all half duplex and full duplex modem configurations. The Local Loopback Command (ILB) connects the transmitter's output through a buffer amplifier to the receiver input, thereby allowing a check of the local modem. The ILB command squelches the input to the receiver and loops the analog signal from the transmitter to the receiver input.

An internal pattern generator is also incorporated in the modem which can be used when no modem test set is available.

Tone Generation And Detection

The transmitter can be used to transmit single frequency tones for disabling echo suppressors or for system signaling. Tones that can be transmitted (selected through software control) are: 1100 Hz, 1300 Hz, 1650 Hz, 1850 Hz, 2025 Hz, and 2100 Hz. Other tones are also possible and the carrier frequency can be altered by selection of values for a binary bit stream.

External Data Clock

The data input to the transmitter can be clocked from an external source when the external clock is used as a reference input to the data clock's phase locked loop. By applying an external clock the reference input will cause the transmitter data clock to track the frequency and phase of the reference. The frequency of the reference clock must be within 100 ppm of nominal in order for the receiver's baud timing to properly track that of the transmitter. The reference clock can be equal to the nominal data clock frequency or be a subharmonic of it as long as the frequency tolerance is adhered to.

300 bps FSK Modem Operation

A CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 channel 2 modulation system can also be configured. The FSK modem is capable of generating the 1100, 1300, 1650 and 1850 Hz tones.

SPECIFICATIONS

V96P/1 Specifications

DC Voltages			
Voltage	Tolerance	Current (Typical)	Current (Max)
+ 5 volt	±5%	135 ma	<200 ma
+12 volt	±5%	40 ma	< 70 ma
-12 volt	±5%	175 ma	<230 ma
NOTE: All voltages must have ripple ≤0.1 volts peak-to-peak.			
Environment			
Temperature:	Operating: 0°C to +60°C (32 to 140°F) Storage: -40°C to +80°C (-40 to 176°F) (Stored in heat sealed antistatic bag and shipping container)		
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.		
Mechanical			
Board Structure:	Single PC board with edge connector		
Mating Connector:	100 pin, edge connector, two sided, with 0.1 in (2.54 cm) centers. Recommended Viking 3VH50/IJND5 or equivalent mating connector.		
Dimensions:	Width—9.188 in (23.338 cm) . Depth—6.288 in (15.972 cm)		
Weight:	Less than 0.45 lbs (0.20 kg)		



R48DP **4800 BPS DATA PUMP MODEM**

PRELIMINARY

INTRODUCTION

The Rockwell R48DP is a synchronous serial 4800 bps modem designed for full-duplex operation over either four-wire dedicated unconditioned lines or half-duplex operation over the general switched telephone network.

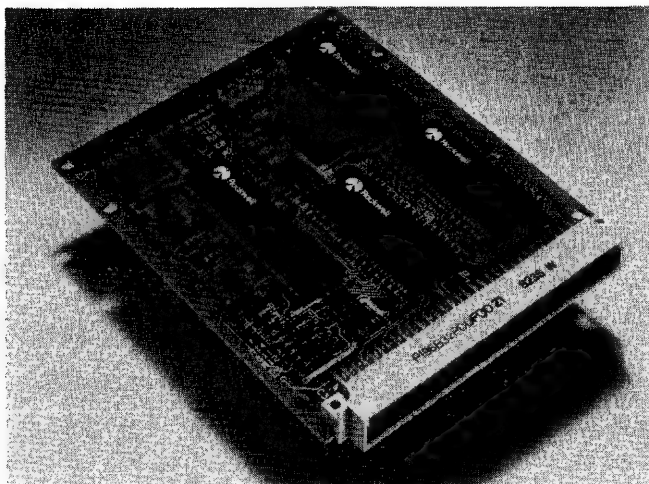
The modem satisfies telecommunications requirements specified in CCITT Recommendations V.27 bis/ter.

The small size and low power consumption of the modem offer the user flexibility in creating a 4800 bps modem design customized for specific packaging and functional requirements.

The modem is capable of operating at 4800 and 2400 bps.

FEATURES

- User Compatibility:
 - CCITT V.27 bis/ter
- Full-Duplex (4-Wire)
- Half-Duplex
- Programmable Tone Generation
- Dynamic Range -43 dBm to 0 dBm
- Diagnostic Capability
- Equalization:
 - Automatic Adaptive
 - Compromise Cable (Selectable)
 - Compromise Link (Selectable)
- DTE Interface:
 - Microprocessor Bus
 - CCITT V.24 (RS-232-C Compatible)
- Loopbacks (V.54 Loop 2, 3 and 4)
 - Local Analog
 - Remote Analog (Locally Activated)
 - Remote Digital (Locally Activated)
- Small Size — 100 mm × 120mm (4.0 × 4.8 inches)
- Low Power Consumption (3 watts, typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R48DP Modem

TECHNICAL SPECIFICATIONS

The following are the technical specifications for the R48DP modem.

TRANSMITTER CARRIER FREQUENCIES

The transmitter carrier frequencies are given in the following table:

Transmitter Carrier Frequencies

Frequency Type	Specification (Hz \pm 0.5 Hz)
V.27 bis/ter Carrier	1800

tone GENERATION

Under control of the host processor, the R48DP can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

SIGNALING AND DATA RATES

The signaling and data rates for the R48DP are defined in the table below:

Signaling/Data Rates

Parameter	Specification (\pm 0.01%)
Signaling Rate:	1600 Baud
Data Rate:	4800 bps
Signaling Rate:	1200 Baud
Data Rate:	2400 bps

DATA ENCODING

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 bis/ter.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 bis/ter.

EQUALIZERS

The R48DP provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. 1200 Baud. Square root of 90 percent
2. 1600 Baud. Square root of 50 percent

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R48DP incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with V.27 bis/ter.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R48DP can adapt to received frequency error of up to ± 10 Hz with less than 0.2 dB degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from 0 dBm to -43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

The R48DP provides a data derived Receive Data Clock (RDCLK) output in the form of a squarewave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a $\pm 0.01\%$ frequency error in the associated transmit timing source.

TRANSMIT LEVEL

The transmitter output level is accurate to ± 1.0 dB and is programmable from -1.0 dBm to -15.0 dBm in 2 dB steps.

TRANSMIT TIMING

The R48DP provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. Frequency. Selected data rate of 4800 or 2400 Hz ($\pm 0.01\%$).
2. Duty Cycle. 50% $\pm 1\%$

Input data presented on TXD is sampled by the R48DP at the low to high transition of TDCLK. Data on TXD must be stable for at least one microsecond prior to the rising edge of TDCLK and remain stable for at least one microsecond after the rising edge of TDCLK.

EXTERNAL TRANSMIT CLOCK

The transmitter data clock (TDCLK) can be phase locked to a signal on input XTCLK. This input signal must equal the desired data rate to $\pm 0.01\%$ with a duty cycle of $50\% \pm 20\%$.

TURN-ON SEQUENCE

A total of 8 selectable turn-on sequences can be generated as defined in the following table:

Turn-On Sequences

Performance Sequence			
No.	V.27 bis/ter	CTS Response Time (milliseconds)	Comments
1	4800 bps long	708	
2	2400 bps long	943	
3	4800 bps short	50	
4	2400 bps short	67	
5	4800 bps long	913	Preceded by Echo Suppressor Disable Tone for lines using echo suppressors*
6	2400 bps long	1148	
7	4800 bps short	255	
8	2400 bps short	272	
*For short echo protect tone, subtract 155 ms from values of CTS response time.			

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) whenever the Received Line Signal Detector (RLSD) is off.

RESPONSE TIMES OF CLEAR-TO-SEND (CTS)

The time between the off-to-on transition of Request-To-Send (RTS) and the off-to-on transition of CTS is dictated by the length of the training sequence and the echo suppressor disable tone, if used. These times are listed in the Turn-On Sequences table. If training is not enabled RTS/CTS delay is less than 1 ms.

The time between the on-to-off transition of RTS and the on-to-off transition of CTS in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR (RLSD)

For V.27 bis/ter, RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 15 ± 10 ms. The RLSD on-to-off response time for V.27 is 10 ± 5 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Four threshold options are provided:

1. Greater than -43 dBm (RLSD on)
Less than -48 dBm (RLSD off)
2. Greater than -33 dBm (RLSD on)
Less than -38 dBm (RLSD off)
3. Greater than -26 dBm (RLSD on)
Less than -31 dBm (RLSD off)
4. Greater than -16 dBm (RLSD on)
Less than -21 dBm (RLSD off)

NOTE

Performance may be at a reduced level when the received signal is less than -43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated carrier signal applied to the receiver's audio input (RXA).

MODES OF OPERATION

The R48DP is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

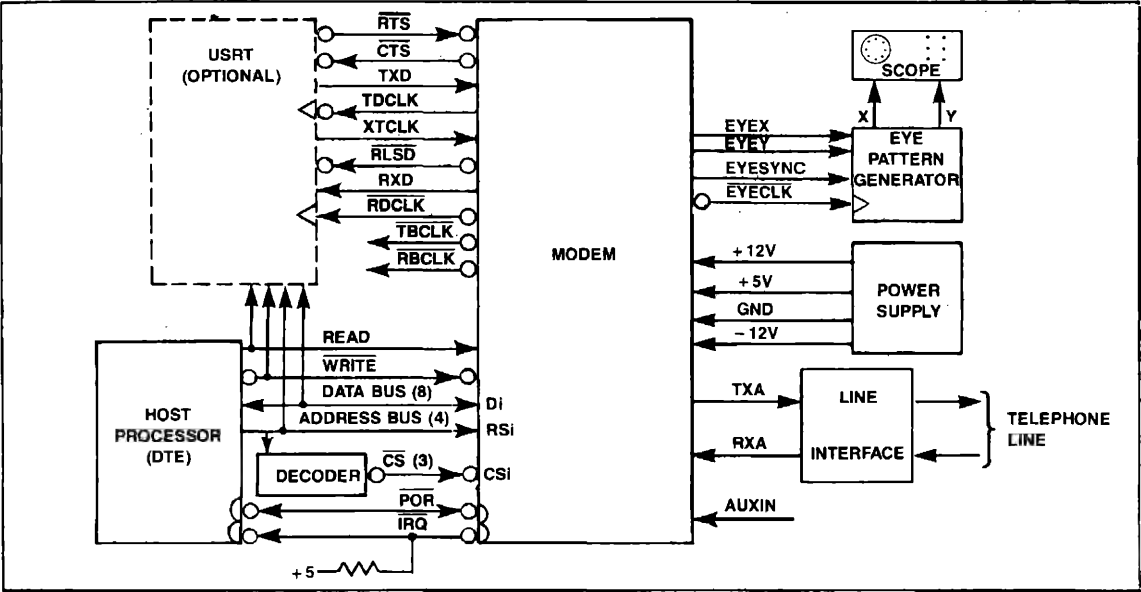
The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R48DP has the capability of transferring channel data up to eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the R48DP is configured by the host processor via the microprocessor bus.



R48DP Functional Interconnect Diagram

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 48-byte interface memory.

HARDWARE SUPERVISORY CIRCUITS

Signal names and descriptions of the hardware supervisory circuits, including the microprocessor interface, are listed in the R48DP Hardware Supervisory Circuits table. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R48DP Hardware Supervisory Circuits

Name	I/O	Pin No.	Description
A. OVERHEAD:			
AGND	I	31C,32C	Analog Ground
DGND	I	3C,8C,5A,10A	Digital Ground
+5 volts	I	19C,23C,26C,30C	+5 volt supply
+12 volts	I	15A	+12 volt supply
-12 volts	I	12A	-12 volt supply
POR	I/O	13C	Power-on-reset

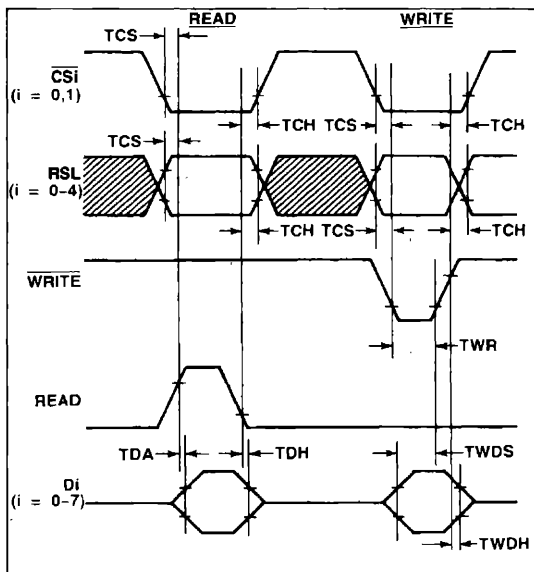
R48DP Hardware Supervisory Circuits (Cont.)

Name	I/O	Pin No.	Description
B. MICROPROCESSOR INTERFACE:			
D7	I/O	1C	Data Bus (8 Bits)
D6	I/O	1A	
D5	I/O	2C	
D4	I/O	2A	
D3	I/O	3A	
D2	I/O	4C	
D1	I/O	4A	
D0	I/O	5C	
RS3	I	6C	Register Select (4 Bits)
RS2	I	6A	
RS1	I	7C	
RS0	I	7A	
CS0	I	10C	Chip Select for Bank 0
CS1	I	9C	Chip Select for Bank 1
CS2	I	9A	Chip Select for Bank 2
READ	I	12C	Read Enable
WRITE	I	11A	Write Enable
IRQ	O	11C	Interrupt Request
C. V.24 INTERFACE:			
RDCLK	O	21A	Receive Data Clock
TDCLK	O	23A	Transmit Data Clock
XTCLK	I	22A	External Transmit Clock
RTS	I	25A	Request-to-Send
CTS	O	25C	Clear-to-Send
TXD	I	24C	Transmitter Data
RXD	O	22C	Receiver Data
RLSD	O	24A	Received Line Signal Detector

R48DP Hardware Supervisory Circuits (Cont.)

Name	I/O	Pin No.	Description
D. ANCILLARY CIRCUITS:			
RBCLK	O	26A	Receiver Baud Clock
TBCLK	O	27C	Transmitter Baud Clock
E. ANALOG SIGNALS:			
TXA	O	31A	Transmitter Analog Output
RXA	I	32A	Receiver Analog Input
AUXIN	I	30A	Auxiliary Analog Input

registers are collectively referred to as interface memory. See R48DP Interface Memory table. Access to the three banks of registers (bank 0, bank 1 and bank 2) is enabled by the Chip Select signals CS0, CS1 and CS2 respectively. Four Register Select signals (RS0, RS1, RS2, and RS3) are provided to address an individual register within an enabled bank. Registers in bank 1 operate at the sample rate of 9600 samples per second. Registers in banks 0 and 2 operate at the selected baud rate.



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
CSI, RSI setup time prior to Read or Write	TCS	30	—	nsec
Data access time after Read	TDA	—	140	nsec
Data hold time after Read	TDH	10	50	nsec
CSI, RSI hold time after Read or Write	TCH	10	—	nsec
Write data setup time	TWDS	75	—	nsec
Write data hold time	TWDH	10	—	nsec
Write strobe pulse width	TWR	75	—	nsec

INTERFACE MEMORY

The R48DP has three banks of 16 input/output (I/O) registers to which an external (host) microprocessor has access. Although these I/O registers are within the modem, they may be addressed as part of the host processor's memory space. These I/O

R48DP Interface Memory

Bank	(HEX) Reg No.	Description
0	F	Do Not Use
0	E	Transmitter Handshake
0	D	Do Not Use
0	C	Do Not Use
0	B	Do Not Use
0	A	Do Not Use
0	9	Do Not Use
0	8	Do Not Use
0	7	Transmitter Option
0	6	Transmitter Configuration
0	5	Equalizer
0	4	Loop/Level
0	3	FREQM
0	2	FREQI
0	1	Do Not Use
0	0	Transmitter Data
1	F	Do Not Use
1	E	Receiver Sample Handshake
1	D	Do Not Use
1	C	Do Not Use
1	B	Receiver Baud Status
1	A	Do Not Use
1	9	Receiver Sample Status 2
1	8	Receiver Sample Status 1
1	7	Receiver Option
1	6	Receiver Configuration
1	5	Diagnostic Control XS
1	4	Diagnostic Control YS
1	3	Diagnostic Data XSM
1	2	Diagnostic Data XSL
1	1	Diagnostic Data YSM
1	0	Diagnostic Data YSL; Receiver Data
2	F	Do Not Use
2	E	Receiver Baud Handshake
2	D	Do Not Use
2	C	Do Not Use
2	B	Do Not Use
2	A	Do Not Use
2	9	Do Not Use
2	8	Do Not Use
2	7	Do Not Use
2	6	Do Not Use
2	5	Diagnostic Control XB
2	4	Diagnostic Control YB
2	3	Diagnostic Data XBM
2	2	Diagnostic Data XBL
2	1	Diagnostic Data YBM
2	0	Diagnostic Data YBL

When information in these I/O registers is being discussed, the format Y:Z:Q is used. The bank is specified by Y(0-2), the register by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a 1.

SOFTWARE SUPERVISORY CIRCUITS

The operation of the R48DP is affected by a number of software control inputs. These inputs are written into registers within the modem via a microprocessor bus under external control. Bits designated by an X are "Don't Care" inputs that can be set to either 1 or 0. Modem operation is monitored by various software flags that are read from modem registers using the same microprocessor bus. Bits designated by an X are "undefined" outputs that may be either 1 or 0. The functions of all modem I/O registers are listed in the R48DP Interface Memory table and are defined as follows:

TRANSMITTER CONFIGURATION REGISTER

The host processor configures the R48DP transmitter by writing a control byte into the transmitter configuration register (0:6) in its interface memory space as shown in the following table:

Transmitter Configuration Register (0:6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TNXMT	0	TLTS	X	X	X	TDR2	TDR1

Definition of Transmitter Configuration Terms:

- TNXMT:** Tone Transmit
TLTS: Transmitter Long Training Sequence
TDR2: Transmitter Data Rate 2
 Selects 4800 bps/V.27
TDR1: Transmitter Data Rate 1
 Selects 2400 bps/V.27

Control bytes for the three configurations are given in hexadecimal format in the following table:

Configuration Control Bytes

No.	Configuration	Configuration Bytes (HEX)
1	V.27 4800 Long	22
	V.27 2400 Long	21
	V.27 4800 Short	02
	V.27 2400 Short	01
2	Tone Transmit	80

Definition of Transmitter Configurations:

- V.27.** When any of the V.27 configurations have been selected, the modem operates as specified in CCITT recommendation V.27.
- Tone Transmit.** In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by the user. Two registers in the host interface memory space contain the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents 0.146484 Hz \pm 0.01%.

TRANSMITTER OPTION

The host processor conveys option information to the transmitter by writing a control byte into the Option Register (0:7) in its interface memory space as shown in the table below:

Transmitter Option Register (0:7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTS	TTDIS	SDIS	MHLD	EDIS	TPDM	XCEN	SEDT

Definition of Transmitter Option Terms:

- RTS:** Request-to-Send
TTDIS: Transmitter Training Disable
SDIS: Scrambler Disable
MHLD: Mark Hold
EDIS: Echo Protector Disable
TPDM: Transmitter Parallel Data Mode
XCEN: External Clock Enable
SEDT: Short Echo Protection Disable Tone

Definition of Transmitter Options:

- Request-to-Send.** The R48DP begins a transmit sequence when the RTS bit (0:7) is turned on and continues transmitting until RTS is turned off and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input.
- Transmitter Training Disable.** When the TTDIS bit (0:7:6) is on, the transmitter does not generate a training sequence at the start of transmission.
- Scrambler Disable.** When the SDIS bit (0:7:5) is on, the transmitter scrambler circuit is removed from the data path.
- Mark Hold.** When the MHLD bit (0:7:4) is on, the transmitter input data stream is forced to all marks (1's).
- Echo Protector Disable.** When the EDIS bit (0:7:3) is on, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission.

6. *Transmitter Parallel Data Mode.* When the TPDM bit (0:7:2) is on, the transmitter accepts data for transmission from the data input register rather than the serial hardware data input.
7. *External Clock Enable.* When the XCEN bit (0:7:1) is on, the transmitter timing is established by the external clock supplied at the hardware input XTCLK (pin 22A).
8. *Short Echo Protector Disable Tone.* When the SEDT bit (0:7:0) is on, the echo protector disable tone is 30 ms long rather than 185 ms.

EQUALIZER

The host processor conveys equalizer selection information to the modem by writing a control byte into the equalizer register (0:5) in the interface memory space as shown in the following:

Equalizer Register (0:5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	CABS2	CABS1	LAEN	LDEN	A3L	D3L

Definition of Equalizer Terms:

CABS1,2: Cable Equalizer (Selects bits 1 or 2)
LAEN: Link Amplitude Equalizer Enable
LDEN: Link Delay Equalizer Enable
A3L: Amplitude 3-Link Select
D3L: Delay 3-Link Select

Definition of Equalizer Parameters:

1. *Cable Equalizer.* The cable equalizer select bits simultaneously control amplitude and delay compromise equalizers in both the transmit and receive paths. The following table gives the possible bit combinations.

Cable (0.4 mm diameter) Equalizer Selection

CABS2	CABS1	Cable Length
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

2. *Link Equalizer.* The link equalizer enable and select bits control separate amplitude and delay compromise equalizers in the receive path. The following tables give the possible bit combinations.

Link Amplitude Equalizer Selection

LAEN	A3L	Curve Matched
0	X	No Equalizer
1	0	U.S. Survey Long
1	1	Japanese 3-Link

Link Delay Equalizer Selection

LDEN	D3L	Curve Matched
0	X	No Equalizer
1	0	U.S. Survey Long
1	1	Japanese 3-Link

LOOP/LEVEL

The host processor conveys loopback selection and transmitter output level to the modem by writing a control byte into the loop/level register (0:4) in the interface memory space as shown in the following table:

Loop/Level Register (0:4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L3ACT	L4ACT	L4HG	TL3	TL2	TL1	L2ACT	X

Definition of Loop/Level Terms:

L3ACT: Local Analog Loopback (CCITT loop 3) Activate
L4ACT: Remote Analog Loopback (CCITT loop 4) Activate
L4HG: Loop 4 High Gain
TL3-TL1: Transmitter Level (Selects bits 3, 2, and 1)
L2ACT: Remote Digital Loopback (CCITT loop 2) Activate

Definition of Loop/Level Control:

1. *Local Analog Loopback Activate.* When the L3ACT bit (0:4:7) is on, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT recommendation V.54 loop 3.
2. *Remote Analog Loopback Activate.* When the L4ACT bit (0:4:6) is on, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier.
3. *Loop 4 High Gain.* When the L4HG bit (0:4:5) is on, the loop 4 variable gain amplifier is set for +16 dB. When L4HG is off, the gain is 0 dB.
4. *Remote Digital Loopback Activate.* When the L2ACT bit (0:4:1) is on, the receiver digital output is connected to the transmitter digital input in accordance with CCITT recommendation V.54 loop 2.
5. *Transmitter Level Select 3, 2 and 1.* Transmitter analog output level is determined by bits TL3, TL2, and TL1 as shown in the following table:

Transmitter Level Selection

TL3	TL2	TL1	Transmitter Analog Output
0	0	0	- 0.5 dBm \pm 0.5 dB*
0	0	1	- 2.5 dBm \pm 0.5 dB
0	1	0	- 4.5 dBm \pm 0.5 dB
0	1	1	- 6.5 dBm \pm 0.5 dB
1	0	0	- 8.5 dBm \pm 0.5 dB
1	0	1	- 10.5 dBm \pm 0.5 dB
1	1	0	- 12.5 dBm \pm 0.5 dB
1	1	1	- 14.5 dBm \pm 0.5 dB

*Each step is a 2 dB change \pm 0.2 dB

TRANSMITTER DATA

The host processor conveys output data to the transmitter in parallel mode by writing a data byte to the transmitter Data Register (0:0) in the interface memory space. The data must be divided on integral baud boundaries as shown in the following table:

Transmitter Data Register (0:0)

Configuration	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
V.27 4800 bps	X			Baud 1			Baud 0	
V.27 2400 bps		Baud 3		Baud 2		Baud 1		Baud 0

NOTE: Data Transmitted Bit 0 First.

FREQM/FREQL

The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQM/FREQL registers (0:3 and 0:2) in the interface memory space as shown in the following tables:

FREQM Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸

FREQL Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰

The frequency number (N) determines the frequency (F) as follows: $F = 0.146484N \text{ Hz} \pm 0.01\%$

Hexadecimal frequency numbers (FREQM, FREQL) for commonly generated tones are given in the following table:

Commonly Generated Tones

Frequency	FREQM	FREQL
462 Hz	0C	52
1100 Hz	1D	55
1650 Hz	2C	00
1850 Hz	31	55
2100 Hz	38	00

TRANSMITTER HANDSHAKE

The host processor performs a handshake sequence with the transmitter by controlling and testing bits in the transmitter handshake register (0:E) in the interface memory space as shown in the following table:

Transmitter Handshake Register (0:E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIA	X	X	X	TSB	TIE	X	TBA

Definition of Transmitter Handshake Terms:

TIA: Transmitter Interrupt Active

TSB: Transmitter Setup Bit

TIE: Transmitter Interrupt Enable

TBA: Transmitter Buffer Available

Definition of Transmitter Handshake Sequences:

1. *Transmitter Buffer Available.* The TBA bit goes off when the host processor writes data to transmitter data register (0:0). When the transmitter empties register 0:0 the TBA bit is on.
2. *Transmitter Interrupt Enable.* When the host processor writes a 1 in the TIE bit, the IRQ line of the hardware interface is driven low when TBA is on.
3. *Transmitter Interrupt Active.* Status bit TIA is on whenever the transmitter is driving IRQ low.
4. *Transmitter Setup Bit.* When the host processor changes the transmitter configuration register, the host must write a 1 in the TSB bit. Bit TSB goes to 0 when the change becomes effective.

RECEIVER CONFIGURATION

The host processor configures the receiver by writing a control byte into the receiver configuration register (1:6) in the interface memory space as shown in the following table:

Receiver Configuration Register (1:6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	RLTS	X	X	X	RDR2	RDR1

Definition of Receiver Configuration Terms:

RLTS: Receiver Long Training Sequence

RDR2: Receiver Data Rate 2
Selects 4800 bps/V.27)

RDR1: Receiver Data Rate 1
Selects 2400 bps/V.27)

Control words for receiver configuration are given in hexadecimal format in the following table:

Receiver Configuration Control

No.	Configuration	Configuration Word (HEX)
1	V.27 4800 Long	22
	V.27 2400 Long	21
	V.27 4800 Short	02
	V.27 2400 Short	01

Definition of Receiver Configurations:

When any of the V.27 configurations has been selected, the transmitter operates as specified in CCITT recommendation V.27.

RECEIVER OPTION

The host processor conveys option information to the transmitter by writing a control byte into the option register (1:7) in its interface memory space, as shown in the following table:

Receiver Option Register (1:7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTH2	RTH1	DDIS	RPDM	SWRT	BWRT	T2	RTDIS

Definition of Receiver Option Terms:

RTH2, 1: Receiver Energy Detector Threshold (Bits 2 and 1)
DDIS: Descrambler Disable
RPDM: Receiver Parallel Data Mode
SWRT: Sample Write
BWRT: Baud Write
T2: T/2 Equalizer Select
RTDIS: Receiver Training Disable

Definition of Receiver Options:

1. **Receiver Energy Detector Threshold (Bits 2 and 1).** The receiver energy detector threshold is set by bits RTH2 and RTH1 according to the following table:

Receiver Energy Detect Thresholds

RTH2	RTH1	RLSD On	RLSD Off
0	0	> -43 dBm	< -48 dBm
0	1	> -33 dBm	< -38 dBm
1	0	> -26 dBm	< -31 dBm
1	1	> -16 dBm	< -21 dBm

2. **Descrambler Disable.** When the DDIS bit (1:7:5) is on, the receiver descrambler circuit is removed from the data path.
3. **Receiver Parallel Data Mode.** When the RPDM bit (1:7:4) is on, the receiver supplies data to the receiver data register (1:0) in parallel with the hardware serial data output.
4. **Sample Write.** When the SWRT bit (1:7:3) is on, the 16-bit word in registers 1:1 and 1:0 is written in the RAM location specified by the contents of register 1:4.
5. **Baud Write.** When the BWRT bit (1:7:2) is on, the 16-bit word in locations 2:1 and 2:0 is written in the RAM location specified by the contents of register 2:4.

6. **T/2 Equalizer Select.** When the T2 bit (1:7:1) is on, an adaptive equalizer with two taps per baud is used. When T2 is off the equalizer has one tap per baud.

7. **Receiver Training Disable.** When the RTDIS bit (1:7:0) is on, the receiver is prevented from recognizing a training sequence.

RECEIVER SAMPLE HANDSHAKE

The host processor performs a handshake sequence with the receiver sample rate device by controlling and testing bits in the receiver sample handshake register (1:E) in the interface memory space as shown in the following table:

Receiver Sample Handshake Register (1:E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSIA	X	X	X	RSSB	RSIE	X	RSDA

Definition of Receiver Sample Handshake Terms:

RSIA: Receiver Sample Interrupt Active
RSSB: Receiver Sample Setup Bit
RSIE: Receiver Sample Interrupt Enable
RSDA: Receiver Sample Data Available

Definition of Receiver Sample Handshake Sequence:

1. **Receiver Sample Data Available.** The RSDA bit goes on when the receiver writes data into the receiver data register (1:0). The bit goes off when the host processor reads data from register 1:0.
2. **Receiver Sample Interrupt Enable.** When the host processor writes a 1 in the RSIE bit, the IRQ line of the hardware interface is driven low when RSDA is on.
3. **Receiver Sample Interrupt Active.** Status bit RSIA is on whenever the Receiver Sample rate device is driving IRQ low.
4. **Receiver Setup Bit.** When the host processor changes the receiver configuration or bits 6 or 7 in the option register, the host must write a 1 in the RSB bit. Bit RSB goes to 0 when the changes become effective.

RECEIVER BAUD HANDSHAKE

The host processor performs a handshake sequence with the receiver baud rate device by controlling and testing bits in the receiver baud handshake register (2:E) in the interface memory space as shown in the following table:

Receiver Baud Handshake Register (2:E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBIA	X	X	X	X	RBIE	X	RBDA

Definition of Receiver Baud Handshake Terms:

RBIA: Receiver Baud Interrupt Active
 RBIE: Receiver Baud Interrupt Enable
 RBDA: Receiver Baud Data Available

Definition of Receiver Baud Handshake Sequence:

1. *Receiver Baud Data Available.* The RBDA bit goes on when the receiver writes data into register (2:0). The bit goes off when the host processor reads data from register 2:0.
2. *Receiver Baud Interrupt Enable.* When the host processor writes a 1 in the RBIE bit, the $\overline{\text{IRQ}}$ line of the hardware interface is driven low when RBDA is on.
3. *Receiver Baud Interrupt Active.* Status bit RBIA is on whenever the receiver baud rate device is driving $\overline{\text{IRQ}}$ low.

RECEIVER SAMPLE STATUS

The host processor has access to various status bits that reflect operation of the receiver sample rate device. These bits can be tested by the host by reading the receiver sample status word (1:8 and 1:9) in the interface memory space as shown in the following tables:

Receiver Sample Status Register 1 (1:8)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	P2DET	X	X

Receiver Sample Status Register 2 (1:9)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	FED	X	X	X	X	X	X

Definition of Receiver Sample Status Terms:

P2DET: Period Two Detector
 FED: Fast Energy Detector

Definition of Receiver Sample Status Conditions:

1. *Period Two Detector.* When the P2DET bit (1:8:2) is off, it indicates that a P2 sequence has been detected. This bit sets to a 1 at the start of the receive data state.
2. *Fast Energy Detector.* When the FED bit (1:9:6) is off, it indicates that energy above the receiver threshold is present in the passband.

RECEIVER BAUD STATUS

The host processor has access to status bits that reflect operation of the receiver baud rate device. These bits can be tested by the host by reading the receiver baud status word (1:B) in the interface memory space as shown in the following table:

Receiver Baud Status Register (1:B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	PNDET	X	X	X	X	X	CDET

Definition of Receiver Baud Status Terms:

PNDET: Period N Detector
 CDET: Carrier Detector

Definition of Receiver Baud Status Conditions:

1. *Period N Detector.* When the PNDET bit (1:B:6) is off, it indicates a PN sequence has been detected. This bit sets to a 1 at the end of the PN sequence.
2. *Carrier Detector.* When the CDET bit (1:B:0) is off, it indicates that passband energy is being detected and that a training sequence is not in process. It goes off at start of data state and goes to a 1 at end of received signal.

RECEIVER DATA

The host processor accepts input data from the receiver in parallel mode by reading a byte from the receiver data register (2:0) in the interface memory space. The data is divided on integral baud boundaries identical to the transmitter data register with bit 0 received first. Note that the receiver data register is used for diagnostic data in the serial mode.

DIAGNOSTIC CAPABILITIES

The R48DP provides the user with access to much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

HARDWARE DIAGNOSTIC CIRCUITS

Signal names and descriptions of the hardware diagnostic circuits are given in the following table:

Hardware Diagnostic Circuits

Name	I/O	Pin No.	Description
EYEX	0	15C	Eye Pattern Data — X Axis
EYEX	0	14A	Eye Pattern Data — Y Axis
EYECLK	0	14C	Eye Pattern Clock
EYESYNC	0	13A	Eye Pattern Synchronizing Signal

Eye Pattern Generation — The four hardware diagnostic circuits allow the user to generate and display an eye pattern. Circuits EYEX and EYEW serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the rising edge of the EYECLK output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

SOFTWARE DIAGNOSTIC CIRCUITS

Each receiver device (sample rate and baud rate) contains six registers in the interface memory space dedicated to reading and writing modem RAM locations from the host processor bus. Four of these registers are organized into 2-byte data words and the remaining two registers form 1-byte control registers that hold RAM access codes. Data is read from RAM into the data registers. Data is written into RAM from the data registers. The RAM location involved in the data transfer is specified by the RAM access code stored in the associated diagnostic control register. The diagnostic registers are related as shown in the following table:

Software Diagnostic Registers

Device	Control Register	Write Bit	Data Word (MSB)	Data Word (LSB)
Sample	XS (1:5)	None	XSM (1:3)	XSL (1:2)
Sample	YS (1:4)	SWRT (1:7:3)	YSM (1:1)	YSL (1:0)*
Baud	XB (2:5)	None	XBM (2:3)	XBL (2:2)
Baud	YB (2:4)	BWRT (1:7:2)	YBM (2:1)	YBL (2:0)

*In parallel mode, register 1:0 is used for receive data and not diagnostic data.

Data transfer is regulated by the appropriate data available bit. Reading always takes place at the designated rate, and data left in the data registers is overwritten each cycle. When the associated write bit is set, a write cycle is performed each time the associated data available bit is off.

The eight bits of registers 2:3 and 2:1 are continuously presented serially on hardware interface lines EYEX and EYEW respectively.

RAM ACCESS CODES

The following table lists access codes for frequently used RAM data:

RAM Access Codes

Bank	Function	Real Access	Imag. Access
1	Received Signal Samples	C0	—
	Demodulator Output	C2	42
	Low Pass Filter Output	D4	54
	Average Energy	—	5C
	AGC Gain Word — MSB's	81	—
	AGC Gain Word — LSB's	—	01
2	Equalizer Input	C0	40
	Equalizer Tap Coefficients	81-A0	01-20
	Unrotated Equalizer Output	E1	61
	Rotated Equalizer Output (Received Points)	A2	22
	Decision Points (Ideal Data Points)	E2	62
	Error	E3	63
	Rotation Angle	—	00
	Frequency Correction (MSB's)	AA	—
	Frequency Correction (LSB's)	—	2A
	EQM	A7	—

POWER-ON INITIALIZATION

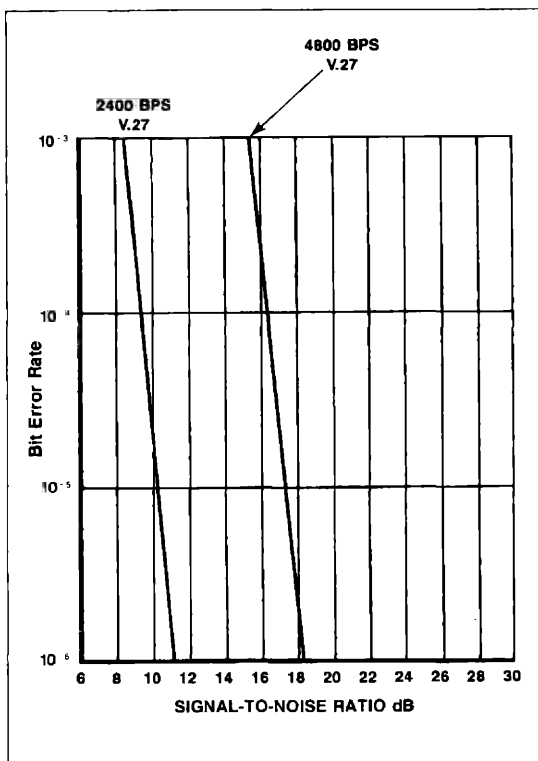
When power is applied to the R48DP, a period of 100 to 300 ms is required for initialization. The power-on-reset signal (POR) remains low during the initialization period. After the low to high transition of POR, the modem is ready to operate. At POR time the modem defaults to the following configuration: V.27, 4800 bps, T/2, long echo protect disable tone, serial data mode, internal clock, cable select 1.8 Km, amplitude and delay equalizers enabled and Japanese 3-link curves selected, transmitter output level set to $-0.5 \text{ dBm} \pm 0.5 \text{ dB}$, interrupts disabled, and receiver threshold set to -43 dBm .

POR can also be used to initialize the users's host processor. It may be connected to a user supplied power-on-reset signal in a wire-or configuration.

PERFORMANCE

Functioning as a V.27 bis/ter type modem, the R48DP provides the user with unexcelled high performance.

Bit Error Rates — The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of -20 dBm as illustrated.



Typical Bit Error Rate Performance

Phase Jitter —At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps (V.27 bis/ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

INTERFACE CIRCUIT CHARACTERISTICS

DIGITAL INTERFACE CIRCUITS

Digital Input Characteristics

Input Logic State	Allowed Input Voltage Levels
Low	0.0V to +0.8V at $-2.5 \mu\text{A}$
High	+2.0V to +5.0V at $+2.5 \mu\text{A}$

Notes

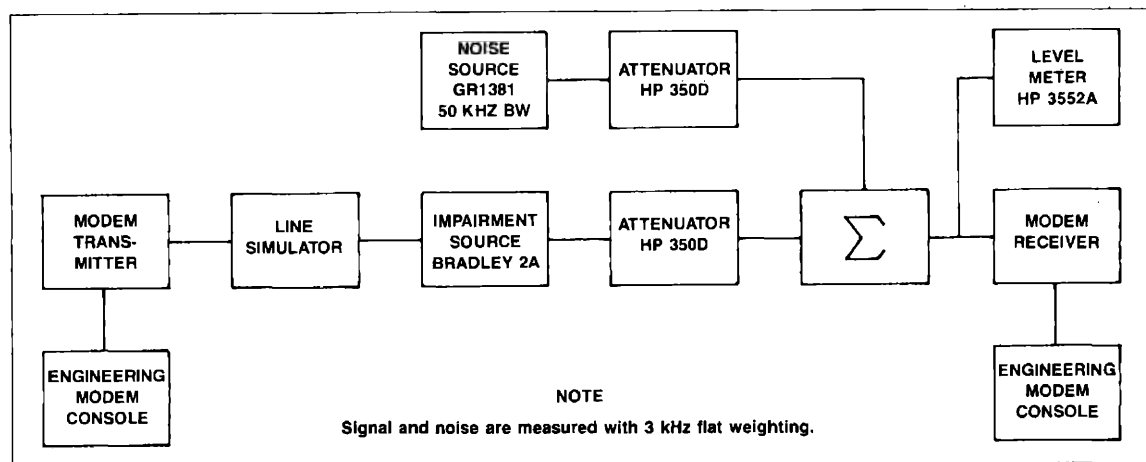
1. The digital inputs are directly TTL/CMOS compatible. The capacitive loading on each input is 25 pF (maximum).
2. Positive current is defined as current into the node.

Digital Output Characteristics

Output Logic State	Output Voltage Level
Low	+0.4V at +1.6 mA
High	+2.4V at $-100 \mu\text{A}$

Notes

1. The digital outputs are directly TTL/CMOS compatible. Capacitive drive capability is 25 pF.
2. Positive current is defined as current into the node.



NOTE

Signal and noise are measured with 3 kHz flat weighting.

BER Performance Test Set-up

ANALOG INTERFACE CIRCUITS

Transmitter Output Level — The transmitter output level is adjustable in 2 dB steps from - 0.5 dBm to - 14.5 dBm accurate to ± 0.5 dB. This level is measured at TXA into a 600 ohm impedance.

Receiver Input — The receiver input impedance is 63.4K ohm $\pm 5\%$.

Auxiliary Transmitter Input — The auxiliary transmitter input (AUXIN) allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, signals above 4800 Hz will cause aliasing errors. The input impedance is 1K ohm and the gain to transmitter output is 0dB.

R48DP SPECIFICATIONS**Power Requirements**

Voltage	Tolerance	Current (Max)
+5 Vdc	$\pm 5\%$	< 700 mA
+12 Vdc	$\pm 5\%$	< 20 mA
-12 Vdc	$\pm 5\%$	< 80 mA

Note: All voltages must have ripple ≤ 0.1 volts peak-to-peak.

Environmental

Parameter	Specification
Temperature: Operating— Storage—	0°C to +60°C (32 to 140°F) - 40°C to +90°C (- 40 to 176°F) Stored in heat sealed antistatic bag and shipping container
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Mechanical Information

Parameter	Specification
Board Structure:	Single PC board with single right angle header with 64 pins, DIN 41612 or equivalent mating connector.
Dimensions:	Width—3.94 in. (100 mm) Length—4.70 in. (120 mm) Height—0.55 in. (1.40 cm)
Weight:	Less than .22 lbs. (.08 kg)



V27P/1 **HIGH SPEED 4800 BPS MODEM**

INTRODUCTION

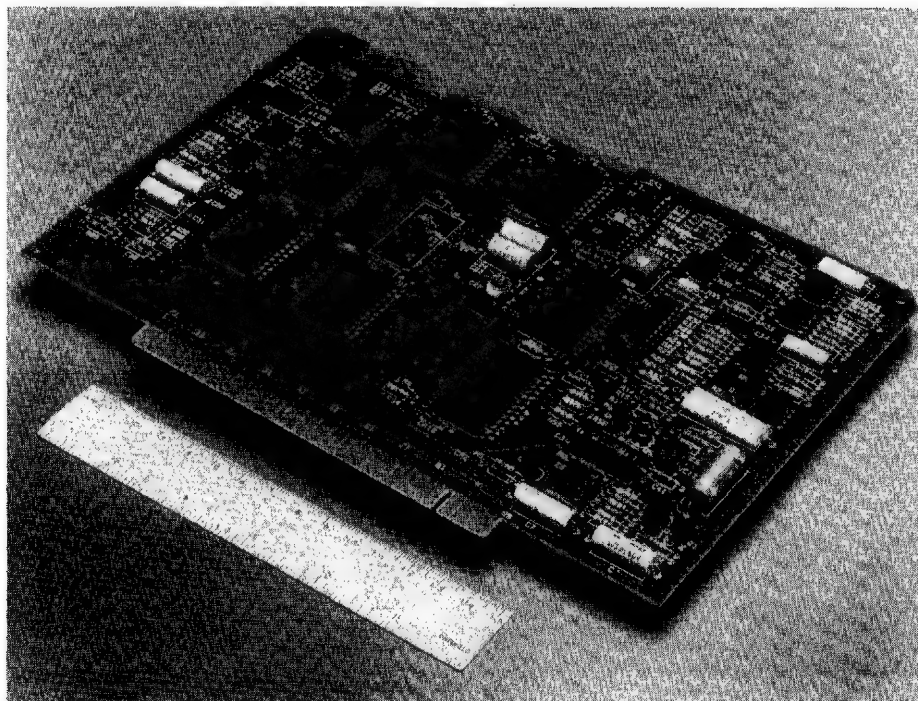
The Rockwell V27P/1 is a versatile, high performance, 4800 bps modem on a single printed circuit board. Being CCITT V.27 compatible, the V27P/1 (with minimal interface circuitry) can operate on dedicated 2-wire or 4-wire half-duplex or 4-wire full-duplex lines. The V27P/1 can also operate in half-duplex on the general switched network.

Measuring approximately 9.2 inches (23.3 cm) by 6.3 inches (16.0 cm), the V27P/1 is the smallest full-feature 4800 bps modem that approaches data communication theoretical performance limits.

The V27P/1 meets the tolerances specified in the CCITT V.27 bis (alternate A), V.27 ter and FSK T.30 specifications. In addition, the V27P/1 can be configured to be functionally compatible with those enhanced specifications available in the Rockwell V27P and M48P modem series.

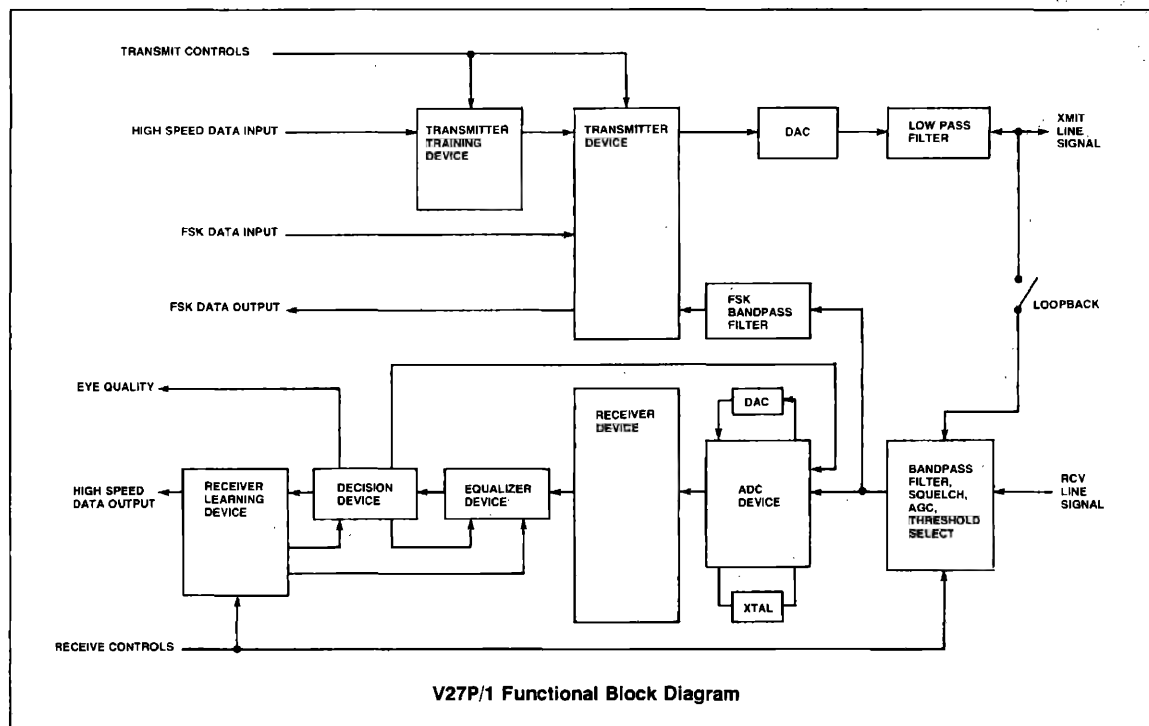
FEATURES

- Single printed circuit card
- 4800/2400 bps modes
- Full-duplex or half-duplex
- Dedicated or general switched network lines operation
- Ultimate user flexibility:
 - CCITT V.27 ter, V.27 bis compatible
 - Also 300 bps binary signalling per CCITT T.30
- TTL compatibility
- Automatic adaptive equalizer
- Analog loopback test circuitry
- 0 to -45 dBm dynamic AGC
- LSI signal processing
- High reliability
- Low power consumption:
 - Typically 3.5 watts
- Automatic training sequence for receiver



10

FUNCTIONAL SPECIFICATIONS



Transmit Carrier and Signalling Frequencies

Carrier Frequency Codex

Compatible QAM: 1706.667 Hz \pm 0.01%Carrier Frequency V.27: 1800 Hz \pm 0.01%Echo Suppression Frequencies: 2100 Hz \pm 0.01%2025 Hz \pm 0.01%Signalling Frequencies of T.30: 1850 Hz \pm 0.01%1650 Hz \pm 0.01%1300 Hz \pm 0.01%1100 Hz \pm 0.01%

Received Signal Frequency Tolerance

The receiver can receive frequency errors of up to \pm 10 Hz with less than a 0.2 dB degradation in Bit Error Rate performance.

Data Signalling and Modulation Rate

At 1600 baud:

Signalling Rate— 1600 baud \pm 0.01%Data Rate— 4800 bps \pm 0.01%

At 1200 baud:

Signalling Rate— 1200 baud \pm 0.01%Data Rate— 2400 bps \pm 0.01%

Transmitted Data Spectrum

At 1600 baud the transmitted spectrum is shaped by approximately a square root of 50 percent raised cosine filter func-

tion. At 1200 baud the spectrum is shaped by approximately a square root of 90 percent raised cosine filter function.

The 1600 and 1200 baud configurations require a usable bandwidth from 950 Hz to 2650 Hz and 1150 Hz to 2450 Hz respectively.

Data Encoding

At 1600 baud the data stream is divided into groups of three bits (tribits). The data rate of 4800 bps may use either an 8-point QAM structure or 8-phase structure. Encoding of the tribits in the 8-phase structure are per CCITT Recommendation V.27 ter.

At 1200 baud the data stream is divided into groups of two bits (dibits). The data rate of 2400 bps uses a 4-phase data structure. Encoding of the dibits may be per the fallback rate of CCITT Recommendation V.27 bis and ter (same as V.26A) or V26B depending on the selected configuration.

Turn-on, Turn-off Sequences

The V27P/1 turn-on sequences are compatible with CCITT Recommendations V.27 bis (alternate i), V.27, and Rockwell M48P modem specifications.

The turn-off sequences for all V.27 modes (except the 1600 baud rate manual V.27 mode) consists of 5 to 10 millisec-

onds of remaining data followed by continuous scrambled 1's followed by no transmission energy. The period of no transmission energy is provided by turning off the transmitter key signal for a recommended duration of 20 milliseconds.

The turn-off sequences for all non-V.27 modes consists of 4 to 7 milliseconds of remaining data followed by a period of no transmission energy.

Ready For Sending Response Times

The Ready For Sending response time to a Request To Send is determined by the configuration selected and its corresponding training time. In Table 1 the Training Times are shown in milliseconds. Note, however, that the 1600 baud manual CCITT configurations actually specify the synchronizing sequence timing per CCITT V.27 rather than the training time. Also note the following abbreviations.

ITC (1P-5P): Transmitter Configuration Inputs 1 through 5. These five bits establish the octal code

IRC (1P-5P):

IRSS (1P-2P),

ITSS (1P-2P):

shown where P1 and P2 are the most significant octal digit and P3 through P5 establish the least significant octal digit shown in the chart.

Receiver Configuration Inputs 1 through 5. These five bits establish the octal code shown where P1 and P2 are the most significant octal digit and P3 through P5 establish the least significant octal digit shown in the chart.

Receiver Signal Structure and Transmitter Signal Structure. Where P1 and P2 establish an octal code of 0, 1, 2, or 3. They define the signal structures as follows:

1 selects 8 point QAM

3 selects DPSK as:

8-phase at 1600 baud

4-phase at 1200 baud

V27P/1 Configurations

No.	Configuration	Transmitter ITC (1P-5P) (Octal Code)	Receiver IRC (1P-5P) (Octal Code)	Signal Structure IRSS (1P-2P) ITSS (1P-2P) (Octal Code)	Data Rate (bps)	Training Time (msec)	Carrier Frequency (hz)
1.	1600 Baud DIAL, CCITT DIAL	22	22	1,3	4800	181	NOTE
2.	1600 Baud DIAL — T/2	22	36	1,3	4800	181	NOTE
3.	1600 Baud DIAL Slow	36	22	1,3	4800	221	NOTE
4.	1600 Baud P-P	20	20	1,3	4800	141	NOTE
5.	1600 Baud P-P — T/2	20	32	1,3	4800	141	NOTE
6.	1600 Baud Manual CCITT	32	30	3	4800	20 (Sync Sequence)	1800
7.	1600 Baud Manual CCITT	30	30	3	4800	50 (Sync Sequence)	1800
8.	1600 Baud V27 DIAL/P-P	23	23	3	4800	708	1800
9.	1600 Baud V27 DIAL/P-P EP	27	23	3	4800	923	1800
10.	1600 Baud V27 DIAL/P-P — T/2	23	33	3	4800	708	1800
11.	1600 Baud V27 DIAL/P-P — T/2 EP	27	33	3	4800	923	1800
12.	1600 Baud V27 Multipoint — T/2	21	27	3	4800	50	1800
13.	1600 Baud V27 Resync (use with configuration 8)	21	25	3	4800	50	1800
14.	1600 Baud V27 Resync EP (use with configuration 9)	25	25	3	4800	265	1800
15.	1600 Baud V27 Resync — T/2 (use with configuration 10)	21	35	3	4800	50	1800
16.	1600 Baud V27 Resync — T/2 EP (use with configuration 11)	25	35	3	4800	265	1800
17.	1200 Baud DIAL	14	10	3	2400	170	1800
18.	1200 Baud P-P	10	10	3	2400	117	1800
19.	1200 Baud V27 DIAL/P-P	13	11	3	2400	943	1800
20.	1200 Baud V27 DIAL/P-P EP	17	11	3	2400	1158	1800
21.	1200 Baud V27 Multipoint	11	15	3	2400	66	1800
22.	1200 Baud V27 Resync (use with configuration 19)	11	13	3	2400	66	1800
23.	1200 Baud V27 Resync EP (use with configuration 20)	15	13	3	2400	281	1800

Note: Carrier frequency is 1706 2/3 Hz when IRSS (1P-2P) is a 1 (8-point).
Carrier frequency is 1800 Hz when IRSS (1P-2P) is a 3 (8-phase DPSK).

Received Line Signal Detector (D109)

The time response of the Received Line Signal detector circuit (D109) is a function of the length of the received turn-on sequence. Circuit D109 turns on after synchronizing is completed and prior to user data appearing on the received output line. D109 turns on for approximately 2 milliseconds after the echo protect tone disappears in the V27EP configurations (No. 9, 11, 14, 16, 20 and 23 of the V27P/1 Configuration Chart).

For non-CCITT configurations (No. 1, 2 and 3 in the table on page 3), D109 momentarily goes on at the beginning of the synchronizing sequence.

When no synchronizing signal is detected at the receiver, D109 turns on in 5 to 15 milliseconds for an applied signal greater than 3 dB above the turn on threshold. If training is not enabled at the receiver, D109 turns on in 5 to 15 milliseconds.

Three threshold options are provided:

- | | |
|--------------------------|----------|
| 1) Greater than -43 dBm: | D109 ON |
| Less than -48 dBm: | D109 OFF |
| 2) Greater than -26 dBm: | D109 ON |
| Less than -31 dBm: | D109 OFF |
| 3) Greater than -16 dBm: | D109 ON |
| Less than -21 dBm: | D109 OFF |

The three threshold options are controlled by the condition of the THRESH1 and THRESH2 control lines as indicated below.

dB LEVEL	THRESH1	THRESH2
-43 dBm ON	Open Circuit	Open Circuit
-26 dBm ON	Open Circuit	0 to -0.5V
-16 dBm ON	0 to -0.5V	Open Circuit

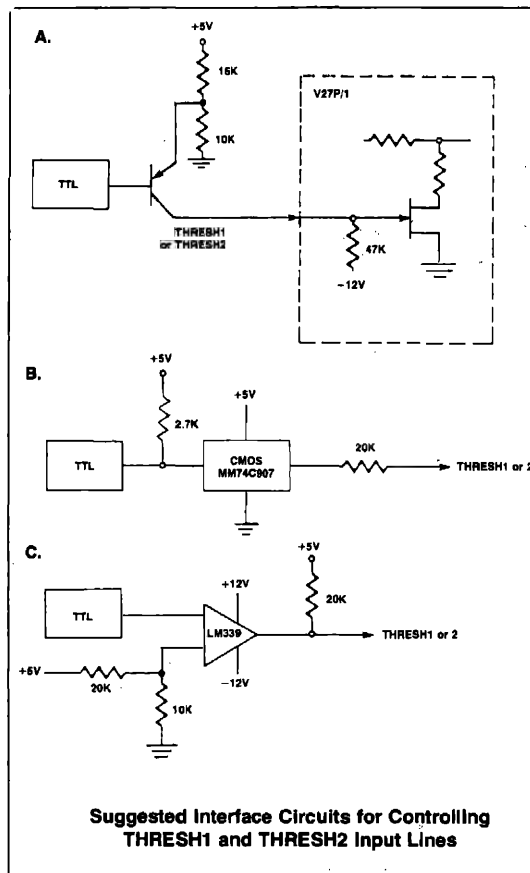
When the received signal drops 5 dB below the D109 turn off threshold, D109 will turn off in 5 to 15 milliseconds. The condition of D109 between the selected turn on and turn off thresholds is not specified except that a hysteresis action of greater than 2 dB exists between the off-to-on and on-to-off transition levels.

Recommended circuits to control THRESH1 and THRESH2 input interface lines are shown in diagrams (A, B and C).

Bit Error Rates

The V27P/1 is thoroughly tested to guarantee Bit Error Rate (BER) performance under test conditions equivalent to CCITT Recommendation V.26. The test set-up used by Rockwell is shown in the BER Performance Test Set-up diagram.

The results of these BER performance tests are shown in the Typical Bit Error Rate Performance diagram.

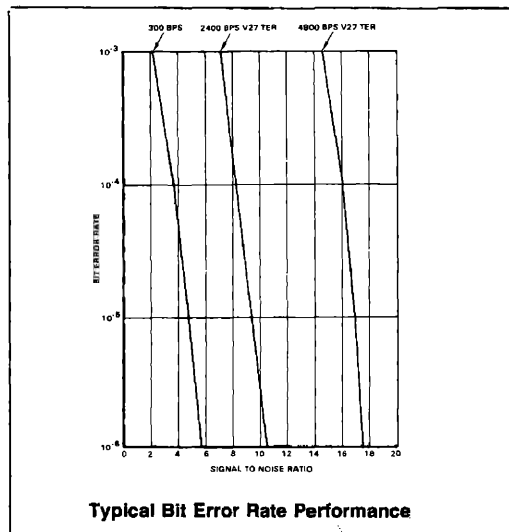
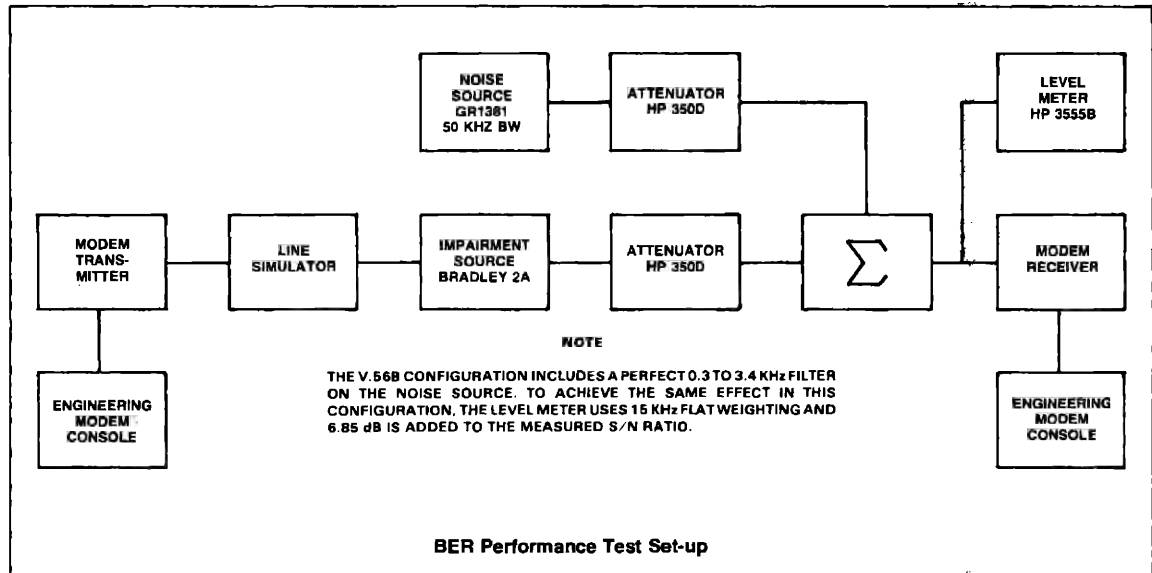


Data Scrambler Selection

The V27P/1 makes available to the user one CCITT V.29 compatible scrambler, five different period 127 scramblers (and descramblers), and a no scramble option. These scramblers provide data transmitted by the V27P/1 with the degree of randomness necessary to ensure the continued convergence of all adaptive processes at the receiver. The seven possible scrambler configurations that are user software selectable are:

- Period 127 cryptographic
- Period 127 synchronizing
- CCITT period 127 self synchronizing (compatible with CCITT Recommendation V.27)
- Period 8,388,607 self synchronizing (compatible with CCITT Recommendation V.29)
- Period 127 self synchronizing with 8-bit protection
- CCITT period 127 self synchronizing (compatible with CCITT Recommendations V.27 bis and ter)
- No scrambler

All scramblers can be used with all modem configurations listed in the table on page 3.



MODES OF OPERATION

The V27P/1 has two modes of operation; a training mode and a data mode. In order for the receiver to correctly decode the transmitted data the V27P/1 must detect the presence of a line signal, adjust the AGC, detect the presence of a training sequence, recover the baud timing of the transmitter, phase and frequency lock to the carrier associated with the received signal, and adapt the equalizer to the amplitude and delay characteristics of the channel. This learning process is accomplished most efficiently when the transmitter initiates a training sequence whenever a new transmitter-receiver connection is made. It is possible to set up the receiver

without a training sequence, but it is a manual mode requiring considerable user effort. In a training mode, an internally generated pattern is transmitted to the receiver to facilitate synchronization. During the training mode, the data input line to the receiver is ignored and the output line does not reflect the state of the data input.

In the data mode of operation, information on the data input is strobed by the transmitter signal element clock and transmitted to the receiver. The receiver demodulates and decodes the passband signal and outputs the recovered data on the output where it is then ready to be strobed by the receiver signal element clock.

Request To Send—Ready For Sending

To initiate transmitter operation in the data or training mode, the Request to Send input is brought high. If a training mode is not initiated the Ready for Sending indicator goes high within one baud interval and data transmission commences.

The mode of the receiver is indicated by the data channel received line signal detector (D109). For data mode, D109 is high and the receiver training mode indicator is low.

If the receiver enters the training mode, the receiver training mode indicator goes high until the training mode is completed. When training is completed the receiver training mode indicator goes low and, if sufficient signal energy is present on the input line, D109 goes high, enabling the data mode.

Training Mode—Dial and Point-To-Point

For dial and point-to-point configurations, the V27P/1 receiver training is automatically initiated whenever a training sequence is detected in the received line signal. The training sequence consists of two phases: Phase 1 causes the training detector to turn on and also makes a coarse adjustment of the carrier

frequency variable which compensates for any frequency translation due to the channel; Phase 2 is used to converge the adaptive equalizer which is part of the V27P/1 structure.

A short scrambler synchronization sequence follows Phase 2 and is used to generate the success indicator. In order for training to be successful, the incoming training sequence must have been generated by a similarly configured transmitter using a compatible training sequence.

At the receiver, detection of a training sequence requires that there be sufficient signal energy and that the receiver's carrier frequency variable be within 30 Hz of nominal.

Training Resync (V.27 bis/ter Turnaround)

In a 2-wire half duplex data communication system, data can be transmitted in only one direction at any given instant. Therefore, the modems at the local and remote sites are required to interchange their roles as the receiver and the transmitter respectively. This turnaround operation requires constant resynchronization to meet CCITT Recommendations for V.27 bis/ter.

The resync configurations are used for reacquiring synchronization in turnaround operation without having to go through the normal long training sequence. The resync training sequences are relatively short and are used for recovering carrier phase, symbol timing and achieving equalizer convergence without resetting carrier frequency and equalizer taps.

Training Mode—Multipoint

In the V27P/1 modem, two multipoint configurations are provided for 4-wire circuits conforming to M1020 which permit short training sequences. In these configurations, the first train signal must be high to process the short training sequences; otherwise the receiver will ignore the training sequence and enter directly into the data mode. The receiver will enter into the training mode if the first train signal is high and there is sufficient signal energy.

For 4-wire circuits which are worse than M1020 and for 2-wire circuits, a long training sequence should be used rather than the multipoint configuration. These training sequences require that the receiver be in the proper dial/point-to-point configuration.

Training Mode—Manual

The V27P/1 modem includes two manual configurations in which the remote modem need not transmit a special training sequence to the local receiver. In these configurations, the equalizer tap coefficients for the local receiver must be initialized from an external source. The tap coefficients may be initialized by controlling three input terms—ICR, ICI and ICLCP—in synchronization with the Baud Rate Clock.

In order to operate the modem in the manual configurations, both the transmitter and receiver must be set according to

the code shown in Table 1. Manual configuration code octal 30 has a longer synchronizing sequence than configuration code octal 32, but both synchronizing sequences conform to the CCITT Recommendation V.27. However, neither sequence is of sufficient duration to aid in training the receiver.

Receiver Operation During Loss of Line Signal

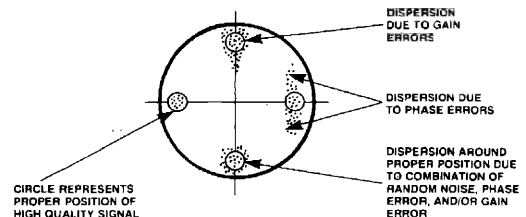
When there is no line signal present, all receiver update relating to the equalizer, carrier frequency variable and baud timing are inhibited and the current values of the equalizer taps and the carrier frequency variable are retained.

DATA QUALITY

The receiver generates an Eye Quality Monitor (EQM) signal that can be used to determine the equivalent Gaussian signal to noise ratio of the overall system within approximately ± 2 db. Eye quality is determined by calculating the difference between the received signal point after equalization and the transmitted or expected signal point. The receiver output DEQ2P is a filtered version of this error signal. It is a serial word clocked by the system bit clock (345.6 KHz or 230.4 KHz, depending on baud rate). Output signal DQGTP is a gating signal which delineates the eight MSB's of DEQ2P. The use and interpretation of these binary signals are quite complex and are dependent on the application and the signal structure. The user can derive a meaningful interpretation of the EQM readings by monitoring them while testing the modem against his performance criteria.

Visual Display of Eye Pattern

A visual indication of the modem's performance can be obtained by displaying the received baseband signal structure after equalization. This is done by converting the eight MSB's of the real and imaginary equalized signal points available on DRERP and DIERP to analog voltages which are then used to drive the horizontal and vertical sweeps of an oscilloscope. The resultant display will be a symmetrical dot pattern of 16 points, 8 points, or 4 points which is a time representation of the received baseband signal. Any uncompensated distortion over the transmission path will cause each dot in the pattern to enlarge or otherwise show distortion. A typical visual eye pattern of a 4 point display is shown in the following diagram.



Typical Eye Pattern

Success Indicator

A second data quality indicator is provided for in all configurations except the 1200 baud non-V.27 modes. This signal provides a rough indication that the training has been successful and that data will be properly received. This "success" output (DSUCP) will go high during the last one to twenty milliseconds of receiver training, provided training has been successful. During the data mode (DRTMP low and D109 high), DSUCP will go high whenever 15 consecutive data marks or spaces are decoded at the receiver data output.

ADDITIONAL CAPABILITIES

The V27P/1 provides many additional capabilities germane to data communication system design and implementation. Capabilities such as local loopback, tone generation and detection, external clock facilities, and 300 bps FSK operation are briefly described in the following paragraphs.

Local Loopback Capability

A local loopback option is available for all half duplex and full duplex modem configurations. The Local Loopback Command (ILB) connects the transmitter's output through a buffer amplifier to the receiver input, thereby allowing a check of the local modem. The ILB command squelches the input to the receiver and loops the analog signal from the transmitter to the receiver input.

An internal pattern generator is also incorporated in the modem which can be used when no modem test set is available.

SPECIFICATIONS

V27P/1 Specifications

DC Voltages			
Voltage	Tolerance	Current (Typical)	Current (Max)
+ 5 volt	±5%	135 ma	<200 ma
+12 volt	±5%	40 ma	< 70 ma
-12 volt	±5%	175 ma	<230 ma
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.			
Environment			
Temperature:	Operating: 0°C to +60°C (32 to 140°F) Storage: -40°C to +80°C (-40 to 176°F) (Stored in heat sealed antistatic bag and shipping container)		
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.		
Mechanical			
Board Structure:	Single PC board with edge connector		
Mating Connector:	100 pin, edge connector, two sided, with 0.1 in (2.54 cm) centers. Recommended Viking 3VH50/IJND5 or equivalent mating connector.		
Dimensions:	Width—9.188 in (23.338 cm) Depth—6.288 in (15.972 cm)		
Weight:	Less than 0.45 lbs (0.20 kg)		

Tone Generation And Detection

The transmitter can be used to transmit single frequency tones for disabling echo suppressors or for system signaling. Tone that can be transmitted (selected through software control) are: 1100 Hz, 1300 Hz, 1650 Hz, 1850 Hz, 2025 Hz, and 2100 Hz. Other tones are also possible. The carrier frequency can be altered by selection of values for a binary bit stream.

External Data Clock

The data input to the transmitter can be clocked from an external source when the external clock is used as a reference input to the data clock's phase locked loop. By applying an external clock the reference input will cause the transmitter data clock to track the frequency and phase of the reference. The frequency of the reference clock must be within 100 ppm of nominal in order for the receiver's baud timing to properly track that of the transmitter. The reference clock can be equal to the nominal data clock frequency or be a subharmonic of it as long as the frequency tolerance is adhered to.

300 bps FSK Modem Operation

A CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 channel 2 modulation system can also be configured. The FSK modem is capable of generating the 1100, 1300, 1650 and 1850 Hz tones.



R1212 **1200 BPS FULL-DUPLEX MODEM**

PRELIMINARY

INTRODUCTION

The Rockwell R1212 is a high performance full-duplex 1200 bps modem. Using state-of-the-art VLSI and signal processing technology, the R1212 provides the user with enhanced performance and reliability on a single printed circuit board of less than 22 square-inches—overall size.

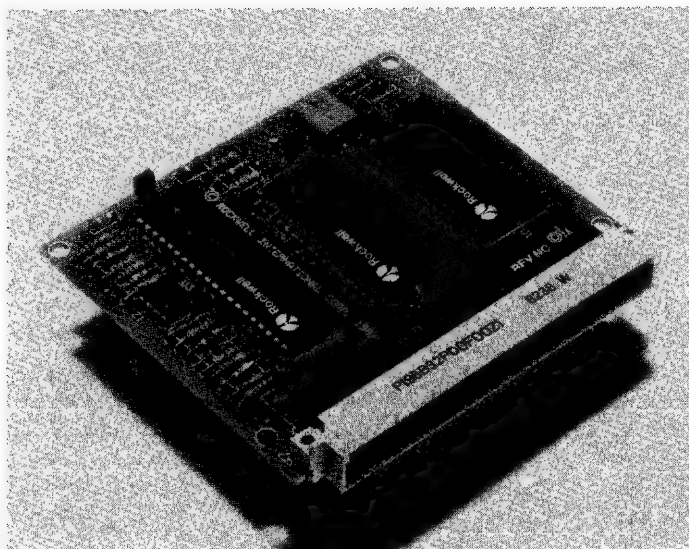
The R1212 modem is ideal for data transmission over the 2-wire dial-up telephone network. The direct-connect, auto dial/answer features are specifically designed for remote and central site computer applications. The bus interface allows easy integration into a personal computer, box modem, microcomputer, terminal or any other communications product that demands the utmost in reliability and performance.

The added test features, such as local analog loopback, remote digital loopback, and a self-test function, offer the user flexibility in creating a 1200 bps modem design customized for specific packaging and functional requirements.

Being CCITT V.22 A, B compatible, as well as Bell 212A and 103 compatible, this modem fits any application for full-duplex 1200 bps (synchronous and asynchronous) and 0 to 300 bps asynchronous data transmission over the general switched telephone network.

FEATURES

- CCITT V.22 A, B Compatible
- Bell 212A and 103 Compatible
- Synchronous: 1200 bps, 600 bps $\pm 0.01\%$
- Asynchronous: 1200 bps, 600 bps $\pm 1\%$, -2.5% , 0-300 bps
—Character length 8, 9, 10, or 11 bits
- DTE Interface
—Functionally: Microprocessor Bus (Control) and RS-232-C Interface (Data/Control)
—Electrically: TTL Compatible
- Operation: 2-wire full-duplex
- Adaptive and Fixed Compromise Equalization
- Test Configurations:
—Local Analog Loopback
—Remote Digital Loopback
—Self Test
- Auto/Manual Answer
- Auto/Manual Dial:
—Tone or Pulse Dial
- Power Consumption: 3 Watts Typical
- Power Requirements: +5 Vdc, ± 12 Vdc
- Plug-compatible member of new Rockwell modem line
- Two Versions: R1212DC (Direct Connect) with FCC approved DAA Part 68 Interface and R1212M (Module) without DAA



R1212 Full-Duplex Modem

TECHNICAL SPECIFICATIONS

The following are the technical specifications for the R1212 modem.

TRANSMITTER CARRIER AND SIGNALING FREQUENCIES

The transmitter carrier and signaling frequencies are given in the following table:

**Transmitter Carrier and Signaling
Frequencies Specifications**

Frequency	Specification (Hz \pm 0.01%)
V.22 low channel, Originate Mode	1200
V.22 high channel, Answer Mode	2400
Bell 212A high channel Answer Mode	2400
Bell 212A low channel Originate Mode	1200
Bell 103/113 Originating Mark	1270
Bell 103/113 Originating Space	1070
Bell 103/113 Answer Mark	2225
Bell 103/113 Answer Space	2025

tone generation

The specifications for tone generation are as follows:

- Answer Backtones:** The R1212 is capable of generating echo disabling tones both of the CCITT and Bell versions, as follows:
 - CCITT: 2100 Hz \pm 15 Hz.
 - Bell: 2225 Hz \pm 10 Hz.
- Guard Tones:** If GTS is low, an 1800 Hz guard tone frequency is selected; if GTS is high, a 553.846 Hz tone is employed. In accordance with the CCITT V.22 Recommendation, the level of transmitted power for the 1800 Hz guard tone should be 6 \pm 1dB below the level of the data power in the main channel. The total power is transmitted to the line should be the same whether or not a guard tone is enabled. If a 553.846 Hz guard is used, its transmitted power should be 3 \pm 1dB

below the level of the main channel power, and again the overall power transmitted to the line should remain constant whether or not a guard tone is enabled. The device accomplishes this by reducing the main channel transmit path gain by .97dB and 1.76dB for the cases of the 1800 Hz and 553.846 Hz guard tones respectively.

- DTMF Tones:** The R1212 is capable of generating dual tone multi-frequency tones. When the transmission of DTMF tones are required, the CRQ and DTMF bits must be set to a 1. (see Interface Memory). When in this mode, the specific DTMF tones generated are decided by loading transmit register with the appropriate digit as shown in the following table:

Interface Memory Signals

BCD				Dial Digits	Tone Pairs
0	0	0	0	0	941 1336
0	0	0	1	1	697 1209
0	0	1	0	2	697 1336
0	0	1	1	3	697 1477
0	1	0	0	4	770 1209
0	1	0	1	5	770 1336
0	1	1	0	6	770 1477
0	1	1	1	7	852 1209
1	0	0	0	8	852 1336
1	0	0	1	9	852 1477
1	0	1	0	*	941 1209
1	0	1	1	Spare (B)	697 1633
1	1	0	0	Spare (C)	770 1633
1	1	0	1	Spare (D)	852 1633
1	1	1	0	#	941 1477
1	1	1	1	Spare (F)	941 1633

tone detection

The R1212 can detect tones in the 340 to 645 Hz band.

SIGNALING AND DATA RATES

The signaling and data rates for the R1212 are defined in the table below:

Signaling and Data Rates

Operating Mode	Signaling Rate (Baud)	Data Rate
V.22: (Alternative A)		
Mode i	600	1200 bps \pm 0.01% Synchronous
Mode iii	600	600 bps \pm 0.01% Synchronous
(Alternative B)		
Mode i	600	1200 bps \pm 0.01% Synchronous
Mode iii	600	600 bps \pm 0.01% Synchronous
Mode ii	600	1200 bps Asynchronous
Mode iv		8, 9, 10, or 11 Bits Per Character 800 bps Asynchronous 8, 9, 10, or 11 Bits Per Character
Bell 212A	600 0 to 300	1200 bps \pm 0.01% Synchronous/Asynchronous 0 to 300 Bps Asynchronous

DATA ENCODING

The specifications for data encoding are as follows:

1. *1200 bps (V.22 and Bell 212A)*. The transmitted data is divided into groups of two consecutive bits (dibits) forming a four-point signal structure.
2. *600 bps (V.22)*. Each bit is encoded as a phase change relative to the phase preceding signal elements.

EQUALIZERS

The R1212 provides equalization functions which can be used to improve performance when operating over poor lines.

Automatic Adaptive Equalizer—An automatic adaptive equalizer is provided in the receiver circuit for V.22 and Bell 212A configurations.

Fixed Compromise Equalizer—Compromise equalizers are provided in the transmitter and receiver.

TRANSMITTED DATA SPECTRUM

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by the square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ± 100 microseconds over the frequency range 800 to 1600 Hz (low channel) and 2000 to 2800 Hz (high channel).

SCRAMBLER/DESCRAMBLER

The R1212 incorporates a self-synchronizing scrambler/descrambler. In accordance with the CCITT V.22 and the Bell 212A recommendations.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R1212 can adapt to received frequency errors of up to ± 7 Hz with less than a 0.2 dBm degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the R1212 satisfies all specified performance requirements for the received line signals from -12 dBm to -45 dBm. The received line signal is measured at the receiver analog input RXA.

RECEIVE TIMING

The R1212 provides a Receive Data Clock (RDCLK) output in the form of a ($50 \pm 1\%$ duty cycle) squarewave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a $\pm 0.01\%$ frequency error in the associated transmit timing source.

TRANSMIT LEVEL

The R1212M output control circuitry contains a variable gain buffer which reduces the modem output level. The R1212M can be strapped via the host interface memory to accomplish this.

Transmit Level

Configuration Word	Transmit Level
0 0 0	0 dbm
0 0 1	-2 dbm
0 1 0	-4 dbm
0 1 1	-6 dbm
1 0 0	-8 dbm
1 0 1	-10 dbm
1 1 0	-12 dbm
1 1 1	-14 dbm

PERMISSIVE/PROGRAMMABLE CONFIGURATIONS

The R1212M transmit level is set to 0 dBm to allow a DAA to be used. The DAA would then determine the permissive or programmable configuration.

The R1212DC transmit level is strapped in the permissive mode so that the maximum output level is -9.5 dBm ± 0.5 dBm.

TRANSMIT TIMING

The R1212 provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency*. Selected data rate of 1200 or 600 Hz ($\pm 0.01\%$).
2. *Duty Cycle*. $50 \pm 1\%$.

Transmit Data (TXD) must be stable during the one microsecond periods immediately preceding and following the rising edge of TDCLK.

CLAMPING

The following clamp is provided with the R1212:

1. *Receive Data (RXD)*. RXD is clamped to a constant mark (1) whenever RLSD is off.

RECEIVED LINE SIGNAL DETECTOR

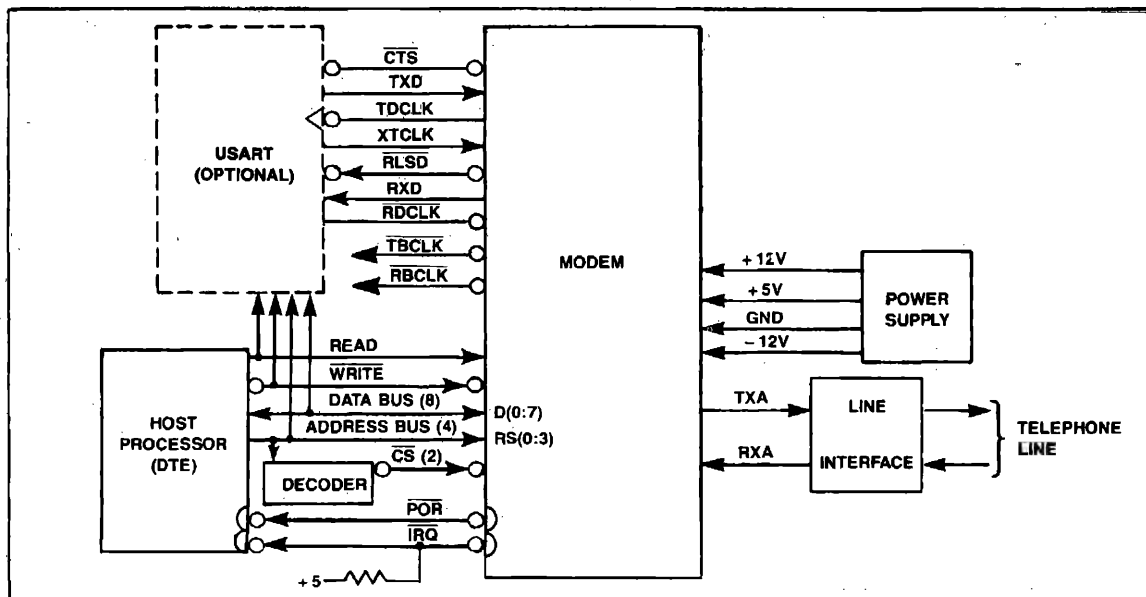
The high and low channel thresholds are greater than -45 dBm (RLSD on) and less than -48 dBm (RLSD off) for V.22 and Bell 212A configurations.

DATA SET READY

The on condition of the R1212 output Data Set Ready (DSR) indicates that the modem is in the data transfer state. The off condition of DSR is an indication that the DTE is to disregard all signals appearing on the interchange circuits—except the calling indicator and the test signal. DSR will switch to the off state when in test state. The on condition of DSR indicates the following:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem is generating an answer tone or detecting answer tone.
4. After ring indicate goes on, DSR waits at least two seconds before turning on to allow the bell equipment to be engaged.

DSR will go off 50 msec after DTR goes off or 50 msec plus a maximum of 4 sec when SSD is enabled.



R1212 Functional Interconnect Diagram

DATA TERMINAL READY

An on condition of DTR prepares the modem to be connected to the communications channel, and maintains the connection established by the DTE (manual answering) or internal (automatic answering) means. The off condition places the modem in the disconnect state.

MODES OF OPERATION

The R1212 is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USART device (shown in the diagram above) illustrates this capability.

CONTROL SELECTION

Selection of either the serial or parallel control is by means of bits ([0,1]:D:7). To enable the parallel control, the bits must be set to a one. In either mode, the R1212 is configured by the host processor via the microprocessor bus.

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 32-byte interface memory.

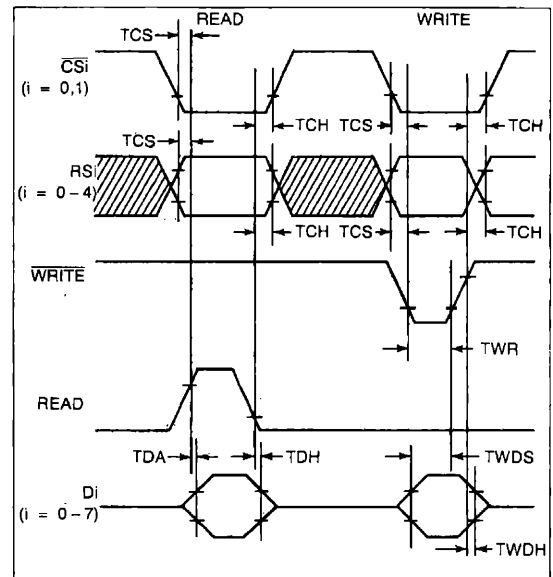
HARDWARE SUPERVISORY CIRCUITS

Signal names and descriptions of the hardware supervisory circuits, including the microprocessor interface, are given in the following table. The microprocessor interface was designed to be compatible with an 8080, 6500, 6800, and 68000 microprocessor.

10

R1212 Hardware Supervisory Circuits

Name	Type	Pin No.	Description
A. OVERHEAD			
DGND	G	5A, 10A, 3C, 8C	Digital Ground
AGND	G	31C, 32C	Analog Ground
+5 VDC	P	19C, 23C, 26C, 30C	+5 Volt Supply
+12 VDC	P	15A	+12 Volt Supply
-12 VDC	P	12A	-12 Volt Supply
POR	OC	13C	Power-On-Reset
B. MICROPROCESSOR INTERFACE			
D7	B	1C	Data Bus (8-Bits)
D6	B	1A	
D5	B	2C	
D4	B	2A	
D3	B	3A	
D2	B	4C	
D1	B	4A	
D0	B	5C	
RS3	I	6C	Register Select (4-Bits)
RS2	I	6A	
RS1	I	7C	
RS0	I	7A	
CS0	I	10C	Chip Select for Bank 0
CS1	I	9C	Chip Select for Bank 1
READ	I	12C	Read Enable
WRITE	I	11A	Write Enable
IRQ	OC	11C	Interrupt Request
C. V.24 INTERFACE			
XTCLK	I	22A	External Transmit Clock
TDCLK	O	23A	Transmit Data Clock
RDCLK	O	21A	Receive Data Clock
CTS	O	25C	Clear-to-Send
TXD	I	24C	Transmit Data
RXD	O	22C	Receive Data
RLSD	O	24A	Received Line Signal Detector
DTR	I	21C	Data Terminal Ready
DSR	O	20A	Data Set Ready
Ri	O	18A	Ring Indicator In
D. ANALOG SIGNALS (R1212M ONLY)			
RXA	I	32A	Receive Analog
TXA	O	31A	Transmit Analog
E. SIGNALS TO DAA (R2424M ONLY)			
RD	I	27A	Ring Detect
RCCT	O	28A	Request Coupler Cut Through
CCT	I	29C	Coupler Cut Through
OH	O	29A	Off-Hook Relay Control
F. ANCILLARY FUNCTIONS			
TBCLK	O	27C	Transmit Baud Clock
RBCLK	O	26A	Receive Baud Clock
TLK	I	28C	Talk TLK = Data
ORG	I	16C	Originate ORG = Answer
B	Bidirectional		
I	Input		
O	Output		
OC	Open Collector		
P	Power		
G	Ground		



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
\overline{CS}_i , \overline{RS}_i setup time prior to Read or Write	TCS	30	—	NS
Data Access time after Read	TDA	—	140	NS
Data hold time after Read	TDH	10	50	NS
\overline{CS}_i , \overline{RS}_i hold time after Read or Write	TCH	10	—	NS
Write data setup time	TWDS	75	—	NS
Write data hold time	TWDH	10	—	NS
Write strobe pulse width	TWR	75	—	NS

INTERFACE MEMORY

The R1212 has two banks of 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. These registers, as shown in the following table, are referred to as interface memory.

When information in these registers is being discussed, the format Y:Z:Q is used. The bank is specified by Y (0 or 1), the register by Z (0-F), and the bit by Q (0-7, 0 = LSB). A bit is considered to be 'on' when set to a one.

R1212 Interface Memory

Bank	Reg No. (HEX)	Description	Bank	Reg No. (HEX)	Description
0	0	Do Not Use	1	0	Dial Digit Register
0	1	Do Not Use	1	1	Do Not Use
0	2	Diagnostic Data Real LSB's	1	2	Diagnostic Data Real LSB's
0	3	Diagnostic Data Real MSB's	1	3	Diagnostic Data Real MSB's
0	4	Diagnostic Data Imaginary LSB's	1	4	Diagnostic Data Imaginary LSB's
0	5	Diagnostic Data Imaginary MSB's	1	5	Diagnostic Data Imaginary MSB's
0	6	Do Not Use	1	6	Do Not Use
0	7	Do Not Use	1	7	Do Not Use
0	8	Receiver Status	1	8	Transmitter Status
0	9	Receiver Status	1	9	Configuration
0	A	Configuration	1	A	Configuration
0	B	Configuration	1	B	Configuration
0	C	Configuration	1	C	Configuration
0	D	Configuration	1	D	Configuration
0	E	Handshake Status	1	E	Handshake Status
0	F	Diagnostic Control Register	1	F	Diagnostic Control Register

The interface memory bits are defined in the following table:

Interface Memory Definitions

Name	Definition	Memory Location	Description
AAE	Auto Answer Enable	1:D:4	When on, AAE causes the modem to automatically answer when a ringing signal is present on the line.
AL	Analog Loopback	(0,1):B:0	When on, AL places the modem in analog loopback. (See Software Diagnostic Circuits).
BUS	Bus Select	(0,1):D:7	When on, BUS places the modem in the parallel control mode. When off, the modem is configured for the serial control mode. Bus can be in either state to configure the modem.
CHAR	Character Length Select	(0,1):C:(3,4)	These bits select either 8, 9, 10, or 11 bit characters. (See Character Length table).
CRQ	Call Request	(0,1):D:6	When on, CRQ places the transmitter in auto dial and the receiver in tone detect mode. The data placed in the dial digit buffer is then treated as digits to be dialed. After the last digit has been dialed, FF (Hex) should be loaded into the buffer to tell the modem to go to the data state. CRQ in the transmitter (Bank 1) when turned off causes the modem to go on-hook. Therefore, it should be on for the duration of the call and not turned off until it is desired to go on-hook. CRQ in the receiver (Bank 0) must be turned off immediately after ringback is detected to put the modem in the data mode, otherwise no answerback tone will be detected.
CTS	Clear-to-Send	1:8:8	When on, CTS indicates to the terminal equipment that the modem will transmit any data which are present at TXD.
DATA	Talk/Data	1:D:5	When on, DATA places the modem in data state and when off in the talk state.

Interface Memory Definitions (Continued)

Name	Definition	Memory Location	Description
DDEI	Dial Digit Empty Interrupt	1:E:2	When on, DDEI causes an interrupt to occur when the dial digit register (1:0) is empty (DDRE = 1).
DDRE	Dial Digit Register Empty	1:E:0	When on, DDRE indicates that the dial digit register is empty and can be loaded with new digits to be dialed. After the register is loaded, DDRE goes off.
DL	Digital Loopback (Manual)	(0,1):A:5	When on, DL manually places the modem in digital loopback. (See Software Diagnostic Circuits).
DLO	Data Line Occupied	1:8:7	When on, DLO indicates that the modem is in auto dial, i.e., CRQ is on and the modem is off-hook ready to dial.
DSR	Data Set Ready	1:8:5	When on, DSR indicates that the modem handshake has begun and that the data state will follow. DSR alone should not be used to indicate that the communication channel has been completely established. DSR in conjunction with CTS and RLSD will determine this. DSR will be off in all test states (except optionally for analog loopback) and when the channel is being used for voice communication (talk).
DSRA	Data Set Ready In Analog Loopback	1:C:7	When on, DSRA causes DSR to be on during analog loopback.
DTMF	Touch Tones/ Pulse Dialing	1:B:1	When on, DTMF tells the modem to auto dial using tones. When off the modem should dial using pulses.
DTR	Data Terminal Ready	1:D:3	DTR must be on before the modem will enter the data state, either manually or automatically. DTR must also be on in order for the modem to automatically answer an incoming call.
ENSI	Enable New Status Interrupt	(0,1):E:6	When on, ENSI causes an interrupt to occur when the status bits in registers (0:[8, 9]) and (1:8) are updated. (NEWS = 1)
ERDL	Enable Response to Remote Digital Loopback	(0,1):A:7	When on, ERDL enables the modem to respond to another modem's remote digital loopback request, thus going into loopback.
GTE	Guard Tone Enable	1:B:4	When on, GTE causes the specified guard tone to be transmitted (CCITT Configurations only).
GTS	Guard Tone Select	1:B:3	When off, GTS selects the 1800 Hz tone and when on the 550 Hz tone.
IRQ	Interrupt Request	(0,1):E:7	When on, IRQ indicates that an interrupt has been generated.
LCD	Enable Loss of Carrier Disconnect	0:D:2	When on, LCD causes the modem to terminate a call when a loss of received carrier energy is detected after approximately 350 msec.
MODE	Mode Select	(0,1):A:(0-3)	These bits select the compatibility at which the modem is to operate. (See Mode Select table).
NEWC	New Configuration	(0,1):E:3	When on, NEWC tells the modem that a new configuration has been written into the configuration registers. The modem will then read the configuration registers and then reset NEWC. NEWC must be set after a new configuration has been written into the following registers: (0:[A-D]) and (1:[9-D]). The remaining registers do not require the use of NEWC to tell the modem that new data was written into them.
NEWS	New Status	(0,1):E:5	When on, NEWS tells the user that there has been a change of status in the status registers.

Interface Memory Definitions (Continued)

Name	Definition	Memory Location	Description
ORG	Originate/Answer	1:9:5	When on, ORG tells the modem that it is originating a call and when low answering a call. This is only valid in manual originate/answer and analog loopback.
RDL	Initiate Remote Digital Loopback	(0,1)::A:6	When on, RDL causes the modem to initiate a request for the remote modem to go into digital loopback.
RDLI	Remote Digital Loopback Indicator	0:8:1	When on, RDLI indicates that the modem has received an RDL request and is in remote digital loopback.
RI	Ring Indicator	1:8:4	When on, RI indicates that a ringing signal is being detected.
RLSD	Received Line Signal Detector	0:8:0	When on, RLSD indicates that the carrier has successfully been received. RLSD will not respond to the 550, 1800, 2100, or 2225 Hz tones.
RSD	Enable Receive Space Disconnect	0:D:1	When on, RSD causes the modem to go on-hook after receiving approximately 1.6 seconds of continuous spaces.
SPEED	Speed Indication	0:9:(4,5)	00 = 300 bps 10 = 1200 bps 01 = 600 bps
SSD	Enable Send Space Disconnect	1:D:0	When on, SSD causes the modem to transmit approximately 4 seconds of spaces before disconnecting, when DTR is turned off.
ST	Self Test	(0,1):A:4	When on, ST activates self test. ST must be turned off to end the test. (See Software Diagnostic Circuits).
3DB	3 dB Loss to Receive Signal	1:B:2	When on, 3DB attenuates the received signal 3dB. This is only used if the R1212M will see 0dBm or greater line signal at the receiver input. Insertion of the 3dB loss will then prevent saturation. This bit is not needed with the R1212DC.
TONE	Tone Detect	0:8:7	TONE follows the energy detected in the 340 to 645 Hz frequency band. The user must determine which tone is present on the line by determining the duty cycle. TONE is active only when CRQ in Bank 0 is on.
TXCLK	Transmit Clock Select	1:C:(5,6)	TXCLK allows the user to designate the origin of the transmitter data clock. (See Transmit Clock table).

SOFTWARE SUPERVISORY CIRCUITS

The operation of the R1212 is affected by a number of software control inputs. These inputs are written into registers within the modem via a microprocessor bus under external control. Modem operation is monitored by various software flags that are read from modem registers using the same microprocessor bus.

The transmit and receive registers contain many bits which perform identical functions and are located in the same memory location only in different banks. Care must be taken to set these bits according to the desired function.

CONFIGURATION REGISTER

The host processor configures the R1212 by writing a control word into the configuration registers in its interface memory space as shown in the following tables:

Mode

Configuration	Configuration Word
Bell 212A 1200 Sync.	0 0 1 0
Bell 212A 1200 Async.	0 0 1 1
Bell 212A 300 Async.	0 1 0 0
V.22A 1200 Sync.	1 0 0 0
V.22B 1200 Async.	1 0 0 1
V.22A 600 Sync.	1 0 1 0
V.22B 600 Async.	1 0 1 1

Character Length

Configuration	Configuration Word
8 bits	0 0
9 bits	0 1
10 bits	1 0
11 bits	1 1

Transmit Clock

Configuration	Configuration Word
Internal	0 0
Not Used	0 1
External	1 0
Slave	1 1

Receiver Interface Memory Bank 0 (CS0)

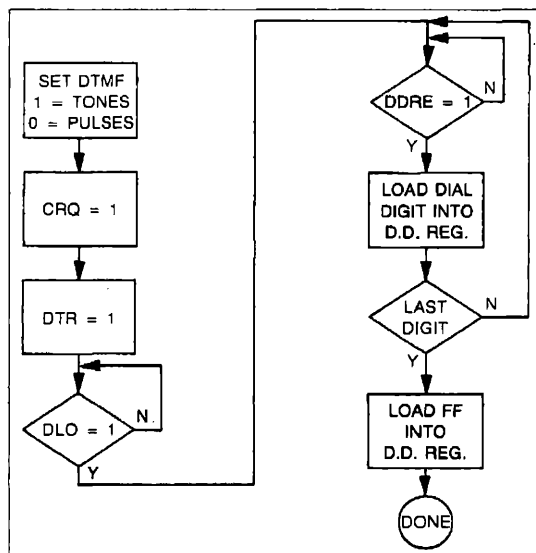
Bit	7	6	5	4	3	2	1	0
Register								
0								
1								
2	Diagnostic Data Real Low							
3	Diagnostic Data Real High							
4	Diagnostic Data Imaginary Low							
5	Diagnostic Data Imaginary High							
6								
7								
8	TONE						RDLI	RLSD
9			Speed					
A	ERDL	RDL	DL	ST			Mode	
B								AL
C				CHAR				
D	BUS	CRQ				LCD	RSD	
E	IRQ	ENSI	NEWS		NEWC			
F	Diagnostic Control Register							

Transmitter Interface Memory Bank 1 (CS1)

Bit	7	6	5	4	3	2	1	0
Register								
0	Dial Digit Register							
1								
2	Diagnostic Data Real Low							
3	Diagnostic Data Real High							
4	Diagnostic Data Imaginary Low							
5	Diagnostic Data Imaginary High							
6								
7								
8	DLO	CTS	DSR	RI				
9			ORG					
A	ERDL	RDL	DL	ST		Mode		
B	TX LEVEL		GTE	GTS	3DB	DTMF		AL
C	DSRA	TXCLK		CHAR				
D	BUS	CRQ	DATA	AAE	DTR			SSD
E	IRQ	ENSI	NEWS		NEWC	DDEI		DDRE
F	Diagnostic Control Register							

AUTO DIAL SEQUENCE

The following flow chart defines the auto dial sequence via the microprocessor interface memory.



Auto Dial Sequence Flow Diagram

Note: The modem timing for the auto dialer accounts for inter-digit delay for pulses and tones.

DIAGNOSTIC CAPABILITIES

The R1212 provides the user with access to much of the data stored in the modems memories. This data is a useful tool in performing certain diagnostic functions.

RAM ACCESS CODES

The RAM access codes defined in the table below allow the host processor to read diagnostic data from the modem receiver. The access codes should be loaded into the diagnostic control register (0:F). The appropriate diagnostic data will then be available in the diagnostic data registers (0:[2-5]).

RAM Access Codes Bank 0

Function	Access	Data Type
Scrambled Data (Imag. Reg.)	00	Real
Self Test Error Counter (Real Reg.)	00	Real
Equalizer Tap Coefficients	01-09	Complex
Phase Error (Real Reg.)	0C	Real
Rotated Equalizer Output (Received Point Eye Pattern)	0D	Complex
Rotated Angle (Imag. Reg.)	0E	Real
Low Pass Filter Output	40	Complex
Input Signal to Equalizer Tap Coefficients	41-49	Complex
Decision Points (Ideal)	4D	Complex
Rotated Error	4E	Complex
Equalizer Output	4F	Complex
Demodulator Output	52	Complex

TEST

The specifications for R1212 tests are defined as follows:

Self tests can be initiated by setting bits ([0,1]:A:4) to a 1. It is possible to perform the tests with or without the DTE connected to the modem. During any self test TXD and RTS are ignored. Note that self tests do not test asynchronous-to-synchronous converter circuits in either the transmitter or receiver.

Error detection is accomplished by monitoring a counter in the RAM. If the counter increments during the self test, an error was made. The counter contents are available in the diagnostic registers when the RAM access code 00 is loaded in the diagnostic control register (0:F).

Self test end-to-end—Upon activation of self-test an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate are applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals are connected to the output of the descrambler.

Self test with loop 3—Loop 3 is applied to the modem as defined in recommendation V.54. Self-test is activated and DCE operation is as in the end-to-end test. In this test DTR is ignored.

Self test with loop 2—The modem is conditioned to instigate a loop 2 at the remote modem as specified in recommendation V.54. Self-test is activated and DCE operation is as in the end-to-end test.

Loopbacks—Remote digital loopback, digital loopback, and local analog loopback can be initiated via the interface memory, as follows:

1. **Digital Loopback.** The R1212 can be manually conditioned to loop the received data back to the transmitter by setting

the DL bits ([0,1]:A:5). DL should be set during the data mode. DSR and CTS will be off. The local modem can then be tested from the far-end by using the terminal equipment at the far-end to transmit a test pattern and examine the looped data. At the far-end modem, all interface circuits behave normally as in the data mode. At the conclusion of the test, DL must be turned off. The local modem will then return to the normal data mode with control reverting to the DTE's DTR.

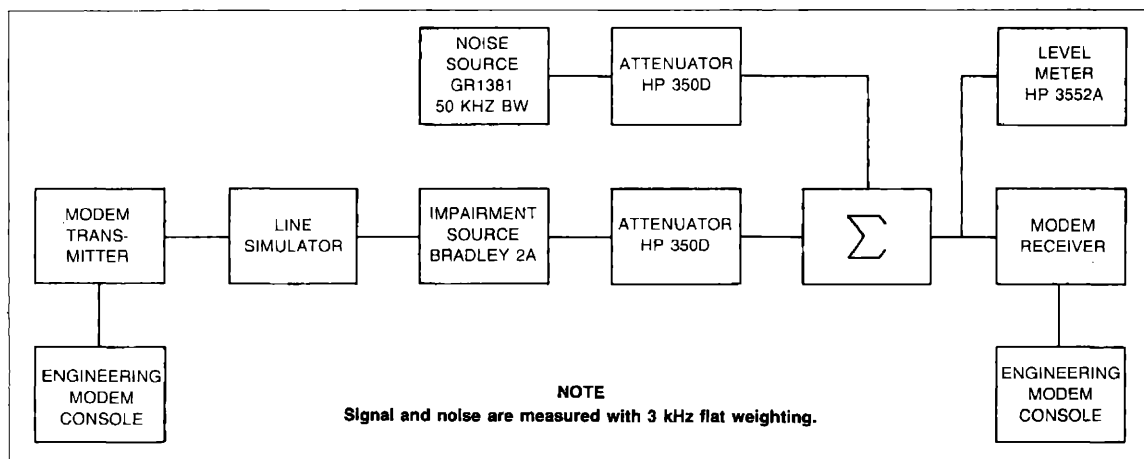
2. **Local Analog Loopback (V.54 Loop 3).** The R1212 is capable of entering into a local analog loopback (V.54 Loop 3). In this loop, the transmitter's analog output is coupled to the receiver's analog input at a point near the modem's telephone line interface. An attenuator is introduced into the loop such that the signal level coupled into the receive path is approximately — 16 dBm attenuation.
3. **Remote Digital Loopback (V.54 Loop 2) (Bell 212A and CCITT V.22 bis and V.22).** The R1212 is capable of entering into a remote digital loopback. Remote digital loopback may be locally entered by the interface memory. Remote digital loopback cannot be performed simultaneously with local analog loopback.

POWER-ON INITIALIZATION

When power is applied to the R1212, a period of 100 to 300 ms is required for initialization. The power-on-reset (POR) signal remains low during the initialization period. After the low to high transition of POR, the modem is ready to be configured.

The modem automatically defaults to Bell 212A 1200 bps, answer state using serial start-stop data, 10 bits per character.

POR can also be used to initialize the user's host processor. It may be connected to a user supplied power-on-reset signal in a wire-or configuration.



BER Performance Test Set-up

PERFORMANCE

Whether functioning as a V.22, or Bell 212A type modem, and regardless of simulated line condition or introduced line impairment, the R1212 provides unexcelled high performance to the user.

BIT ERROR RATES

The Bit Error Rate (BER) performance of the R1212 is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of -43 dBm.

INTERFACE CIRCUIT CHARACTERISTICS

DIGITAL INTERFACE CIRCUITS

Digital Input Characteristics

Input Logic State	Allowed Input Voltage Levels
Low	0.0V to +0.8V at $-2.5 \mu\text{A}$
High	+2.0V to +5.0V at $+2.5 \mu\text{A}$
Notes:	
1. The digital inputs are directly TTL/CMOS compatible. The capacitive loading on each input is 25 pF (maximum).	
2. Positive current is defined as current into the node.	

Digital Output Characteristics

Output Logic State	Allowed Output Voltage Levels
Low	+0.4V at +1.6 mA
High	+2.4V at $-100 \mu\text{A}$
Notes:	
1. The digital outputs are directly TTL/CMOS compatible. The capacitive loading on each output is 50 pF (maximum).	
2. Positive current is defined as current into the node.	

ANALOG INTERFACE CIRCUITS

TRANSMISSION LINE INTERFACE

The R1212DC interface to the telephone line is the Tip and Ring leads. Lightning induced surge voltages and other hazardous voltages which may appear on the telephone line are limited to approximately 7V peak between the secondary leads of the line coupling transformer.

The DAA (R1212DC only) is bi-directional as required by 2-wire full-duplex circuits.

Connection to the telephone line interface pins of the R1212DC to the network are made via the RJ11, as shown in the table below:

R1212DC Network Interface

Connection Type	Telco	Mnemonic	Function
VSOC	1	R	Ring-one side of telephone line Tip-one side of telephone line
	2		
RJ11	3		
Jack	4	T	
	5		
	6		

RING INDICATOR

The R1212 provides a ring indicator ($\overline{\text{RI}}$) output; its low state indicates the presence of a ring signal on the line. The low condition appears approximately coincident with the on segment of the ring cycle (during rings) on the communication channel. (The ring signal cycle is typically two seconds on, four seconds off.) The high condition of the indicator output is maintained during the off segment of the ring cycle (between rings) and at all other times when ringing is being received. The operation of $\overline{\text{RI}}$ is not disabled by an off condition on Data Terminal Ready.

$\overline{\text{RI}}$ will respond to ring signals in the frequency range of 15.3 Hz to 68 Hz with voltage amplitude levels of 40 to 150 Vrms (applied across Tip and Ring), with the response times given in the following table:

RI Response Time

RI Transition	Response Time
Off-to-On	125 ms to 400 ms
On-to-Off	75 ms to 250 ms

This off-to-on (on-to-off) response time is defined as the time interval between the sudden connection (removal) of the ring signal across Tip and Ring and the subsequent on (off) transition $\overline{\text{RI}}$.

OH (OFF-HOOK)

The R1212M provides an output OH (Off-Hook) which indicates the state of the OH relay. A low condition on OH implies the OH relay is closed and the modem is connected to the telephone line. A high condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.

RD

RD indicates to the R1212M by an on (low) condition that a ringing signal is present. The RD signal should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40V rms, 15 to 68 Hz appearing across Tip and Ring with respect to ground.

RCCT

RCCT is used to request that a data transmission path through the DAA be connected to the telephone line. When RCCT goes off (low), the cut-through buffers are disabled and CCT should go off (high) within 1 msec. RCCT should be off during dialing but on for tone address signaling.

CCT

An on (low) signal to the CCT lead indicates to the R1212M that the data transmission path through the DAA is connected.

AUDIO INTERFACE INPUT IMPEDANCE

The specifications for the audio interface input impedance are given in the following table:

Audio Interface Input Impedance

On/Off Hook	Measurement
On-Hook (DC)	The DC resistance between Tip and Ring, and between either Tip or Ring and signal ground is greater than 10 megohms for DC voltages up to 100 volts.
On-Hook (AC)	The on-hook AC impedance measured between Tip and Ring is less than 40K ohms (15.3 Hz minimum).
Off-Hook (DC)	Less than 200 ohms.
Off-Hook (AC)	600 ohms nominal when measured between Tip and Ring.

TRANSMITTER OUTPUT

Basic telephone company requirement is that the signal level received at the relevant local central office not exceed -12 dBm. Several different "connection arrangements" have been established (as documented in Part 68) to accomplish this goal.

When the permissive connection arrangement is used, the transmit output signal level appearing across Tip and Ring (with a 600 ohm resistive load across Tip and Ring) will not exceed -9 dBm. The output level is set at a fixed -10 dBm (nominal). The permissive wall jacks used for data connections are the same jacks used for standard voice installations. The permissive connection arrangement allows greater mobility for user equipment.

When the programmable connection arrangement is used, the maximum output transmit signal level allowed to appear across the Tip and Ring (again, terminated with 600 ohms) is set by a resistor installed by the telephone company in their wall jack at the customer location. The resistor (which is one of thirteen possible values) interacts with the modem through modem leads PR and PC to program the maximum output level, in one dB steps between -12 dBm and 0 dBm. (The resistor is selected by the telephone company jack installer after he has measured the line loss from the customer location to the local telephone company central office).

INSTALLATION**IMPORTANT NOTICE TO USER**

The modem contains protective circuitry registered with the Federal Communications Commission (FCC) Part 68 to allow direct connection to the switched telephone network. To comply with the FCC is required:

1. All direct connections to the telephone lines shall be made through standard plugs and telephone company provided jacks.
2. It is prohibited to connect the modem to pay telephones or party lines.
3. You are required to notify the local telephone company prior to the connection and upon final disconnection of the modem. You must supply to the telephone company the make, model number, FCC registration number, ringer equivalence and particular line to which the connection is to be made. If the proper jacks are not available, you must order the type of jacks to be used from the telephone company.
4. You should disconnect the modem from the telephone line if it appears to be malfunctioning. Reconnect it only when it can be determined that the telephone line is the source of trouble. If the modem needs repair, return it to Rockwell International. This applies to equipment both in and out of warranty. Do not attempt to repair the unit as this will violate FCC rules.
5. The modem contains protective circuitry to prevent harmful voltages from being transmitted to the telephone network. If however such harmful voltages do occur, then the telephone company shall:
 - Promptly notify you of the discontinuance.
 - Afford you the opportunity to correct the situation which caused the discontinuance.

The FCC requires that the following label be prominently displayed on an outside surface of the OEM's end product.

 - Unit contains Registered Protective Circuitry which complies with Part 68 of FCC Rules.
 - FCC Registration Number: Applied For
 - Ringer Equivalence: 0.5

Size of the label should be such that all the required information is legible without magnification.

GENERAL SPECIFICATIONS

The general specifications for the R1212 are given in the following tables:

Power Requirements

Voltage*	Tolerance	Current (Max)
+5 Vdc	±5%	<500 ma
+12 Vdc	±5%	< 10 ma
-12 Vdc	±5%	< 50 ma

*All voltages must have ripple ≤0.1 volts peak-to-peak.

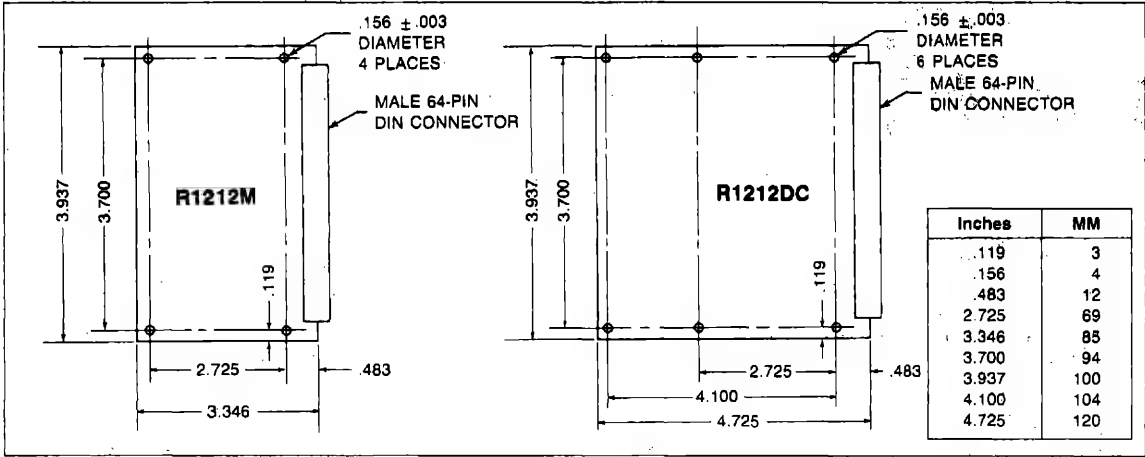
Environmental

Parameter	Specification
Temperature: Operating Storage*	0°C to +60°C (32 to 140°F) -40°C to +80°C (-40 to 176°F)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude:	-200 to +10,000 feet

*PCB's are stored in heat sealed antistatic bags and shipping containers.

Mechanical

Board Structure:	Single PC board with right angle male DIN connector.
Mating Connector:	Female 3 row 64 pin Euroconnector (DIN) with rows A and C populated. Recommended mating connector: Winchester 96S-6043-0531-1 or equivalent.
PCB Dimensions:	
DC Version	Width 3.94 in. (100 mm) × Length 4.725 in. (120 mm) × Height 0.75 in. (19 mm)
M Version	Width 3.94 in. (100 mm) × Length 3.35 in. (85 mm) × Height 0.40 in. (10 mm)
Weight:	Less than 0.45 lbs. (0.20 kg.)



Printed Circuit Board Dimensions



R2424 2400 BPS FULL-DUPLEX MODEM

PRELIMINARY

INTRODUCTION

The Rockwell R2424 is a high performance full-duplex 2400 bps modem. Using state-of-the-art VLSI and signal processing technology, the R2424 provides the user with enhanced performance and reliability on a single printed circuit board of less than 22 square-inches—overall size.

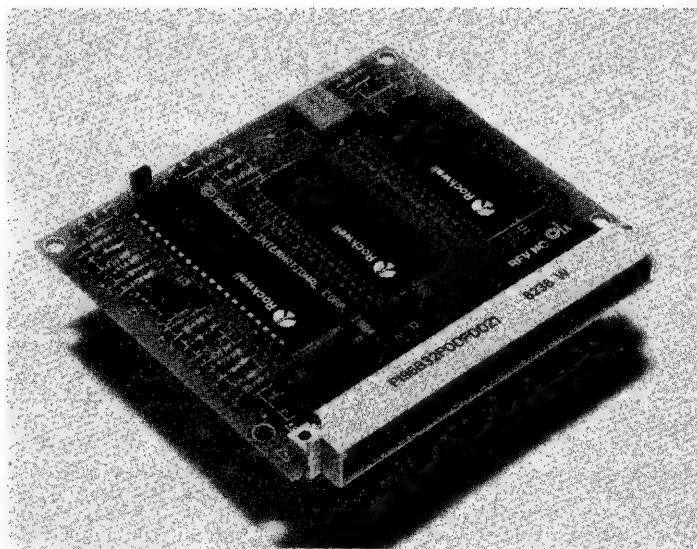
The R2424 modem is ideal for data transmission over the 2-wire dial-up telephone network. The direct-connect, auto dial/answer features are specifically designed for remote and central site computer applications. The bus interface allows easy integration into a personal computer, box modem, microcomputer, terminal or any other communications product that demands the utmost in reliability and performance.

The added test features, such as local analog loopback, remote digital loopback, and a self-test function, offer the user flexibility in creating a 2400 bps modem design customized for specific packaging and functional requirements.

Being CCITT V.22 bis, V.22 A, B compatible, as well as Bell 212A and 103 compatible, this modem fits most applications for full-duplex 2400 and 1200 bps fallback (synchronous and asynchronous) and 0 to 300 bps asynchronous data transmission over the general switched telephone network.

FEATURES

- CCITT V.22 bis, V.22 A, B Compatible
- Bell 212A and 103 Compatible
- Synchronous: 2400 bps, 1200 bps, 600 bps $\pm 0.01\%$
- Asynchronous: 2400 bps, 1200 bps, 600 bps $\pm 1\%$, -2.5% , 0-300 bps
 - Character length 8, 9, 10, or 11 bits
- DTE Interface
 - Functionally: Microprocessor Bus (Control) and RS-232-C Interface (Data/Control)
 - Electrically: TTL Compatible
- Operation: 2-wire full-duplex
- Adaptive and Fixed Compromise Equalization
- Test Configurations:
 - Local Analog Loopback
 - Remote Digital Loopback
 - Self Test
- Auto/Manual Answer
- Auto/Manual Dial:
 - Tone or Pulse Dial
- Power Consumption: 3 Watts Typical
- Power Requirements: +5 Vdc, ± 12 Vdc
- Plug-compatible member of new Rockwell modem line
- Two Versions: R2424DC (Direct Connect) with FCC approved DAA Part 68 Interface and R2424M (Module) without DAA



R2424 Full-Duplex Modem

TECHNICAL SPECIFICATIONS

The following are the technical specifications for the R2424 modem.

TRANSMITTER CARRIER AND SIGNALING FREQUENCIES

The transmitter carrier and signaling frequencies are given in the following table:

Transmitter Carrier and Signaling Frequencies Specifications

Frequency	Specification (Hz $\pm 0.01\%$)
V.22 bis low channel, Originate Mode	1200
V.22 low channel, Originate Mode	1200
V.22 bis high channel, Answer Mode	2400
V.22 high channel, Answer Mode	2400
Bell 212A high channel Answer Mode	2400
Bell 212A low channel Originate Mode	1200
Bell 103/113 Originating Mark	1270
Bell 103/113 Originating Space	1070
Bell 103/113 Answer Mark	2225
Bell 103/113 Answer Space	2025

tone generation

The specifications for tone generation are as follows:

- Answer Backtones:** The R2424 is capable of generating echo disabling tones both of the CCITT and Bell versions, as follows:
 - CCITT: 2100 Hz ± 15 Hz.
 - Bell: 2225 Hz ± 10 Hz.
- Guard Tones:** If GTS is low, an 1800 Hz guard tone frequency is selected; if GTS is high, a 553.846 Hz tone is employed. In accordance with the CCITT V.22 Recommen-

ation, the level of transmitted power for the 1800 Hz guard tone should be 6 ± 1 dB below the level of the data power in the main channel. The total power transmitted to the line should be the same whether or not a guard tone is enabled. If a 553.846 Hz guard tone is used, its transmitted power should be 3 ± 1 dB below the level of the main channel power, and again the overall power transmitted to the line should remain constant whether or not a guard tone is enabled. The device accomplishes this by reducing the main channel transmit path gain by .97 dB and 1.76 dB for the cases of the 1800 Hz and 553.846 Hz guard tones respectively.

- DTMF Tones:** The R2424 is capable of generating dual tone multi-frequency tones. When the transmission of DTMF tones are required, the CRQ and DTMF bits must be set to a 1 (see Interface Memory). When in this mode, the specific DTMF tones generated are decided by loading transmit register with the appropriate digit as shown in the following table:

Interface Memory Signals

BCD				Dial Digits	Tone Pairs	
0	0	0	0	0	941	1336
0	0	0	1	1	697	1209
0	0	1	0	2	697	1336
0	0	1	1	3	697	1477
0	1	0	0	4	770	1209
0	1	0	1	5	770	1336
0	1	1	0	6	770	1477
0	1	1	1	7	852	1209
1	0	0	0	8	852	1336
1	0	0	1	9	852	1477
1	0	1	0	*	941	1209
1	0	1	1	Spare (B)	697	1633
1	1	0	0	Spare (C)	770	1633
1	1	0	1	Spare (D)	852	1633
1	1	1	0	#	941	1477
1	1	1	1	Spare (F)	941	1633

Signaling and Data Rates

Operating Mode	Signaling Rate (Baud)	Data Rate
V.22 bis:	600	Synchronous/Asynchronous 2400 bps $\pm 0.01\%$
V.22 bis:	600	Synchronous/Asynchronous 1200 bps $\pm 0.01\%$
V.22: (Alternative A) Mode i	600	1200 bps $\pm 0.01\%$ Synchronous
Mode iii	600	600 bps $\pm 0.01\%$ Synchronous
(Alternative B) Mode i	600	1200 bps $\pm 0.01\%$ Synchronous
Mode iii	600	600 bps $\pm 0.01\%$ Synchronous
Mode ii		1200 bps Asynchronous 8, 9, 10, or 11 Bits Per Character
Mode iv		600 bps Asynchronous 8, 9, 10, or 11 Bits Per Character
Bell 212A:	600	1200 bps $\pm 0.01\%$ Synchronous/Asynchronous
	0 to 300	0 to 300 bps Asynchronous

TONE DETECTION

The R2424 can detect tones in the 340 to 645 Hz band.

SIGNALING AND DATA RATES

The signaling and data rates for the R2424 are defined in the table below:

DATA ENCODING

The specifications for data encoding are as follows:

1. *2400 bps (V.22 bis)*. The transmitted data is divided into groups of four consecutive bits (quad bits) forming a 16-point signal structure.
2. *1200 bps (V.22 and Bell 212A)*. The transmitted data is divided into groups of two consecutive bits (dibits) forming a four-point signal structure.
3. *600 bps (V.22)*. Each bit is encoded as a phase change relative to the phase preceding signal elements.

EQUALIZERS

The R2424 provides equalization functions which can be used to improve performance when operating over poor lines.

Automatic Adaptive Equalizer—An automatic adaptive equalizer is provided in the receiver circuit for V.22 bis, V.22 and Bell 212A configurations.

Fixed Compromise Equalizer—Compromise equalizers are provided in the transmitter and receiver.

TRANSMITTED DATA SPECTRUM

1. *V.22 bis*. The transmitted line signals (excluding the characteristics of the fixed compromise equalizer) have a frequency amplitude spectrum shaped by the square root of a 75 percent raised cosine filter. The group delay of the transmitter output is within ± 100 microseconds over the frequency ranges 900 to 1500 Hz (low channel) and 2100 to 2700 Hz (high channel).
2. *V.22*. After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by the square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ± 100 microseconds over the frequency range 800 to 1600 Hz (low channel) and 2000 to 2800 Hz (high channel).

SCRAMBLER/DESCRAMBLER

The R2424 incorporates a self-synchronizing scrambler/descrambler. In accordance with the CCITT V.22 bis, V.22 and the Bell 212A recommendations.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R2424 can adapt to received frequency errors of up to ± 7 Hz with less than a 0.2 dBm degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the R2424 satisfies all specified performance requirements for the received line signals from -12 dBm to -45 dBm. The received line signal is measured at the receiver analog input RXA.

RECEIVE TIMING

The R2424 provides a Receive Data Clock (RDCLK) output in the form of a ($50 \pm 1\%$ duty cycle) squarewave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a $\pm 0.01\%$ frequency error in the associated transmit timing source.

TRANSMIT LEVEL

The R2424M output control circuitry contains a variable gain buffer which reduces the modem output level. The R2424M can be strapped via the host interface memory to accomplish this.

Transmit Level

Configuration Word	Transmit Level
0 0 0	0 dbm
0 0 1	-2 dbm
0 1 0	-4 dbm
0 1 1	-6 dbm
1 0 0	-8 dbm
1 0 1	-10 dbm
1 1 0	-12 dbm
1 1 1	-14 dbm

PERMISSIVE/PROGRAMMABLE CONFIGURATIONS

The R2424M transmit level is set to 0 dBm to allow a DAA to be used. The DAA would then determine the permissive or programmable configuration.

The R2424DC transmit level is strapped in the permissive mode so that the maximum output level is -9.5 dBm ± 0.5 dBm.

TRANSMIT TIMING

The R2424 provides a Transmit Data Clock (TDCLK) output with the following characteristics:

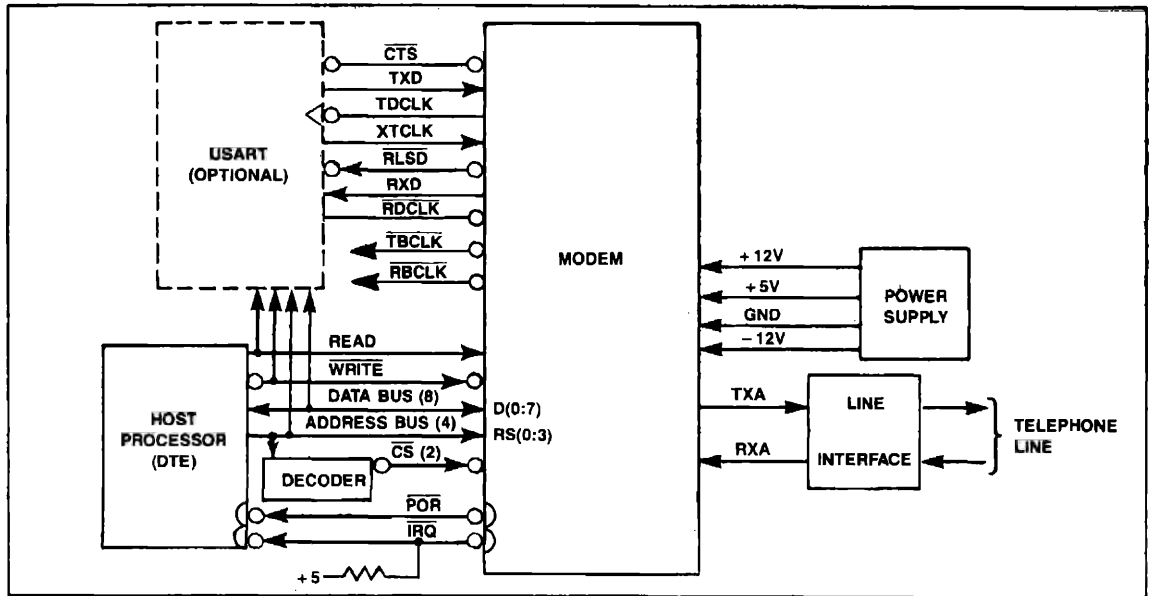
1. *Frequency*. Selected data rate of 2400, 1200 or 600 Hz ($\pm 0.01\%$).
2. *Duty Cycle*. $50 \pm 1\%$.

Transmit Data (TXD) must be stable during the one microsecond periods immediately preceding and following the rising edge of TDCLK.

CLAMPING

The following clamp is provided with the R2424:

1. *Receive Data (RXD)*. RXD is clamped to a constant mark (1) whenever RLSD is off.



R2424 Functional Interconnect Diagram

RECEIVED LINE SIGNAL DETECTOR

The high and low channel thresholds are greater than -45 dBm (RLSD on) and less than -48 dBm (RLSD off) for V.22 bis, V.22 and Bell 212A configurations.

DATA SET READY

The on condition of the R2424 output Data Set Ready (DSR) indicates that the modem is in the data transfer state. The off condition of DSR is an indication that the DTE is to disregard all signals appearing on the interchange circuits—except the calling indicator and the test signal. DSR will switch to the off state when in test state. The on condition of DSR indicates the following:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem is generating an answer tone or detecting answer tone.
4. After ring indicate goes on, DSR waits at least two seconds before turning on to allow the bell equipment to be engaged.

DSR will go off 50 msec after DTR goes off or 50 msec plus a maximum of 4 sec when SSD is enabled.

DATA TERMINAL READY

An on condition of DTR prepares the modem to be connected to the communications channel, and maintains the connection

established by the DTE (manual answering) or internal (automatic answering) means. The off condition places the modem in the disconnect state.

MODES OF OPERATION

The R2424 is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USART device (shown in the diagram above) illustrates this capability.

CONTROL SELECTION

Selection of either the serial or parallel control is by means of bits ([0,1]:D:7). To enable the parallel control, the bits must be set to a one. In either mode, the R2424 is configured by the host processor via the microprocessor bus.

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 32-byte interface memory.

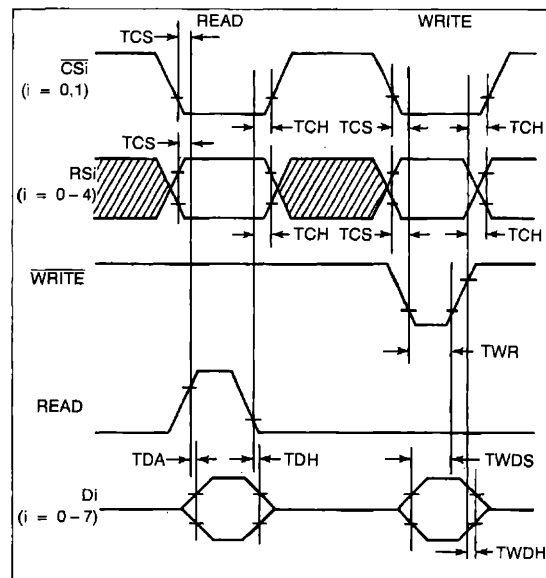
R2424 Hardware Supervisory Circuits

Name	Type	Pin No.	Description
A. OVERHEAD			
DGND	G	5A, 10A, 3C, 8C	Digital Ground
AGND	G	31C, 32C	Analog Ground
+5 VDC	P	19C, 23C, 26C, 30C	+5 Volt Supply
+12 VDC	P	15A	+12 Volt Supply
-12 VDC	P	12A	-12 Volt Supply
POR	OC	13C	Power-On-Reset
B. MICROPROCESSOR INTERFACE			
D7	B	1C	Data Bus (8-Bits)
D6	B	1A	
D5	B	2C	
D4	B	2A	
D3	B	3A	
D2	B	4C	
D1	B	4A	
D0	B	5C	
RS3	I	6C	Register Select (4-Bits)
RS2	I	6A	
RS1	I	7C	
RS0	I	7A	
CS0	I	10C	Chip Select for Bank 0
CS1	I	9C	Chip Select for Bank 1
READ	I	12C	Read Enable
WRITE	I	11A	Write Enable
IRQ	OC	11C	Interrupt Request
C. V.24 INTERFACE			
XTCLK	I	22A	External Transmit Clock
TDCLK	O	23A	Transmit Data Clock
RDCLK	O	21A	Receive Data Clock
CTS	O	25C	Clear-to-Send
TXD	I	24C	Transmit Data
RXD	O	22C	Receive Data
RLSD	O	24A	Received Line Signal Detector
DTR	I	21C	Data Terminal Ready
DSR	O	20A	Data Set Ready
RI	O	18A	Ring Indicator In
D. ANALOG SIGNALS (R2424M ONLY)			
RXA	I	32A	Receive Analog
TXA	O	31A	Transmit Analog
E. SIGNALS TO DAA (R2424M ONLY)			
RD	I	27A	Ring Detect
RCCT	O	28A	Request Coupler Cut Through
CCT	I	29C	Coupler Cut Through
OH	O	29A	Off-Hook Relay Control
F. ANCILLARY FUNCTIONS			
TBCLK	O	27C	Transmit Baud Clock
RBCLK	O	26A	Receive Baud Clock
TLK	I	28C	Talk TLK = Data
ORG	I	16C	Originate ORG = Answer

B Bidirectional
 I Input
 O Output
 OC Open Collector
 P Power
 G Ground

HARDWARE SUPERVISORY CIRCUITS

Signal names and descriptions of the hardware supervisory circuits, including the microprocessor interface, are given in the following table. The microprocessor interface was designed to be compatible with an 8080, 6500, 6800, and 68000 microprocessor.



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
\overline{CS}_i , \overline{RS}_i setup time prior to Read or Write	TCS	30	—	NS
Data Access time after Read	TDA	—	140	NS
Data hold time after Read	TDH	10	50	NS
\overline{CS}_i , \overline{RS}_i hold time after Read or Write	TCH	10	—	NS
Write data setup time	TWDS	75	—	NS
Write data hold time	TWDH	10	—	NS
Write strobe pulse width	TWR	75	—	NS

INTERFACE MEMORY

The R2424 has two banks of 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. These registers, as shown in the following table, are referred to as interface memory.

When information in these registers is being discussed, the format Y:Z:Q is used. The bank is specified by Y (0 or 1), the register by Z (0-F), and the bit by Q (0-7, 0 = LSB). A bit is considered to be 'on' when set to a one.

R2424 Interface Memory

Bank	Reg No. (HEX)	Description	Bank	Reg No. (HEX)	Description
0	0	Do Not Use	1	0	Dial Digit Register
0	1	Do Not Use	1	1	Do Not Use
0	2	Diagnostic Data Real LSB's	1	2	Diagnostic Data Real LSB's
0	3	Diagnostic Data Real MSB's	1	3	Diagnostic Data Real MSB's
0	4	Diagnostic Data Imaginary LSB's	1	4	Diagnostic Data Imaginary LSB's
0	5	Diagnostic Data Imaginary MSB's	1	5	Diagnostic Data Imaginary MSB's
0	6	Do Not Use	1	6	Do Not Use
0	7	Do Not Use	1	7	Do Not Use
0	8	Receiver Status	1	8	Transmitter Status
0	9	Receiver Status	1	9	Configuration
0	A	Configuration	1	A	Configuration
0	B	Configuration	1	B	Configuration
0	C	Configuration	1	C	Configuration
0	D	Configuration	1	D	Configuration
0	E	Handshake Status	1	E	Handshake Status
0	F	Diagnostic Control Register	1	F	Diagnostic Control Register

The interface memory bits are defined in the following table:

Interface Memory Definitions

Name	Definition	Memory Location	Description
AAE	Auto Answer Enable	1:D:4	When on, AAE causes the modem to automatically answer when a ringing signal is present on the line.
AL	Analog Loopback	(0,1):B:0	When on, AL places the modem in analog loopback. (See Software Diagnostic Circuits.)
BUS	Bus Select	(0,1):D:7	When on, BUS places the modem in the parallel control mode. When off, the modem is configured for the serial control mode. BUS can be in either state to configure the modem.
CHAR	Character Length Select	(0,1):C:(3,4)	These bits select either 8, 9, 10, or 11 bit characters. (See Character Length table.)
CRQ	Call Request	(0,1):D:6	When on, CRQ places the transmitter in auto dial and the receiver in tone detect mode. The data placed in the dial digit buffer is then treated as digits to be dialed. After the last digit has been dialed, FF (Hex) should be loaded into the buffer to tell the modem to go to the data state. CRQ in the transmitter (Bank 1) when turned off causes the modem to go on-hook. Therefore, it should be on for the duration of the call and not turned off until it is desired to go on-hook. CRQ in the receiver (Bank 0) must be turned off immediately after ringback is detected to put the modem in the data mode, otherwise no answerback tone will be detected.
CTS	Clear-to-Send	1:8:6	When on, CTS indicates to the terminal equipment that the modem will transmit any data which are present at TXD.
DATA	Talk/Data	1:D:5	When on, DATA places the modem in data state and when off in the talk state.
DDEI	Dial Digit Empty Interrupt	1:E:2	When on, DDEI causes an interrupt to occur when the dial digit register (1:0) is empty (DDRE = 1).
DDRE	Dial Digit Register Empty	1:E:0	When on, DDRE indicates that the dial digit register is empty and can be loaded with new digits to be dialed. After the register is loaded, DDRE goes off.

Interface Memory Definitions (Continued)

Name	Definition	Memory Location	Description
DL	Digital Loopback (Manual)	(0,1):A:5	When on, DL manually places the modem in digital loopback. (See Software Diagnostic Circuits.)
DLO	Data Line Occupied	1:8:7	When on, DLO indicates that the modem is in auto dial, i.e., CRQ is on and the modem is off-hook ready to dial.
DSR	Data Set Ready	1:8:5	When on, DSR indicates that the modem handshake has begun and that the data state will follow. DSR alone should not be used to indicate that the communication channel has been completely established. DSR in conjunction with CTS and RLSD will determine this. DSR will be off in all test states (except optionally for analog loopback) and when the channel is being used for voice communication (talk).
DSRA	Data Set Ready In Analog Loopback	1:C:7	When on, DSRA causes DSR to be on during analog loopback.
DTMF	Touch Tones/ Pulse Dialing	1:B:1	When on, DTMF tells the modem to auto dial using tones. When off the modem should dial using pulses.
DTR	Data Terminal Ready	1:D:3	DTR must be on before the modem will enter the data state, either manually or automatically. DTR must also be on in order for the modem to automatically answer an incoming call.
ENSI	Enable New Status Interrupt	(0,1):E:6	When on, ENSI causes an interrupt to occur when the status bits in registers (0:[8, 9]) and (1:8) are updated. (NEWS=1)
ERDL	Enable Response to Remote Digital Loopback	(0,1):A:7	When on, ERDL enables the modem to respond to another modem's remote digital loopback request, thus going into loopback.
GTE	Guard Tone Enable	1:B:4	When on, GTE causes the specified guard tone to be transmitted (CCITT Configurations only).
GTS	Guard Tone Select	1:B:3	When off, GTS selects the 1800 Hz tone and when on the 550 Hz tone.
IRQ	Interrupt Request	(0,1):E:7	When on, IRQ indicates that an interrupt has been generated.
LCD	Enable Loss of Carrier Disconnect	0:D:2	When on, LCD causes the modem to terminate a call when a loss of received carrier energy is detected after approximately 350 msec.
MODE	Mode Select	(0,1):A:(0-3)	These bits select the compatibility at which the modem is to operate. (See Mode Select table).
NEWC	New Configuration	(0,1):E:3	When on, NEWC tells the modem that a new configuration has been written into the configuration registers. The modem will then read the configuration registers and then reset NEWC. NEWC must be set after a new configuration has been written into the following registers: (0:[A-D]) and (1:[9-D]). The remaining registers do not require the use of NEWC to tell the modem that new data was written into them.
NEWS	New Status	(0,1):E:5	When on, NEWS tells the user that there has been a change of status in the status registers.
ORG	Originate/Answer	1:9:5	When on, ORG tells the modem that it is originating a call and when low answering a call. This is only valid in manual originate/answer and analog loopback.
RDL	Initiate Remote Digital Loopback	(0,1):A:6	When on, RDL causes the modem to initiate a request for the remote modem to go into digital loopback.

Interface Memory Definitions (Continued)

Name	Definition	Memory Location	Description
RDLI	Remote Digital Loopback Indicator	0:8:1	When on, RDLI indicates that the modem has received an RDL request and is in remote digital loopback.
RI	Ring Indicator	1:8:4	When on, RI indicates that a ringing signal is being detected.
RLSD	Received Line Signal Detector	0:8:0	When on, RLSD indicates that the carrier has successfully been received. RLSD will not respond to the 550, 1800, 2100, or 2225 Hz tones.
RSD	Enable Receive Space Disconnect	0:D:1	When on, RSD causes the modem to go on-hook after receiving approximately 1.6 seconds of continuous spaces.
SPEED	Speed Indication	0:9:(4,5)	00 = 300 bps 10 = 1200 bps 01 = 600 bps 11 = 2400 bps
SSD	Enable Send Space Disconnect	1:D:0	When on, SSD causes the modem to transmit approximately 4 seconds of spaces before disconnecting, when DTR is turned off.
ST	Self Test	(0,1):A:4	When on, ST activates self test. ST must be turned off to end the test. (See Software Diagnostic Circuits.)
3DB	3 dB Loss to Receive Signal	1:B:2	When on, 3DB attenuates the received signal 3dB. This is only used if the R2424M will see 0dBm or greater line signal at the receiver input. Insertion of the 3dB loss will then prevent saturation. This bit is not needed with the R2424DC.
TONE	Tone Detect	0:8:7	TONE follows the energy detected in the 340 to 645 Hz frequency band. The user must determine which tone is present on the line by determining the duty cycle. TONE is active only when CRQ in Bank 0 is on.
TXCLK	Transmit Clock Select	1:C:(5,6)	TXCLK allows the user to designate the origin of the transmitter data clock. (See Transmit Clock table.)

SOFTWARE SUPERVISORY CIRCUITS

The operation of the R2424 is affected by a number of software control inputs. These inputs are written into registers within the modem via a microprocessor bus under external control. Modem operation is monitored by various software flags that are read from modem registers using the same microprocessor bus.

The transmit and receive registers contain many bits which perform identical functions and are located in the same memory location only in different banks. Care must be taken to set these bits according to the desired function.

Mode

Configuration	Configuration Word
Bell 212A 1200 Sync.	0 0 1 0
Bell 212A 1200 Async.	0 0 1 1
Bell 212A 300 Async.	0 1 0 0
V.22A 1200 Sync.	1 0 0 0
V.22B 1200 Async.	1 0 0 1
V.22A 600 Sync.	1 0 1 0
V.22B 600 Async.	1 0 1 1
V.22 bis 2400 Sync.	1 1 0 0
V.22 bis 2400 Async.	1 1 0 1
V.22 bis 1200 Sync.	1 1 1 0
V.22 bis 1200 Async.	1 1 1 1

CONFIGURATION REGISTER

The host processor configures the R2424 by writing a control word into the configuration registers in its interface memory space as shown in the following tables:

Character Length

Configuration	Configuration Word
8 bits	0 0
9 bits	0 1
10 bits	1 0
11 bits	1 1

Transmit Clock

Configuration	Configuration Word
Internal	0 0
Not Used	0 1
External	1 0
Slave	1 1

Receiver Interface Memory Bank 0 (CS0)

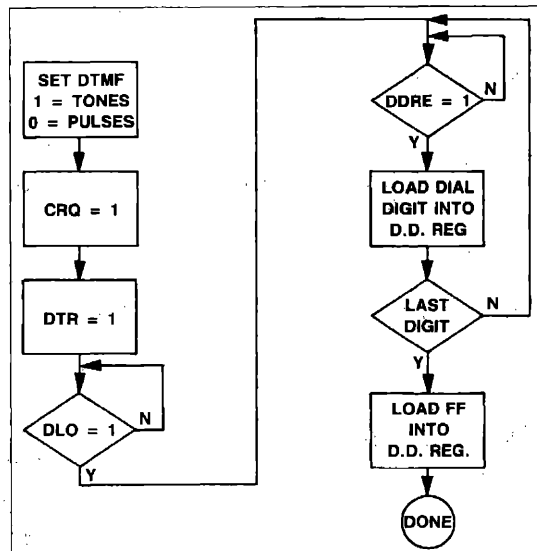
Bit	7	6	5	4	3	2	1	0
Register								
0								
1								
2	Diagnostic Data Real Low							
3	Diagnostic Data Real High							
4	Diagnostic Data Imaginary Low							
5	Diagnostic Data Imaginary High							
6								
7								
8	TONE						RDLI	RLSD
9				Speed				
A	ERDL	RDL	DL	ST				Mode
B								AL
C					CHAR			
D	BUS	CRQ				LCD	RSD	
E	IRQ	ENSI	NEWS		NEWC			
F	Diagnostic Control Register							

Transmitter Interface Memory Bank 1 (CS1)

Bit	7	6	5	4	3	2	1	0
Register								
0	Dial Digit Register							
1								
2	Diagnostic Data Real Low							
3	Diagnostic Data Real High							
4	Diagnostic Data Imaginary Low							
5	Diagnostic Data Imaginary High							
6								
7								
8	DLO	CTS	DSR	RI				
9			ORG					
A	ERDL	RDL	DL	ST				Mode
B			TX LEVEL	GTE	GTS	3DB	DTMF	AL
C	DSRA		TXCLK		CHAR			
D	BUS	CRQ	DATA	AAE	DTR			SSD
E	IRQ	ENSI	NEWS		NEWC	DDEI		DDRE
F	Diagnostic Control Register							

AUTO DIAL SEQUENCE

The following flow chart defines the auto dial sequence via the microprocessor interface memory.



Auto Dial Sequence Flow Diagram

Note: The modem timing for the auto dialer accounts for inter-digit delay for pulses and tones.

DIAGNOSTIC CAPABILITIES

The R2424 provides the user with access to much of the data stored in the modems memories. This data is a useful tool in performing certain diagnostic functions.

RAM ACCESS CODES

The RAM access codes defined in the table below allow the host processor to read diagnostic data from the modem receiver. The access codes should be loaded into the diagnostic control register (0:F). The appropriate diagnostic data will then be available in the diagnostic data registers (0:[2-5]).

RAM Access Codes Bank 0

Function	Access	Data Type
Scrambled Data (Imag. Reg.)	00	Real
Self Test Error Counter (Real Reg.)	00	Real
Equalizer Tap Coefficients	01-09	Complex
Phase Error (Real Reg.)	0C	Real
Rotated Equalizer Output (Received Point Eye Pattern)	0D	Complex
Rotated Angle (Imag. Reg.)	0E	Real
Low Pass Filter Output	40	Complex
Input Signal to Equalizer Tap Coefficients	41-49	Complex
Decision Points (Ideal)	4D	Complex
Rotated Error	4E	Complex
Equalizer Output	4F	Complex
Demodulator Output	52	Complex

TEST

The specifications for R2424 tests are defined as follows:

Self tests can be initiated by setting bits ([0,1]:A:4) to a 1. It is possible to perform the tests with or without the DTE connected to the modem. During any self test TXD and RTS are ignored. Note that self tests do not test asynchronous-to-synchronous converter circuits in either the transmitter or receiver.

Error detection is accomplished by monitoring a counter in the RAM. If the counter increments during the self test, an error was made. The counter contents are available in the diagnostic registers when the RAM access code 00 is loaded in the diagnostic control register (0:F).

Self test end-to-end—Upon activation of self-test an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate are applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals are connected to the output of the descrambler.

Self test with loop 3—Loop 3 is applied to the modem as defined in recommendation V.54. Self-test is activated and DCE operation is as in the end-to-end test. In this test DTR is ignored.

Self test with loop 2—The modem is conditioned to instigate a loop 2 at the remote modem as specified in recommendation V.54. Self-test is activated and DCE operation is as in the end-to-end test.

Loopbacks—Remote digital loopback, digital loopback, and local analog loopback can be initiated via the interface memory, as follows:

1. **Digital Loopback.** The R2424 can be manually conditioned to loop the received data back to the transmitter by setting

the DL bits ([0,1]:A:5). DL should be set during the data mode. DSR and CTS will be off. The local modem can then be tested from the far-end by using the terminal equipment at the far-end to transmit a test pattern and examine the looped data. At the far-end modem, all interface circuits behave normally as in the data mode. At the conclusion of the test, DL must be turned off. The local modem will then return to the normal data mode with control reverting to the DTE's DTR.

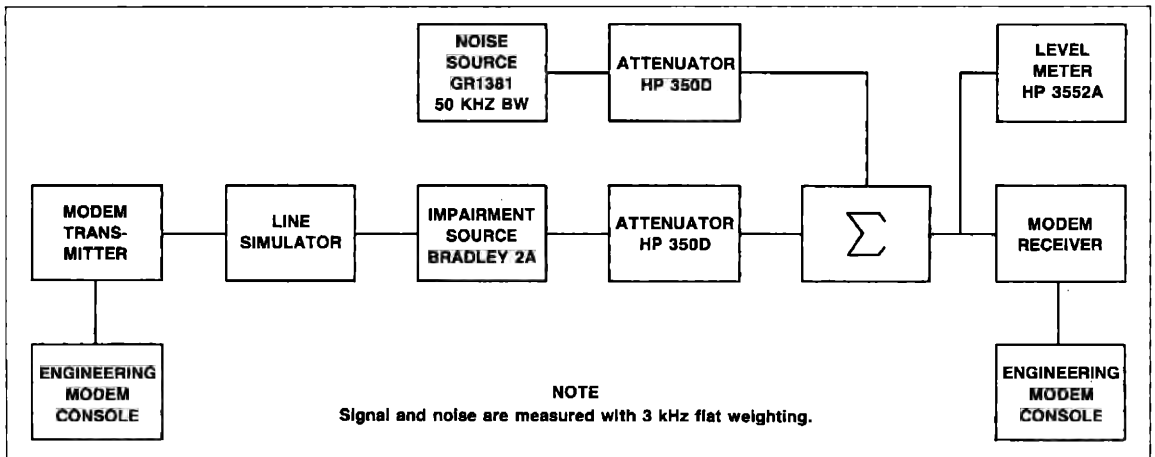
2. **Local Analog Loopback (V.54 Loop 3).** The R2424 is capable of entering into a local analog loopback (V.54 Loop 3). In this loop, the transmitter's analog output is coupled to the receiver's analog input at a point near the modem's telephone line interface. An attenuator is introduced into the loop such that the signal level coupled into the receive path is approximately — 16 dBm attenuation.
3. **Remote Digital Loopback (V.54 Loop 2) (Bell 212A and CCITT V.22 bis and V.22).** The R2424 is capable of entering into a remote digital loopback. Remote digital loopback may be locally entered by the interface memory. Remote digital loopback cannot be performed simultaneously with local analog loopback.

POWER-ON INITIALIZATION

When power is applied to the R2424, a period of 100 to 300 ms is required for initialization. The power-on-reset (POR) signal remains low during the initialization period. After the low to high transition of POR, the modem is ready to be configured.

The modem automatically defaults to V.22 bis 2400 bps, answer state using serial start-stop data, 10 bits per character.

POR can also be used to initialize the user's host processor. It may be connected to a user supplied power-on-reset signal in a wire-or configuration.



BER Performance Test Set-up

PERFORMANCE

Whether functioning as a V.22 bis, V.22, or Bell 212A type modem, and regardless of simulated line condition or introduced line impairment, the R2424 provides unexcelled high performance to the user.

BIT ERROR RATES

The Bit Error Rate (BER) performance of the R2424 is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of -43 dBm.

INTERFACE CIRCUIT CHARACTERISTICS

DIGITAL INTERFACE CIRCUITS

Digital Input Characteristics

Input Logic State	Allowed Input Voltage Levels
Low	0.0V to +0.8V at -2.5 μ A
High	+2.0V to +5.0V at +2.5 μ A
Notes:	
1. The digital inputs are directly TTL/CMOS compatible. The capacitive loading on each input is 25 pF (maximum).	
2. Positive current is defined as current into the node.	

Digital Output Characteristics

Output Logic State	Allowed Output Voltage Levels
Low	+0.4V at +1.6 mA
High	+2.4V at -100 μ A
Notes:	
1. The digital outputs are directly TTL/CMOS compatible. The capacitive loading on each output is 50 pF (maximum).	
2. Positive current is defined as current into the node.	

ANALOG INTERFACE CIRCUITS

TRANSMISSION LINE INTERFACE

The R2424DC interface to the telephone line is the Tip and Ring leads. Lightning induced surge voltages and other hazardous voltages which may appear on the telephone line are limited to approximately 7V peak between the secondary leads of the line coupling transformer.

The DAA (R2424DC only) is bi-directional as required by 2-wire full-duplex circuits.

Connection to the telephone line interface pins of the R2424DC to the network are made via the RJ11, as shown in the table below:

R2424DC Network Interface

Connection Type	Telco	Mnemonic	Function
VSOC	1		
RJ11	2		
	3	R	Ring-one side of telephone line
Jack	4	T	Tip-one side of telephone line
	5		
	6		

RING INDICATOR

The R2424 provides a ring indicator (\overline{RI}) output; its low state indicates the presence of a ring signal on the line. The low condition appears approximately coincident with the on segment of the ring cycle (during rings) on the communication channel. (The ring signal cycle is typically two seconds on, four seconds off.) The high condition of the indicator output is maintained during the off segment of the ring cycle (between rings) and at all other times when ringing is being received. The operation of \overline{RI} is not disabled by an off condition on Data Terminal Ready.

\overline{RI} will respond to ring signals in the frequency range of 15.3 Hz to 68 Hz with voltage amplitude levels of 40 to 150 Vrms (applied across Tip and Ring), with the response times given in the following table:

RI Response Time

RI Transition	Response Time
Off-to-On	125 ms to 400 ms
On-to-Off	75 ms to 250 ms

This off-to-on (on-to-off) response time is defined as the time interval between the sudden connection (removal) of the ring signal across Tip and Ring and the subsequent on (off) transition \overline{RI} .

OH (OFF-HOOK)

The R2424M provides an output OH (Off-Hook) which indicates the state of the OH relay. A low condition on OH implies the OH relay is closed and the modem is connected to the telephone line. A high condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.

RD

RD indicates to the R2424M by an on (low) condition that a ringing signal is present. The **RD** signal should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40V rms, 15 to 68 Hz appearing across Tip and Ring with respect to ground.

RCCT

RCCT is used to request that a data transmission path through the DAA be connected to the telephone line. When **RCCT** goes off (low), the cut-through buffers are disabled and **CCT** should go off (high) within 1 msec. **RCCT** should be off during dialing but on for tone address signaling.

CCT

An on (low) signal to the **CCT** lead indicates to the R2424M that the data transmission path through the DAA is connected.

AUDIO INTERFACE INPUT IMPEDANCE

The specifications for the audio interface input impedance are given in the following table:

Audio Interface Input Impedance

On/Off Hook	Measurement
On-Hook (DC)	The DC resistance between Tip and Ring, and between either Tip or Ring and signal ground is greater than 10 megohms for DC voltages up to 100 volts.
On-Hook (AC)	The on-hook AC impedance measured between Tip and Ring is less than 40K ohms (15.3 Hz minimum).
Off-Hook (DC)	Less than 200 ohms.
Off-Hook (AC)	600 ohms nominal when measured between Tip and Ring.

TRANSMITTER OUTPUT

Basic telephone company requirement is that the signal level received at the relevant local central office not exceed -12 dBm. Several different "connection arrangements" have been established (as documented in Part 68) to accomplish this goal.

When the permissive connection arrangement is used, the transmit output signal level appearing across Tip and Ring (with a 600 ohm resistive load across Tip and Ring) will not exceed -9 dBm. The output level is set at a fixed -10 dBm (nominal). The permissive wall jacks used for data connections are the same jacks used for standard voice installations. The permissive connection arrangement allows greater mobility for user equipment.

When the programmable connection arrangement is used, the maximum output transmit signal level allowed to appear across the Tip and Ring (again, terminated with 600 ohms) is set by a resistor installed by the telephone company in their wall jack at the customer location. The resistor (which is one of thirteen possible values) interacts with the modem through modem leads PR and PC to program the maximum output level, in one dB steps between -12 dBm and 0 dBm. (The resistor is selected by the telephone company jack installer after he has measured the line loss from the customer location to the local telephone company central office).

INSTALLATION**IMPORTANT NOTICE TO USER**

The modem contains protective circuitry registered with the Federal Communications Commission (FCC) Part 68 to allow direct connection to the switched telephone network. To comply with the FCC regulations the following is required:

1. All direct connections to the telephone lines shall be made through standard plugs and telephone company provided jacks.
2. It is prohibited to connect the modem to pay telephones or party lines.
3. You are required to notify the local telephone company prior to the connection and upon final disconnection of the modem. You must supply to the telephone company the make, model number, FCC registration number, ringer equivalence and particular line to which the connection is to be made. If the proper jacks are not available, you must order the type of jacks to be used from the telephone company.
4. You should disconnect the modem from the telephone line if it appears to be malfunctioning. Reconnect it only when it can be determined that the telephone line is the source of trouble. If the modem needs repair, return it to Rockwell International. This applies to equipment both in and out of warranty. Do not attempt to repair the unit as this will violate FCC rules.
5. The modem contains protective circuitry to prevent harmful voltages from being transmitted to the telephone network. If however such harmful voltages do occur, then the telephone company shall:
 - Promptly notify you of the discontinuance.
 - Afford you the opportunity to correct the situation which caused the discontinuance.

The FCC requires that the following label be prominently displayed on an outside surface of the OEM's end product.

 - Unit contains Registered Protective Circuitry which complies with Part 68 of FCC Rules.
 - FCC Registration Number: Applied For
 - Ringer Equivalence: 0.5

Size of the label should be such that all the required information is legible without magnification.

GENERAL SPECIFICATIONS

Power Requirements

Voltage*	Tolerance	Current (Max)
+ 5 Vdc	± 5%	< 500 ma
+ 12 Vdc	± 5%	< 10 ma
- 12 Vdc	± 5%	< 50 ma

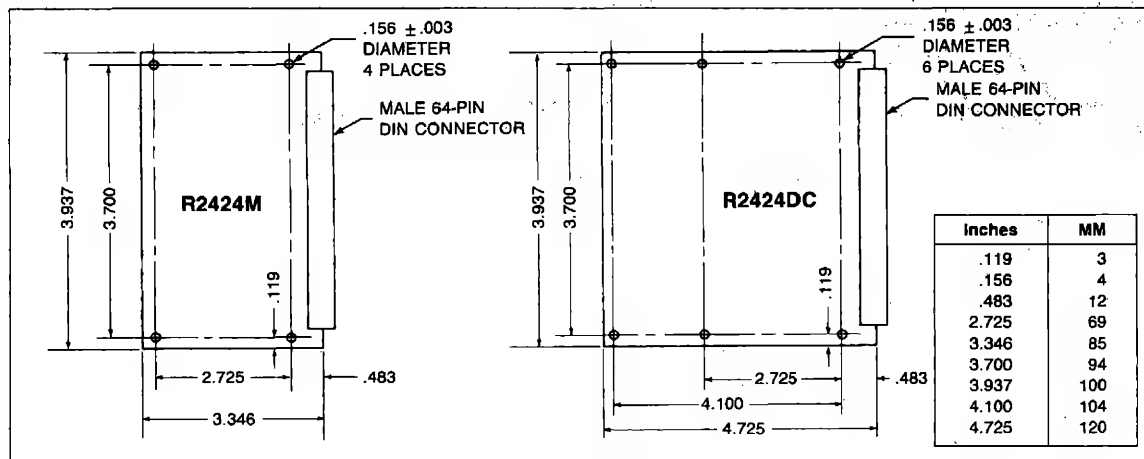
*All voltages must have ripple ≤ 0.1 volts peak-to-peak.

Environmental

Parameter	Specification
Temperature: Operating	0°C to +60°C (32 to 140°F)
Storage*	-40°C to +80°C (-40 to 176°F)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude:	-200 to +10,000 feet
*PCB's are stored in heat sealed antistatic bags and shipping containers.	

Mechanical

Board Structure:	Single PC board with right angle male DIN connector.
Mating Connector:	Female 3 row 64 pin Euroconnector (DIN) with rows A and C populated. Recommended mating connector: Winchester 96S-6043-0531-1 or equivalent.
PCB Dimensions:	
DC Version	Width 3.94 in. (100 mm) × Length 4.725 in. (120 mm) × Height 0.75 in. (19 mm)
M Version	Width 3.94 in. (100 mm) × Length 3.35 in. (85 mm) × Height 0.40 in. (10 mm)
Weight:	Less than 0.45 lbs. (0.20 kg.)



Printed Circuit Board Dimensions



R24DC **2400 BPS DIRECT CONNECT MODEM**

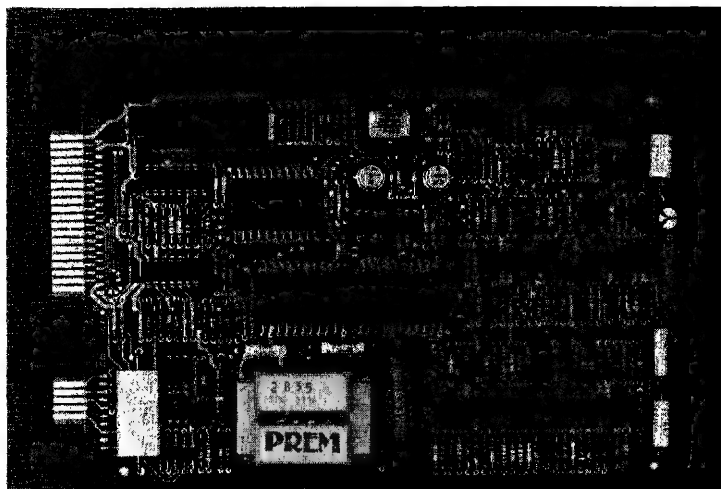
INTRODUCTION

The Rockwell R24DC is a high performance synchronous serial 2400 bps DPSK modem. Extensively utilizing MOS/LSI technology with registered protective circuitry, the R24DC is ideally suitable for direct connection to the domestic switched network or two-wire private lines. Performance and versatility are enhanced while cost and size are reduced by the on-board Rockwell PPS-4/1 One Chip Microcomputer

Having Bell 201C and CCITT V.26 bis compatibility, the R24DC offers the user a high performance 2400 bps modem that is FCC registered for direct connection to the dial-up network. No re-registration of OEM equipment is required when the simple installation instructions, supplied with the R24DC, are followed. OEM's can easily incorporate this single (5" x 8") card into their computer terminals, communication networks, PABX equipment, data concentrators, stand-alone box modems or almost any application where reliable data communication is required.

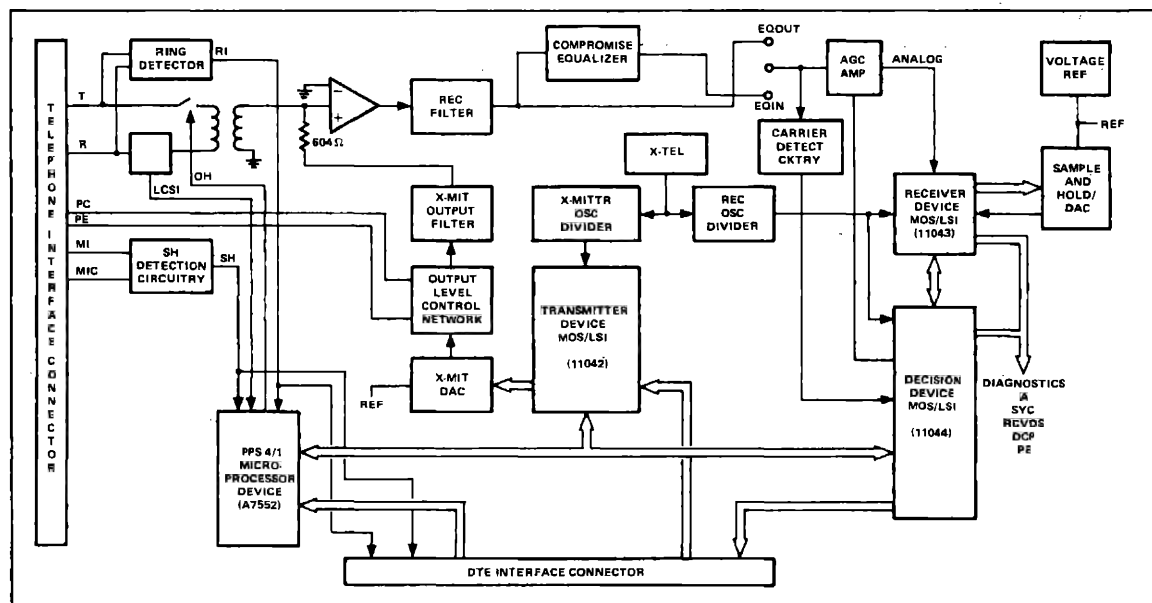
FEATURES

- High Performance; Low Cost
- LSI High Density; Low Power
- Microcomputer Controlled Line Connect/Disconnect Sequence; Low Component Count
- Bell 201 C, CCITT V.26 bis Compatible
- Half Duplex (2-Wire) Operating Mode
- 2400 BPS Data Rate
- Auto or Manual Answer
- Auto or Manual Dial Through (Pulse Dialing)
- Automatic Answer Back Tone Generation upon Auto Answer
- Direct Connect to Switched Network
- Programmable or Permissive Connection Arrangement
- Local Analog Loopback Test Mode
- Compromise Equalizer (Strap Selectable)
- Scrambler/Descrambler Facility (Selectable)
- Line Current Sensing (Selectable)
- DTE Interface LSTTL/CMOS Compatible Levels. RS-232-C Functions
- External Transmit Data Clock Tracking
- Power Requirements, $\pm 12V$, $+5V$
- Typical Power Consumption 3 Watts
- Diagnostic Outputs Available for Eye Pattern and Data Quality Monitor
- 15 Second Abort Timer (Selectable)



R24DC Modem

FUNCTIONAL SPECIFICATIONS



R24DC Functional Block Diagram

Transmitter Carrier Frequency — $1800 \text{ Hz} \pm 0.01\%$

Echo Suppression and Answering Tone Frequencies — $2100 \text{ Hz} \pm 0.01\%$ or $2025 \text{ Hz} \pm 0.01\%$.

Received Signal Frequency Tolerance — The receiver can adapt to received frequency errors up to $\pm 10 \text{ Hz}$ with less than a 0.5 dB degradation in bit error rate.

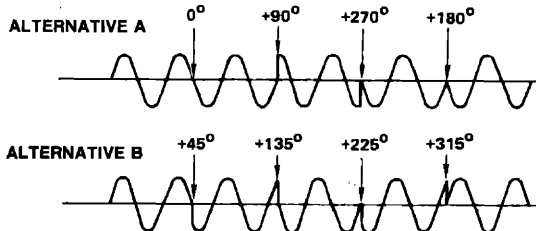
Data Signaling and Modulation Rate — The normal signaling rate is $1200 \text{ baud} \pm 0.01\%$, and a data rate of $2400 \text{ bps} \pm 0.01\%$. The fallback signaling rate is $1200 \text{ baud} \pm 0.01\%$, and a data rate of $1200 \text{ bps} \pm 0.01\%$.

Transmitted Data Spectrum — The transmitted spectrum's bandwidth extends from 800 Hz to 2800 Hz . Phase distortion characteristics are within the limits specified in CCITT Recommendation V.26 bis. The out of band signal power limitations meet those specified by Part 68 or Tariff 261 of the FCC's regulations, and typically exceed the requirements of international regulatory bodies as well.

Data Encoding (DPSK) — At 2400 bps , differential 4-phase modulation is employed. The data stream to be transmitted is

2400 BPS		
DIBIT	PHASE CHANGE	
	V.26A	V.26B/Bell 201
00	0°	$+45^\circ$
01	$+90^\circ$	$+135^\circ$
11	$+180^\circ$	$+225^\circ$
10	$+270^\circ$	$+315^\circ$

divided into pairs of consecutive bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element. Two alternative arrangements of coding are possible (in accordance with CCITT Recommendations V.26 and V.26 bis) as shown in the following chart.



Reference Line Signal Diagram (V.26 A&B)

At 1200 bps , differential 2-phase modulation is employed. Each bit to be transmitted is encoded as a phase change relative to the phase of the immediately preceding signal element. The encoding is in accordance with CCITT Recommendation V.26 bis as shown in the following chart.

1200 BPS	
BIT	PHASE CHANGE
0	$+90^\circ$
1	$+270^\circ$

Turn On Sequences — A total of six selectable turn on sequences can be generated by the transmitter of the R24DC, as shown in the following chart.

TYPE OF LINE SIGNAL	SEGMENT 1	SEGMENT 2	TOTAL OF SEGMENTS 1, 2	
TURN-ON SEQUENCE NUMBER	CONTINUOUS UNSCRAMLED ONES	CONTINUOUS SCRAMBLED ¹ ONES	NOMINAL TOTAL TURN ON SEQUENCE TIME ²	COMMENTS
1	90 ms	0 ms	90 ms	V.26, V.26 bis
2	8.33 ms	81.67 ms	90 ms	(scrambler inserted)
3	148.3 ms	0 ms	148.3 ms	Bell 201C
4	8.33 ms	140 ms	148.3 ms	(scrambler inserted)
5	220 ms	0 ms	220 ms	V.26 bis
6	8.33 ms	211.7 ms	220 ms	(scrambler inserted)

As is evident from the above for those turn-on sequences for which the scrambler is inserted, the transmitted line signal corresponds to a continuous "one", unscrambled, for 8.33 ms-ten baud (symbol) intervals — followed by the transmission of a continuous "one", scrambled, for the remainder of the turn-on sequence.

Turn Off Sequence — When the R24DC transmitter has been sending data and Request-to-Send is turned off, any remaining data bit information is transmitted within 6 milliseconds.

Response Times of Clear-to-Send — The Clear-to-Send response times are determined by the selected configuration of the R24DC and its associated turn-on sequence, as shown in the following chart.

TURN-ON SEQUENCE NUMBER	CLEAR-TO-SEND RESPONSE TIMES ¹		COMMENTS
	OFF-TO-ON	ON-TO-OFF	
1	90 ms	0 ms	V.26 bis
2	90 ms	0 ms	V.26 bis w/scrambler
3	148.3 ms	0 ms	Bell 201C
4	148.3 ms	0 ms	Bell 201C w/scrambler
5	220 ms	0 ms	V.26 bis
6	220 ms	0 ms	V.26 bis w/scrambler

The tolerance on each Off-to-On and On-to-Off response time is (+3.4, -0.1) ms.

Scrambler/Descrambler — The R24DC incorporates a self-synchronizing scrambler/descrambler. This feature is enabled by a discrete digital input.

Carrier Detection — The receiver circuit of the R24DC contains a received line signal detector which indicates the presence of energy at the receiver input above a certain threshold for a minimum amount of time.

Carrier Detect Thresholds

Received Level	Carrier Detect
Greater than -43 dBm	On (Line signal present)
Less than -48 dBm	Off (Line signal not present)

Carrier Detect Response Time

Carrier Detect Transition	Response Time
Off-to-On	14 ± 1 ms
On-to-Off	8 ± 3 ms

Clamping — The following clamps are provided:

1. Received Data. The Received Data output is clamped to a mark when Carrier Detect is off. This action prevents disturbances on the line from getting through the receiver circuit to the data output.
2. Carrier Detect Clamp. The Carrier Detect output is clamped off (squelched) during the time when Request-to-Send is on. An option extends this clamp for 148 ms beyond transitioning off; thus providing echo protection.
3. Receive Clock Clamp. The Receive Clock output is clamped off when Carrier Detect is off. This action prevents any disturbances from propagating through the receiver circuit to the receive clock output.

Equalizer — The R24DC contains a fixed compromise delay equalizer, which can be used to improve performance over the domestic switched network. The equalizer may optionally be positioned in the receiver, or removed entirely, by means of a jumper plug. The equalizer has a nominally flat 0.0 dB amplitude response.

Test Pattern Generation — The scrambler/descrambler function can be used to implement a 127-bit test pattern feature. For example, a constant mark input could be scrambled and transmitted as a pseudo-random signal to be descrambled at the receiver back to the constant mark. A transmission error would be represented as a space for the duration of an incorrect bit.

Receive Level — The R24DC receives line signals from 0 to -43 dBm.

Transmit Timing — The R24DC generates a Transmit Clock having the following characteristics: Frequency — 2400 Hz ± 0.01% (1200 Hz ± 0.01% in fallback mode), duty cycle — 50 ± 1%. The R24DC is also optionally capable of tracking an External Transmit Clock supplied by the user. Both have similar characteristics.

Receive Timing — The modem provides a data derived Receive Clock output in the form of a nominal squarewave (50 ± 1% duty cycle). The modem timing recovery function is capable of tracking a ± 0.01% frequency error in the associated transmit timing source.

Transmit Level — The R24DC transmitted output line signal level may be regulated in either the permissive or programmable modes. In the permissive mode, the transmitted line signal level is -9 dBm maximum. In the programmable mode, the transmitted line signal level is set by an external resistor installed by the telephone company in the wall jack. Using this method, the transmitted line signal level can be controlled in increments of 1 dBm from 0.0 to -12 dBm, depending on the value of resistance installed.

Answering Tone Generation — When in the automatic answering mode, the R24DC generates a selectable answering tone of 2100 Hz \pm 0.01% or 2025 Hz \pm 0.01%. It is also capable of optionally providing this tone when in the manual answer mode.

Answering Tone Frequency

INPUT SELECT 1 (P1-34)	ANSWERING TONE FREQUENCY
High	2100 Hz
Low	2025 Hz

Satellite Option and DSR Selection

Satellite Option	DSR (P1-30) During Analog Loopback	AL-DSR Enable (P1-12)
Yes	OFF (High)	High
No	ON (Low)	Low
Yes	ON Low	Wired to Analog Loopback
No	OFF (High)	Wired to Analog Loopback ¹
1. Inverse of Signal applied to Analog Loopback Input.		

Baud Clocks — Symbol or baud timing is available for both the transmitter and receiver functions. These signals have characteristics similar to the data clocks except that their frequency is equal to the signalling rate of 1200 Hz \pm 0.01%.

Analog Loopback — The R24DC can be locally commanded into local analog loopback (CCITT Loop 3) via digital input Analog Loopback, when in the wait mode.

Data Structure

INPUT		DATA STRUCTURE
DATA SIGNALLING RATE SELECTOR (P1-16)	V.26 A/B (P1-14)	
Low	Low	2400 bps Alternate A
Low	High	2400 bps V.26 Alternate B (Bell 201C)
High	Low or High	1200 bps

Abort Timer — The R24DC contains a 15 \pm 1 second abort timer, which may be enabled via the Abort Enable input.

Line Current Interrupt Disconnect — The R24DC contains a 475 \pm 125 ms line current interrupt abort timer, which may be enabled via the LCIS Enable input.

The digital interchange circuits provide control, status indicators, data clocks and data interface. Traditional RS232-type control functions and additional signals allow the user to access the inherent flexibility and monitoring capabilities of the R24DC.

Carrier Detect Squelch

INPUTS			SQUELCH STATUS ¹
ANALOG LOOPBACK (P1-33)	SELECT 2 (P1-35)	REQUEST- TO-SEND (P1-11)	
Low	Low or High	Low or High	No Squelch
High	Low or High	Low	Squelch
High	High	Low \Rightarrow High	Extended Squelch ²
High	Low	Low \Rightarrow High	No Extended Squelch
¹ "Squelch" means that Carrier Detect is clamped off (high) regardless of the level of received line signal. When "extended squelch" is enabled, squelch occurs both during the time when Request-to-Send is on (low) and for 148.3 ms (+3.4, -0.1 ms) following the On-to-Off transition of Request-to-Send.			

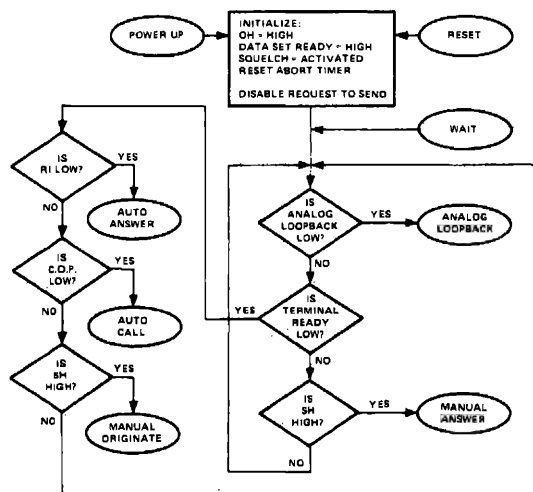
Selection Of Clear-To-Send Response Times

TURN-ON SEQUENCE	INPUTS			CLEAR-TO-SEND RESPONSE TIME ¹ (ms)	
	SELECT 1 (P1-34)	SCRAMBLER ENABLE (P1-15)	SELECT 2 (P1-35)	OFF-TO-ON	ON-TO-OFF
1	High	Low	Low	90	0
2	High	High	Low	90	0
3	Low	Low	Low or High	148.3	0
4	Low	High	Low or High	148.3	0
5	High	Low	High	220	0
6	High	High	High	220	0
The tolerance on each Off-to-On and On-to-Off response is (-3.4, -0.1 ms).					

OPERATING MODES

Line connect and disconnect sequences are controlled automatically by the R24DC which is at all times in one of the following modes:

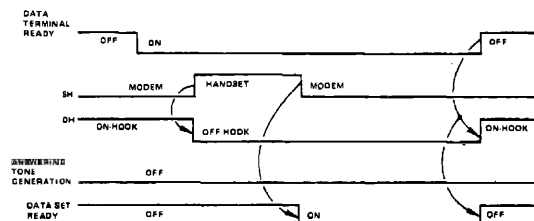
Wait Mode — This is a hot-standby mode. The R24DC enters this mode upon a power-up, Reset, or whenever an operational mode is exited. The following diagrams illustrate the sequence of events for the Wait mode.



Wait Mode Flow Diagram

Analog Loopback Mode — This mode provides the capability of diagnosing a problem in the communications link. In this mode, the transmitter's analog output is connected to the receiver's analog input through an attenuator.

Manual Originate Mode — This mode provides the capability of manual call origination. Calls may be originated in the usual manner by a telephone set. Signal sequence for this mode is shown in the following diagram.



Manual Originate Mode Sequence

Automatic Call Mode — This mode provides the capability of automatically originating calls by using the pulse dialing technique.

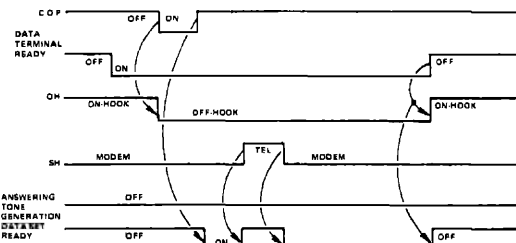
The R24DC allows the user to auto dial by controlling inputs DTR, C.O.P. and DP. To originate a call, DTR and C.O.P. must

be on. Then DP (normally off) is pulsed at a rate of 9.5 ± 1.5 pulses per second.

The pulse requirement is a uniform train with break intervals at 58% to 64%.

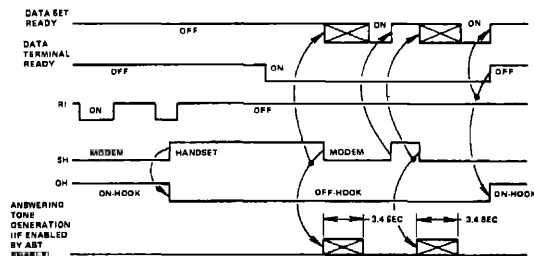
The interdigit time (i.e., the time between the end of the last pulse of a given digit and the beginning of the first pulse of a subsequent digit) should be between 700 ms and 3 seconds.

C.O.P. is turned off after the called modem answers. Signal sequence for this mode is shown in the following diagram.



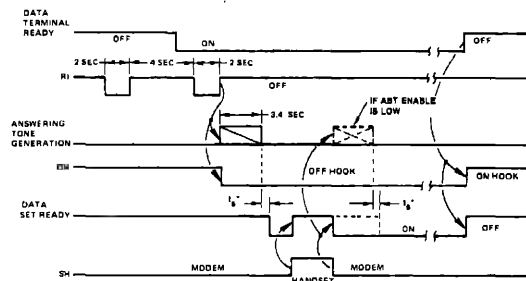
Automatic Call Mode Sequence

Manual Answer Mode — This mode provides the capability of manually answering calls with a telephone set. Signal sequence for this mode is shown in the following diagram.



Manual Answer Mode Sequence

Automatic Answer Mode — This mode provides the capability of automatically answering calls. Signal sequence for this mode is shown in the following diagram.



$t_{\text{SH}} = 275 \text{ ms}$ if satellite option is selected
 $= 65 \text{ ms}$ if satellite option is not selected

Automatic Answer Mode Sequence

INTERFACE CRITERIA

The R24DC interface signals are classified as digital interchange signals and analog signals. These signals interface to the user through the board edge connector.

Digital Interchange Circuits — The characteristics of the R24DC digital inputs and outputs are given in the following charts.

Digital Input Characteristics

Input Logic State	Allowed Input Voltage Levels
Low	0.0V to 0.8V sinking $<10 \mu\text{A}$
High	+4.0V (VSS - 1V) to +5.0V (VSS) sourcing $<10 \mu\text{A}$
The digital inputs are directly CMOS compatible. The capacitive loading on each input is 25 pF (maximum).	

Digital Output Characteristics

Output Logic State	Allowed Output Voltage Levels
Low	0.0V to 0.4V sinking 0.36 mA
High	4.0V (VSS - 1V) to 5.0V (VSS) sourcing 100 μA
The digital outputs are directly CMOS or low-power Schottky TTL compatible.	

DIGITAL OUTPUT CHARACTERISTICS (EXCEPTIONS)

The exceptions to the above are outputs OH, RI, SH and A. Outputs OH, RI and SH have the following characteristics:

Output Logic State	Allowed Output Voltage Levels
Low	0.0V to 0.4V sinking 0.36 mA
High	2.4V to 5.0V (VSS) sourcing 100 μA

Output A, useful in the generation of eye pattern and diagnostic information, switches from +5.0V to -12.0V.

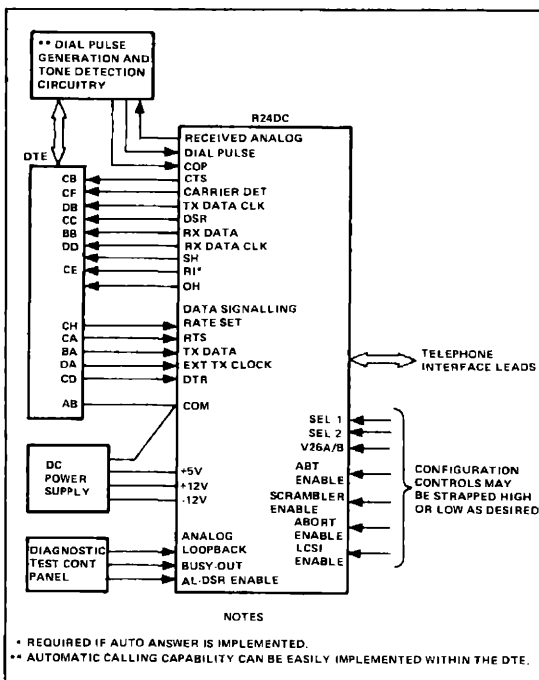
Audio Interface Input Impedance

Parameter	Specification
On-Hook DC	DC resistance between Tip and Ring, and between either Tip or Ring and signal ground is greater than 10 megohms for DC voltages up to 100 volts.
On-Hook AC	On-hook AC impedance measured between Tip and Ring is less than 40 K ohms (15.3 Hz minimum)
Off-Hook DC	Less than 200 ohms
Off-Hook AC	600 ohms nominal when measured between Tip and Ring
Longitudinal Balance	Meets requirements of FCC Rules, Part 68
FCC Registration Number: AMQ9SQ-68B13-DM-R Ringer Equivalence: 0.9B	

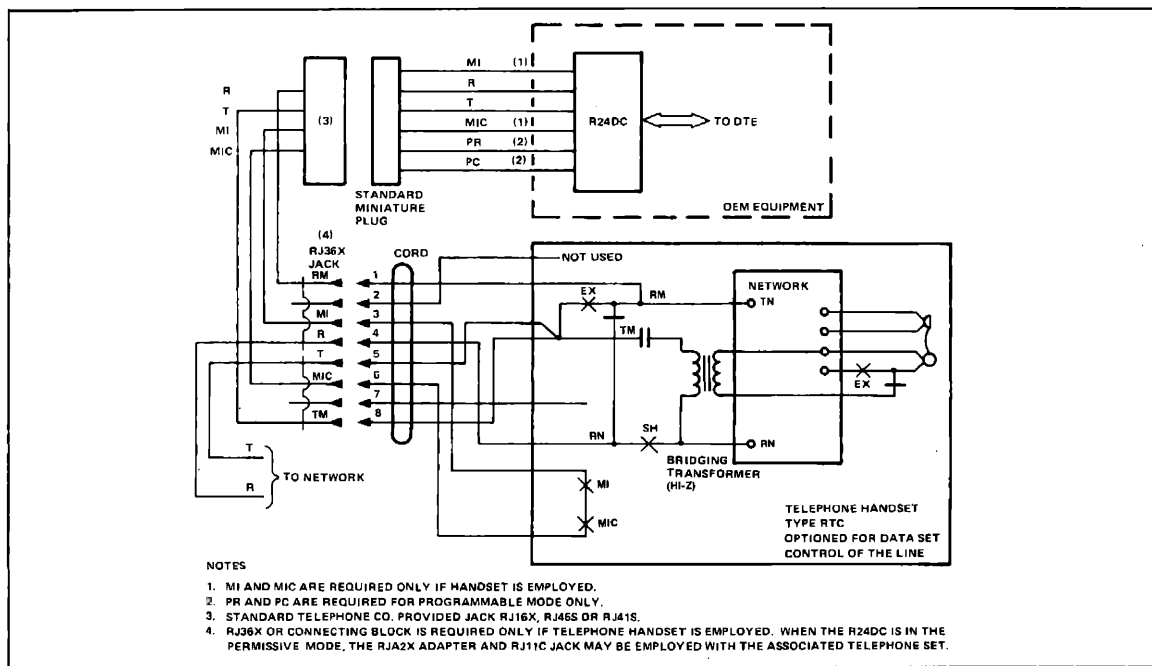
Analog Interface Circuits — The analog interface circuits defined in the following charts provide power and switched network connections and a means for the user to monitor the incoming line signals.

Analog Interface Circuits

TERM	PIN NUMBER	DESCRIPTION
+12V	P1-40	+12V Power Supply
-12V	P1-38	-12V Power Supply
+5V	P1-1	+5V Power Supply
COMMON	P1-2, P1-4	Ground (signal and power return)
Receiver Analog	P1-32	Low impedance output of R24DC receive filter. Gain from Tip and Ring to Receiver Analog is nominally 12.7 dB
TELEPHONE INTERFACE LEADS		
TIP	P2-9	Telephone Line Leads
RING	P2-10	
PR	P2-2	Leads to external wall jack resistor for programmable mode
PC	P2-4	
MI	P2-3	Leads routed to contact on exclusion key of associated telephone set
MIC	P2-1	



Typical R24DC to OEM Interconnections
for Half-Duplex Applications



Typical R24DC to Network Interconnection

Telephone Line and OEM Connections — Connection of the R24DC telephone interface pins to the network is made via standard jacks and plugs. A typical installation, including an optional telephone set, is illustrated.

Telephone Set — If it is desirable to have manual call origination or alternate voice capability, an exclusion key telephone set (configured as Modem Controls the Line) may be ordered from your local telephone company.

Mounting and Signal Routing — The R24DC may be physically incorporated into your OEM end product by using either the four corner (0.156 inch) diameter mounting holes or by using board guides. The electrical interface is via edge connector(s).

Interface Mating Connectors

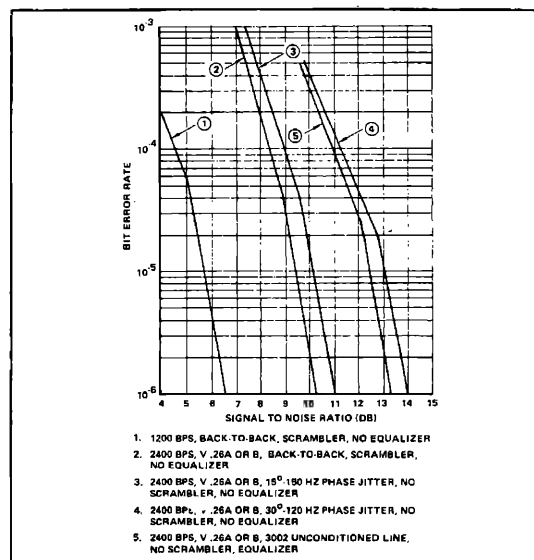
Type/ Manufacturer	P1 (DTE) Connector	P2 (Telephone Line) Connector
Type:	40 pin 0.100 in. spacing 20 pins per side	10 pin 0.100 in. spacing 20 pins per side
Winchester:	53-40-0	53-10-0
T&B Ansley:	609-4015M	609-1015M
Spectra-Strip:	807-4005-001	807-1005-001

PERFORMANCE DATA

The R24DC is a high performance synchronous 2400 bps DPSK modem, utilizing a coherent demodulation technique to achieve reliable operation over the switched network or unconditioned lines.

Timing Jitter — The maximum steady state timing jitter of Received Clock with respect to Transmit Clock is less than 10% p-p for an input signal-to-noise ratio of 12 dB.

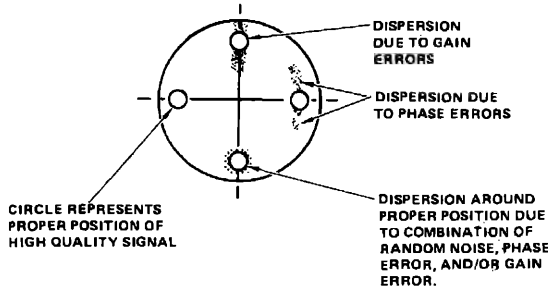
Bit Error Rate — The following graph represents typical R24DC performance.



Typical Bit Rate Performance

Phase Error — Phase error can be measured by using the modem's output signals PE, SYC, and A. With an external test circuit, a numerical value can be derived to indicate the quality of received data. This numerical value can be directly correlated to bit error rate performance. The required test circuit can be implemented with discrete circuitry or in software within a microcomputer.

Eye Pattern — By using the modems digital output signals RCVDS, SYC, and A along with an added test circuit, the user can generate an oscilloscope quadrature eye pattern. This pattern displays the received signal as a group of dots in the base-band signal plane; hence, it is a graphic representation of modem performance.



Typical Eye Pattern: 4 Phase-2400 BPS-1200 Baud (V26A)

Phase error and eye pattern can be extremely useful for modem acceptance testing, product evaluation, and observation of line signal quality under actual operation.

POWER REQUIREMENTS

Voltage	Ripple	Maximum Current
+5 VDC $\pm 5\%$	100 mV p-p	110 mA
+12 VDC $\pm 5\%$	50 mV p-p	70 mA
-12 VDC $\pm 5\%$	50 mV p-p	140 mA

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature: 0°C to 60°C
Storage Temperature: -40°C to +90°C
Relative Humidity: to 95% (non-condensing)
Altitude: -200 to 10,000 feet (-61 meters to 3,049 meters)
Burn-In: 96 hours at 70°C

MAXIMUM DIMENSIONS

Width: 4.988 in. (12.669 cm)
Length: 7.900 in. (20.066 cm)
Height: 0.500 in. (1.270 cm)



R24LL **2400 BPS MODEM**

INTRODUCTION

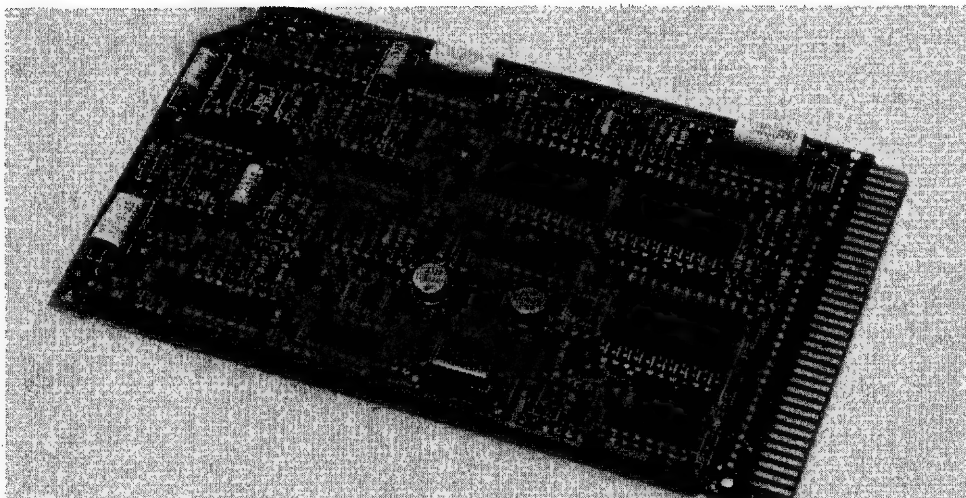
The Rockwell R24LL is a high-performance serial synchronous 2400 bps DPSK modem. By utilizing state-of-the-art MOS/LSI technology, the R24LL provides the user with enhanced performance and reliability in a small package. Implemented on a single printed circuit board, the R24LL is less than 26 square inches.

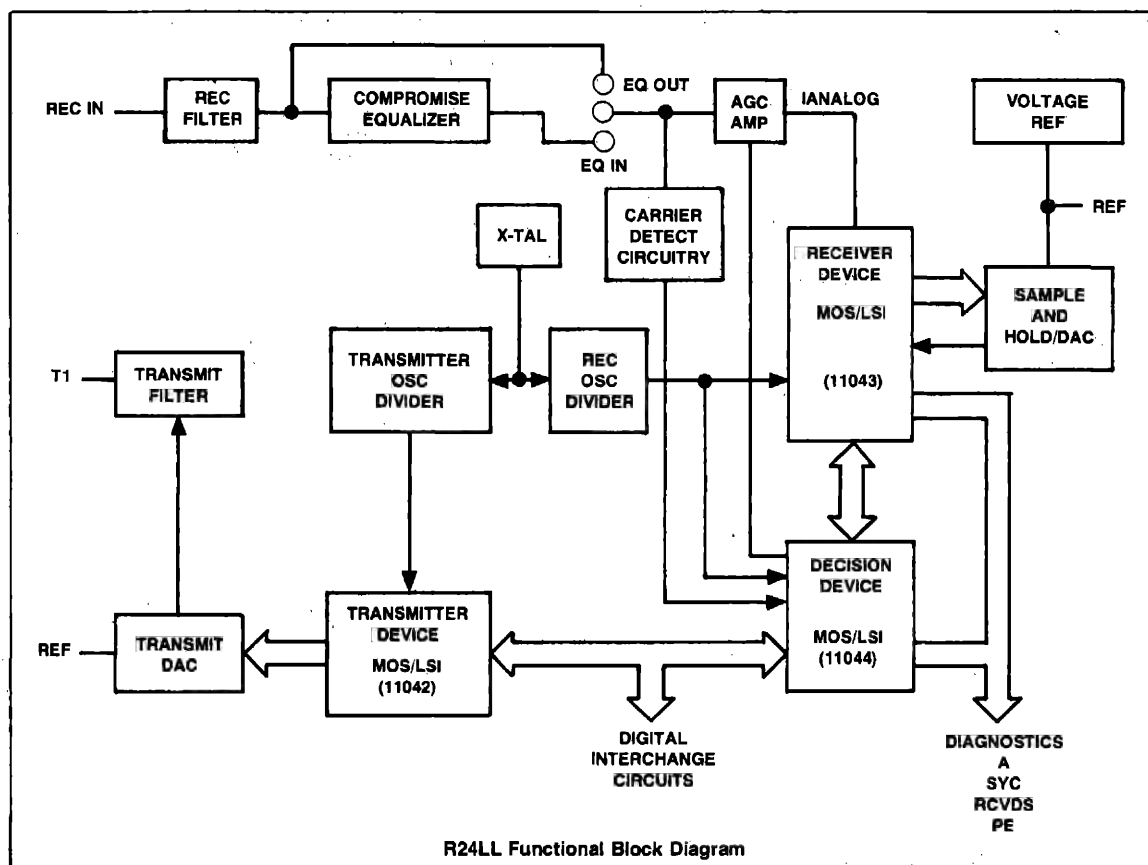
The R24LL operates in either the full-duplex (4-wire telephone connection) or half-duplex (2-wire telephone connection) mode. The R24LL is designed for easy integration into a user's system, e.g., a simple box or rack-mount modem, statistical multiplexor, error controller, terminal, PBX, or any other communications product that requires the utmost in reliability and performance for data transmission over voice-grade telephone lines.

The R24LL is ideal for data transmission applications over either 2-wire or 4-wire leased (dedicated) telephone lines or the dial-up telephone network. Bell 201 B/C, CCITT V.26 A/B and V.26 bis A/B compatible, the R24LL modem offers the user flexibility in creating a 2400 bps modem design customized for specific packaging and functional requirements.

FEATURES

- High Performance—Low Cost
- LSI High Density—Low Power
- Bell 201 B/C, CCITT V.26 A/B Compatibility and V.26 bis A/B Compatibility
- DTE Interface LSTTL/CMOS Compatibility
- External Transmit Data Clock Tracking
- Diagnostic Outputs Available for Eye Pattern Generation and Data Quality Monitoring
- Fixed Compromise Equalizer (Strap Selectable)
- 2400/1200 bps Modes
- Transmitter-Differential Phase Modulation
- Receiver-Coherent Phase Detection
- Operating Modes:
 - Half-Duplex (2-wire)
 - Full-Duplex (4-wire)
- Outstanding Performance Over Unconditioned Lines
- V.27 Scrambler/Descrambler Compatibility
- Answer-Back Tone Generation
- Clear-to-Send Delay Options
- NSYNC Option for Rapid Resynchronization in Multi-Point Applications
- Small Size—Less than 26 sq. in.
- Typical Power Consumption—3 watts
- Power Requirements, +5 Vdc and ± 12 Vdc





FUNCTIONAL SPECIFICATIONS

Transmitter Carrier Frequency— $1800 \text{ Hz} \pm 0.01\%$

Echo Suppression and Answering Tone Frequencies— $2100 \text{ Hz} \pm 0.01\%$ or $2025 \text{ Hz} \pm 0.01\%$

Received Signal Frequency Tolerance—The receiver can adapt to received frequency errors up to $\pm 10 \text{ Hz}$ with less than a 0.5 dB degradation in bit error rate.

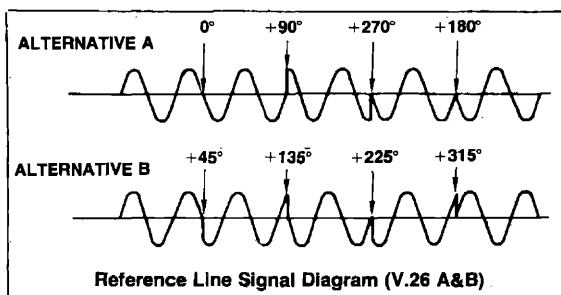
Data Signaling and Modulation Rate—The normal signaling rate is $1200 \text{ baud} \pm 0.01\%$ and a data rate of $2400 \text{ bps} \pm 0.01\%$. The fallback signaling rate is $1200 \text{ baud} \pm 0.01\%$ and a data rate of $1200 \text{ bps} \pm 0.01\%$.

Transmitted Data Spectrum—The transmitted spectrum's bandwidth extends from 800 Hz to 2800 Hz . Phase distortion characteristics fall within the limits specified in CCITT Recommendation V.26 bis. The out-of-band signal power limitations meet those specified by Part 68 of Tariff 261 of the FCC's regulations and typically exceed the requirements of international regulatory bodies as well.

Data Encoding (DPSK)—At 2400 bps , differential 4-phase modulation is employed. The data stream to be transmitted divides into pairs of consecutive bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element. Two alternative arrangements of coding are possible (in accordance with CCITT Recommendations V.26 and V.26 bis) as shown in the following chart.

Data Encoding

2400 BPS		
Dibit	Phase Change	
	V.26A	V.26B/Bell 201
00	0°	$+45^\circ$
01	$+90^\circ$	$+135^\circ$
11	$+180^\circ$	$+225^\circ$
10	$+270^\circ$	$+315^\circ$



At 1200 bps, differential 2-phase modulation is employed. Each bit to be transmitted is encoded as a phase change relative to the phase of the immediately preceding signal element. The encoding is in accordance with CCITT Recommendation V.26 bis as shown in the following chart.

Data Encoding

1200 BPS	
Bit	Phase Change
0	+90°
1	+270°

Turn On Sequences—The transmitter of the R24LL can generate a total of 13 selectable turn-on sequences, as shown in the following chart.

Turn-On Sequences

Type of Line Signal	Segment 1	Segment 2	Total of Segments 1, 2	Comments
Turn-On Sequence Number	Continuous Unscrambled Ones	Continuous Scrambled ¹ Ones	Nominal Total Turn On Sequence Time ²	
1	0 ms	0 ms	0 ms	V.26
2	6.67 ms	0 ms	6.67 ms	
3	8.33 ms	0 ms	8.33 ms	
4	30 ms	0 ms	30 ms	
5	8.33 ms	21.67 ms	30 ms	(scrambler inserted)
6	90 ms	0 ms	90 ms	V.26, V.26 bis
7	8.33 ms	81.67 ms	90 ms	
8	148.3 ms	0 ms	148.3 ms	(scrambler inserted)
9	8.33 ms	140 ms	148.3 ms	
10	220 ms	0 ms	220 ms	V.26 bis
11	8.33 ms	211.7 ms	220 ms	(scrambler inserted)
12	800 ms	0 ms	800 ms	V.26 bis
13	8.33 ms	791.7 ms	800 ms	(scrambler inserted)

Notes:

- See paragraph titled Scrambler/Descrambler for a description of scrambler/descrambler facility.
- For those turn-on sequences in which the scrambler is inserted, the transmitted line signal corresponds to a continuous "one", unscrambled, for 8.33 ms-ten baud (symbol) intervals, followed by the transmission of a continuous "one", scrambled, for the remainder of the turn-on sequence.

Turn Off Sequence—When the transmitter has been sending data and "Request-to-Send" is turned off, any remaining data bit information transmits within 6 milliseconds.

Response Times of Clear-to-Send—The selected configuration of the R24LL and its associated turn-on sequence determine the Clear-to-Send response times, as shown in the following chart.

Scrambler/Descrambler—The R24LL incorporates a self-synchronizing scrambler/descrambler enabled by a discrete digital input.

Carrier Detection—The R24LL contains a received line signal detector. This detector indicates the presence of energy at the receiver input above a certain threshold for a minimum amount of time.

Carrier Detect Thresholds

Received Level	Carrier Detect
Greater than -43 dBm	On (line signal present)
Less than -48 dBm	Off (line signal not present)

Carrier Detect Response Time

Carrier Detect Transition	Response Time
Off-to-On	14 ± 1 ms
On-to-Off	8 ± 3 ms

Clear-To-Send Response Times

Turn-On Sequence Number	Clear-To-Send Response Times*		Comments
	Off-to-On	On-to-Off	
1	0 ms	0 ms	
2	6.67 ms	0 ms	switched carrier 4-wire (BELL 201)
3	8.33 ms	0 ms	switched carrier 4-wire
4	30 ms	0 ms	CCITT 4-wire
5	30 ms	0 ms	CCITT 4-wire with scrambler
6	90 ms	0 ms	CCITT 2-wire
7	90 ms	0 ms	CCITT 2-wire with scrambler
8	143.3 ms	0 ms	switched carrier 2-wire
9	143.3 ms	0 ms	switched carrier 2-wire with scrambler
10	220 ms	0 ms	CCITT 2-wire echo protection
11	220 ms	0 ms	switched 2-wire echo protection with scrambler
12	800 ms	0 ms	CCITT 2-wire auto call
13	800 ms	0 ms	CCITT 2-wire auto call with scrambler
Note: * The tolerance on each Off-to-On and On-to-Off response time is (+.9, -.1) ms.			

Clamping Options—The following clamps are provided with the R24LL:

1. **Received Data.** The Received Data output is clamped to a mark when Carrier Detect is off. This action prevents disturbances on the line from getting through the receiver circuit to the data output.
2. **Carrier Detect Clamp.** The Carrier Detect output is clamped off (squelched) when Request-to-Send is on. An option extends this clamp for 148 milliseconds beyond transitioning-off, thus providing echo protection.
3. **Receive Clock Clamp.** The Receive Clock output is clamped off when Carrier Detect is off. This action prevents any disturbances from propagating through the receiver circuit to the receive clock output.

Equalizer—The R24LL contains a fixed compromise delay equalizer which improves performance over the domestic switched network. The equalizer may optionally be positioned in the receiver or removed entirely by means of a jumper plug. It has a nominally flat 0.0 dB amplitude response.

Test Pattern Generation—The scrambler/descrambler function can be used to implement a 127-bit test pattern feature. For example, a constant mark input could be scrambled and transmitted as a pseudo-random signal to be descrambled at the receiver back to the constant mark. A transmission error would be represented as a space for the duration of an incorrect bit.

Receive Level—The R24LL receives line signals from 0 to -43 dBm.

Transmit Timing—The R24LL generates a Transmit Clock with the following characteristics: Frequency—2400 Hz \pm 0.01% (1200 Hz \pm 0.01% in full back mode), duty cycle—50 \pm 1%. The R24LL can also optionally track an External Transmit Clock supplied by the user. Both have similar characteristics.

Receive Timing—The R24LL provides a data derived Receive Clock output in the form of a nominal squarewave (50 \pm 1% duty cycle). The timing recovery function can track a \pm 0.01% frequency error in the associated transmit timing source.

Secondary Channel—The R24LL provides the user sufficient flexibility to add an external secondary channel if desired. (A secondary channel is a data transmission channel having a lower signalling rate and occupying a different portion of the telephone line bandwidth than the primary channel. The primary and secondary channels share the same transmission facility, the telephone line.) Additional receive filtering to allow simultaneous operation of the secondary channel must be provided external to the R24LL.

Transmit Level—The transmitted output line signal level of the modem is -1.0 dBm \pm 1.0 dBm when the transmitter output is terminated with a 600 ohm resistor in series. This applies to all possible transmitted data patterns both at 2400 bps and 1200 bps, as well as to answering tone generation.

Answering Tone Generation—The R24LL can generate an answering tone at 2100 Hz \pm 0.01% or 2025 Hz \pm 0.01% (selectable) for 3.4 \pm 0.2 seconds under the control of an input logic signal (CAUTO). The R24LL also provides a digital output (TONA) indicating the conclusion of answering tone generation.

New Sync—Pulsing the New Sync (NSYNC) digital input forces Carrier Detect Off and causes the R24LL to resynchronize rapidly on sequences of incoming messages. This feature is necessary in some polling applications because the receiver maintains the timing information of the previous message for some time after it has ended—this may interfere with resynchronization on receipt of the next message from a different remote transmitter.

Fast Energy Detector—A received line signal detector, the fast energy detector's output (RLSD) has the same threshold and hysteresis characteristics as the Carrier Detect. For RLSD the maximum turn-on time is 1.6 ms and the maximum turn-off time is 6.6 ms (both times for Equalizer not inserted). Furthermore, the RLSD output will respond to transient line conditions (no momentary dropout or momentary-on glitch protection).

Baud Clocks—Symbol or baud timing is available for both the transmitter and receiver functions. These signals have characteristics similar to the data clocks' except that their frequency is equal to the signalling rate ($1200 \text{ Hz} \pm 0.01\%$). Transitions on Transmitter Baud Clock and Receiver Baud Clock coincide with Off-to-On transitions of Transmit Clock and Receive Clock, respectively. For 2400 bps operation both baud clocks are low for the first data bit in a baud and high for the second data bit.

Analog Loopback—The R24LL provides the flexibility to implement a variety of analog loopback schemes using a minimum amount of external circuitry.

Eye Pattern/Data Quality Detector—The R24LL outputs digital signals (RCVDS, SYC, A) which the user can decode to generate a quadrature eye pattern. The eye pattern is a visual (oscilloscope) display showing the received signal as groupings of dots in the baseband signal plane. It is useful as an incoming modem test and product evaluation tool and as an indication of a line condition in actual operation (useful for some network control applications).

The modem also outputs digital signals (PE, SYC, A) which the user can decode to generate a data signal quality detector. This indicates if a reasonable probability of errors is received on the data channel.

CONFIGURATIONS

The R24LL modem provides the user with a wide range of modem functional configurations. Some of the possibilities are described below.

Half-Duplex (2-Wire)—In a half-duplex application, the user needs both transmit and receive capabilities (although not simultaneously) on a 2-wire connection.

If a hybrid (4-wire \rightarrow 2-wire) transformer is not employed as a line interface device, REC IN would be strapped to T1 through an external resistor, the user perhaps selecting this resistor to produce a specific output impedance or to compensate for losses in any line interface circuitry.

Digital interface connections. In a typical application, the user controls basic modem operation through the digital signals T103, T105, T106, T114, T104, T115, T109, and perhaps RBCK, T113, or TBC. (T113 is used if transmit timing is to be locked to the customer's clock; TBC may be employed to minimize certain timing delays and is useful in some multiplexing operations). A number of digital inputs can either be fixed (tied directly and permanently to the +5V supply [high] or to signal ground or the -12V supply [low] in accordance with the specific requirements) or, if the user desires programmable flexibility, these signals can be interfaced with his equipment. Signals of this type include T111, V26A, 1, S8GR, K, Y, TC06, 800MS, E, T2W/4W, CP04,

CP15, RW/4W, TH09, FSYC, TC09, and PBS. If answerback or echo suppression tone generation capability is required, the input CAUTO (which should be strapped low if not used) and the output TONA are available. Implementation of the New Sync function requires any new sync pulses to be inputted to NSYNC. The outputs SYC, RCVDS, DCP, A, and PE can be used to generate eye pattern and phase error diagnostic information.

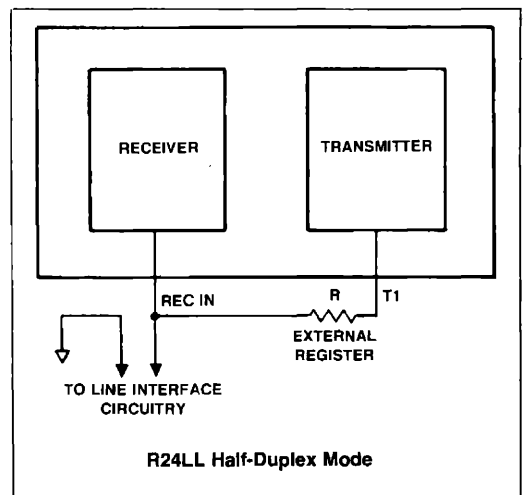
Analog interface connections. The GAIN-G1-G2 jumper (for threshold set selection) should be in the proper location as described in the table at the top of page 9. Note that input impedance at REC IN is a resistive 15.8K ohms. If a 600 ohm receiver input impedance is desired, an external resistor to signal ground must be added. Take care when routing to REC IN (for low level receive signal) from any telephone interface circuitry. Also note that it is possible to insert the equalizer into the receiver or not to insert it by use of the jumper on the board. Implementation of a local analog loopback scheme could be achieved in many ways. If the line interface connection as shown in the diagram below is employed, the user can create a local analog loopback simply by deactivating squelch. To isolate the telephone line during this loopback (no transmitted line signal), additional circuitry must be added.

Full-Duplex—In a full-duplex application, the user needs both transmit and receive capabilities simultaneously. A 4-wire line connection is required.

The only differences with half-duplex are that REC IN is no longer connected to T1 (the transmitter and receiver have independent transmission paths) and the squelch function would be deactivated (except during New Sync) by use of the input T2W/4W.

Digital interface connection is the same as for the half-duplex.

Analog interface connections. With the exception of the 4-wire line interface, analog interface connections are the same as half-duplex. Implementation of a variety of local or remote analog or digital loopback schemes requires the addition of a minimal amount of external circuitry.



INTERFACE CRITERIA

The R24LL interface signals are classified as digital interchange signals and analog signals. The signals interface to the modem user through the board edge connector.

Digital Interchange Circuits—The characteristics of the R24LL digital inputs and outputs are given in the following charts:

Digital Input Characteristics

Input Logic State	Allowed Input Voltage Levels
Low	–12V (V_{DD}) to 0.8V sinking $<10\ \mu\text{A}$
High	+4.0V ($V_{SS} - 1\text{V}$) to +5.0V (V_{SS}) sourcing $<10\ \mu\text{A}$
The digital inputs are directly CMOS compatible. The capacitive loading on each input is 25 pF (maximum).	

Digital Output Characteristics

Output Logic State	Allowed Output Voltage Levels
Low	0.0V to 0.4V (–0.4V to +0.4V for RLSD) sinking 0.36 mA
High	+4.0V ($V_{SS} - 1\text{V}$) to +5.0V (V_{SS}) sourcing 100 μA
The digital outputs are directly CMOS or low-power Schottky TTL compatible.	

Digital Interchange Circuits

Term	Pin Number	Description
TONA	P1-A5	Output indicating completion of answering tone.
800MS	P1-A6	Input affecting Clear-to-Send response time.
TC06	P1-A7	Input affecting Clear-to-Send response time.
K	P1-A8	Input affecting Ready-for-Sending response time.
X	P1-A9	Input affecting T109 Squelch.
CAUTO	P1-A10	Input initiation transmission of answering tone.
New Sync (NSYNC)	P1-A13	Input affecting T109 Squelch.
CLAMP	P1-A15	Input forcing squelch of T109.
Fast Energy Detector (RLSD)	P1-A17	Input generating T109.
Fast Sync (RSYC)	P1-A18	Input determining whether fast sync feature (fast resynchronization upon recovery of received line signal following momentary drop-out) is enabled.
S8GR	P1-A19	Input determining whether the modulo 8 pattern guard will be incorporated into the scrambler facility.

DCP	P1-A21	Digital output enabling user to generate eye pattern and phase error diagnostic information.
R2W/4W	P1-A22	Input affecting state of THRH output.
Receiver Baud Clock (RBCK)	P1-A23	For 2400 bps operation.
PBS	P1-A24	Input determining T109 On-to-Off response time.
TH09	P1-A25	Input affecting state of THRH output.
Transmitted Data (T103)	P1-A29	Input for digital data to be transmitted.
Clear-to-Send or Ready-for-Sending (T106)	P1-A30	Output indicating readiness to accept data for transmission.
Data Signalling Rate Selector (T111)	P1-A32	Input determining whether transmitted data rate is 2400 bps or 1200 bps.
Receive Clock (T115)	P1-A33	Output providing received signal element timing information.
E	P1-B6	Inputs affecting Clear-to-Send response time and T109 Squelch.
T2W/4W	P1-B7	
Y	P1-B8	Input affecting Ready-for-Sending response time and answering tone frequency.
Transmitter Baud Clock (TBC)	P1-B10	Output baud clock (1200 Hz).
A	P1-B11	Digital output enabling user to generate eye pattern and phase error diagnostic information.
I	P1-B15	Input determining whether scrambler is to be inserted.
THRH	P1-B18	Output used in conjunction with carrier detect circuitry to implement T109 threshold set select function.
V26A/B	P1-B19	Input selecting dibit encoding at 2400 bps operation as per V.26 Alternate A or V.26 Alternate B.
CP15	P1-B20	Input selecting optional clamping of Receive Clock (T115).
RCVDS	P1-B21	Digital outputs enabling user to generate eye pattern and phase error diagnostic information.
SYC	P1-B22	
PE	P1-B23	
TC09	P1-B24	Input determining T109 Off-to-On response time.
CP04	P1-B25	Input determining T104 damping.
External Transmit Clock (T113)	P1-B29	Input providing modem with transmitted signal element timing information.
Request-to-Send (T105)	P1-B30	Input to transmitter.
Received Data (T104)	P1-B31	Digital data output from modem receiver.
Transmit Clock (T114)	P1-B33	Output providing user with transmitted signal element timing information.
Carrier Detect (T109)	P1-B24	Output indicating presence of signal energy on receiver line.

Note:

The following P1 connector pin locations should be left open and unconnected:
A4, A11, A12, A14, A16, A20, A35, B1, B12, B13, B14, B17, B32, and B35.

Data Structure

Input		Data Structure
Data Signalling Rate Selector (P1-A32)	V26 A/B (P1-B19)	
Low	Low	2400 bps Alternate A
Low	High	2400 bps V.26 Alternate B (Bell 201C)
High	Don't Care	1200 bps

Tone Generation

Inputs		Outputs	
CAUTO (P1-A10)	Y (P1-B8)	TONA (P1-A5)	Transmitted Signal
Low	Don't Care	High	Normal Operation
High	High	High	2100 Hz Answering Tone
High	Low	High	2025 Hz Answering Tone
High	Don't Care	Low	Normal Operation

Selection of Clear-To-Send Response Times

Turn-On Sequence	Inputs							Clear-To-Send Response Times (ms)	
	Y (P1-B8)	800MS (P1-A6)	K (P1-A8)	TC06 (P1-A7)	T2W/4W (P1-B7)	I (P1-B15)	E (P1-B6)	Off-to-On	On-to-Off
1	Low	High	Don't Care	Don't Care	High	Low	Don't Care	6.67	0
2	High	High	Low	High	High	Low	Don't Care	8.33	0
3	High	High	Low	Low	High	Low	Don't Care	30	0
4	High	High	Low	Don't Care	High	High	Don't Care	30	0
5	High	High	Don't Care	High	Low	Low	Low	90	0
5	High	High	High	High	High	Low	Don't Care	90	0
6	High	High	Don't Care	High	Low	High	Low	90	0
6	High	High	High	High	High	High	Don't Care	90	0
7	Low	High	Don't Care	Don't Care	Low	Low	Don't Care	148.3	0
8	Low	High	Don't Care	Don't Care	Don't Care	High	Don't Care	148.3	0
9	High	High	High	Low	Don't Care	Low	Don't Care	220	0
9	High	High	Don't Care	Don't Care	Low	Low	High	220	0
9	High	High	Don't Care	Low	Low	Low	Don't Care	220	0
10	High	High	High	Low	Don't Care	High	Don't Care	220	0
10	High	High	Don't Care	Don't Care	Low	High	High	220	0
10	High	High	Don't Care	Low	Low	High	Don't Care	220	0
11	High	Low	Don't Care	Don't Care	Don't Care	Low	Don't Care	220	0
12	High	Low	Don't Care	Don't Care	Don't Care	High	Don't Care	800	0

Note: The tolerance on each Off-to-On and On-to-Off response time is (+0.9, -0.1 ms).

Carrier Detect Squelch

Inputs					Squelch Status
X (P1-A9)	T2W/4W (P1-B7)	E (P1-B6)	T105 (P1-B30)	NSYNC (P1-A13)	
Don't Care	Don't Care	Don't Care	Don't Care	Low	Squelch
Don't Care	High	Don't Care	Don't Care	High	No Squelch
Low	Low	Don't Care	Don't Care	High	No Squelch
High	Low	Don't Care	High	High	Squelch
High	Low	High	High→Low	High	Extended Squelch
High	Low	Low	High→Low	High	No Extended Squelch

Notes:

"Squelch" means that Carrier Detect (T109) is clamped off regardless of the level of received line signal. During squelch, CLAMP (T-13) is a low impedance to ground. For normal operation (no squelch) CLAMP (T-13) is in a high impedance ("open drain") state.

When "extended squelch" is enabled, squelch occurs both when Request-to-Send (T105) is On (High) and for 148.3 ms (+0.9, -0.1 ms) following the On-to-Off (High to Low) transition of T105.

Carrier Detect Threshold Selection

THRH	Gain Strap	Selected Threshold Set
High Impedance	G1	-43 dBm, -48 dBm
High Impedance	G2	-33 dBm, -38 dBm
Low impedance to ground	G1 or G2	-26 dBm, -31 dBm

Gain must be shorted to either G1 or G2.

THRH Operation

Input		THRH
TH09	R2W/4W	
Low	Low	High Impedance
High	Low	High Impedance
Low	High	High Impedance
High	High	Low Impedance

THRH is an open-drain driver representing either a low impedance to ground (<500 ohms) or a very high impedance state.

Scrambler/Descrambler

Input		Scrambler/Descrambler Configuration
I (P1-B15)	S8GR (P1-A19)	
Low	Don't Care	No Scrambler
High	Low	Scrambler V.27 bis, ter (modulo 8 pattern guard)
High	High	(no modulo 8 pattern guard)

Analog Interface Circuits—The analog interface circuits of the R24LL defined in the following chart provide the power, the switched network connections, and a means for the user to monitor the incoming line signals.

Analog Interface Circuits

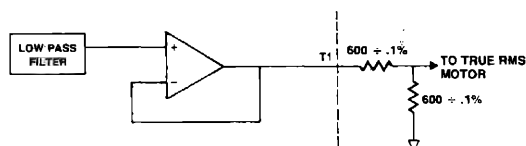
Term	Pin Number	Description
+12V	P1-B5, B9	+12V Power Supply
-12V	P1-A1	-12V Power Supply
+5V	P1-A2, B2	+5V Power Supply
COMMON	P1-A3, A31, B3	Ground (signal and power return)
T1	P1-A34	T1 is the low impedance transmitter analog output (line signal). The T1 allows the user the flexibility needed to customize his output impedance (to compensate for transformer losses, for instance).
SECONDARY IN	P1-B4	Secondary channel input from the DTE.
REC IN	P1-B36	Receive filter input. Input impedance is a resistive 15.8 K ohms \pm 1%.

Audio Interface—The audio interface includes the R24LL's interface with the transmission network.

The receiver and transmitter line interfaces are single-ended (non-transformer coupled) signals with the following characteristics:

Transmitter Voice Frequency Output T1

- Output Impedance: Impedance of Op-Amp
- Maximum Output Level: ≤ 0.0 dBm as measured per the following diagram using a true RMS meter.



Receiver Voice Frequency Input REC IN

- Input Impedance: 15.8K ohms \pm 1% resistive
- Maximum Input Level: ≤ 0.0 dBm

The output level at the R24LL line interface is less than -60 dBm in the frequency band of 1 Hz to 12 Hz when the modem is not transmitting. A period of 100 milliseconds is required for the line interfaces to stabilize following power turn-on.

Low impedance voice frequency output T1 satisfies applications interfacing with lossy transformers or hybrids. The characteristics of T1 output are:

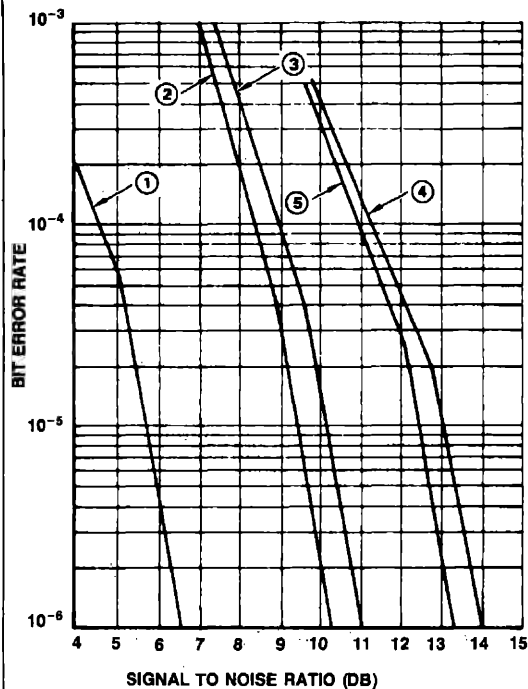
- Output Impedance: Essentially zero ohms when loaded to ground with greater than 400 ohms (resistive). This is a direct output from an operational amplifier.
- Minimum Load: ≥ 400 ohms (resistive) as measured between T1 and signal ground.

PERFORMANCE DATA

The R24LL is a high performance synchronous 2400 bps DPSK modem. It utilizes a coherent demodulation technique to achieve reliable operation over the switched network or unconditioned lines.

Timing Jitter—The maximum steady state timing jitter of Received Clock with respect to Transmit Clock is less than 10% p-p for an input signal-to-noise ratio of 12 dB.

Bit Error Rate—The following graph represents typical R24LL performance.

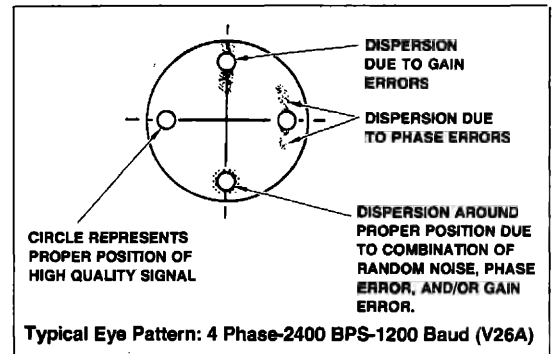


1. 1200 BPS, BACK-TO-BACK, SCRAMBLER, NO EQUALIZER
2. 2400 BPS, V.26A OR B, BACK-TO-BACK, SCRAMBLER, NO EQUALIZER
3. 2400 BPS, V.26A OR B, 15°-150 HZ PHASE JITTER, NO SCRAMBLER, NO EQUALIZER
4. 2400 BPS, V.26A OR B, 30°-120 HZ PHASE JITTER, NO SCRAMBLER, NO EQUALIZER
5. 2400 BPS, V.26A OR B, 3002 UNCONDITIONED LINE, NO SCRAMBLER, EQUALIZER

Typical Bit Error Rate Performance

Phase Error—Phase error can be measured with the modem's output signals PE, SYNC, and A. With an external test circuit, a numerical value can be derived to indicate the quality of received data and then directly correlated to bit error rate performance. The required test circuit can be implemented with discrete circuitry or in software within a microcomputer.

Eye Pattern—By using the modem's digital output signals RCVD, SYNC, and A along with an added test circuit, the user can generate an oscilloscope quadrature eye pattern. This pattern displays the received signal as a group of dots in the baseband signal plane: it is a graphic representation of modem performance.



Phase error and eye pattern can be extremely useful for modem acceptance testing, product evaluation, and observation of line signal quality under actual operation.

RECOMMENDED MATING CONNECTORS

The R24LL connector mating contacts are *not* gold covered; therefore, a high quality gas-tight card edge connector should always be used to maintain reliable operation. Rockwell recommends the following in order of preference:

1. Burndy GTBH Series
2. Continental 6100-200 Series
3. Elco 00-6307 Series

POWER REQUIREMENTS

Voltage	Ripple	Maximum Current
+5 VDC \pm 5%	100 mV p-p	102 mA
+12 VDC \pm 5%	50 mV p-p	64 mA
-12 VDC \pm 5%	50 mV p-p	142 mA

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature: 0°C to 60°C
 Storage Temperature: -40°C to +80°C
 Relative Humidity: to 90% (non-condensing) or a wet bulb temperature up to 35°C, whichever is less.
 Altitude: -200 to 10,000 feet (-61 meters to 3,049 meters)



R24 2400 BPS INTEGRAL MODEM

INTRODUCTION

The Rockwell R24 is a high performance synchronous serial 2400 bps DPSK modem. Utilizing extensive MOS/LSI technology, the R24 is implemented in three modular building blocks. It is innovatively designed to enable its economic integration by system designers in a broad range of communication, computer, and control equipment.

Having Bell 201 B/C and CCITT V.26 compatibility, the modular R24 offers the user sufficient flexibility to customize a 2400 bps modem to his specific packaging and functional requirements. With a minimum amount of interface circuitry, the modem can be configured for operation on leased lines or on the general switched network.

MODULE VERSATILITY

The versatility of the R24 design is achieved by dividing the modem's functions into three modules:

Transmitter — Module T
Receiver — Modules R1 and R2

Each module can be plugged into standard connectors or can be wave soldered on one or more printed circuit boards. The pin spacing is on 100 mil centers. Modem modules are functionally independent.

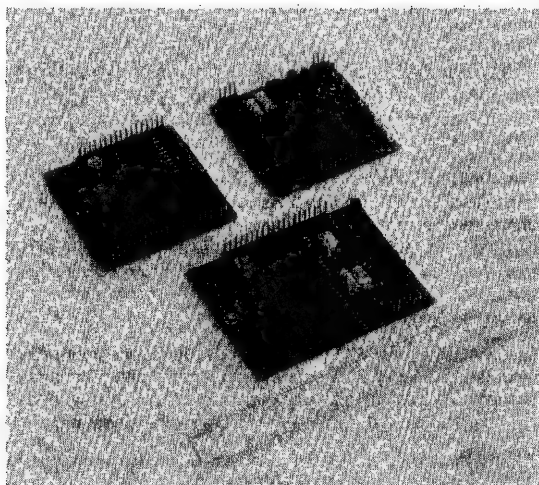
MODEM OPERATION MODES

In general, the modules can be configured to operate in the following modes:

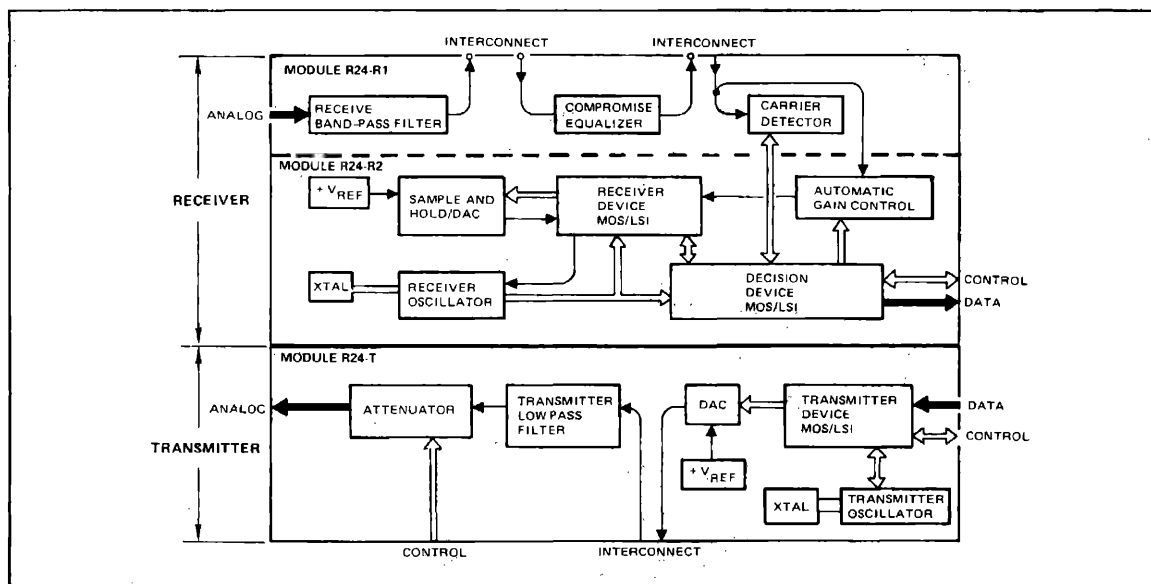
- Simplex — Transmit only: Only the transmitter module (T) is used.
- Simplex — Receive only: R1 and R2 modules are used to implement a complete receiver function.
- Half Duplex (2-Wire): Requires both transmit and receive functions (although not simultaneously), therefore, all three modules are used.
- Full Duplex (4-Wire): Requires both transmit and receive functions simultaneously, again all three modules are used.

FEATURES:

- LSI high density; low power
- 2400/1200 bps modes
- Transmitter-Differential phase shift keying
- Receiver-Coherent phase detection
- Bell 201 B/C, CCITT V.26 compatible
- CCITT A/B encoding options
- Operating modes:
 - Half duplex (2 wire)
 - Full duplex (4 wire)
 - Simplex (Transmit or Receive only)
- Outstanding performance over unconditioned lines
- LSTTL/CMOS compatible digital interface
- Fixed compromise equalizer
- V.27 compatible scrambler/descrambler
- Answer-back tone generation
- Clear-to-send delay options
- New sync option provides rapid resynchronization
- Typical power consumption 2 watts
- Total module area 25 sq. in.
- R24 Modem Evaluation Board facilitates evaluation and design-in tasks.



R24 Integral Modem



R24 Functional Diagram

TECHNICAL DESCRIPTION

Transmitter carrier frequency — 1800 Hz $\pm 0.01\%$

Echo suppression and answer tone frequencies — 2100 Hz $\pm 0.01\%$ or 2025 Hz $\pm 0.01\%$

Received signal frequency tolerance — The receiver can adapt to received frequency errors up to ± 10 Hz with less than a 0.5 dB degradation in bit error rate.

Data signaling and modulation rate:

- 1) Normal: Signaling Rate — 1200 baud $\pm 0.01\%$.
Data Rate — 2400 bps $\pm 0.01\%$.
- 2) Fallback: Signaling Rate — 1200 baud $\pm 0.01\%$.
Data Rate — 1200 bps $\pm 0.01\%$.

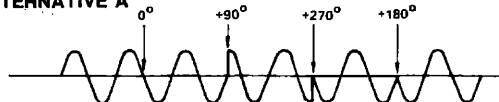
Transmitted Data Spectrum — The transmitted spectrum's bandwidth extends from 800 Hz to 2800 Hz. Phase distortion characteristics are within the limits specified in CCITT Recommendation V.26 bis. The out of band signal power limitations meet those specified by Part 68 or Tariff 261 of the FCC's regulations, and typically exceed the requirements of international regulatory bodies as well.

Data Encoding (DPSK) — At 2400 bps, differential four-phase modulation is used. The data stream is transmitted in pairs of consecutive bits (dibits). Each dibit is encoded as a phase change relative to the phase of the preceding signal element.

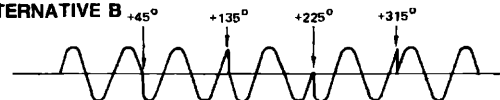
The R24 implements the phase A and B recommendations of CCITT V.26. The modulation coding in Bell 201 modems is the same as V.26B. Definition of these coding arrangements is shown in the following table:

DIBIT	2400 BPS	
	V.26A	V.26B/Bell 201
0 0	0°	+45°
0 1	+90°	+135°
1 1	+180°	+225°
1 0	+270°	+315°

ALTERNATIVE A



ALTERNATIVE B



Line Signal Diagram (V.26 A & B)

At 1200 bps, differential two-phase modulation is used. Each bit is transmitted at a relative phase change to preceding signal element in accordance with CCITT V.26 bis.

BIT	1200 BPS	
	PHASE CHANGE	
0	+90°	
1	+270°	

Turn On Sequences — A total of twelve selectable turn on sequences can be generated by the transmitter module.

Turn Off Sequence — When the transmitter has been sending data and "Request to Send" is turned off, any remaining data bit information is transmitted within 6 milliseconds.

Ready for Sending (T106) Response Times — These response times are determined by the modem configuration selected and its associated turn on sequence.

Turn On Sequence Number	Ready for Sending Response Time	Configuration and Carrier Type
1	6.67 msec	Switched Carrier — 4-Wire (Bell 201)
2	8.33 msec	Switched Carrier — 4-Wire
3	30 msec	CCITT — 4-Wire
4	30 msec	CCITT — 4-Wire with Scrambler
5	90 msec	CCITT — 2-Wire
6	90 msec	CCITT — 2-Wire with Scrambler
7	148.3 msec	Switched Carrier — 2-Wire
8	148.3 msec	Switched Carrier — 2-Wire with Scrambler
9	220 msec	CCITT — 2-Wire Echo Protection
10	220 msec	Switched 2-Wire Echo Protection with Scrambler
11	800 msec	CCITT — 2-Wire Auto Call
12	800 msec	CCITT — 2-Wire Auto Call with Scrambler
Response Time tolerance (+ 0.9, -0.1) msec		

Scrambler/Descrambler — As a selectable option, the scrambler/descrambler may be inserted into the transmitter/receiver path. The purpose of this scrambler is to ensure that the line signal will evenly span the allocated bandwidth. This minimizes pattern sensitivity problems arising from simple fixed and periodic data sequences. The scrambler is V.27 or V.27 bis/ter compatible.

Carrier Detect (T109) — The modem receiver incorporates a line signal energy detector whose output responds to three selectable threshold levels.

Set 1 (V.26 bis, switched network)	Greater than -43 dBm = ON Less than -48 dBm = OFF
Set 2 (V.26 bis, switched network)	Greater than -33 dBm = ON Less than -38 dBm = OFF
Set 3 (V.26, leased line)	Greater than -26 dBm = ON Less than -31 dBm = OFF

Selectable T109 Response Times — This time is defined as the interval between the sudden connection or removal of the received line signal to the modems receive filter, and the subsequent transition of Carrier Detect (T109) from one state to the other.

Carrier Detect Transition	Response Time
OFF to ON (connection)	6 ± 1 ms } Selectable 14 ± 1 ms }
ON to OFF (removal)	8 ± 3 ms } Selectable 22 ± 3 ms }

Receive Level — The modem receives line signals from 0 to -43 dBm.

Transmit Timing — The modem generates a Transmit Clock (T114) having the following characteristics: Frequency — 2400 Hz ± 0.1% (1200 Hz ± 0.1% in fallback mode), duty cycle — 50 ± 1%. The modem is also optionally capable of tracking an External Transmit Clock (T113) supplied by the modem user. T113 has similar characteristics to T114.

Receive Timing (T115) — The modem provides a data derived "Receive Clock" output in the form of a nominal squarewave (50 ± 1% duty cycle). The modem timing recovery function is capable of tracking a ± 0.01% frequency error in the associated transmit timing source.

Transmitter Output Levels — This output can be strap controlled in 2 ± 0.2 dB steps from -1 dBm ± 1 dB to -15 dBm ± 1 dB.

Answer Tone Generation — The modem generates a selectable answering tone of 2100 Hz ± 0.01% or 2025 Hz ± 0.01%. The 2100 Hz tone meets CCITT Recommendations G.161 and V.25, and the 2025 Hz tone meets Bell System requirements for both answering tone and echo suppressor disabling tone.

Equalizer — As a strap option, the modem contains a fixed compromise delay equalizer which can be used to improve performance over unconditioned schedule 3002 lines. This option is normally positioned in the receiver, but it can be repositioned in the transmitter or bypassed entirely. It is designed to compensate for the mean of the range of group delay distortions generally encountered in the United States. Its amplitude response is nominally flat at 0.0 dB.

Test Pattern Generation — The scrambler/descrambler function can be used to implement a 127-bit test pattern feature. For example, a constant mark input could be scrambled and transmitted as a pseudo-random signal to be descrambled at the receiver back to the constant mark. A transmission error would be represented as a space for the duration of an incorrect bit.

Multipoll Synchronization — The "new sync" (NSYNC) digital input can be pulsed to cause rapid resynchronization of the receiver for sequences of incoming messages. This feature is necessary in some polling applications. However, if the user's hardware/software does not support the use of "new sync" (NSYNC), then the optional "fast sync" (FSYNC) can be utilized to enable a fast resynchronization procedure.

Selectable Clamping Options —

- Received Data (T104) — This output is clamped to a selectable constant (space or mark) when "Carrier Detect" is off, to prevent disturbances on the line from getting through the receiver to the data output.
- Carrier Detect (T109) Clamp — This output may be clamped OFF (squelched) in a 2-wire applications during the time when "Request to Send" (T105) is on. An additional option extends this clamp for 148 msec beyond T105 transitioning off, providing echo protection.
- Receive Clock (T115) — This clock output can be clamped OFF when "Carrier Detect" is off, thereby preventing any disturbances from propagating through the receiver to the receive clock output.

SYSTEM DESIGN

The R24 modem modules provide the user with sufficient flexibility to implement a wide range of modem functional configurations. This flexibility is achieved by digital control at the module interfaces. For a given application, such as a lease network V.26 Alternative B modem (Bell 101B), the complexity of the user interface can be significantly reduced by strapping those data interface inputs which do not change. The modem interface can also be under software control.

Figures 1 and 2 show the basic interface connections for the transmitter module (T) and the receiver modules (R1,R2). These diagrams are applicable for any operation mode of the modem—simplex, half-duplex, or full-duplex.

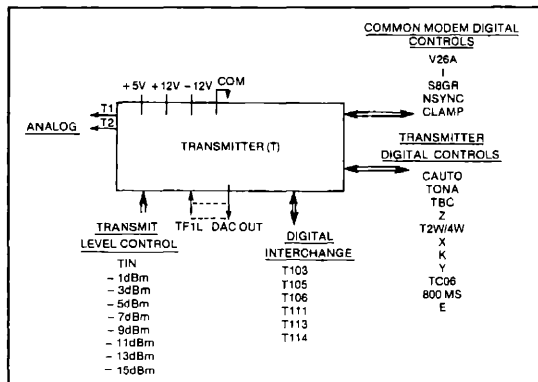


Figure 1. Transmitter Interfaces

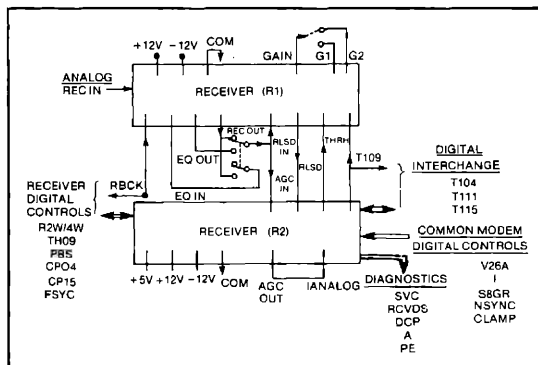


Figure 2. Receiver Interconnection

MODEM OPERATION — HALF OR FULL-DUPLEX

Figure 3 indicates the module interconnections necessary for half-duplex operation. For full-duplex operation, the transmitter/receiver interconnections are similar to the half-duplex case with the exception that "REC IN" is not connected to T2 or T1. In full-duplex operations, the transmission and receiver paths are independent.

As shown, a transformer is sufficient to connect directly to a leased line in the U.S. For the switched network, registered protective circuitry or a data access arrangement (DAA) is generally required. Rockwell offers an FCC registered protective circuitry product to support this application. Requirements for line interface and protective circuitry vary internationally.

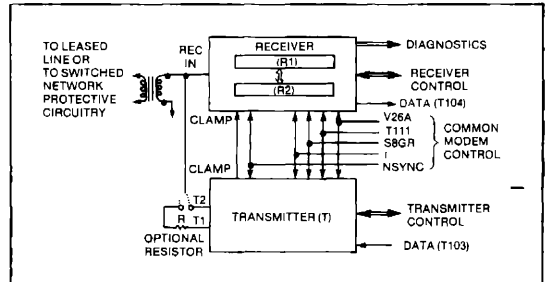
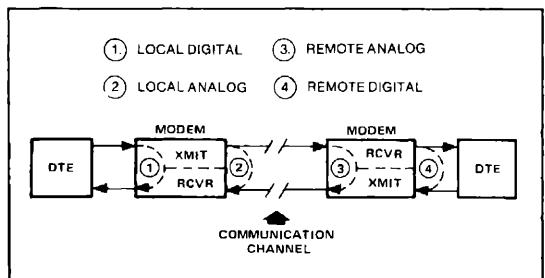


Figure 3. Transmitter-Receiver Interconnection (Half Duplex)

Secondary Channel — The modem modules provide the user with all the interface connections needed to add an external secondary channel if required. This data transmission channel would operate at a lower rate, and in a different portion of the available bandwidth than the primary. Additional external receive filtering would also have to be added to allow simultaneous operation of the primary and secondary channels.

Analog and Digital Loopback — To check out or diagnose the communication link, loopback testing is often performed. A test word is transmitted and "looped" back to the originating DTE. Typical types of loopback tests are:



DTE — Data Terminal Equipment

The modem modules provide the user with all the necessary interfaces connections to implement almost any loopback scheme desired. With a minimum amount of external circuitry, loopback testing can be controlled via a communications adapter/software approach or manually. For local analog, remote analog and remote digital loopback, the V.27 scrambler within the modem can be used to generate a 127-bit word.

INTERFACE DESCRIPTION

STANDARD DIGITAL INTERCHANGE

Term (CCITT V.24 Equivalent)	EIA RS232C Equivalent	Module Interface		Description
		Input	Output	
T103	BA	T-9		Transmitted Data
T104	BB		R2-5	Received Data
T105	CA	T-8		Request to Send
T106	CB		T-6	Ready for Sending (Clear to Send)
T109	CF	R1-4	R2-22	Data Channel Received Line Signal Detector (Carrier Detect)
T111	CH	T-12, R2-9		Data Signalling Rate Selector Selects 2400 bps or 1200 bps Mode
T113	DA	T-7		External Transmit Clock (Transmitted Signal Element Timing)
T114	DB		T-10	Transmit Clock (Transmitted Signal Element Timing)
T115	DD		R2-6	Receive Clock (Receive Signal Element Timing)

ANALOG LINE INTERFACES

Term	Module Interface		Description
	Input	Output	
REC IN	R1-12		Analog Line Signal Input (Receive Filter Input)
T1		T-1	Low Impedance Transmitter Output
T2		T-2	Standard Transmitter Output 600 ohms Impedance

COMMON MODEM DIGITAL CONTROLS

Term	Module Interface		Description
	Input	Output	
V26A	T-16 R2-13		Selects V.26A or V.26B Dibit Encoding
I	{ T-15 R2-12 T-17 R2-14 }		Controls for Scramble Operation
S8GR			
NSYNC	T-14 R2-11		Controls T109 to Force Rapid Resynchronization of the Receiver
CLAMP	R2-10	T-13	Implements Squelch for Carrier Detect (T109)

TRANSMITTER DIGITAL CONTROLS

Term	Module Interface		Description
	Input	Output	
CAUTO	T-3		Initiates Answer Tone
TONA		T-5	Indicates Completion of Transmission of Answer Tone
TBC		T-4	Transmitter Baud Clock
Z	T-28		Input Forcing Transmit Clock (T114) to Phase and Frequency Lock to External Transmit Clock (T113)
T2W/4W	T-11		Inputs Affecting Ready for Sending
X	T-24		Response Times, Answer Tone Frequency
K	T-25		and Carrier Detect (T109) Squelch
Y	T-26		
TC06	T-27		
800MS	T-29		
E	T-30		

TRANSMITTER ANALOG CONTROLS

Term	Module Interface		Description
	Input	Output	
DAC OUT		T-22	Output of Digital to Analog Converter
TFIL	T-23		Input to Low Pass Filter. DAC OUT is Normally Connected to TFIL Unless Additional Filtering or an Equalizer is to be Inserted.
TIN	T-31		These Nine Signals Implement the Transmitter Output Level Attenuator. One of the Signals -1dBm, ..., -15dBm is Strapped to TIN to Set the Desired Output Level.
-1dBm		T-39	
-3dBm		T-38	
-5dBm		T-37	
-7dBm		T-36	
-9dBm		T-35	
-11dBm		T-34	
-13dBm		T-33	
-15dBm		T-32	

RECEIVER DIGITAL CONTROLS

Term	Module Interface		Description
	Input	Output	
R8CK	R1-1	R2-25	Receiver Baud Clock
RLSD	R2-24	R1-2	Control Signals to Generate Carrier Detect (T109) and Implement T109 Threshold Set Select Function
THRH	R1-3	R2-23	
R2W/4W	R2-8		
TH09	R2-18		
TC09	R2-15		Determines Carrier Detect (T109) Off-to-On Response
PBS	R2-16		Determines Carrier Detect (T109) On-to-Off Response
CP04	R2-17		Clamps Received Data (T104) to a mark or space when Carrier Detect (T109) is Off
CP15	R2-19		Optional Clamping of Received Clock (T115)
FSYC	R2-20		Fast Sync Optional Fast Resynchronization Procedure

RECEIVER DIGITAL DIAGNOSTICS

Term	Module Interface		Description
	Input	Output	
SYC		R2-1	Digital Outputs which Enable User to Generate Eye Pattern and Phase Error Information
RCVDS		R2-2	
DCP		R2-4	
A		R2-3	
PE		R2-7	

RECEIVER ANALOG CONTROLS

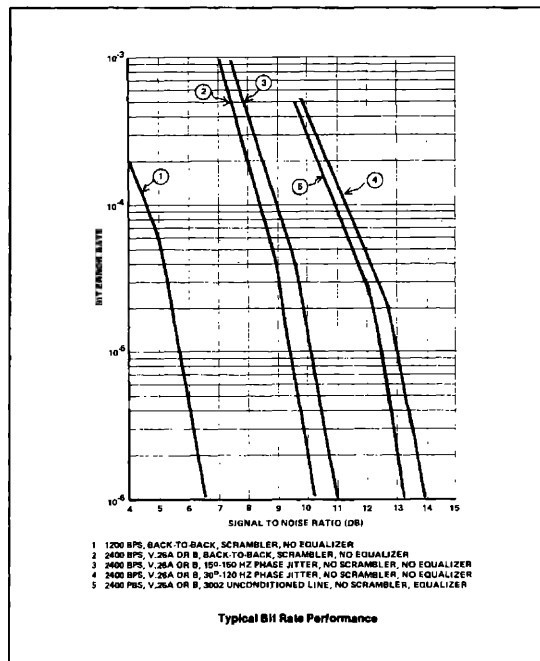
Term	Module Interface		Description
	Input	Output	
REC OUT	R1-7		Receive Filter Output
EQ IN	R1-8		Equalizer Input
EQ OUT	R1-6		Equalizer Output
RLSD IN	R1-5		Carrier Detect Circuitry Input
AGC IN	R2-21		Automatic Gain Control Circuitry Input
AGC OUT		R2-26	Automatic Gain Control Circuitry Output
GAIN		R1-10	Optional Carrier Detect (T109) Threshold Selection Controls
G1	R1-11		
G2	R1-9		
ANALOG	R2-27		Sample and Hold Circuitry Input

MODEM PERFORMANCE

The R24 is a high performance synchronous 2400 bps DPSK modem, utilizing a coherent demodulation technique to achieve reliable operation over the switched network or unconditioned lines. This section contains a quantitative discussion of the R24's typical performance under varying test conditions.

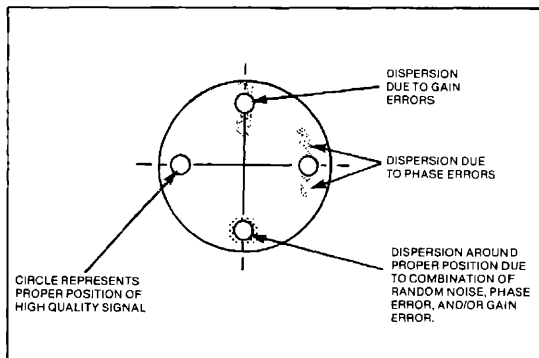
Timing Jitter — The maximum steady state timing jitter of "receive clock" with respect to "transmit clock" is less than 10% p-p for an input signal-to-noise ratio of 12 dB.

Bit Error Rate — The following graph represents typical R24 performance:



Phase Error — Phase error can be measured by using the modem's output signals PE, SYC, and A. With an external test circuit, a numerical value can be derived to indicate the quality of received data. This numerical value can be directly correlated to bit error rate performance. The required test circuit can be implemented with discrete circuitry or in software within a microcomputer.

Eye Pattern — By using the modems digital output signals RCVDC, SYC, and A along with an added test circuit, the user can generate an oscilloscope quadrature eye pattern. This pattern displays the received signal as a group of dots in the baseband signal plane; hence, it is a graphic representation of modem performance.



Typical Eye Pattern: 4 Phase-2400 bps-1200 Baud (V26A)

Phase error and eye pattern can be extremely useful for modem acceptance testing, product evaluation, and observation of line signal quality under actual operation.

ELECTRICAL CHARACTERISTICS

POWER REQUIREMENTS

Module	Voltage	Ripple	Maximum Current
T	+5 Vdc $\pm 5\%$	100 mV p-p	38 mA
	+12 Vdc $\pm 5\%$	50 mV p-p	16 mA
	-12 Vdc $\pm 5\%$	50 mV p-p	48 mA
R1	+12 Vdc $\pm 5\%$	50 mV p-p	23 mA
	-12 Vdc $\pm 5\%$	50 mV p-p	16 mA
R2	+5 Vdc $\pm 5\%$	100 mV p-p	64 mA
	+12 Vdc $\pm 5\%$	50 mV p-p	25 mA
	-12 Vdc $\pm 5\%$	50 mV p-p	78 mA

Maximum total power consumption approximately 3 watts.
Typical total power consumption approximately 2 watts.

DIGITAL INTERFACE

The R24 provides LS TTL or CMOS compatible logic levels that are functionally equivalent to EIA RS232/449 and CCITT V.24.

Input Logic	Allowed Input Voltage Levels
Low	-12.0V to +0.8V Sinking $<10 \mu A$
High	+4.0V to +5.0V Sourcing $<10 \mu A$

Digital inputs are directly CMOS compatible. Interfacing with standard TTL or low-power Schottky TTL requires an external pull-up resistor.

Output Logic	Allowed Output Voltage Levels
Low	0.0V to +0.4V Sinking 0.36 mA
High	+4.0V to +5.0V Sourcing 100 μA

Digital outputs are directly CMOS or low-power Schottky TTL compatible.

The R24 provides an analog interface that must generally be transformer coupled to ensure normal telephone line isolation. Through appropriate selection of transformers and other interface circuitry, the R24 can be configured to operate on leased or dial-up telephone lines, or on other special private networks. For the dial-up interface, Rockwell offers an FCC registered module that allows direct connection to this network. For the leased line interface, only transformers with characteristics similar to those utilized on the R24 modem evaluation board are required for this connection.

Transmitter Output (Normal)

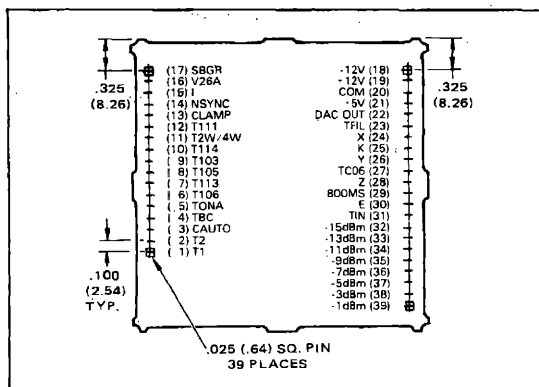
Transmitter Output (Alternate) Low Impedance:

Output Impedance: 0 ohms (op amp output)
Maximum output level $\leq +6.0$ dB

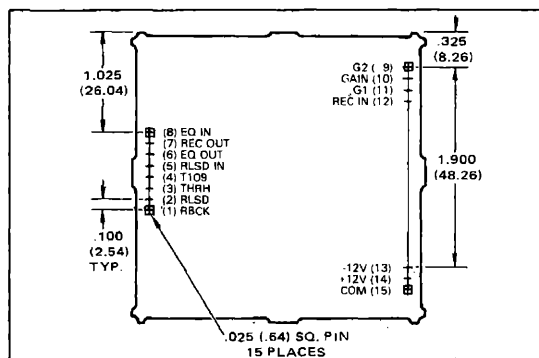
Note: This output for transformer loss compensation.

Receiver Input:

Input Impedance: 15.8K ohms $\pm 1\%$
Maximum Input Level: 0.0 dBm



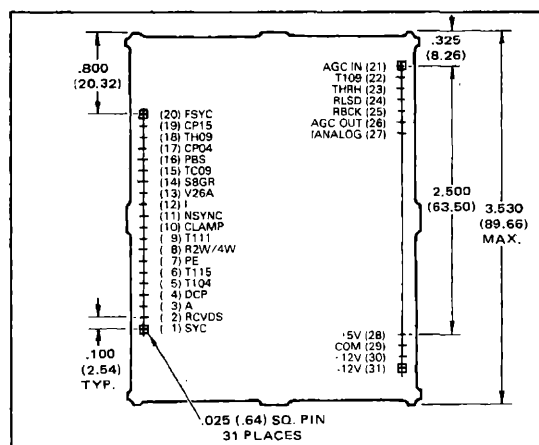
Transmitter Module Package



Receiver — R1 Module Package

Technical drawing of a lead assembly. The drawing shows a horizontal lead pipe with two vertical components attached. The left component is labeled ".300 MAX. (COMPONENTS)". The right component is labeled ".344 ± .005". The distance between the centers of these two components is 2.400. The total length of the lead pipe is 2.75 ± .03. The distance from the right end of the lead pipe to the center of the right component is .080 ± .007. The distance from the right end of the lead pipe to the right edge of the right component is .100. The distance from the right end of the lead pipe to the right edge of the left component is .062. The drawing is labeled (LEAD PROTECTION).

NOTE: This cross-section is common to all modules.



Receiver — R2 Module Package

NOTES: 1) Dimensions in inches (millimeters).
2) Component side shown

PRINTED CIRCUIT BOARD MOUNTING OPTIONS FOR THE R24 MODULES

Three methods of mounting are commonly used. Each configuration has certain distinct advantages.

Mounting Method	Type of Connection or Connector Used	Basic Advantage
Standard Flush PCB Component Mount	Wave Soldered Into Standard PCB Eyelets	Lowest Height Profile
Above Board Low Profile Socket	Connectors (SAE Series 3000 or Methode Series 1000) These Sockets are Wave Soldered Into Standard PCB Eyelets	Plug-in Capability at Low Cost
PCB Plug-in Sockets (Bullets)	Connectors (AMP Miniature Spring Sockets.) Pin Sockets are Individually Soldered Into PCB Eyelets	Lowest Profile for Plug-in Capability

ENVIRONMENTAL SPECIFICATIONS:

Operating temperature: 0°C to 60°C

Storage temperature: -40°C to +80°C

Relative humidity: to 95% (non-condensing)

Altitude: -200 to 10,000 feet (-6.1 meters to 3,049 meters)

Burn-In: 96 hours at 70°C

Ordering Information

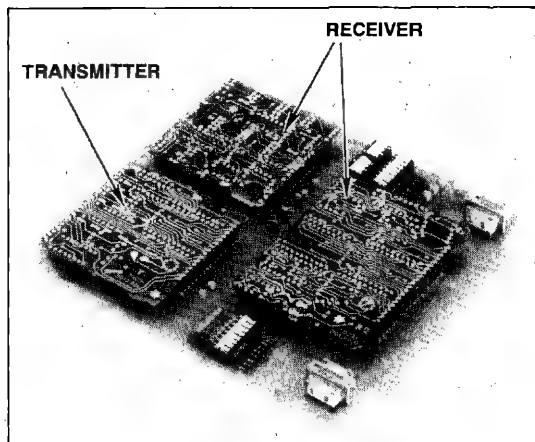
When ordering, specify products as follows:

R24 — Set of 3 modules (T, R1, R2)

R24MEB — Modem Evaluation Board

R24 MODEM EVALUATION BOARD

To facilitate evaluation and design-in of the R24 modem for new and existing equipment designs, an R24 Modem Evaluation Board (R24MEB) is available. The R24MEB can be easily combined with terminal systems for real-time performance evaluation.



R24 Modem Evaluation Board (R24MEB)

The Modem Evaluation Board is equipped with a standard 31 pin edge connector, control switches, output level jumper, and interface transformers. These features allow full control of the interface circuitry. In addition, this unit can be used directly in a U.S. leased line configuration. The R24MEB is recommended for all first-time users to assist in their evaluation. Complete documentation is supplied with each initial R24MEB.



R24MEB MODEM EVALUATION BOARD

INTRODUCTION

To aid the user in the design phase of leased line modems, Rockwell has made available the R24 Modem Evaluation Board (MEB). The R24MEB is a convenient cost effective means for evaluation and design-in of the R24 2400 bps Integral Modem.

The Modem Evaluation Board is equipped with pin receptacles for mounting and interfacing the three R24 receiver and transmitter modules (R1, R2 and T). In addition to all interconnections being etched on the back of the board, the R24MEB also provides telephone coupling transformers, transient protection circuits, DIP switches (for option selection and gain control) and a DIP socket for jumper selection of the transmitter output level. A 31-pin edge connector (with Industry standard 0.125 inch contact centers) provides pin-in/pin-out, as well as power connections for analog and digital interface signals.

These features allow full control of the modem interface circuitry. Also, the complete R24 modem can be used directly in a U.S. leased line configuration. The R24MEB is recommended for all first-time users to assist in their evaluation. Complete documentation is supplied with each initial R24MEB.

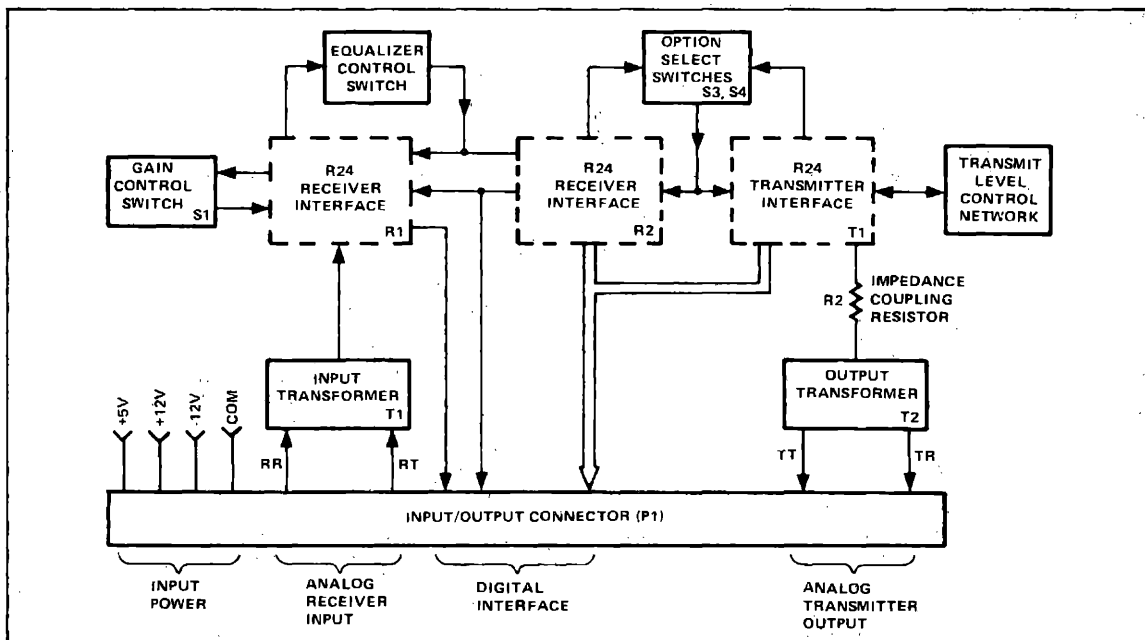
FEATURES

- Convenient evaluation method of R24 Integral Modem modules
- Exercises all R24 Integral Modem features
- Easily integrated into a prototype system
- Cost effective for low-volume applications
- Will serve as incoming test vehicle
- Standard board edge connector
- Pin receptacles for easy mounting/interfacing R24 modules (R, R2, T)
- Complete option select switches
- Transmitter output level strap selectable
- Backed by complete customer support documentation package



R24MEB Modem Evaluation Board

10



R24MEB Functional Diagram

ORDERING INFORMATION

When ordering, specify products as follows:

R24MEB — Modem Evaluation Board
 R24 — Set of 3 modules (T, R1, R2)

BOARD DIMENSIONS

Width: 5.875 in. (14.923 cm)
 Depth: 6.813 in. (17.305 cm)



RDAA ROCKWELL DATA ACCESS ARRANGEMENT MODULE

PRELIMINARY

SECTION 1 — INTRODUCTION

This document is an aide to customers installing, operating and troubleshooting the Rockwell Data Access Arrangement (RDAA) Module designed and manufactured by Rockwell International.

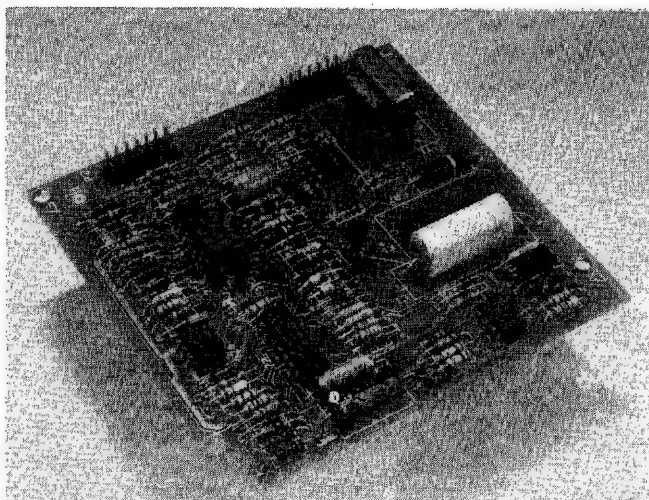
THE RDAA MODULE

The RDAA Module enables the modem user to make direct connections of their modems to the domestic switched telephone network. The RDAA is completely registered with the Federal Communications Commission under Rules Part 68. Therefore, *no* user re-registration of OEM data communication equipment is necessary when used with the RDAA. This means a definite cost-savings for the OEM equipment designer.

In addition to establishing your desired data transmission path, the RDAA also features an automatic answering function, line surge and hazardous voltage protection, switch hook status indication, ringing indication and automatic signal level control. Automatic dialing can be performed by pulsing the OH relay or by transmitting tone pairs.

FEATURES

- Pre-registered (under FCC Rules, Part 68) for direct connection to dial telephone network
- Integral Data Access Arrangement (DAA)
- Automatic dialing—pulse or tone
- Establishes data transmission path
- Automatic answering function
- Surge and hazardous voltage protection
- Switch hook status indication
- Ringing indication
- Automatic line signal output limiting
- Programmable or Permissive (strap selectable) connection arrangements
- Small size (approximately 3.95" by 3.94") (100 mm. by 100 mm.)



RDAA Module

10

The RDAA is easily incorporated into the users end product by either using the provided mounting holes, and/or using the card-guides without card-edge connector. The small size of the RDAA makes it ideal for piggyback type mounting.

The Rockwell RDAA printed circuit board is 3.94 inches (100 mm.) in width and 3.94 inches (100 mm.) in depth.

SELECTABLE CONFIGURATIONS

As a prerequisite, telephone companies require that the signal level received at their local central office not exceed -12 dBm. Several different connection arrangements have been established (as documented in the FCC Rules, Part 68) to meet this requirement.

By jumper selection (Figure 1) the RDAA can be configured to operate in either the Programmable (PG) or Permissive (PM) connection arrangement. This is accomplished by placing the jumper in either the W2 or W1 locations for the desired mode. W1 jumper in, W2 jumper out for the permissive mode. W2 jumper in, W1 jumper out for the programmable mode.

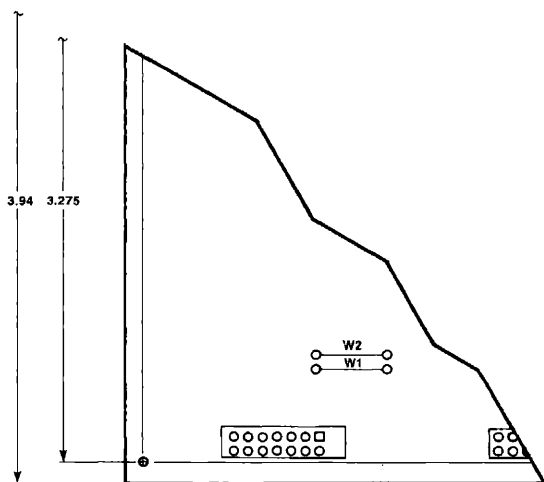


Figure 1. RDAA Module Jumper Selection Location

When using the Programmable connection arrangement, the maximum signal level allowed to be transmitted across T and R is set by a resistor installed by the telephone company in their wall jack (RJ45S or RJ41S) at the customer location. The resistor interacts with the RDAA through the leads PR and PC to program the maximum output level in one dB steps between -12 dBm and 0 dBm. Selection of the resistor from thirteen possible values is based on loop loss measurements performed by the telephone jack installer. The Programmable arrangement provides for the transmission of the maximum allowable amount of power. Therefore, this arrangement offers optimum performance over long loops.

When the Permissive connection arrangement is employed, the maximum signal output level across T and R is fixed at -9 dBm. The Permissive jacks (RJ11C) used for line connections are the same jacks used for standard voice installations. Therefore, this arrangement provides for greater mobility of user equipment.

RDAA DIMENSIONS

The dimensions for the RDAA Module are given in Figure 2.

MATING CONNECTORS

The mating connectors of the RDAA are as follows:

1. Two row (14 pins) ribbon type connectors .1" spacing between pins.

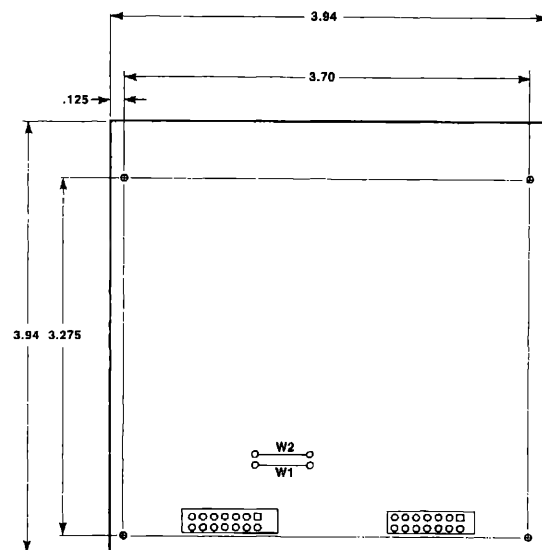


Figure 2. RDAA Module Dimensions

SECTION 2 — INTERFACE DESCRIPTION

INTERFACE CIRCUIT DESCRIPTION

The following paragraphs describe in detail the RDAA interface circuits shown in the block diagram (Figure 3) and the interface circuits listing (Table 2-1).

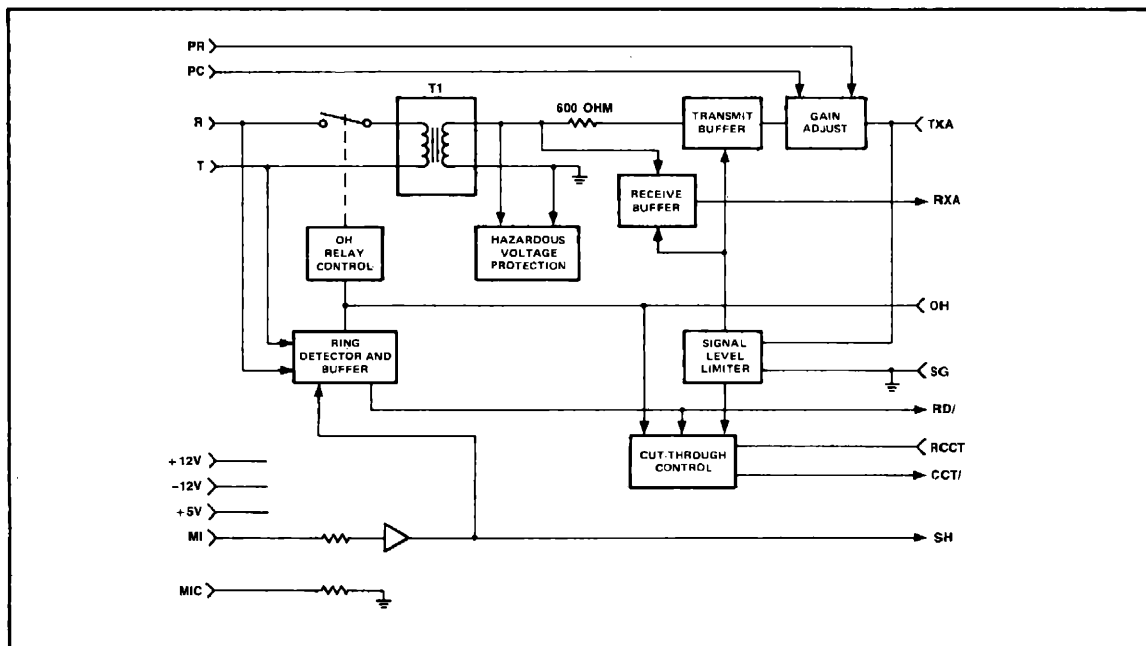


Figure 3. RDAA Functional Block Diagram

Table 2-1. RDAA Interface Circuits

Lead Designation	Signal Direction To:			Function
	User	RDAA	Both	
R, T MI, MIC PR, PC			X X X	Transmission leads for data signals. Leads to telephone set switch hook. Leads to programming resistor.
+5V, +12V, -12V		X		DC power required.
SG RD/ RCCT OH SH CCT/ TXA RXA	X X X X X	 X X X	X	Signal ground required. Ringing signal present indication. To request data transmission path cut through. To control Off-Hook relay. Status of telephone set switch hook. Transmission path cut through indication. Lead to modem output. Lead to modem input.

SG

The SG (Signal Ground) is the common reference for all modem interface signals.

RD/

RD/ (Ring Detect) indicates to the user by an ON (Low) condition that a ringing signal is present. The RD/ signal will not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40V rms, 15 to 68 Hz appearing across Tip and Ring with respect to ground. RD/ is also used to disable the transmission path. The electrical characteristics of the RD/ signal are shown in Table 2-2.

**Table 2-2. Output Signals RD/
SH and CCT/ Characteristics**

Output Logic State	Output Levels
LOW	0.0 to 0.4V while sinking < 1.6 ma
HIGH	2.4 to 5.0V while sourcing < 40 μ A

RCCT

RCCT (Request Coupler Cut-Through) is used to request that a data transmission path through the RDAA be connected to the telephone line. When RCCT goes OFF (Low), the cut-through buffers are disabled and CCT will go OFF (High) within 1 millisecond. RCCT must be OFF (Low) during dial pulsing but ON (High) for tone address signaling. The electrical characteristics of the RCCT signal are shown in Table 2-3.

Table 2-3. Input Signals RCCT and OH Characteristics

Input Logic State	Input Levels
OFF or LOW ON or HIGH	0.0 to 0.8V, load current \leq 0.36 ma RCCT = 2.0 to 5.0V, load current \leq 20 μ A OH = 2.0V, load current \leq 100 μ A 5.0V, load current \leq 250 μ A

OH

OH controls the OFF-HOOK relay. Applying an ON (High) signal to OH closes the OH relay and establishes a DC path between T and R. Maximum delay between the ON signal to OH and the close of the OH relay is 10 ms. When originating a call, an ON (High) signal is used to request dial tone. After detecting dial tone, OH can be pulsed to generate the dial pulses corresponding to the number of the called station (see Section 4.2). On incoming calls, an ON (High) signal to the OH lead initiates the answering sequence (see Section 4.1). The characteristics of the OH signal is shown in Table 2-3.

NOTE

WARNING. If OH is asserted to a logic high before the incoming call ring signal is completed, the OH reed relay switch contacts may suffer degradation.

SH

An ON (High) signal on the SH lead indicates to the user that the associated telephone (if used) is in the talk mode i.e., a contact closure exists between M1 and MIC. The characteristics of the SH signal are shown in Table 2-2.

CCT/

CCT/ is the Coupler Cut Through. An ON (Low) signal to the CCT/ lead indicates to the user that the data transmission path through the RDAA is connected. The ON (Low) state does not indicate the status of the telephone line or connection. The characteristics of the CCT/ signal are shown in Table 2-2.

TXA

TXA (Transmit Analog) is the lead from modem transmitter output. This lead should be tied to GND when the modem is in the receive only mode.

RXA

RXA (Receive Analog) is the lead to modem receiver input. This lead may be left open when the modem is in the transmit-only mode.

POWER REQUIREMENTS

The following power must be provided at the RDAA interface.

- A. +12 VDC \pm 5% @ 15 ma with a maximum ripple of 50 mv peak-to-peak
- B. +5 VDC \pm 5% @ 20 ma with a maximum ripple of 100 mv peak-to-peak
- C. -12 VDC \pm 5% @ 15 ma with a maximum ripple of 50 mv peak-to-peak.

HAZARDOUS VOLTAGE PROTECTION

Lightning induced surge voltages and other hazardous voltages are limited to 10.0 volts peak between the secondary leads of the coupling transformer T1. The isolation between the relay contacts and coils provides the protection of the telephone line from hazardous voltages appearing on any control lead.

RING DETECTOR AND TIMER

When the Ring Detector detects the presence of a ringing signal ranging from 15.3 to 68 Hz with voltage levels of 40 to 150 VRMS across Tip and Ring (T and R) leads, after a delay of 125 ms to 500 ms, it will send an RD/ (Ring Detect) signal to the user's data terminal equipment (DTE). If the DTE is conditioned for answering, the DTE will return an ON signal on OH and RCCT. The OH signal closes the OH relay and starts a timer. The timer is used to provide a quiet interval of more than two seconds between the closing of OH relay and the connection of data transmission path. This allows the telephone company to properly engage their billing equipment. After this delay the CCT/ interface lead goes ON (Low) and data transmission may begin.

RD/ will go OFF (High) in less than 400 MSEC after the ringing signal is stopped. The ring detector is disabled when OH is ON (High) or SH is ON (High).

SIGNAL LEVEL LIMITER AND GAIN CONTROL CIRCUITRY

The limiter monitors the signal level applied to the RDAA input lead TXA and is unaffected by the level of receive signal. When the applied signal amplitude becomes greater than +7 dBm for a period of 1.3 to 3 seconds, the transmission path is disconnected via the transmit and receive buffers, and the output signal CCT/ will go OFF (High).

NOTE

The off-hook relay is not affected by the limiting function, therefore, so triggering the limiting function need not result in call termination.

Reducing the input signal amplitude to less than +7 dBm will reset the limiter in less than 4 milliseconds, restore the data transmission path, and cause the signal CCT to go ON (Low).

In order not to activate the limiter during normal operation, care must be taken to ensure that the maximum signal amplitude into the RDAA input TXA never exceeds +6 dBm. If the modem output has a tolerance of ± 1 dB, then it is recommended to set the modem output to +5 dBm (± 1 dB), so that the maximum signal amplitude into TXA is 6 dBm.

The output control circuitry contains a variable gain buffer which reduces the RDAA output to the maximum allowed level across T and R. When the RDAA is jumpered to operate in the Programmable mode, the resistor in the telephone company wall jack sets the output level to one of thirteen possible values. If the RDAA is jumpered to operate in the Permissive mode, then an internal resistor will set the output to a fixed value. The relationship between the RDAA input amplitude (in dBm) across TXA and GND and the nominal RDAA output level across T and R is given below:

- A. For Programmable mode: output level across T and R = (input amplitude at TXA - 7 dB + (Programmed level set by wall jack resistor).
- B. For Permissive mode: output level across T and R = (input amplitude at TXA) - 16 dB.

IMPEDANCE SPECIFICATIONS

- On-Hook DC: The DC resistance between T and R, and between either T or R and signal ground are greater than 10 megohms for DC voltages up to 100 volts.
- On-Hook AC: The on-hook AC impedance measured between T and R is less than 40K ohms (15.3 Hz minimum).
- Off-Hook DC: Less than 100 ohms.
- Off-Hook AC: 600 ohms nominal when measured between T and R.
- TXA and GND: 2 megohms typical (operational amplifier voltage follower input impedance).
- RXA and GND: 75 ohms typical (operational amplifier voltage follower output impedance).

INSERTION LOSS

There is no insertion loss for the RDAA. The RDAA contains a receive buffer which compensates for transformer insertion loss. For this reason, additional receive buffering is not necessary.

SECTION 3 — INSTALLATION/CHECKOUT

RDAA CONNECTION TO TELEPHONE LINE

Connection of the telephone line interface pins of the RDAA to the network shall be made via standard jacks and plugs as shown in Figure 4. Cable color codes are also shown in Figure 4. A number of telephone line cord manufacturers produce the standard plugs and cables (Meyer Wire Co., Hamden, CT; Virginia Plastics, Roanoke, VA, etc.)

TELEPHONE SET AND JACK ORDERING INFORMATION

If it is desirable to have manual call origination or alternate voice capability, an exclusion key telephone set may be ordered from a local telephone company. The telephone line may be transferred to the telephone set by lifting both the handset and the exclusion key, if the telephone is configured as Data Set Controls Line. This operation is for manual origination or alternate voice transfer (refer to paragraph 4.4 for manual origination procedure). A call may be terminated by replacing the handset in its cradle and taking OH low if OH is not already low.

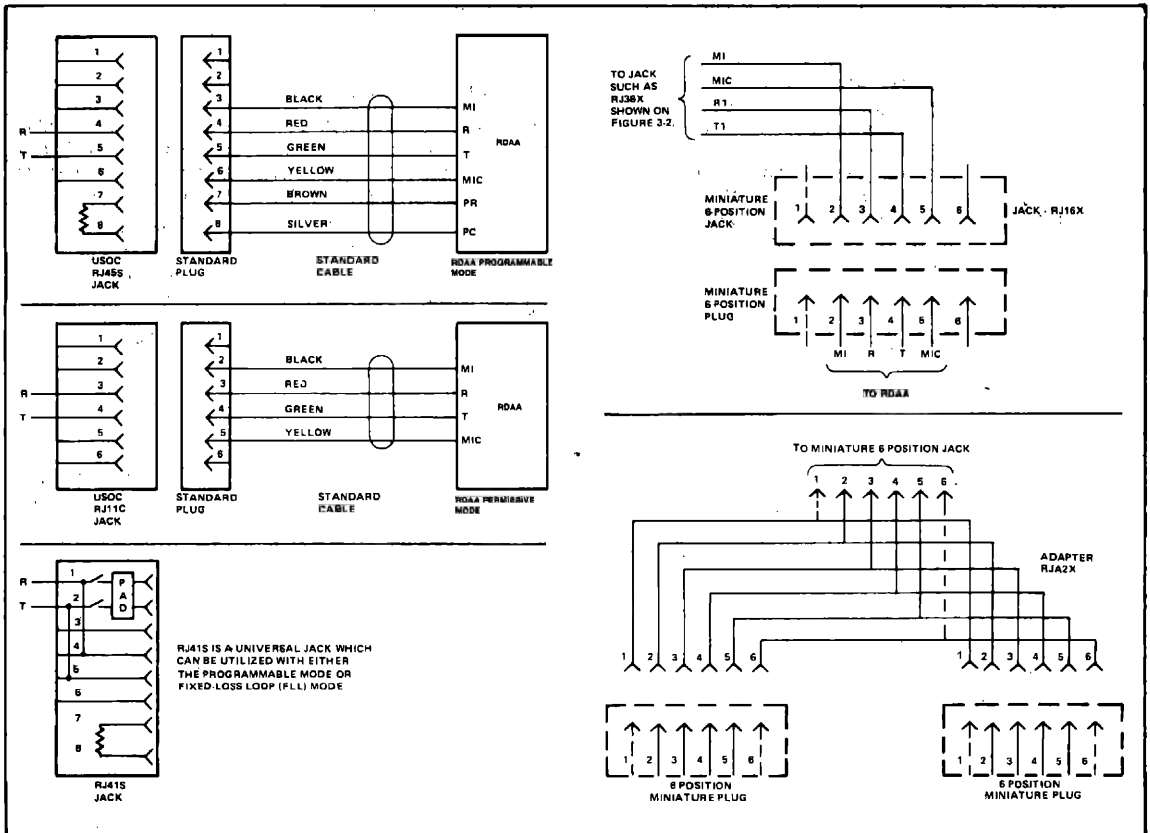


Figure 4. Standard Jacks, Plugs and Cable Color Codes

RDAA
Rockwell Data Access Arrangement Module

The ringer of the telephone set may be disconnected by the telephone company to prevent the bell from ringing.

The telephone company provides an exclusion key telephone under the Universal Service Order Code (USOC) RTC. This telephone set has the following customer options:

- A. A1 - Telephone set controls line
- B. A2 - Data set controls line
- C. B3 - Aural monitoring not provided
- D. B4 - Aural monitoring provided (See Note 1)
- E. C5 - Touch tone dial
- F. C6 - Rotary dial
- G. D7 - Switch hook indication
- H. D8 - Voice mode indication only (See Note 2)

NOTES

- The aural monitoring feature allows the telephone handset to be used for listening to line signals without interfering with data transmission.
- In this option the make contact of the exclusion key and a make contact on the switchhook are connected in series and to the mode indication leads MI and MIC of the data jack. Therefore, the SH signal of the RDAA goes ON only when the exclusion key is lifted.

When ordering this telephone, specify the USOC number RTC and the following options:

- A. A2 - Data set controls line
- B. B3 - Aural monitoring not provided
or
B4 - Aural monitoring provided
- C. C5 - Touch tone dial telephone (503C)
or
C6 - Rotary dial telephone (2503C)
- D. D8 - Voice mode indication only

Another telephone set provided by the telephone company is the Model 502 with exclusion key. To order this telephone set, specify the following:

- A. Modem 502 with exclusion key
- B. Data set controls line

A summary of the information for ordering telephone and jacks is given in Table 3-1. Examples of typical installation are given in Figure 3-2.

Table 3-1. Telephones and Jacks Ordering Information

Output Configuration	Optional Telephone Set	FCC Reg. No.	Ringer Equivalent	Telephone Jack USOC No.	Telephone Set USOC No.
Programmable	With Telephone Set	AMQ9SQ 67943 DP-E	.8B	¹ RJ36X and ^{2,3} RJ45S	RTC or 502 with exclusion key
	Without Telephone Set	AMQ9SQ 67943 DP-E	.8B	^{2,3} RJ45S	N.A.
Permissive	With Telephone Set	AMQ9SQ 67943 DP-E	.8B	¹ RJ36X and RJ16X or ⁴ RJA2X and RJ11C	RTC or 502 with exclusion key
	Without Telephone Set	AMQ9SQ 67943 DP-E	.8B	RJ11C	N.A.
Notes: 1. RJ36X is an 8 position miniature jack into which the telephone plugs. Rather than using an RJ36X jack, the telephone company may use a connecting block to connect the telephone set and data jack to the telephone line. 2. RJ41S is a universal data jack. It may be used for either Programmable or Fixed-Loss Loop mode. The RJ45S jack is preferred, because it costs less. 3. For multiple connections, the RJ45M jack should be ordered. The letter M indicates multiple single line jack for up to 8 lines. Specify the number of lines required when ordering. 4. RJA2X is the adapter shown in Figure 3-1. The use of the RJ36X and RJ16X jacks is recommended.					



For a 4-wire full-duplex configuration, 2 RDAA modules and 2 telephone lines are required. The connection circuitry consists of one 2-wire receive-only connection, and one 2-wire transmit-only connection.

MODULE MOUNTING AND SECURING

The RDAA may be physically incorporated into the OEM's end product by using the four corner (0.156 inch diameter) mounting holes and self-locking plastic standoffs, or by bolting the RDAA module to a rigid structure. The RDAA module may also be mounted using card guides without card edge connector.

A number of manufacturers such as Richlock Corporation, Chicago, IL., produce plastic standoffs (Part Number CBS-3N).

ELECTRICAL INTERFACE

Electrical connection to the RDAA module is made through ribbon type connectors. The connector(s) interface pins (Figure 2) are contained on the component side of the board. There are two test points brought out to the interface connector of the board. Therefore care must be taken to prevent shorting test points with any of the other interface signals.

The RDAA telephone line interface connector pins are physically separated from the RDAA DTE interface connector pins, as shown in Figure 2 and described in Table 3-2.

Table 3-2. RDAA Telephone and Modem Interface

Type Interface Circuit	RDAA Connectors/ Pin No.	Interface Circuit/Signal
DTE Interface Connections	P2-1	CCT/
	P2-2	RXA
	P2-3	TXA
	P2-4	OH
	P2-5	RCCT
	P2-6	RD/
	P2-7	-12V
	P2-8	SH
	P2-9	GND
	P2-10	TP2 EXCESSIVE POWER DETECT
	P2-11	+12V
	P2-12	+5V
	P2-13	N/U
	P2-14	TP1 BILLING DELAY TIME
Telephone Line Interface Connections	P1-4	PC
	P1-3	PR
	P1-1	MIC
	P1-2	MI
	P1-(5-8) & (11-12)	(Not Used)
	P1-9, 10	R
	P1-13, 14	T

Care must be taken in routing the telephone interface pins to the telephone jack. The FCC (Rules, Part 68) requires that the telephone interface leads shall be separated from the leads or metallic paths connecting to power connections.

NOTE

Power connections are those connections between commercial power and any transformer, power supply rectifier, converter, or other circuitry associated with the RDAA. The connection of the interface pins (including the $\pm 12V$ and $+5V$) shown in Figure 2 are not power connections.

The telephone interface leads shall not be routed in the same cable (or use the same connector) as leads or metallic paths connecting to commercial power.

FCC (Rules, Part 68) also requires that the telephone leads T and R be separated from metallic paths to leads connecting to non-registered equipment, when specification details provided to FCC do not show that the interface voltages are less than non-hazardous voltage source limits in Part 68. T and R shall not be routed in the same cable (or use adjacent pins on the same connector) as metallic paths to leads which are not considered non-hazardous. All DTE interface connector signals shown in Table 3-2 have been established as non-hazardous.

Therefore, in routing the telephone interface leads from the RDAA P1 connector to the telephone jack, the following precautions must be strictly adhered to. The telephone jack interface routing path should be as direct as possible. Any cable used in establishing this path should contain no signal leads other than possibly the (previously established as non-hazardous) DTE interface signals shown in Table 3-2. Any connector used in establishing this path should contain no commercial power source signal leads, and adjacent pins to the T and R (Tip and Ring) pins in any such connector should not be utilized by any signals other than possibly those shown in Table 3-2. Also the DTE interface routing path should be made as short as possible.

INSTALLATION PROCEDURE

- Check the telephone line interface cable(s) plug(s) and jack(s) (Figure 4). If the USOC RJ41S jack is used for the Programmable mode, ensure that the jumper W2 is installed and W1 jumper is removed for the programmable mode of operation.
- Make sure the telephone company installer has measured the loop loss correctly and has selected the proper programming resistor in the RJ45S or RJ41S jack.

NOTE

You have the right to know the method used by the installer for measuring loop loss and selecting the programming resistor.

- C. Check the power supplies to see if they meet the proper requirements specified in paragraph 2.2.
- D. Insert the telephone cable plug into the jack, and make the DTE interface connection. Then switch on the power supplies.

OPERATIONAL CHECKOUT PROCEDURE

The following procedures check out the RDAA in association with a modem, a data terminal, a telephone set and an automatic dialer. The telephone set is required only in the manual origination mode (refer to paragraph 4.4) or if alternate voice communication is desired. The automatic dialer is required only in the automatic dial mode (refer to paragraph 4.3).

AUTOMATIC ANSWER MODE

- A. Set the modem transmitted output level to +5 dBm.
- B. Call the local modem from a remote station.
- C. Follow the instructions given in Figure 6.
- D. Transmit data from the local terminal to the remote terminal and monitor the CCT/ signal. It should stay low.
- E. Terminate the call sequence and verify the received data.

AUTOMATIC ORIGINATE MODE

- A. Set the modem transmitted output level to +5 dBm.
- B. Follow the procedure of Figure 8 for touch tone origination or Figure 7 for pulse dial origination.
- C. Transmit data from the local terminal and monitor the CCT/ signal. It should stay low.
- D. Terminate the call sequence and verify the received data.

MANUAL OPERATION MODE

- A. Set the modem transmitted output level to +5 dBm.
- B. Follow the instructions given in paragraph 4.4.
- C. Transmit data from the local terminal. CCT should stay low.
- D. Terminate the call sequence and verify the received data.

SPECIAL INSTRUCTIONS TO USER

Your Rockwell Data Access Arrangement has been registered with the Federal Communications Commission (FCC). To comply with the FCC regulations you are requested to observe the following:

- A. All direct connections to the telephone lines shall be made through standard plugs and jacks as specified in Figure 4 and Table 3-1.
- B. It is prohibited to connect the RDAA to pay telephones or party lines.
- C. You are required to notify the local telephone company of the connection or disconnection of the RDAA, the make, the modem number, the FCC registration number, the ringer equivalence number (refer to Table 3-1) and the particular line to which the connection is made. If the proper jacks are not available, you must order the type of jacks to be used from the telephone company. (Refer to Table 3-1 for the proper jacks and telephones.)
- D. You should disconnect the RDAA from the telephone line if it appears to be malfunctioning. If the RDAA needs repair, return it to Rockwell International. This applies to equipment both in and out of warranty. Do not attempt to repair the unit as this will violate the FCC rules.
- E. The RDAA contains protective circuitry to prevent harmful voltages being transmitted to the telephone network. If however, such harmful voltages do occur, then the telephone company has the right to temporarily discontinue your service. In this case, the telephone company shall:
 - 1. Promptly notify you of the discontinuance.
 - 2. Afford you the opportunity to correct the situation that caused the discontinuance.
 - 3. Inform you of your right to bring a complaint to the FCC concerning the discontinuance.
- F. The telephone company also has the right to make changes in their facilities and services which may affect the operation of your equipment. However, you shall be given notice in writing by the telephone company adequate to allow you to maintain uninterrupted service.
- G. Labeling Requirements:
 - 1. The FCC requires that the following label be prominently displayed on an outside surface of the OEM's end product:

Unit contains Registered Protective Circuitry
which complies with Part 68 FCC Rules

FCC Registration Number:

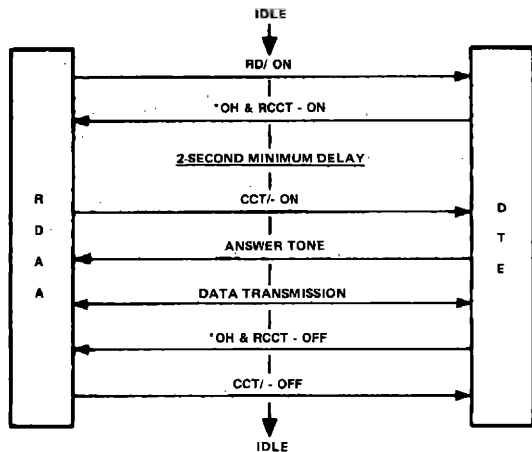
Ringer Equivalence: .8B

- 2. The size of the label should be such that all the required information is legible without magnification.

SECTION 4 — OPERATING INSTRUCTIONS

AUTOMATIC ANSWER

The connection of the data transmission path for automatic answer is as described in paragraph 2.4. To disconnect the data transmission path, just turn off OH and/or DA, as shown in Figure 6.



*DA MAY BE ON PERMANENTLY FOR AUTOMATIC ANSWER.

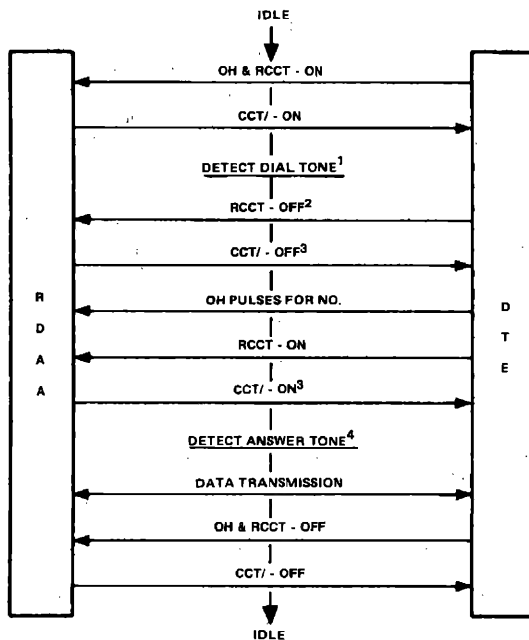
Figure 6. Automatic Answering Sequence

AUTOMATIC DIAL

DIAL PULSE ORIGATION

The DTE must provide the logic to turn ON the OH and DA leads, detect dial tone (or time for 3 seconds to ensure dial tone present), then turn OFF the DA lead and generate the dial pulses corresponding to the called number (Figure 7). The 2-second delay period between OH and DA going ON and the response of CCT going ON will not be invoked in the origination mode. The DTE should monitor for call progress indication (dial tone, busy tone, answer tone, and call intercept).

Requirements for proper call establishment exist on the pulse repetition rate (8 to 11 pulses per second), off duty cycle (60 percent nominal), interdigital delay timing (600 ms to 2 seconds) and chatter and spurious makes and breaks. The RDAA off-hook relay is a Reed relay designed to long life. Bell System requirements for pulse and touch-tone dialing are described in their Communications reference "Electrical Characteristics of Bell System Network Facilities at the Inter-



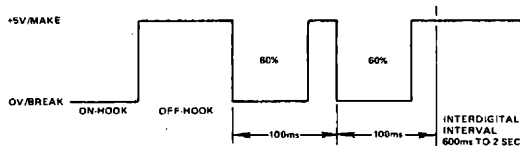
NOTES:

1. DIAL TONE DETECTION IS NOT PROVIDED WITHIN THE RDAA. ALTERNATIVELY, DTE MAY START FROM IDLE, TURN ON OH, THEN TIME FOR 3 SECONDS TO ENSURE DIAL TONE PRESENT AND PULSE OH FOR NUMBER.
2. DA MUST BE OFF DURING DIAL PULSING. DA MAY BE ON AT ALL OTHER TIMES.
3. THE DA TO CCT RESPONSE TIME IS LESS THAN 1 MS.
4. ANSWER TONE DETECTION CIRCUITRY IS NOT PROVIDED WITHIN THE RDAA.

Figure 7. Dial Pulse Origination Sequence

face with Voiceband Ancillary and Data Equipment" (PUB 47001).

The following is an example for pulse dialing the digit #2 through the OH lead.

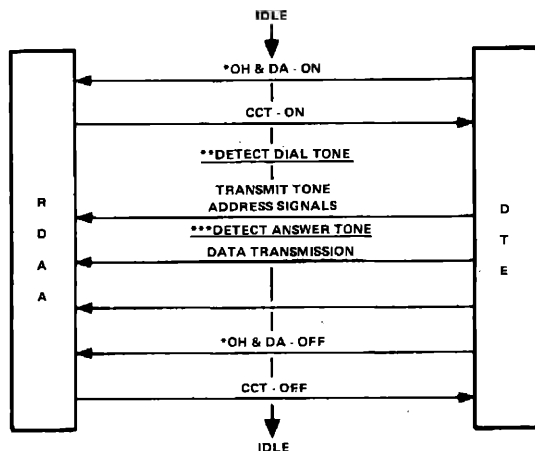


The OH lead can be pulsed directly via microprocessor port, or a commercially available "binary to dial pulse" LSI device such as the Rockwell CRC 8000, the General Instrument AY-5-9151 series, or the Motorola MC 14408. These devices can accept 4-bit binary digital inputs, buffer these digits, and output the OH dial pulses upon command. Also available from numerous semiconductor manufacturers (National, Mostek, General Instrument, Motorola, etc.) are LSI devices capable of interfacing directly to a key board and producing suitable dial pulses.

TOUCH-TONE ORIGATION

The user's terminal must provide the logic to turn ON the OH and RCCT signals, detect the dial tone (or time for 3 seconds to ensure dial tone present) and transmit the tone-address signals via the TXA lead (Figure 8). The 2-second delay period between OH and RCCT going ON and CCT/ going ON is not invoked in the origination mode. The DTE should monitor for call progress indications (dial tone, busy tone, answer tone, and call intercept).

It should be noted that tone address signaling method is significantly more complicated in terms of hardware requirements than simple pulse dialing. The necessary tone pair generators must be added by the user. A number of semiconductor manufacturers produce monolithic LSI tone generators (AMI, Mostek, Motorola, National, General Instrument, Intersil, etc.). These tone pair generators are designed to interface with keyboards or digital ports and may require varying degrees of additional low pass filtering to reduce harmonic distortion. Touch-tone dialing is significantly faster than pulse dialing, but it may not be available in some locations.



*DA MAY BE PERMANENTLY ON.

**ALTERNATIVELY, USER MAY TIME FOR 3 SECONDS TO ENSURE DIAL TONE PRESENT.

***ANSWER TONE DETECTION CIRCUITRY IS NOT PROVIDED WITHIN THE RDAA.

Figure 8. Touch-Tone Origination Sequence

Bell System requirements exist on minimum and maximum tone pair transmit power for proper call address signaling. When the RDAA is in the programmable mode, the gain of the RDAA transmit leg is set by a programming resistor in the telephone jack (over thirteen possible values). This makes establishment of the tone pair signal level to be input to the RDAA (at TXA) which meets the Bell System requirements difficult. It is therefore necessary to operate the RDAA in the Permissive mode for touch-tone origination. In this event the proper input power level (per frequency pair) to the RDAA (at TXA) would be +15 dBm (nominal). This level is well above the RDAA automatic limiter threshold. But the RDAA limiter activates (cuts off transmission path) only if threshold power level is continuously exceeded for about one second minimum, and quickly resets itself if the power level drops below threshold. If the tone pair duration time is restricted to significantly under one second (the minimum duration requirement is only 50 milliseconds) and the minimum interdigital time requirement (45 milliseconds) is observed, the limiter will not be activated. These requirements are easily met if the tone pair generation is under logic control. If the generation is controlled via keyboard input, the limiter will be activated if a key is depressed and held for more than a second, but will recover during the interval between key closures. However, the possibility exists that transients occurring at limiter activation and resetting may endanger proper call origination.

AUTOMATIC CALLING UNIT

Automatic dialing capability may also be added to a data transmission system simply by purchasing or leasing a separate box termed an "Automatic Calling Unit" (ACU). Such units are available from a variety of manufacturers. ACU's are available utilizing pulse or tone dialing. Connections of ACU to the data transmission system may be different for different ACUs. The standard protocol involved in interfacing between the user's data terminal equipment and an ACU is documented in CCITT Recommendation V.25 and also in EIA Standard RS-366, "Interface Between Data Terminal Equipment and Automatic Calling Equipment for Data Communication." It should be re-emphasized that a separate ACU is not necessarily required for automatic dial capability. The RDAA and some external hardware and/or software (as previously described) can suffice.

MANUAL ORIGATION

For manual origination a telephone set with an exclusion key must be ordered from the local telephone company (refer to Table 3-1). After lifting both the handset and the exclusion key, a call may be originated or answered in the same manner as normal telephone service. When the handset and the exclusion key are lifted (MI is shorted to MIC), the signal SH is turned ON. If the user's data terminal is ready, it may respond with OH and RCCT. The RDAA will then turn ON the CCT/ signal. When answer tone is heard, the operator replaces the handset in its cradle. The SH signal will go Low and the data transmission path is connected. When data transmission is completed, the terminal turns OFF the OH signal and returns to the idle state.

SECTION 5 — FAULT ISOLATION

CUSTOMER REPAIR LIMITATIONS

Under the FCC Rules, no customer is authorized to repair an RDAA module. In the event of an RDAA malfunction, return the faulty RDAA to Rockwell International. It is recommended that the following fault isolation instructions provided in this section be performed prior to returning a suspected RDAA module. A periodic check of the DC power supplies is also recommended.

FAULT ISOLATION

The fault isolation flow chart (Figure 9) has been prepared specifically as an aid to the user for locating possible network and/or RDAA module malfunctions.

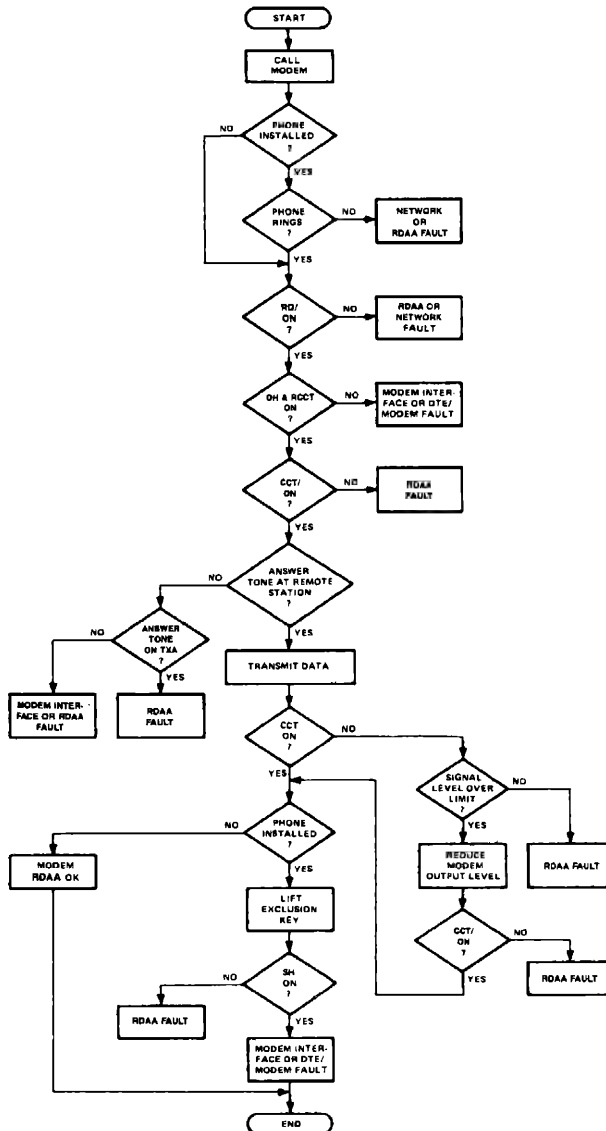


Figure 9. RDAA Fault Isolation Flow Chart

SECTION 11

T-1 AND T-1/CEPT PULSE CODE MODULATION PROTOCOL DEVICES

	Page
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R8040 Tri-Port Memory	11-3
R8050 T-1 Serial Transmitter	11-9
R8060 T-1 Serial Receiver	11-17
R8070 T-1/CEPT Pulse Code Modulation Transceiver	11-23

T-1 AND T-1/CEPT PCM (PULSE CODE MODULATION) PROTOCOL DEVICES Meet AT&T and CCITT Standards

Rockwell International is the first company producing LSI devices for supporting the commercial digital switched network. The 24 or 32 digitized channels meet AT&T and CCITT standards.

This means it is now possible to design T-1/CEPT systems using LSI instead of discrete devices. This results in a much lower parts count, lower power requirements, smaller size and significant cost reductions. It also means an increase in reliability.

Using our LSI devices, the 24 or 32 channels of 64K bps information and signaling are multiplexed over a single pair of wires. All data are transmitted serially, along with framing bits, at 1.544 to 2.048M bps. At the receiving end frame, superframe, and channel synchronization is accomplished,

with signaling information outputted and the 24 or 32 channels uniquely identifiable.

Transmission in digital format instead of analog has inherent ability to perfectly regenerate the signal even after noise in the phone network. The TTL compatible devices operate from a single 5V power supply.

For specialized memory for digital PBX and other telecommunication applications, tri-port memory devices are also available. These allow random read and sequential read simultaneously, and, allow addressing sequentially or randomly. They support either time or space division switching as well as elastic storage applications when transmission and write speeds differ.

Rockwell LSI Devices Provide—

- **Parts Count Reduction**
- **Cabling Reduction**
- **Cost Reduction**
- **Increased Reliability**
- **Increased Performance**



R8040 T-1 TRI-PORT MEMORY

OVERVIEW

The Tri-Port Memory circuit is designed to function as an assembly point and temporary storage area for 8-bit T-1 data. It provides 64 8-bit locations of on-chip random access memory which can be accessed via external addresses or internal sequential addressing.

TRI-PORT MEMORY OPERATION

The Tri-Port Memory device accepts 8-bit parallel input data on lines A through H. This data is stored in an internal memory location that is selected by either random address lines R01 through R32 or by the device's Sequential Address Counter. Write Select signal WSEL determines the source of the address; in the logic 0 state, WSEL selects the random address, in the logic 1 state, WSEL selects the internal sequential address.

The state of Write Enable signal \overline{WE} determines whether or not the data on lines A through H will be written into memory. Data will only be written into memory when \overline{WE} goes low (to a logic 0 state) and the address inputs have stabilized.

The on-chip, six-bit Sequential Address Counter is a binary counter that increments on each positive transition of Sequential Clock (SCLK). When the Counter attains binary 111111, the next positive transition on SCLK will clear it to binary 000000. The Counter will also be cleared unconditionally if Reset signal RST has been set to logic 0 when the positive transition of SCLK occurs.

The Sequential Read Enable signal, \overline{SRE} , enables sequentially-addressed read operations. If \overline{SRE} is logic 0, the sequential accessed data outputs (SA through SH) will become valid within 430 ns after the next positive transition on SCLK. If \overline{SRE} is logic 1, and 350 ns have elapsed since the positive transition of SCLK, the sequential accessed data outputs will become valid 80 ns after the negative transition of \overline{SRE} . The sequential read data will cease to be valid 100 ns after the negative transition of \overline{SRE} or 20 ns after the next positive transition of SCLK, becoming valid with the content of the next sequential location within 430 ns of that SCLK transition.

The Random Read Enable signal, \overline{RRE} , enables random-accessed read operations. If \overline{RRE} is logic 0, the random accessed data outputs (RA through RH) will become valid within 380 ns after the random address lines have stabilized. If \overline{RRE} is logic 1, and 300 ns have elapsed since the random address lines have stabilized, the random accessed data outputs will

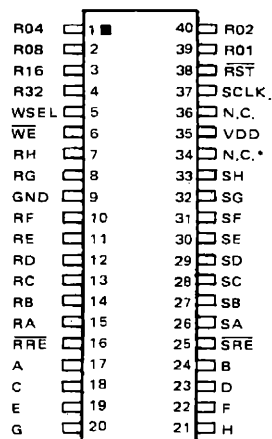
FEATURES

- 64 × 8 bit static memory
- Single +5V supply
- Two totally independent read ports
- Multiple Read access time < 430 ns (worst case)
- Selectable random- or sequential-address Write operation
- On-chip sequential address counter
- Tri-state drivers, for chip-selectable bus operation
- 40-pin plastic dual in-line package
- LSTTL Schottky-compatible (12KΩ pullup, to drive CMOS)

APPLICATIONS

Time-division Multiplex (TDM) digital switching data and control stores

- TDM sequential machines
- Elastic stores
- Hardware/Software control interfaces
- I/O Buffers



*NOTE: PIN 34 HAS AN OUTPUT SIGNAL APPLICABLE ONLY TO ROCKWELL TESTING, MAKE NO CONNECTION TO THIS PIN.

Pin Configuration

become valid 80 ns after the negative transition of \overline{RRE} . The random accessed data outputs will cease to be valid 100 ns after a positive transition of \overline{RRE} or 20 ns after the random address input lines change, becoming valid with the contents of the newly-addressed location within 380 ns after the random address inputs have stabilized.

In the case of a same location read/write cycle, the sequential and/or random data outputs will cease to be valid after a negative transition of \overline{WE} , and will become valid with the newly-written contents within 340 ns of that transition. Control of this parameter minimizes external circuitry required for resolution of read-write contention.

RECOMMENDED OPERATING CONDITIONS

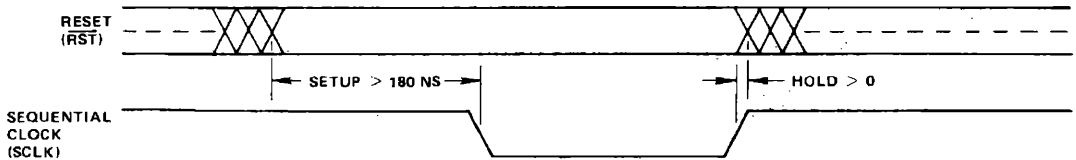
Minimum Setup/Hold Times

Signal	Setup		Hold	
	Measure to	ns	Measure to	ns
SCLK ↑	\overline{WE} ↓	300	\overline{WE} ↑	0
WSEL	\overline{WE} ↓	280	\overline{WE} ↑	0
R01-R32	\overline{WE} ↓	250	\overline{WE} ↑	0
A-H	\overline{WE} ↑	150	\overline{WE} ↑	100
\overline{RST}	SCLK ↓	180	SCLK ↑	0

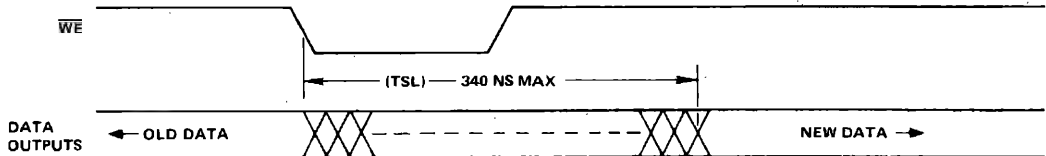
Minimum Pulse Widths

Signal	Minimum Pulse Width
\overline{WE} (=0)	170 ns
SCLK	220 ns

SEQUENTIAL COUNTER RESET SETUP AND HOLD TIMING

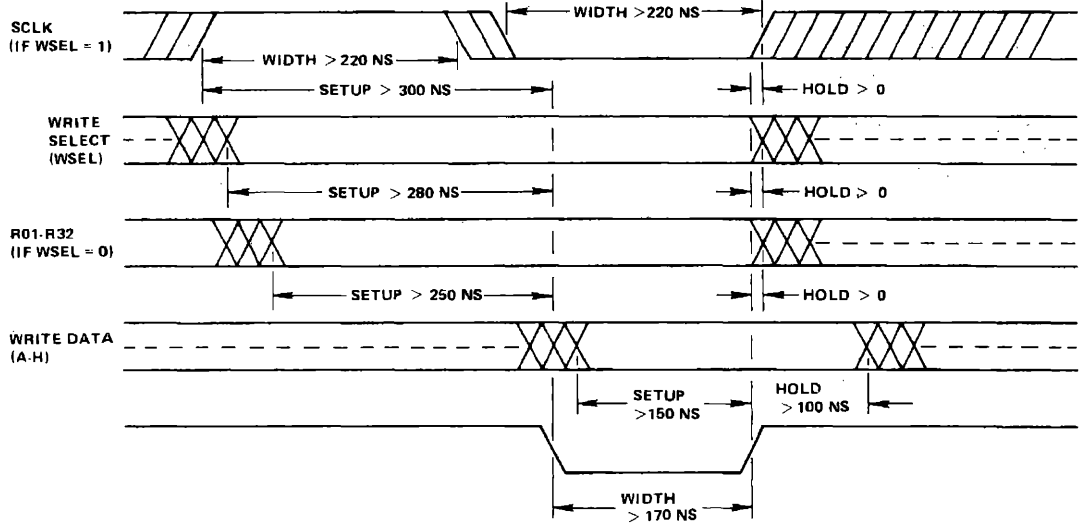
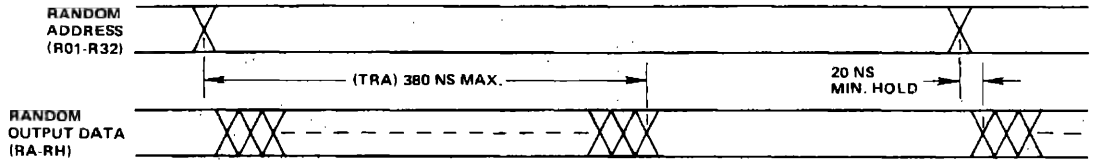
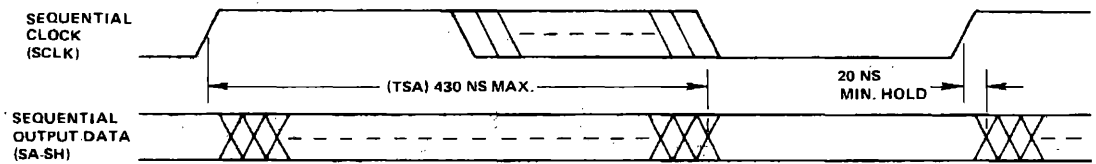
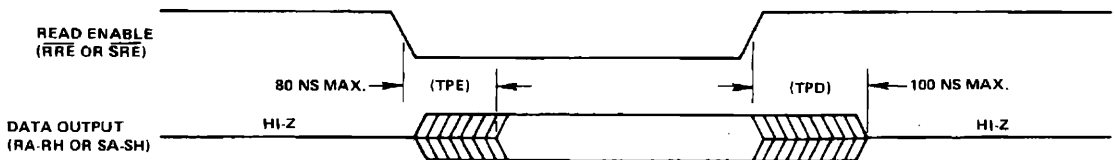


READ OUTPUTS AT SAME LOCATION AS WRITE (ALL OTHER INPUTS STABLE)



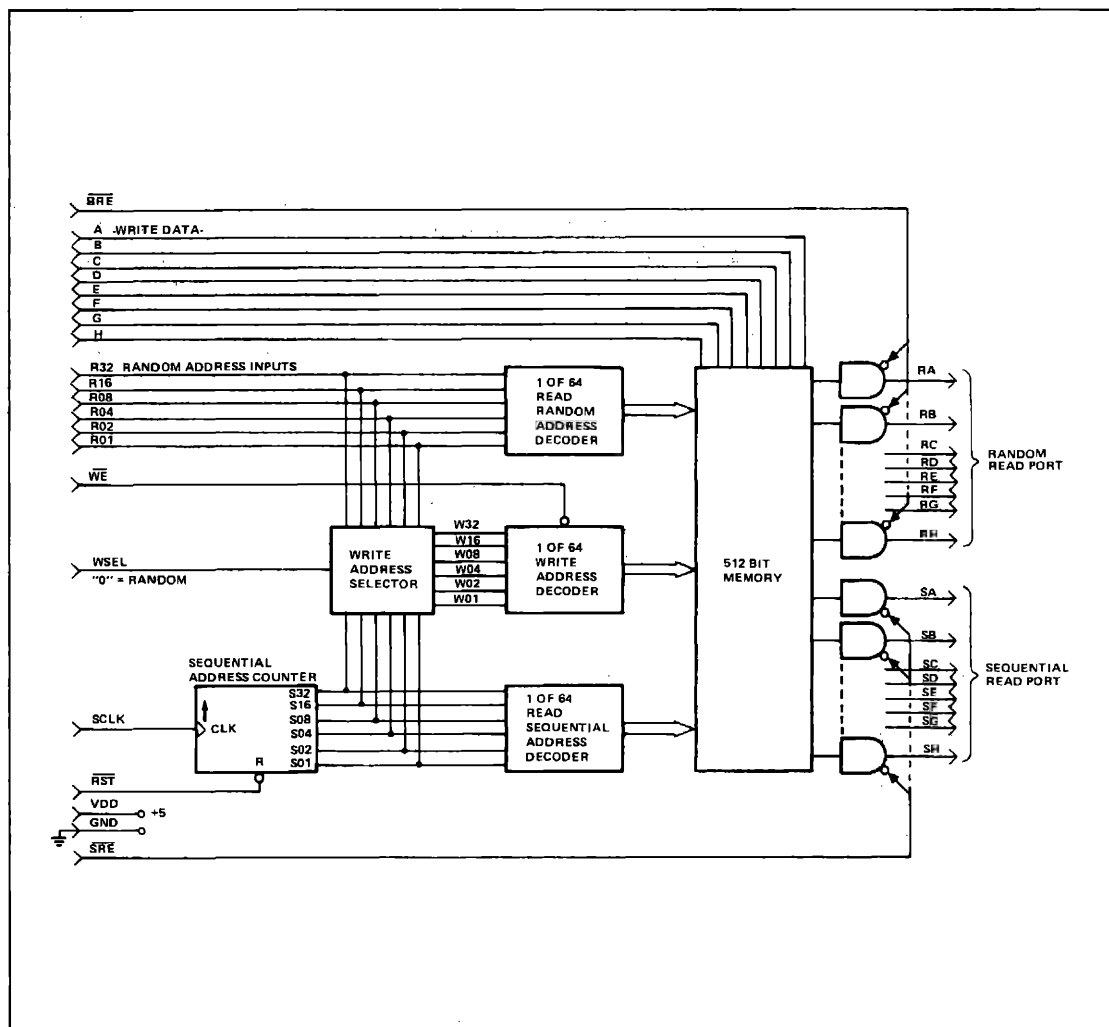
NOTE: RANDOM WRITE ALWAYS AFFECTS RANDOM READ OUTPUTS;
SEQUENTIAL WRITE ALWAYS AFFECTS SEQUENTIAL READ OUTPUTS.
EITHER WRITE WILL AFFECT THE OPPOSITE READ OUTPUT, IF, AND ONLY IF, THE RANDOM ADDRESS AND SEQUENTIAL ADDRESS ARE EQUAL.

WRITE SETUP AND HOLD TIMING

RANDOM READ ($\overline{RRE} = 0, \overline{WE} = 1$)SEQUENTIAL READ ($\overline{SRE} = 0, \overline{WE} = 1$)READ PORT ENABLE/DISABLE (ADDRESS STABLE, $\overline{WE} = 1$)

Propagation Delays

Parameter	Symbol	Min	Max	Units
Random Read Access Time	t_{RA}	0	380	ns
Sequential Read Access Time	t_{SA}	0	430	ns
Read Port Disable (to HI-Z)	t_{PD}	0	100	ns
Read Port Enable	t_{PE}	0	80	ns
Same-Location Read After Write	t_{SL}	0	340	ns



Tri-Port Memory Block Diagram

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+ 4.75 to + 5.25	V
Operating Temperature	T_{OP}	0 to + 70	°C
Storage Temperature	T_{STG}	- 55 to + 150	°C

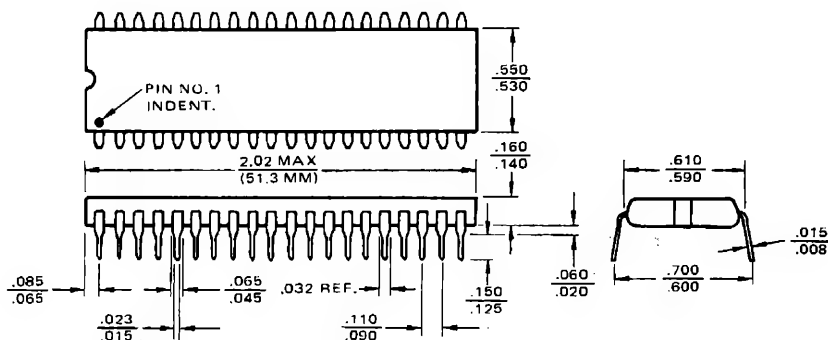
*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD} = +5V \pm 5\%$, $V_{SS} = 0V$, $T_A = 25^\circ C$)

Parameter	Symbol	Min	Max	Unit
Input Logic "1" Voltage	V_{IH}	2.0		V
Input Logic "0" Voltage	V_{IL}		0.8	V
Input Logic "1" Voltage	V_{OL}	2.4		V
Output Logic "0" Voltage	V_{OL}		0.4	V
Output Source Current	I_{OH}	- 100		μA
Output Sink Current	I_{OL}	400		μA
Input Capacitance	C_I		5	pF
Output Capacitance	C_O		25	pF
Power Dissipation (at 25°C)	P_{DSS}		300	mW

PACKAGE DIMENSIONS



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation



R8050 T-1 SERIAL TRANSMITTER

DESCRIPTION

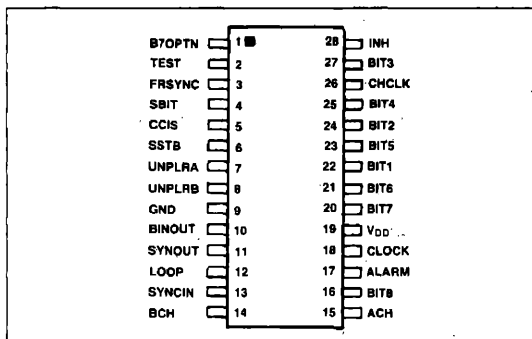
The Rockwell T-1 Serial Transmitter formats data to be serially transmitted according to T-1 D2 or T-1 D3 specifications, inserting framing and signalling bits along with 24 channels of 8-bit channel data. The T-1 Serial Transmitter also provides for alarm reporting via the Bit 2 inhibit method or, with minimal external logic, via the multiframe alignment signal (F_s) modification method.

Figure 1 is a functional block diagram of the T-1 Serial Transmitter. The Mod 193 counter is driven by the clock at 1.544 MHz and is either synchronized to the driving system by input signal SYNCIN or provides synchronization via output signal SYNOUT. Input signal FRSYNC applies synchronization to a Mod 12 counter, which identifies the frame of the 12-frame multiframe being processed.

The input data register latches data during each bit period, when the 8th bit of a channel sample is being transmitted. The data selector outputs the proper sequence of bits, as controlled by a bit count and frame count.

The zero channel monitor function causes Bit 8 or Bit 7 to be transmitted as a "one" if the channel data sample is all "zeros." Input INH provides a means to inhibit the zero channel monitor function. Input B7OPTN controls the particulars of the insertion method.

Two types of transmit formats are provided, a binary output and a paired unipolar output. The unipolar pair provides a means to externally create a single bipolar output with minimal logic.



Pin Configuration

FEATURES

- Single 5V supply, low power Schottky TTL compatible.
- Accepts 8 bits of parallel data as input.
- Generates output as 193 bit serial data stream in T-1, D2, D3 or D4 Mode 3 data format.
- Provides a channel and frame timing signal.
- Provides alternate control for alarm reporting and signalling.
- Provides automatic bit insertion for all-zero channel samples.

T-1 TRANSMITTER INPUTS

Any input $\leq 0.8V$ = logic 0, low. Any input $\geq 2.0V$ = logic 1, high. The transition from a low level to a high level is called a rising edge, while the converse is defined as a falling edge.

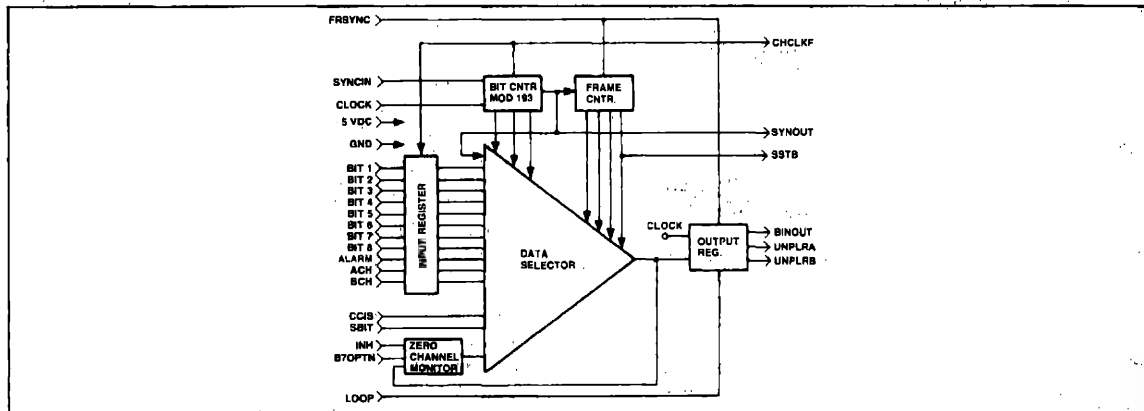


Figure 1. T-1 Serial Transmitter

FRSYNC: Frame Synchronization

Frame sync allows external synchronization of the transmitter's internal frame counter. When FRSYNC becomes high, the frame counter is directly set to frame 1, the first of the twelve frames. If FRSYNC is held high and does not return to zero before a rising edge of CLOCK, the subsequent states of BINOUT, UNPLRA and UNPLRB are high, high and low, respectively, regardless of the states of any other inputs. The latter mechanism is useful for device and/or board testing only and will cause bit errors and/or bipolar violations if used during field operations. See Figures 6 and 7.

SYNCIN: Synchronization Input

SYNCIN allows external synchronization of the internal Modulo 193 bit/channel counter. When SYNCIN becomes high, the Modulo 193 counter is directly set to the state corresponding to the output of the framing (F_T or F_S) bit. The first bit of channel one will be output on BINOUT (and UNPLRA or UNPLRB) as a result of the first rising edge of CLOCK following the return of SYNCIN to logic 0. See Figures 5 and 7.

TEST: Rockwell Device Test Input

Used only for Rockwell device testing. **Keep this input grounded.**

CLOCK: T-1 Clock

Maximum frequency = 1.6 MHz

Minimum pulse width = 275 ns

The T-1 bit period is bounded by the rising edges of this input.

INH: Inhibit Zero Channel Monitor

If INH is high, the zero channel monitor function is disabled, and Bits 7 and 8 are transmitted per corresponding inputs received. See Table 1.

For channels in signalling frames (6 or 12) in which the first six data bits and the signalling highway are all "zero," BIT 7 will be forced to one if INH is low. For any frame except a signalling frame Bit 8 or Bit 7 as selected by B7OPTN will be transmitted as a "one" if the channel input data is "zero" and INH is low.

BITS 1-8: Parallel Channel Data Inputs

Bit 1, the sign bit, will be serially transmitted first, followed by Bits 2 through 8. The falling edge of CHCLKF indicates input channel data has been clocked into the input register and always occurs during the transmission of the final bit (Bit 8) of each channel data sample.

ACH: "A" Channel Highway Signalling

ACH allows the user to transmit one bit of signalling per channel as Bit 8 of each channel data sample in Frame 6 only. ACH is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

BCH: "B" Channel Highway Signalling

BCH allows the user to transmit one bit of signalling per channel as Bit 8 of each channel data sample in Frame 12 only. BCH is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

S-BIT: Multiframe Signalling Bit

SBIT, in conjunction with CCIS, provides an alternate way to control the multiframe signalling bit (F_S) transmission. The S-Bit input is transmitted as the multiframe signalling bit (F_S) if CCIS is held high. Refer to Table 2.

ALARM: Local Alarm

Used for reporting alarm conditions. If the ALARM signal is high, Bit 2 (the most-significant bit) of every channel data sample of every frame is transmitting as a zero. This is commonly called remote alarm signalling. ALARM is clocked into the input register at the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

LOOP: Loop Strap

Provided to aid testing of user applications. When enabled to a high level, LOOP forces the unipolar outputs to transmit alternating ones and zeros, regardless of input conditions, while BINOUT continues to provide normal data outputs. Refer to Figure 3.

CCIS: Common Channel Interoffice Signalling Strap

Provides optional control for replacing the automatic F_S pattern with a 4-kilobit common channel signalling path. When CCIS is high, the SBIT input replaces the F_S pattern and the insertion of ACH and BCH is suspended. The CCIS input may also be used to provide the alternate method of alarm reporting. See Figure 4.

B7OPTN: Bit 7 Option

Provides Bit 7 as an alternate bit position for "one" stuffing, as programmed by the zero channel monitor function. Refer to Table 1.

VSS, VDD: Ground and Power

$V_{DD} = +5 \pm 0.25$ Vdc

$V_{SS} =$ Ground, 0 Vdc

T-1 Transmitter Outputs

Low power TTL Schottky compatible. "1" ≥ 2.4 Vdc, "0" ≤ 0.4 Vdc, CMOS—12K Ω pullup to V_{DD} required.

SSTB: 4 kHz Signalling Channel Strobe

SSTB is the least-significant bit of the frame counter. Unless it is directly set by FRSYNC, SSTB will go high as each framing bit (F_T) is serially transmitted, and will return low as each multiframe alignment signal (F_S) is transmitted. Refer to Figure 2.

SYNOUT: Channel Sync Output

SYNOUT provides a means to synchronize to the internal bit counter (Mod 193). SYNOUT is high for one bit time, beginning just prior to the first data bit of a frame being serially transmitted. Refer to Figure 8. SYNOUT is the only output determined by the falling edge of CLOCK.

CHCLKF: Channel Clock False

The falling edge of CHCLKF, occurring as Bit 8 of any channel is being serially transmitted, indicates input data has been clocked into the input register. With the exception of an extra bit period extending the low level duration at frame bit time, CHCLKF is a divide-by-eight of CLOCK. Refer to Figure 2.

BINOUT: Serial Data Output, Binary Formatted

BINOUT is the binary formatted serial conversion of the parallel input data. The programmed format of BINOUT follows Tables 1 and 2.

BINOUT is synchronously transmitted as a high level if FRSYNC remains high during the rising edge of CLOCK. Refer to Figures 6 and 7.

UNPLRA, UNPLRB: T-1 Serial Data Unipolar Outputs

Two paired unipolar outputs are provided for the purpose of creating a single serial data output transmission in bipolar format. The unipolar output register toggles for each "one" bit to be serially transmitted. UNPLRA and UNPLRB are transmitted as complements for "one" data bits and as low levels for "zero" data bits. See Figure 3.

The input signal LOOP, if high, forces the unipolar outputs to toggle every bit time, regardless of input data.

FRSYNC perturbs the current bits being transmitted by UNPLRA and UNPLRB. If FRSYNC remains high during the rising edge of CLOCK, UNPLRA will be transmitted as a high level and UNPLRB will be low. Refer to Figures 6 and 7.

Table 1. Serial Channel Sample Output Data Truth Table

Inputs X = don't care													Current Frame Number	Binout Serial Output								Notes	
ALARM	INH	B7OPTN	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	ACH	BCH		Channel Bit Position									
														1	2	3	4	5	6	7	8		
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
0	X	X	P	Q	R	S	T	U	V	X	A	X	6	P	Q	R	S	T	U	V	A	2	
0	X	X	P	Q	R	S	T	U	V	X	X	B	12	P	Q	R	S	T	U	V	B	2	
0	X	X	P	Q	R	S	T	U	V	W	X	X	Y	P	Q	R	S	T	U	V	W	2,3	
0	1	X	0	0	0	0	0	0	0	X	A	X	6	0	0	0	0	0	0	0	A		
0	1	X	0	0	0	0	0	0	0	X	X	B	12	0	0	0	0	0	0	0	B		
0	1	X	0	0	0	0	0	0	0	W	X	X	Y	0	0	0	0	0	0	0	W	3	
0	0	X	0	0	0	0	0	0	0	X	0	X	6	0	0	0	0	0	0	1	0		
0	0	X	0	0	0	0	0	0	0	X	X	0	12	0	0	0	0	0	0	1	0		
0	0	1	0	0	0	0	0	0	0	0	X	X	Y	0	0	0	0	0	0	1	0	3	
0	0	0	0	0	0	0	0	0	0	0	X	X	Y	0	0	0	0	0	0	0	1	3	

NOTES: (1) ALARM = 1 has the same effect as BIT 2 = 0
(2) P, Q, R, S, T, U and V may not simultaneously be zero, unless A, B or W is 1
(3) Y is any frame ≠ 6 and ≠ 12 with CCIS = 0, or all frames with CCIS = 1

Table 2. Framing Bit (F_T & F_S) Output Data

Frame Number	Processed Bit	Binout	
		CCIS = 0	CCIS = 1
1	F_T	1	1
2	F_S	0	SBIT
3	F_T	0	0
4	F_S	0	SBIT
5	F_T	1	1
6	F_S	1	SBIT
7	F_T	0	0
8	F_S	1	SBIT
9	F_T	1	1
10	F_S	1	SBIT
11	F_T	0	0
12	F_S	0 (NOTE 1)	SBIT

Notes: (1) Alternate remote alarm reporting may be accomplished by holding SBIT and CCIS both high just prior to initiation of Frame 12.

(2) F_T bit insertion is automatic and no optional control is provided.

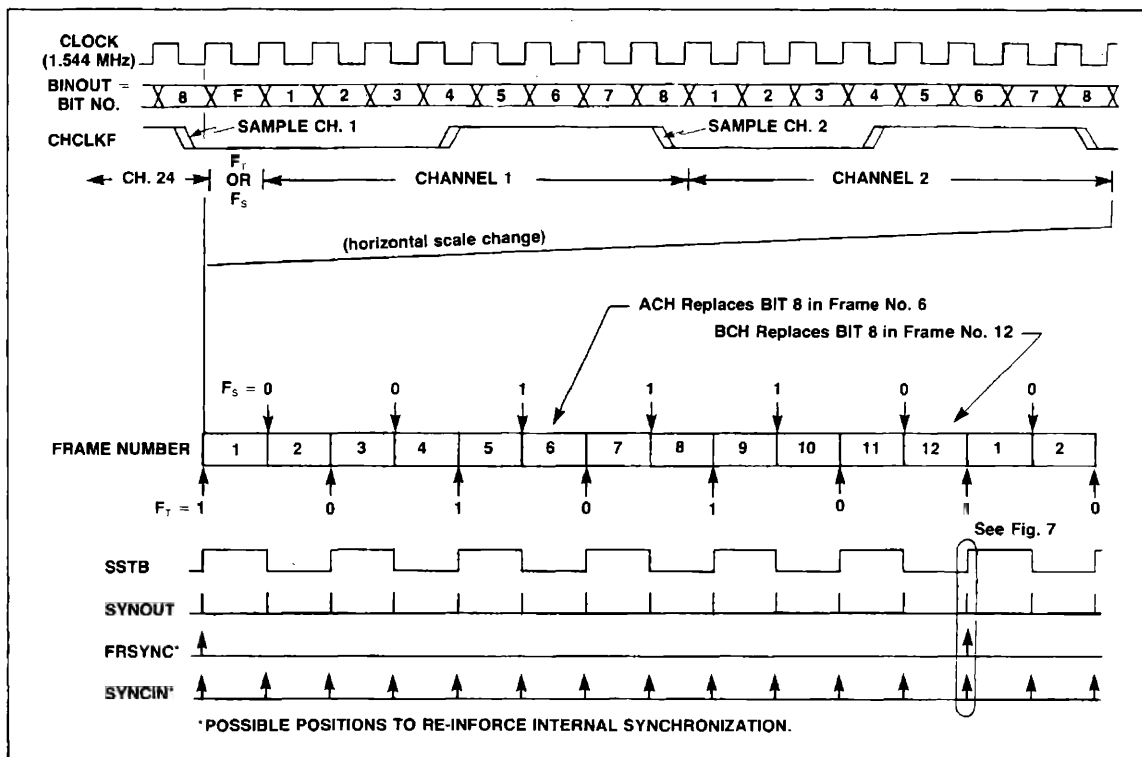


Figure 2. Transmitter Input-Output Signal Relationships

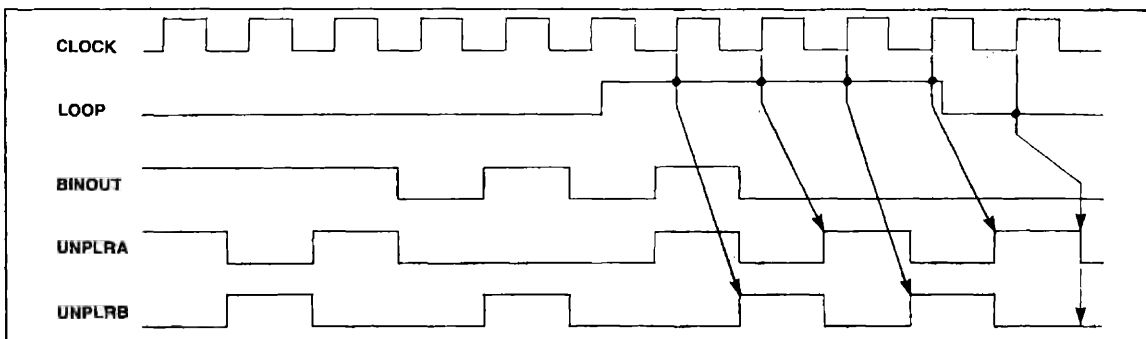


Figure 3. Transmitter Binary, Unipolar Outputs

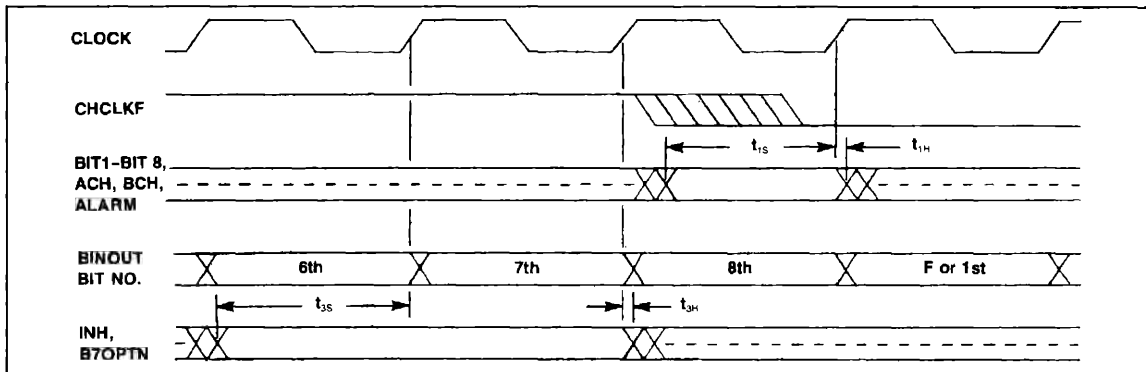


Figure 4 (a). Channel Input Timing

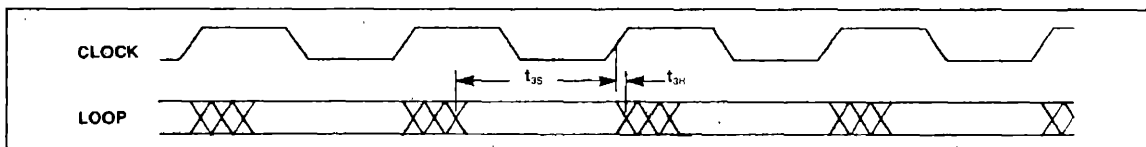


Figure 4 (b). LOOP Input Timing

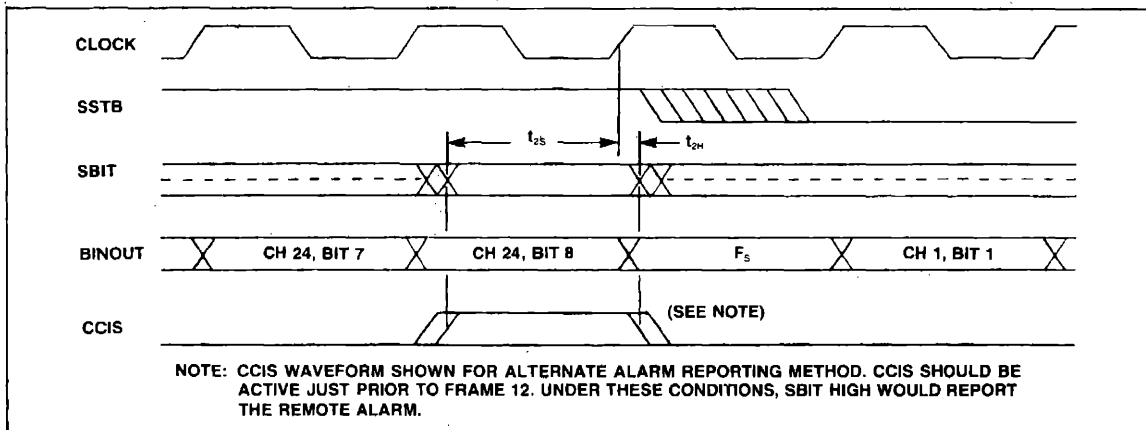


Figure 4 (c). Control Input Timing

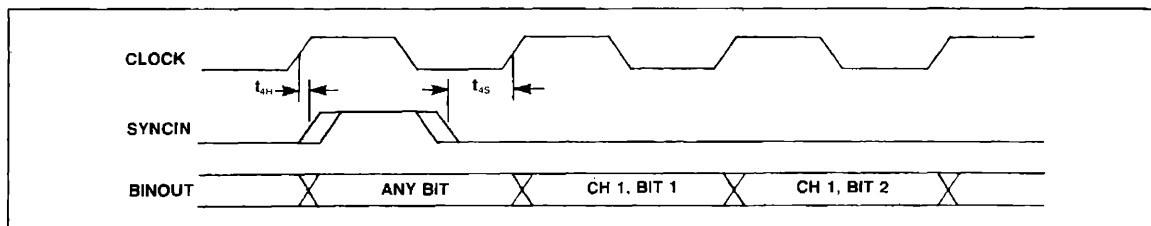


Figure 5. SYNCIN Timing Relationship

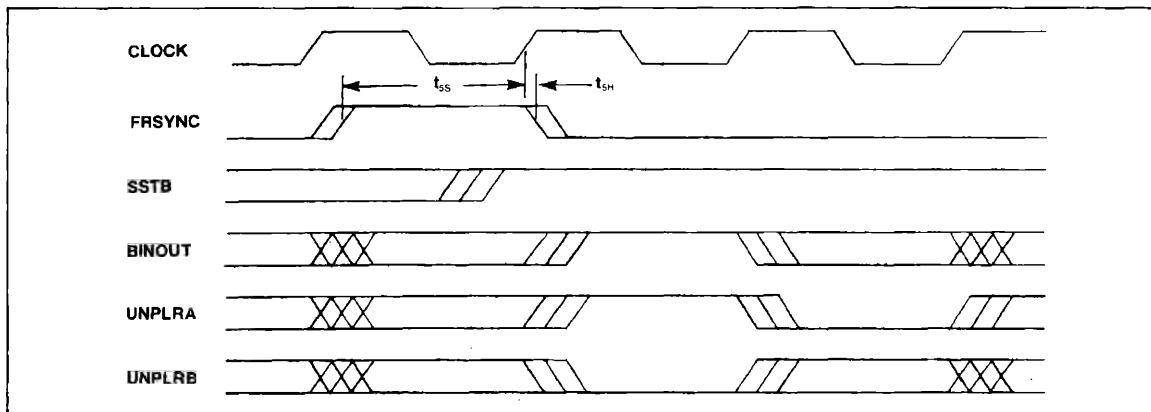


Figure 6. Non-return-to-zero FRSYNC Timing

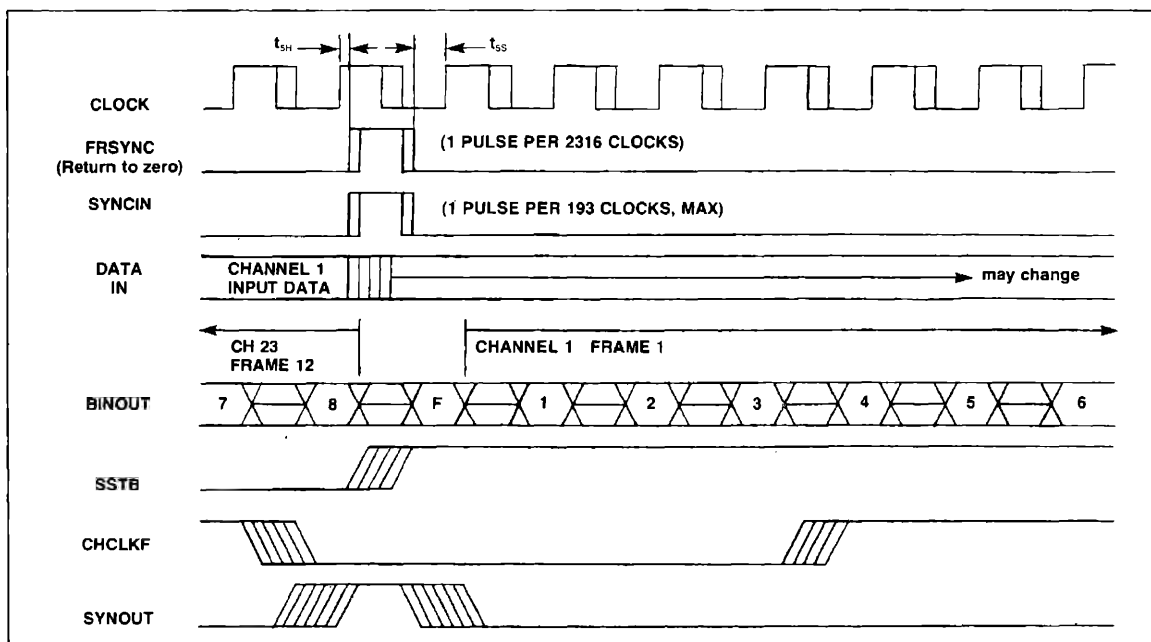


Figure 7. Transmitter External Synchronization (Return-to-zero FRSYNC)

Table 3. Input Timing

		Min	Max	Unit
t_{1S}	Buffered Data Setup Time	450		ns
t_{1H}	Buffered Data Hold Time	0		ns
t_{2S}	Control Input Setup Time	400		ns
t_{2H}	Control Input Hold Time	20		ns
t_{3S}	Asynchronous Control Input Setup Time	350		ns
t_{3H}	Asynchronous Control Input Hold Time	20		ns
t_{4S}	SYNCIN Setup Time	200		ns
t_{4H}	SYNCIN Hold Time	20		ns
	SYNCIN Pulse Width	100		ns
t_{5S}	Frame Sync Setup Time (Return to Zero)	250		ns
t_{5H}	Frame Sync Hold Time (Return to Zero)	20		ns
	Frame Sync Pulse Width	200		ns
t_{5S}	Frame Sync Setup Time (Non-Return to Zero)	525		ns
t_{5H}	Frame Sync Hold Time (Non-Return to Zero)	20		ns

Table 4. Output Propagation Delay, Worst Case
(Measured from Rising Edge of Clock Unless Stated Otherwise)

Output	Max Delay	Unit
SSTB	500	ns
SYNOUT	500	ns
Ref from Falling Edge of Clock		
CHCLKF	500	ns
BINOUT	500	ns
UNPLRA	500	ns
UNPLRB	500	ns

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	Vdc
Operating Temperature	T_{OP}	0 to 70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

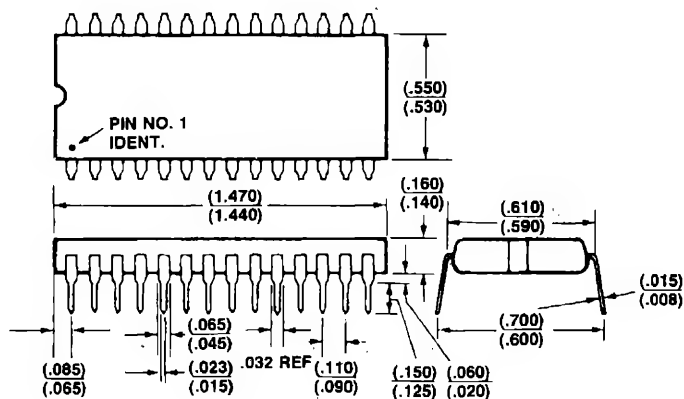
*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD} = 5.0 \pm 5\%$)

Parameter	Symbol	Min	Max	Unit
Logical "1" Input Voltage	V_{OH}	2.0	$V_{DD} + 0.3$	V
Logical "0" Input Voltage	V_{IL}	-0.3	0.8	V
Logical "1" Output Voltage	V_{OH}	2.4	—	V
Logic "0" Output Voltage	V_{OL}	—	0.4	V
Output Source Current	I_{OH}	-100	—	μA
Output Sink Current	I_{OL}	400	—	μA
Capacitance Load (any output)	C	—	25	pF
Input Capacitance (any input)	C_{IN}	—	5	pF
Clock Frequency		—	1.6	MHz
Power Dissipation	P_D	—	250	mW

PACKAGE DIMENSIONS





R8060 and R8060A T-1 SERIAL RECEIVER

DESCRIPTION

The Rockwell T-1 Receiver processes serial unipolar data of a T-1, D2 or T-1, D3 line from which data and a 1.544 MHz clock have been extracted.

Frame synchronization is accomplished by locating the frame bit (F_T) alternating every 386 bits. Loss of frame sync is indicated if a frame bit error occurs within two to four F-Bit frames since the previous frame bit error.

A loss of carrier is indicated if 31 consecutive bit times yield "zeros" at the input. Carrier loss is reset and frame sync search begins when a "one" reappears at the TDATA input.

Signaling bits, which occur 193 bit positions after a framing bit, are monitored to detect signaling frames. The signaling frame output, SIGFR, identifies the present frame as a signaling frame, and the S-Bit output at that time identifies which signaling frame is being processed.

Remote alarm reporting is detected by monitoring the second received bit of every channel sample of every frame. An alarm is indicated if 255 consecutive Bit 2 zeros are received.

Channel data bits are output by an eight-bit parallel register. The rising edge of the signal called channel clock (CHCLK) indicates the extraction of new output channel data.

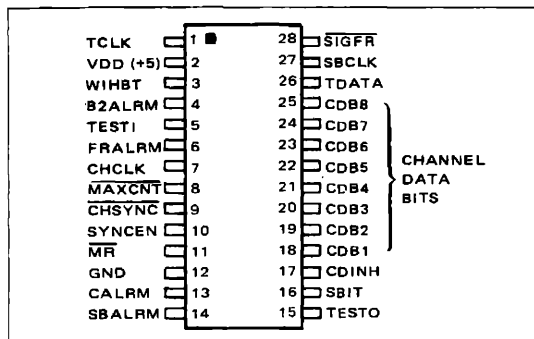
Several signals developed from a MOD 386 counter are provided to aid in the external processing and storage of channel data. Signals are provided to increment counters, synchronize counters, strobe data into memories, etc.

The Rockwell T-1 Receiver chip operates on a single 5 volt supply and directly interfaces to the low power TTL Schottky logic family. The Receiver is packaged in a 28 pin dual in-line (DIP).

Timing relationships are given in figures 3 through 5.

FEATURES

- Synchronizes serial T-1, D2 or T-1, D3 signals in less than 5 ms.
- Extracts 8-bit parallel channel data
- Provides timing signals to capture and synchronize channel and frame information
- Monitors and detects
 - Errors in signaling bit pattern
 - Loss of frame sync
 - Loss of carrier
 - Remote alarm reporting
- Single 5V supply
- LSTTL Schottky compatible



Pin Configuration

ORDERING INFORMATION

The T-1 Serial Receiver is available in two versions. With the standard commercial version, R8060, data will be stable within 900 ns after the bit clock. With the selected version, R8060A, data will be available within 600 ns after the bit clock.

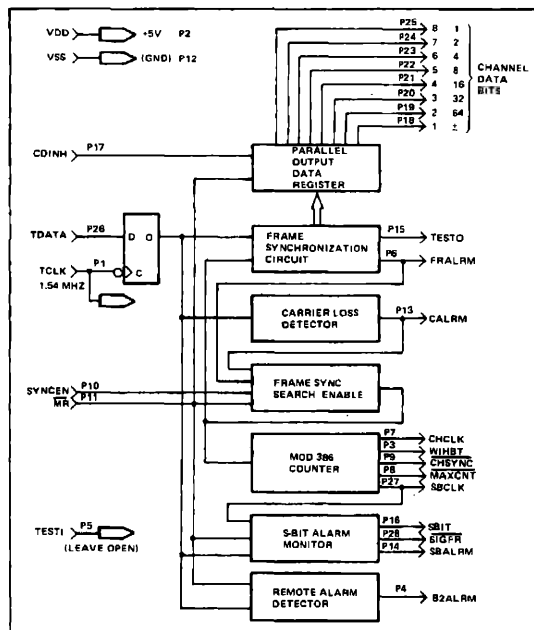


Figure 1. R8060 Block Diagram

T-1 RECEIVER INPUTS

Any input $\leq 0.8V$ = LOGIC 0, LOW, ZERO. Any input $\geq 2.0V$ = LOGIC 1, HIGH, ONE. A transition from a low level to a high level is called a rising edge, while the converse is true for the falling edge.

TDATA: UNIPOLAR T-1-D2, T-1-D3 SERIAL DATA INPUT

Unipolar T-1 Data is clocked in on the falling edge of TCLK. Thereafter, TDATA is processed on the rising edge of TCLK. TDATA must be stable 100 ns before and remain stable 100 ns after the falling edge of TCLK.

TCLK: T-1 CLOCK

Typical clock frequency is 1.544 MHz. Maximum clock frequency is 1.85 MHz. The T-1 bit period is bounded by the rising edges of TCLK.

SYNCEN: FRAME SYNCHRONIZATION ENABLE

Provides a means to disable the automatic resync search initiated by a FRAME ALARM condition. If the SYNCEN signal is low, with synchronization function is inhibited and remains inhibited until SYNCEN transitions high. SYNCEN must be stable 200 ns before the rising edge of FRALRM, in order to inhibit the synchronization function.

MR: MASTER RESET

Master Reset, when low performs an initialization clear of the T-1 Receiver; SBALRM and CALRM are reset to low levels while FRALRM, CHCLK, WIHBT and CHSYNC are set to high levels. Frame synchronization search begins on the rising edge of MR provided that SYNCEN signal has been high for 200 ns. Minimum pulse width is one T-1 clock period.

CDINH: CHANNEL DATA INHIBIT

Provides a means to disable channel data bit outputs. When at a high level, CDINH forces channel data Bits 1 through 7 high. Bit 8, the least significant channel data bit, is not controlled by CDINH.

TESTI: ROCKWELL DEVICE TEST INPUT

Used only for Rockwell device testing, no connection to TESTI is required for normal operation.

VSS, VDD: GROUND AND POWER

VDD = +5.0 \pm 0.25 VDC
VSS = Ground, 0 VDC

T-1 RECEIVER OUTPUTS

Low Power TTL Schottky — compatible
"1" ≥ 2.4 Vdc; "0" ≤ 0.4 Vdc
CMOS — 12 K Ω pullup to VDD required.

CDB (1-8): CHANNEL DATA BIT 1 THROUGH 8

Bit 1 is the sign bit, Bit 2 is the most significant bit and Bit 8 is the least significant bit. If CDINH is low, new parallel channel data becomes valid within 200 ns after the rising edge of CHCLK and remains valid until the next rising edge of CHCLK. If CDINH is high, channel data Bits 1 through 7 are forced to a high level. Bit 8, the least significant bit, is not controlled by CDINH. Channel data Bits 1 through 7 are enabled or disabled within 300 ns (R8060) or 150 ns (R8060A) by CDINH. Refer to Figures 3 through 5.

CHCLK — CHANNEL CLOCK

The rising edge of CHCLK indicates a change of parallel output channel data. CHCLK is four TCLKS high then four TCLKS low except for when an "F" or "S" bit is received. Then CHCLK stretches to five TCLKS high and four TCLKS low. Refer to Figures 3 and 4.

CHSYNC: CHANNEL SYNC

Channel Sync occurs one time in a 24 channel period, making it suitable for synchronizing external counters to the T-1 Frame rate. CHSYNC goes low one TCLK period before the falling edge of CHCLK at channel 24 date sample time. CHSYNC returns high 1 TCLK period after the next rising edge of CHCLK. Refer to Figures 3 through 5.

TESTO: ROCKWELL DEVICE TEST OUTPUT

Designed to aid in Rockwell device testing. No connection required for normal operation.

WIHBT: WRITE INHIBIT

WIHBT covers the parallel channel data transition period. WIHBT is suitable for clocking or strobing channel data into external memories. WIHBT is high for two TCLK periods, beginning one TCLK period before the rising edge of CHCLK. Refer to Figures 3 and 4.

MAXCNT: MAXIMUM COUNT OF 386 MODULUS

MAXCNT is low for one TCLK period, marking the completion of a two-frame period corresponding to the expected receipt of an F-bit at the TDATA input. Refer to Figures 4 and 5.

SBCLK: S-BIT CLOCK

SBCLK will be high during the S-Bit frame and low during the F-bit frame. The transitions will occur within 300 ns after the rising edge of TCLK as channel 24 data is being transferred to the parallel channel outputs. Refer to Figures 3 through 5.

S-BIT: SIGNALING BIT OUTPUT

The S-Bit output monitors the previous S-Bit received which occurred two frames before the receipt of the current S-Bit. An S-Bit output transition occurs one TCLK period after the rising edge of SBCLK.

During a signaling frame (SIGFR is low), frame 6 or "A" highway signaling is identified by S-Bit output being low. If S-Bit is high during a signaling frame, frame 12 or "B" highway signaling is identified. Refer to Figures 3 through 5.

SIGFR: SIGNALING FRAME

SIGFR identifies frame 6 or 12 when low. If the sequence of five consecutive received S-Bits is either 0111X or 1X001 (left to right, as received), SIGFR shall go low after the rising edge, but at least 375 ns before the falling edge of WIHBT corresponding to channel 1 data sample time. SIGFR returns high one frame later (193 bits). Refer to Figures 3 through 5.

SBALRM: S-BIT ALARM

SBALRM goes high if the sequence of the five S-Bits received contains four consecutive ones (01111), and remains high until three consecutive "zero" bits are preceded and followed by a "one" S-Bit (10001). The actual transition of SBALRM output occurs after the rising edge, but at least 375 ns before the falling edge of WIHBT corresponding to channel 1 data sample time.

B2ALRM: BIT 2 ALARM

B2ALRM goes high, detecting a remote alarm condition, if 255 consecutive channel data samples are received with Bit 2 low. B2ALRM returns low upon the receipt of any channel sample with Bit 2 high.

CALRM: CARRIER LOSS ALARM

A carrier loss is detected and CALRM is set high if 31 consecutive low level TDATA bits are received. CALRM is reset low,

FRALRM is set high and frame sync search begins when the first TDATA high level is received.

FRALRM: FRAME ERROR ALARM

FRALRM detects an out-of-frame condition. FRALRM goes high if:

- A) The framing synchronization function is in progress.
- B) Within 250 ns after the falling edge of MR.
- C) An F-Bit is received which is not the inverse of the last F-Bit and the same condition also occurred two or three or four F-Bit frames earlier.
- D) Within 250 ns after the falling edge of CALRM, (CALRM being reset by high level TDATA bit).

FRALRM goes low upon completion of the synchronization function or within 250 ns after the rising edge of CALRM. (Carrier loss condition during frame synchronization function).

OUTPUT CLOCK SIGNALS DURING FRAME SYNCHRONIZATION FUNCTION

Following the Declaration of Frame Sync loss (FRALRM goes high), output signals will continue normally for a two-frame period with the exception of CHSYNC, which has the above mentioned second frame sync pulse inhibited. Following the two-frame period CHCLK, CHSYNC, and WIHBT are held high until frame sync has been located, as indicated by the falling edge of FRALRM. With typical data patterns, frame synchronization takes less than five milliseconds. See Figure 2.

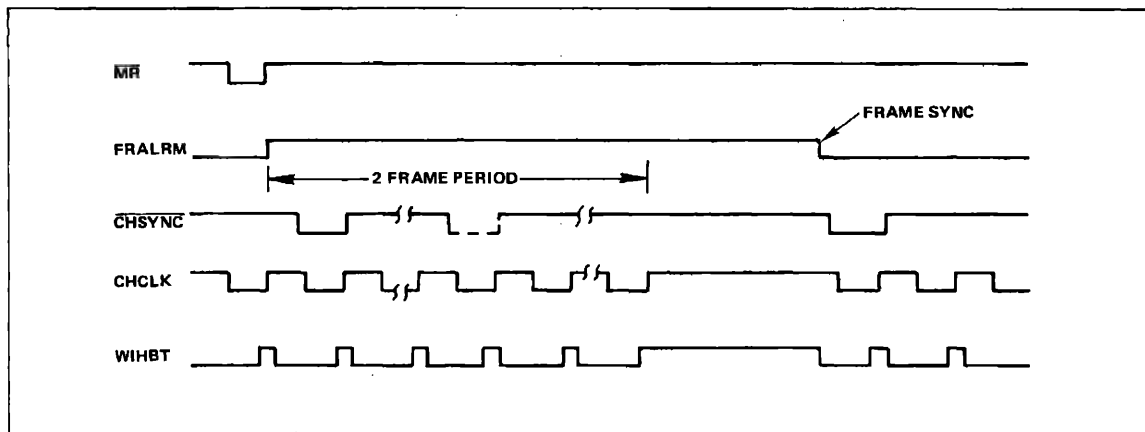
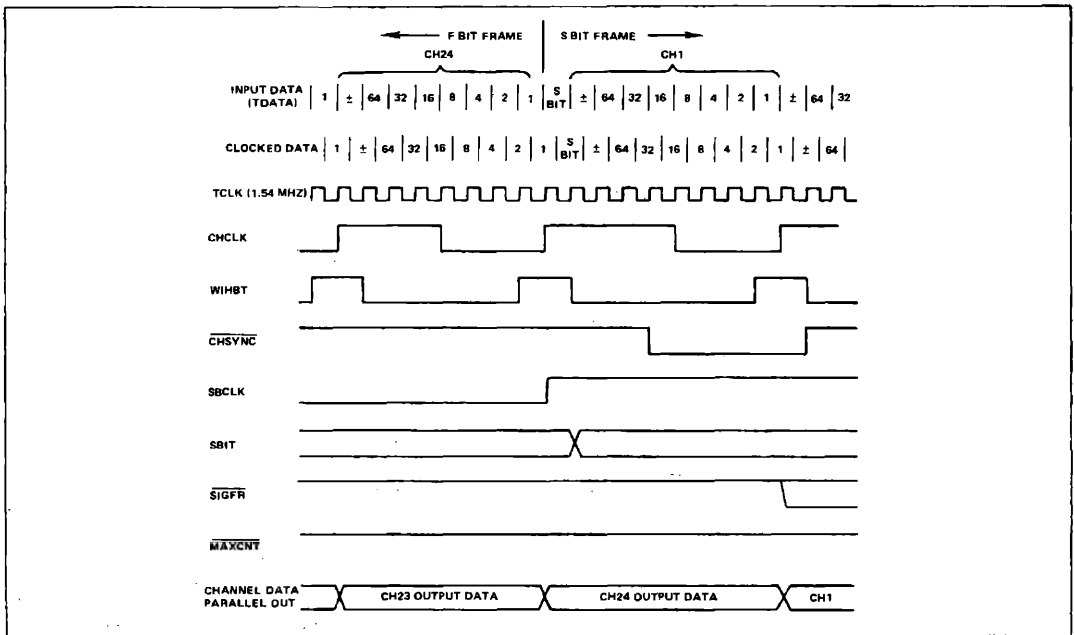
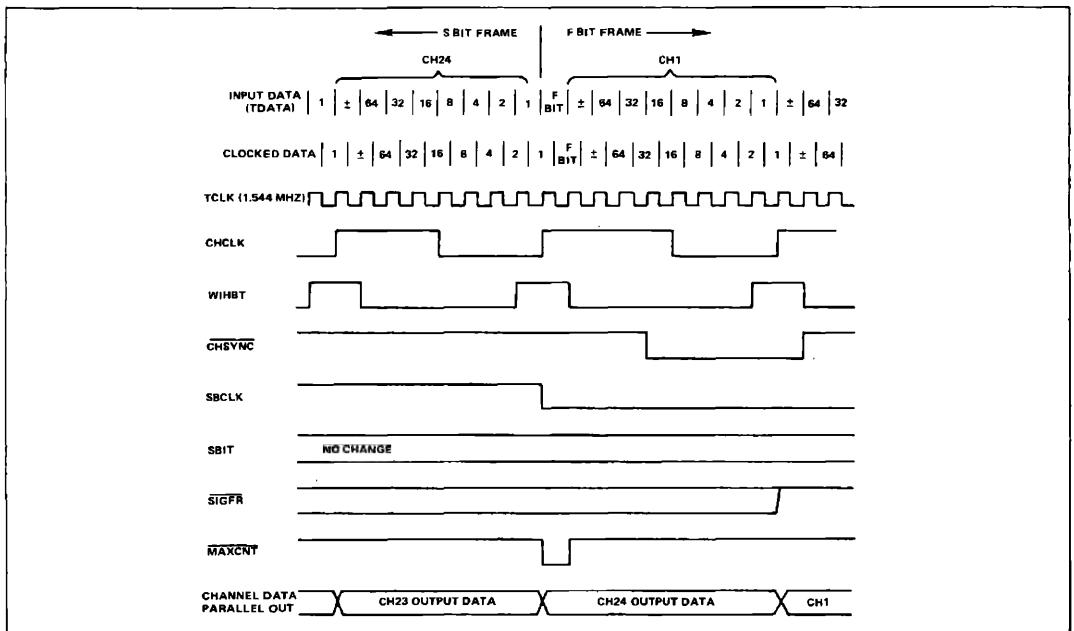


Figure 2. Signal Relationship During Frame Alarm and Search for Resynchronization

Figure 3. Signal Relationships at Beginning of F_s Frame (S-BIT)Figure 4. Signal Relationship at Beginning of F_t Frame (F-BIT)

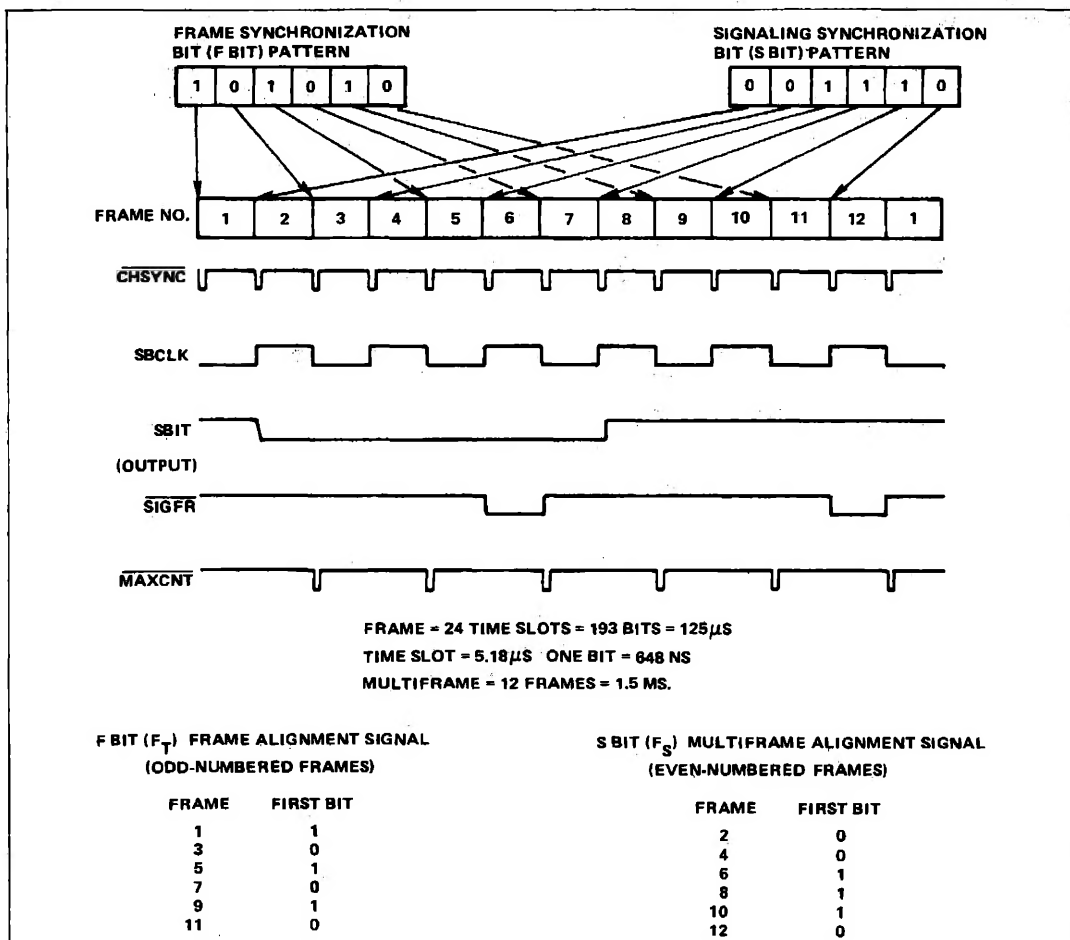
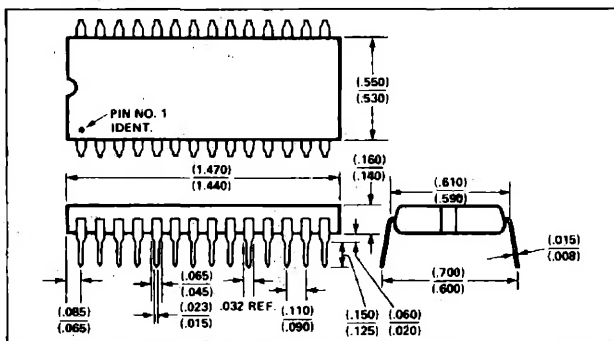


Figure 5. Multiframe Signal Relationships

Table 1. Output Propagation Delay Worst Case, From Rising Edge to TCLK

OUTPUT	MAX DELAY (NS)
CHCLK	300
CHSYNC	300
WIHBT	300
MAXCNT	300
SBCLK	300
SBIT	400
SIGFR	475
SBALRM	475
B2ALRM	450
CALRM	300
FRALRM	900 (R8060)
	600 (R8060A)
CDB (1-8)	400



Packaging Diagram

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	V
Operating Temperature Range	T_{OP}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD} = +5V \pm 5\%$, $T_A = 25^\circ C$)

Parameter	Symbol	Min	Max	Unit
Input Logic "1" Voltage	V_{IH}	2.0	$V_{DD} + 0.3$	V
Input Logic "0" Voltage	V_{IL}	-0.3	0.8	V
Output Logic "1" Voltage	V_{OH}	2.4		V
Output Logic "0" Voltage	V_{OL}		0.4	V
Output Source Current	I_{OH}	-100		μA
Output Sink Current	I_{OL}	400		μA
Clock Frequency	T_{CLK}		1.85	MHz
Input Capacitance	C_I		5	pF
Output Capacitance	C_O		25	pF
Power Dissipation	P_{DSS}		550	mW



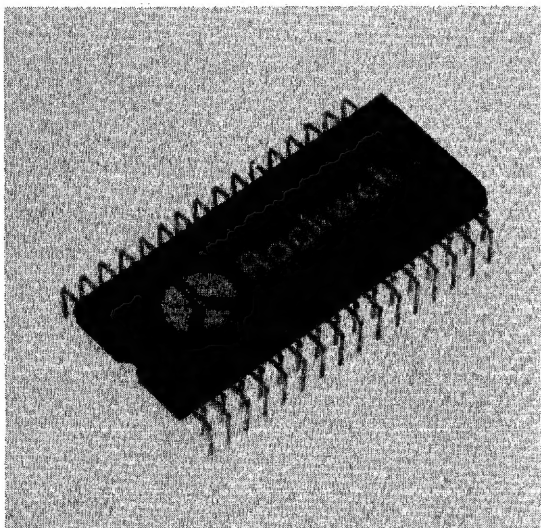
R8070 T-1/CEPT PCM TRANSCEIVER

PRELIMINARY

INTRODUCTION

The R8070 T-1/CEPT Transceiver is a new generation PCM (Pulse Code Modulation) protocol device designed and manufactured by Rockwell International. The new device utilizes CMOS technology providing a higher level of component integration than its predecessors; low power dissipation and many features and capabilities. The device is designed to meet AT&T and CCITT specifications, including EXTENDED FRAME and CLEAR CHANNEL and/or CEPT applications using T-1, T-1C or CEPT specifications.

Product availability of R8070 T-1/CEPT PCM Transceiver is Winter, 1984.



R8070 T-1/CEPT PCM Transceiver

FEATURES

- PCM format transceiver (transmitter and receiver in one chip)
- CMOS technology design
- 5-volt single supply voltage
- 64-pin QJIP package
- Meets CCITT G.732, G.733 and G.703 (applicable parts) specifications, and AT&T advisories

- Operates with EXTENDED FRAMING, CLEAR CHANNEL and/or CEPT formats
- Uses a clock of 1.544 (T-1), 1.576 (½ T-1C), or 2.048 (CEPT) MHz depending on operation mode
- Supports multiplex/demultiplex T-1C, mode 1 (synchronous) operation
- Formats data to be serially transmitted/received according to CCITT and AT&T specifications
- Mode Selectable — provides 17 different data format and zero suppression mode combinations
- Selectable serial or parallel digital data interface
- Provides status and alarm information to peripheral equipments for control and status reporting
- Allows external synchronization of the transmitter's internal circuitry
- Generates signals for external processing of data
- Interfaces between multiplexed digital signals and the PCM highway

APPLICATIONS

- Channel Banks — add signalling and framing information to the multiplexed 24-voice channels
- CPI and DMI — provides bidirectional data communication between systems
- PBX — interfaces between transmission medium and trunk side of PBX
- Time and Space Division Switching — provides interface between PCM highway and dedicated time slot interchange circuitry
- Can be used in virtually any voice/data system designed to AT&T or CCITT specifications for primary rate interface

CUSTOMER BENEFITS

Use of the R8070 will:

- Reduce board layout area
- Save power — CMOS low power dissipation
- Provide higher design reliability — replaces 100 MSI with one chip
- Provide cost reduction
- Meet AT&T and CCITT specifications in a single device
- Provide ease of signal processing on a digital data

SELECTABLE R8070 MODES

MNEMONIC	DESCRIPTION
<u>T-1</u>	
193N	193 bits/frame, no signalling 4 frames per super frame Zero suppression — B8ZS, B7 stuffing, or transparent
193S	193 bits/frame, with signalling 12 frames per super frame Zero suppression — B8ZS, B7 stuffing, or transparent
193E	193 bits/frame, extended frame, with signalling 24 frames per super frame Zero suppression — B8ZS, B7 stuffing, or transparent
193F	193 bits/frame, extended frame, no signalling 24 frames per super frame Zero suppression — B8ZS or transparent
197N	197 bits/frame, ½ synchronous T1-C, no signalling 4 frames per super frame Zero suppression, (None) transparent
197S	197 bits/frame, ½ synchronous T1-C, with signalling 12 frames per super frame Zero suppression, (None) transparent
<u>CEPT</u>	
256N	256 bits/frame, with signalling 2 frames per super frame Zero suppression — HDB3 or transparent
256S	256 bits/frame, with signalling 16 frames per super frame Zero suppression — HDB3 or transparent
Legend: Zero Suppression Key B8ZS = Bipolar 8 Zero Substitution B7 = Bit 7 HDB3 = High Density Bipolar 3 Zero Max	